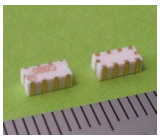
CDM LTCC Chip Delay Lines

The CDM-type Delay Line is an LTCC (Low-Temperature, Co-fired Ceramic) chip Delay Line. By removing one (1) line from the CDKD-type differential Delay Line, we have been able to accommodate a very compact overall area of only 5mm x 2.5mm.

FEATURES

- We have described a CDM/CDKD common land pattern on which the CDM-type should be mounted for delay times within a 3ns delay range, and on which the CDKD-type should be mounted as a single-ended Delay Line, with the 2 differential lines connected in series (CDKD 2-line connection), for delay times over 3ns. We provide a 0.1~10ns delay range using a CDM/CDKD common land pattern.It is a RoHS-compliant component.



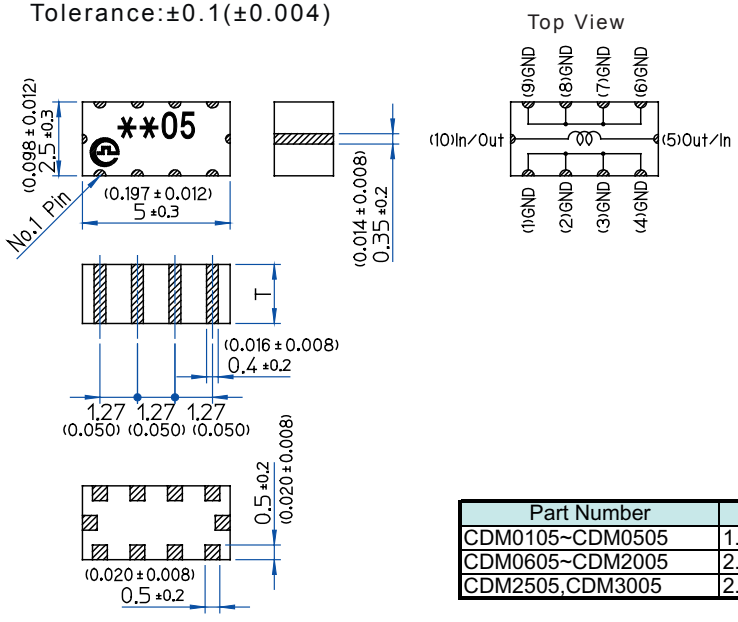
COMMON SPECIFICATIONS

Impedance:	50Ω±10%
Waveform Distortion:	Overshoot/preshoot under 20%
Delay Time Temp. Coefficient:	0~150ppm/°C
Insulation Resistance:	DC50V, over 100MΩ
Operating Temperature Range:	-40°C to +85°C
Storage Temperature Range:	-40°C to +120°C

PACKAGE DIMENSIONS & PIN CONFIGURATION

Unit:mm (inch)

Tolerance:±0.1(±0.004)



Part Number	Dimension of T
CDM0105~CDM0505	1.0Max (0.039Max)
CDM0605~CDM2005	2.0Max (0.079Max)
CDM2505,CDM3005	2.5Max (0.098Max)

Please refer to the CDKD page in the differential Delay Line section for CDKD-series Package Dimensions and Pin Configuration.

CDM LTCC Chip Delay Lines

CDM Product Specifications

Part Number	Delay Time	Rise/Fall Time (20%-80%)	-3dB Passband			DC Resistance
			Actual(1)*	Actual(2)*	Guarantee(3)*	
CDM0105	100ps±50ps	100ps Max.	DC～15GHz	DC～3GHz	DC～3GHz	1.0ΩMax.
CDM0205	200ps±50ps	100ps Max.	DC～10GHz	DC～3GHz	DC～3GHz	1.0ΩMax.
CDM0305	300ps±50ps	100ps Max.	DC～10GHz	DC～3GHz	DC～3GHz	1.0ΩMax.
CDM0405	400ps±50ps	100ps Max.	DC～7.5GHz	DC～3GHz	DC～3GHz	1.5ΩMax.
CDM0505	500ps±50ps	100ps Max.	DC～6GHz	DC～3GHz	DC～3GHz	1.5ΩMax.
CDM0605	600ps±50ps	100ps Max.	DC～5GHz	DC～3GHz	DC～3GHz	3.0ΩMax.
CDM0705	700ps±50ps	110ps Max.	DC～4.3GHz	DC～3GHz	DC～3GHz	3.0ΩMax.
CDM0805	800ps±50ps	120ps Max.	DC～3.8GHz	DC～3GHz	DC～3GHz	3.0ΩMax.
CDM0905	900ps±50ps	130ps Max.	DC～3.3GHz	DC～3GHz	DC～2.7GHz	3.5ΩMax.
CDM1005	1.0ns±50ps	150ps Max.	DC～3GHz	DC～3GHz	DC～2.4GHz	3.5ΩMax.
CDM1205	1.2ns±60ps	180ps Max.	DC～2.5GHz	DC～2.5GHz	DC～2GHz	4.0ΩMax.
CDM1305	1.3ns±65ps	190ps Max.	DC～2.3GHz	DC～2.3GHz	DC～1.9GHz	4.5ΩMax.
CDM1405	1.4ns±70ps	210ps Max.	DC～2.1GHz	DC～2.1GHz	DC～1.7GHz	4.5ΩMax.
CDM1505	1.5ns±75ps	220ps Max.	DC～2GHz	DC～2GHz	DC～1.6GHz	4.0ΩMax.
CDM1605	1.6ns±80ps	240ps Max.	DC～1.8GHz	DC～1.8GHz	DC～1.5GHz	4.5ΩMax.
CDM1805	1.8ns±90ps	270ps Max.	DC～1.7GHz	DC～1.7GHz	DC～1.3GHz	4.5ΩMax.
CDM2005	2.0ns±100ps	300ps Max.	DC～1.5GHz	DC～1.5GHz	DC～1.2GHz	5.0ΩMax.
CDM2505	2.5ns±125ps	360ps Max.	DC～1.2GHz	DC～1.2GHz	DC～960MHz	5.0ΩMax.
CDM3005	3.0ns±150ps	400ps Max.	DC～1.1GHz	DC～1.1GHz	DC～880MHz	5.0ΩMax.

(1)* Actual (1) is the typical value when utilizing land pattern #1.
(2)* Actual (2) is the prospective value when utilizing land pattern #2, derived from EM Simulation.
(3)* The guaranteed value of -3dB passband is limited by the band width of the pin probe during product inspection.

Characteristics of CDKD 2-Line Connection on land pattern #2 (For reference only.)

Part Number	Delay Time	Rise/Fall Time(4)* (20%-80%)	-3dB Passband Actual(4)*	DC Resistance
CDKD2005 (2 Line Connection)	4.0±0.2 ns	0.3ns Typ.	DC～750MHz	10.0ΩMax.
CDKD2505 (2 Line Connection)	5.0±0.25 ns	0.4ns Typ.	DC～600MHz	10.0ΩMax.
CDKD3005 (2 Line Connection)	6.0±0.3 ns	0.5ns Typ.	DC～500MHz	10.0ΩMax.
CDKD3505 (2 Line Connection)	7.0±0.35 ns	0.65ns Typ.	DC～350MHz	12.0ΩMax.
CDKD4005 (2 Line Connection)	8.0±0.4 ns	0.8ns Typ.	DC～300MHz	15.0ΩMax.
CDKD4505 (2 Line Connection)	9.0±0.45 ns	0.9ns Typ.	DC～250MHz	15.0ΩMax.
CDKD5005 (2 Line Connection)	10.0±0.5 ns	1.0ns Typ.	DC～200MHz	15.0ΩMax.

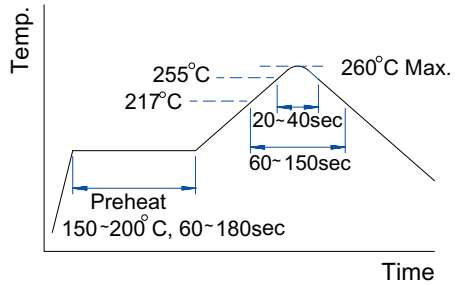
(4)* Rise/Fall time and –3dB passband for 2-line connection use are only reference values, as the CDKD-series is inspected and guaranteed as a differential Delay Line.

REFLOW SOLDERING CONDITIONS

Storage conditions are as per MSL1. These component families are not moisture-sensitive.

Baking prior to reflow is not required.

J-STD-020C Pb-Free Standard



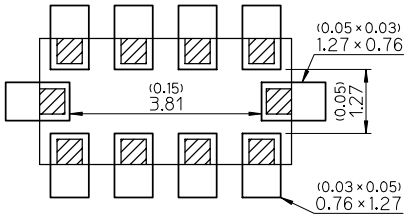
CDM LTCC Chip Delay Lines

SUGGESTED LAND PATTERN

Unit:mm (inch)

Tolerance:±0.1(±0.004)

(1) Land Pattern #1 (CDM only)



Conditions for 50Ω Line

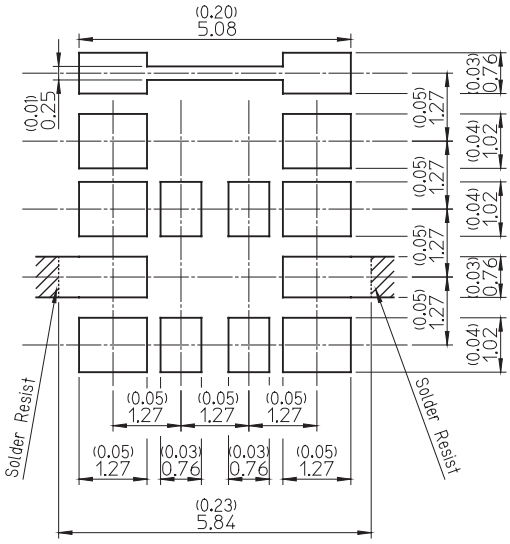
Line width: 0.76mm(0.03inch)

Line thickness: 10~55μm

PWB εr: 4.0

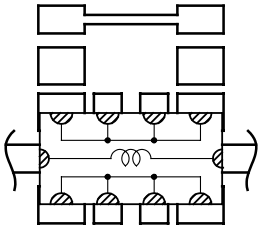
Distance from GND plane: 0.4mm

(2) Land Pattern #2 (CDM/CDKD common land)

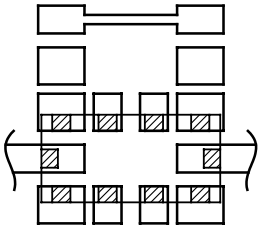


(3) CDM-type mounting configuration, land pattern #2

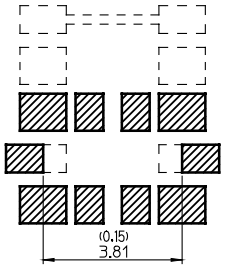
Top View



Pad Position

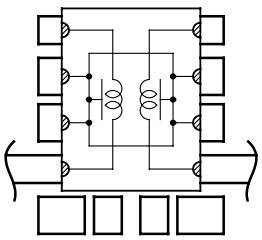


Solder Paste Mask

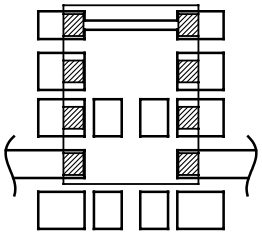


(4) CDKD-type mounting configuration for 2-Line Connection, land pattern #2

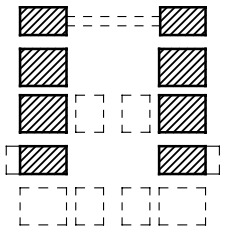
Top View



Pad Position



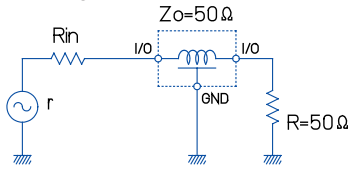
Solder Paste Mask



CDM LTCC Chip Delay Lines

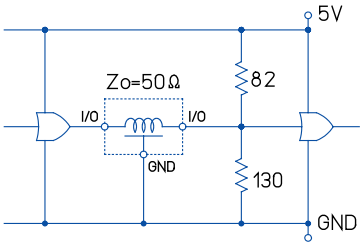
TYPICAL APPLICATIONS AND TERMINATION METHODS

(1) Analog circuit

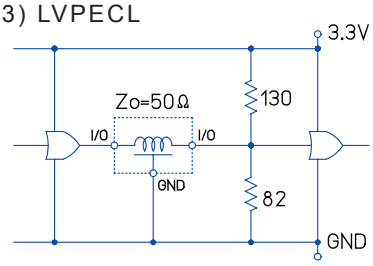


r :Impedance of signal source
Rin:Input adjustment resistance
Zo :Characteristics impedance of internal Elements (=Output impedance)
Ro :Internal adjustment resistance (=Zo)
r+Rin=Zo=R

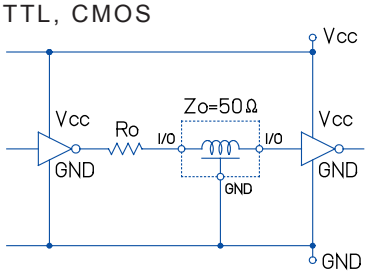
(2) PECL



(3) LVPECL



(4) TTL, CMOS



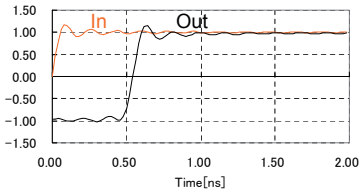
Ro should be adjusted to a value near Zo.

CDM LTCC Chip Delay Lines

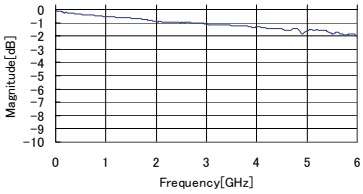
OUTPUT WAVEFORMS (1)

(1) 0.5ns CDM0505, Land Pattern #1

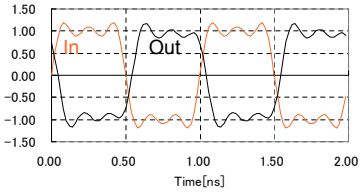
Output waveform (Step function)



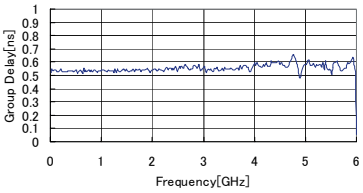
Sdd21 Amplitude / Frequency



Output waveform (1GHz Clock)

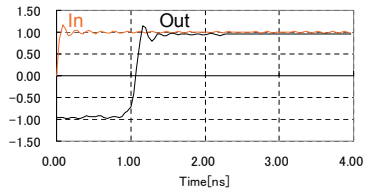


Group Delay

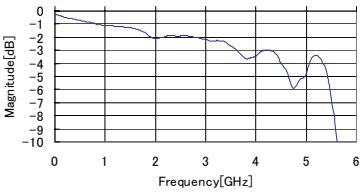


(2) 1ns CDM1005, Land Pattern #1

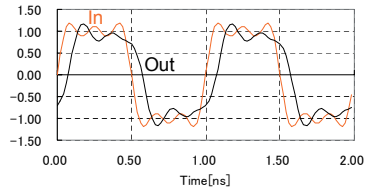
Output waveform (Step function)



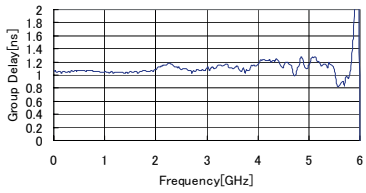
Sdd21 Amplitude / Frequency



Output waveform (1GHz Clock)



Group Delay

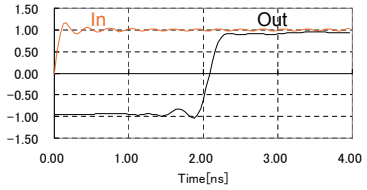


CDM LTCC Chip Delay Lines

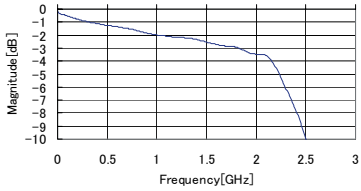
OUTPUT WAVEFORMS (2)

(3) 2ns CDM2005, Land Pattern #1

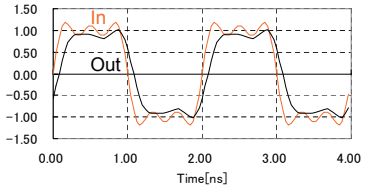
Output waveform (Step function)



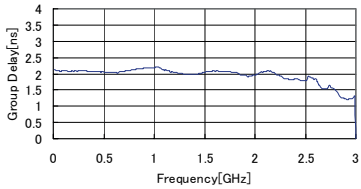
Sdd21 Amplitude / Frequency



Output waveform (500MHz Clock)

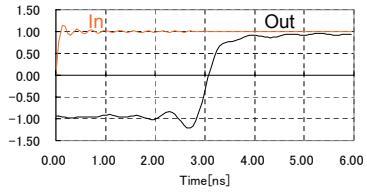


Group Delay

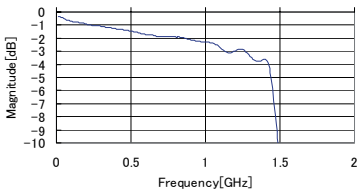


(4) 3ns CDM3005, Land Pattern #1

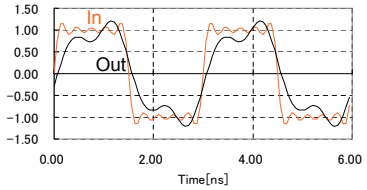
Output waveform (Step function)



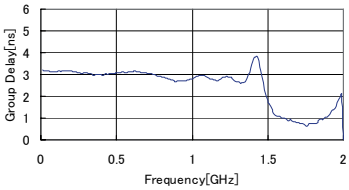
Sdd21 Amplitude / Frequency



Output waveform (333MHz Clock)



Group Delay

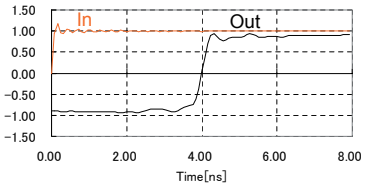


CDM LTCC Chip Delay Lines

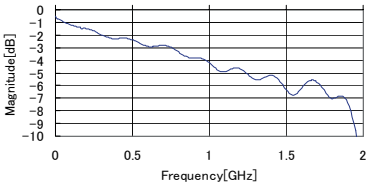
OUTPUT WAVEFORMS (3)

(5) 4ns CDKD2005- 2 Line Connection

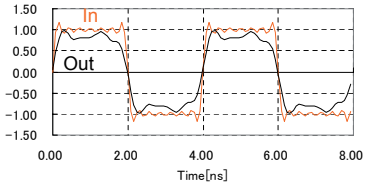
Output waveform (Step function)



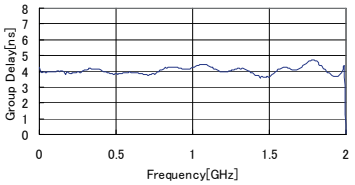
Sdd21 Amplitude / Frequency



Output waveform (250MHz Clock)

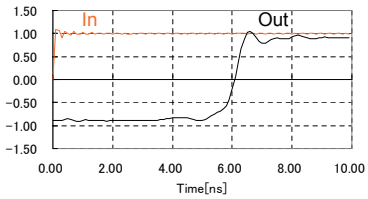


Group Delay

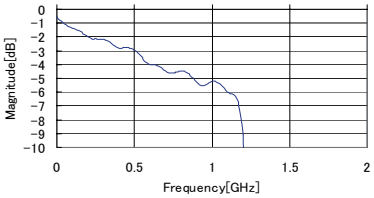


(6) 6ns CDKD3005- 2 Line Connection

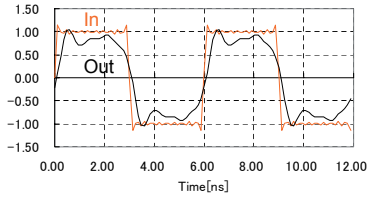
Output waveform (Step function)



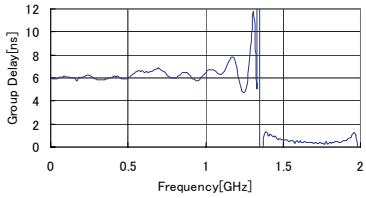
Sdd21 Amplitude / Frequency



Output waveform (167MHz Clock)



Group Delay

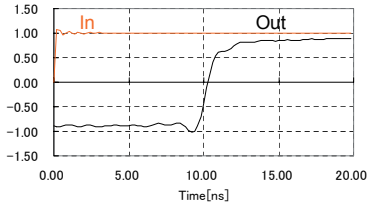


CDM LTCC Chip Delay Lines

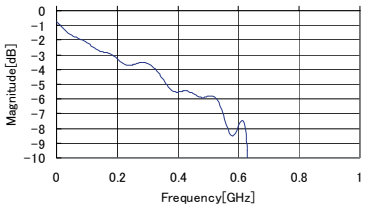
OUTPUT WAVEFORMS (4)

(7) 10ns CDKD5005- 2 Line Connection

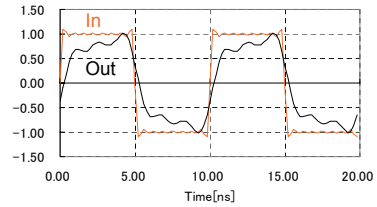
Output waveform (Step function)



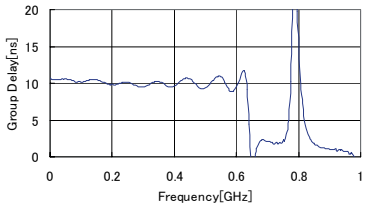
Sdd21 Amplitude / Frequency



Output waveform (100MHz Clock)



Group Delay



RoHS Compliance Status

Initially developed only as a RoHS-compliant component.