SGM41002
Battery Protection IC for 2-Serial to 4-Serial-Cell Pack (Secondary Protection)

GENERAL DESCRIPTION

The SGM41002 is used for secondary protection of lithium-Ion rechargeable batteries, and incorporates a high-accuracy voltage detection circuit and a delay circuit. Short-circuits between cells accommodate series connection of two to four cells.

APPLICATIONS

Lithium-Ion Rechargeable Battery Packs
(For Secondary Protection)

FEATURES

- **High Accuracy Voltage Detection Circuit for Each Cell**
- **Over-Charge Detection Voltage:**
  4.35V, 4.45V, 4.5V
- **Over-Charge Hysteresis Voltage: -0.4V**
- **2.8s Delay Time for Over-Charge Detection**
- **Output Control Function via CTL Pin**
- **Output Form and Logic**
  CMOS Output Active "H"
- **High Withstand Voltage Devices**
  Absolute Maximum Rating: 26V
- **Wide Operating Voltage Range: 3.6V to 24V**
- **Low Current Consumption**
- **Operating Temperature Range: -40℃ to +85℃**
- **Available in Green UTDFN-2×2.5-8L Package**

MODEL	OVER-CHARGE DETECTION VOLTAGE (V_{CU})	OVER-CHARGE HYSTERESIS VOLTAGE (V_{HC})	OVER-CHARGE DETECTION DELAY TIME (t_{CU})	OUTPUT FORM
SGM41002	4.35V	-0.4V	2.8s	CMOS output active "H"
	4.45V	-0.4V	2.8s	CMOS output active "H"
	4.5V	-0.4V	2.8s	CMOS output active "H"

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM41002	UTDFN-2×2.5-8L	-40℃ to +85℃	SGM41002-4.35YUDS8G/TR	GY5 XXXX	Tape and Reel, 3000
	UTDFN-2×2.5-8L	-40℃ to +85℃	SGM41002-4.45YUDS8G/TR	GNC XXXX	Tape and Reel, 3000
	UTDFN-2×2.5-8L	-40℃ to +85℃	SGM41002-4.50YUDS8G/TR	GNB XXXX	Tape and Reel, 3000

NOTE: XXXX = Date Code.

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Input Voltage between VDD and VSS ..... V_{SS} - 0.3V to V_{SS} + 26V
Input Pin Voltage, VC1, VC2, VC3, VC4, CTL ..... V_{SS} - 0.3V to V_{DD} + 0.3V
CO Output Pin Voltage ..... V_{SS} - 0.3V to V_{DD} + 0.3V
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering 10 sec) ..... +260℃
ESD Susceptibility
HBM 2000V
MM 200V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range ..... 4V to 24V
Battery Voltage Range ..... 0V to 24V
Environmental Temperature Range ..... -40℃ to +85℃

OVERSTRESS CAUTION

Stresses beyond those listed may cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

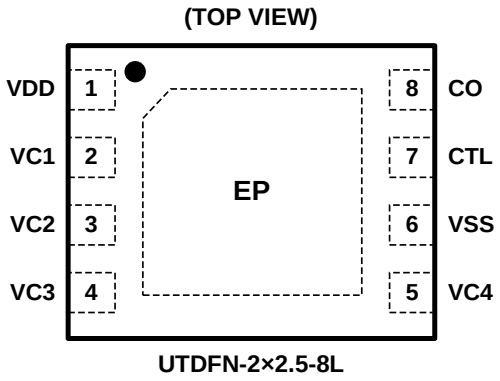
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time.

PIN CONFIGURATION



PIN DESCRIPTION

PIN	NAME	FUNCTION
1	VDD	Positive Power Input Pin.
2	VC1	Positive Voltage Connection Pin of Battery 1.
3	VC2	Positive Voltage Connection Pin of Battery 2. Negative Voltage Connection Pin of Battery 1.
4	VC3	Positive Voltage Connection Pin of Battery 3. Negative Voltage Connection Pin of Battery 2.
5	VC4	Positive Voltage Connection Pin of Battery 4. Negative Voltage Connection Pin of Battery 3.
6	VSS	Negative Power Input Pin. Negative Voltage Connection Pin of Battery 4.
7	CTL	CO Output Control Pin.
8	CO	FET Gate Connection Pin For Charge.
Exposed Pad	EP	Negative Power Input Pin. Negative Voltage Connection Pin of Battery 4.

ELECTRICAL CHARACTERISTICS

(T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DETECTION VOLTAGE							
Over-Charge Detection Voltage n (n = 1, 2, 3, 4)	V_{CUn}	Test Condition 1, Test Circuit 1	SGM41002-4.35	4.314	4.35	4.386	V
			SGM41002-4.45	4.414	4.45	4.486	V
			SGM41002-4.5	4.464	4.5	4.536	V
Over-Charge Hysteresis Voltage n (n = 1, 2, 3, 4)	V_{HCn}	Test Condition 1, Test Circuit 1		-0.422	-0.4	-0.378	V
INPUT VOLTAGE							
Operating Voltage between VDD and VSS	V_{DSOP}				14	24	V
CTL Pin Input High Voltage	V_{CTLH}	Test Condition 5, Test Circuit 2		V_{DD} × 0.95			V
CTL Pin Input Low Voltage	V_{CTLL}	Test Condition 5, Test Circuit 2				V_{DD} × 0.4	V
INPUT CURRENT							
Current Consumption During Operation	I_{OPE}	V1 = V2 = V3 = V4 = 3.5V, Test Condition 6, Test Circuit 3			2.4	3.5	μA
Current Consumption During Over-Discharge	I_{OPED}	V1 = V2 = V3 = V4 = 2.3V, Test Condition 6, Test Circuit 3			2.2	3	μA
VC1 Pin Current	I_{VC1}	V1 = V2 = V3 = V4 = 3.5V, Test Condition 7, Test Circuit 4			0.6	1	μA
VC2 Pin Current	I_{VC2}			-0.5	0.005	0.5	μA
VC3 Pin Current	I_{VC3}			-0.5	0.005	0.5	μA
VC4 Pin Current	I_{VC4}			-0.5	0.005	0.5	μA
CTL Pin Input High Current	I_{CTLH}	V1 = V2 = V3 = V4 = 3.5V, V_{CTL} = V_{DD}, Test Condition 7, Test Circuit 4		0.8	1.2	1.4	μA
CTL Pin Input Low Current	I_{CTLL}	V1 = V2 = V3 = V4 = 3.5V, V_{CTL} = 0V, Test Condition 7, Test Circuit 4		-0.5		0.5	μA
OUTPUT CURRENT							
CO Pin Sink Current	I_{COL}	V_{CO} = V_{SS} + 0.5V, Test Condition 8, Test Circuit 5		0.06	0.1		mA
CO Pin Source Current	I_{COH}	V_{CO} = V_{DD} - 0.5V, Test Condition 8, Test Circuit 5		22	30		μA
DELAY TIME							
Over-Charge Detection Delay Time	t_{CU}	Test Condition 2, Test Circuit 1		1.5	2.8	4.1	s
Over-Charge Timer Reset Delay Time	t_{TR}	Test Condition 3, Test Circuit 1		1.6	9.8	19.2	ms
Over-Charge Release Delay Time	t_{CL}	Test Condition 2, Test Circuit 1		12.8	45.8	83.2	ms
CTL Pin Response Time	t_{CTL}	Test Condition 4, Test Circuit 2		1.5	2.5	3.5	ms

TEST CIRCUITS

● **Test Condition 1 (Test Circuit 1)**

Set V1, V2, V3, and V4 to 3.5V. Over-charge detection voltage 1 (V_{CU1}) is the V1 voltage when CO is "H" after the voltage of V1 has been gradually increased. The over-charge hysteresis voltage (V_{HC1}) is the difference between V1 and V_{CU1} when CO is "L" after the voltage of V1 has been gradually decreased.

Over-charge detection voltage V_{CUn} (n = 2 to 4) and over-charge hysteresis V_{HCn} (n = 2 to 4) can be determined in the same way as when n = 1.

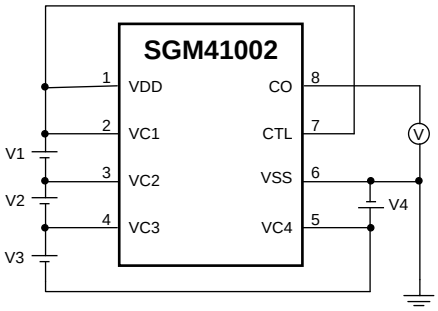
● **Test Condition 2 (Test Circuit 1)**

Set V1, V2, V3, and V4 to 3.5V and in a moment of time (within 10μs) increase V1 up to 5.0V. The over-charge detection delay time (t_{CU}) is the period from when V1 reached 5.0V to when CO becomes "H". After that, in a moment of time (within 10μs) decrease V1 down to 3.5V. The over-charge release delay time (t_{CL}) is the period from when V1 has reached 3.5V to when CO becomes "L".

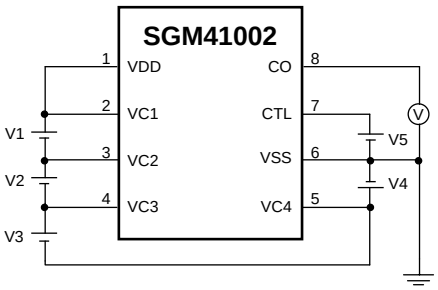
● **Test Condition 3 (Test Circuit 1)**

Set V1, V2, V3, and V4 to 3.5V and in a moment of time (within 10μs) increase V1 up to 5.0V. This is defined as the first rise. Within t_{CU} - 19.2ms after the first rise, in a moment of time (within 10μs) decrease V1 down to 3.5V and then in a moment of time (within 10μs) restore up to 5.0V. This is defined as the second rise. When the period from when V1 was fallen to the second rise is short, CO becomes "H" after t_{CU} has elapsed since the first rise. If the period from when V1 falls to the second rise is gradually made longer, CO becomes "H" when t_{CU} has elapsed since the second rise.

The over-charge timer reset delay time (t_{TR}) is the period from V1 fall till the second rise at that time.



Test Circuit 1



Test Circuit 2

● **Test Condition 4 (Test Circuit 2)**

In the SGM41002, set V1, V2, V3, and V4 to 3.5V and V5 to 14V. The CTL pin response time (t_{CTL}) is the period from when V5 reaches 0V after V5 is in a moment of time (within 10μs) decreased down to 0V to when CO becomes "H".

In the SGM41002, set V1, V2, V3, and V4 to 3.5V and V5 to 14V after an over-voltage is detected and CO becomes "H". In a moment of time (within 10μs) raise V5 from 0V to 14V. The CTL pin response time (t_{CTL}) is the period from when V5 becomes 14V to when CO becomes "L".

● **Test Condition 5 (Test Circuit 2)**

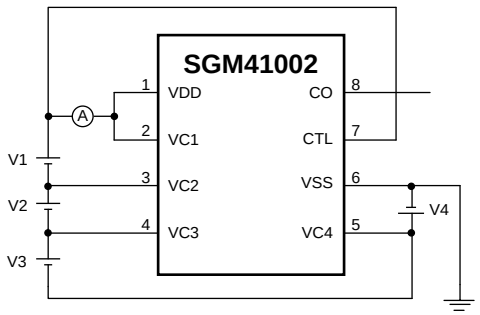
Set V1, V2, V3, and V4 to 3.5V and V5 to 0V. The CTL input "H" voltage (V_{CTLH}) is the maximum voltage of V5 when CO is "L" after V5 has been gradually increased. Next, set V5 to 14V. The CTL input "L" voltage (V_{CTLL}) is the minimum voltage of V5 when CO is "H" after V5 has been gradually decreased.

TEST CIRCUITS (continued)

● **Test Condition 6 (Test Circuit 3)**

The current consumption during operation (I_{OPE}) is the total of the currents that flow in the VDD pin and VC1 pin when V1, V2, V3, and V4 are set to 3.5V.

The current consumption during over-discharge (I_{OPED}) is the total of the currents that flow in the VDD pin and VC1 pin when V1, V2, V3, and V4 are set to 2.3V.

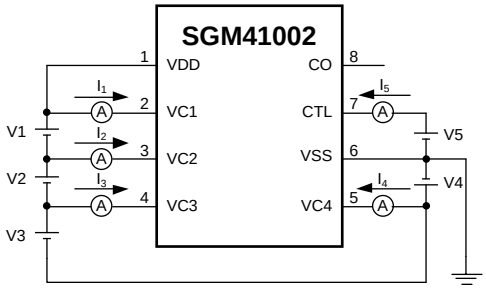


Test Circuit 3

● **Test Condition 7 (Test Circuit 4)**

The VC1 pin current (I_{VC1}) is I_1, the VC2 pin current (I_{VC2}) is I_2, the VC3 pin current (I_{VC3}) is I_3, the VC4 pin current (I_{VC4}) is I_4, and the CTL pin “H” current (I_{CTLH}) is I_5 when V1, V2, V3, and V4 are set to 3.5V, and V5 to 14V.

The CTL pin “L” current (I_{CTLL}) is I_5 when V1, V2, V3, and V4 are set to 3.5V and V5 to 0V.

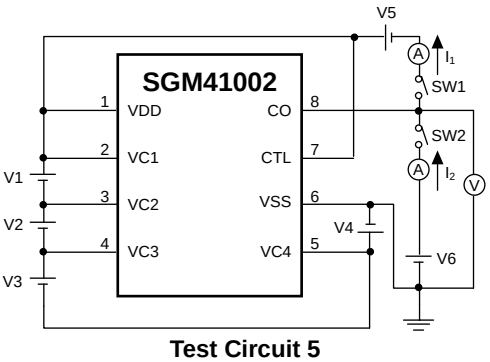


Test Circuit 4

● **Test Condition 8 (Test Circuit 5)**

Set SW1 to OFF and SW2 to ON. The CO pin sink current (I_{COL}) is I_2 when V1, V2, V3, and V4 are set to 3.5V and V6 to 0.5V.

Set SW1 and SW2 to OFF. Set V1 to V5, set V2, V3, and V4 to 3.0V, and set V5 to 0.5V. After t_{CU} has elapsed, set SW1 to ON and SW2 to OFF. I_1 is the CO pin source current (I_{COH}).



Test Circuit 5

OPERATION

Over-Charge Detection

When the voltage of one of the batteries exceeds the over-charge detection voltage (V_{CU}) during charging under normal conditions and the state is retained for the over-charge detection delay time (t_{CU}) or longer, CO becomes “H”. This state is called over-charge. Attaching FET to the CO pin provides charge control and a second protection.

In the SGM41002, if the voltage of all the batteries decreases below the total of the over-charge detection voltage (V_{CU}) and the over-charge hysteresis voltage (V_{HC}) and the state is retained for the over-charge release delay time (t_{CL}) or longer, CO becomes “L”.

Over-Charge Timer Reset

When an over-charge release noise that forces the voltage of the battery temporarily below the over-charge detection voltage (V_{CU}) is input during the over-charge detection delay time (t_{CU}) from when V_{CU} is exceeded to when charging is stopped, t_{CU} is continuously counted if the time the over-charge release noise persists is shorter than the over-charge timer reset delay time (t_{TR}). Under the same conditions, if the time the over-charge release noise persists is t_{TR} or longer, counting of t_{CU} is reset once. After that, when V_{CU} has been exceeded, counting t_{CU} resumes.

CTL Pin

The CTL pin is used to control the output voltage of the CO pin. In the SGM41002, the CTL pin takes precedence over the over-charge detection circuit.

Table 1. Control via CTL Pin

CTL PIN	CO PIN
High	Normal State (1)
Open	“H”
Low	“H”
Low to High	−
High to Low	−

NOTE: 1. The state is controlled by the over-charge detection circuit.

OPERATION (continued)

Timing Charts

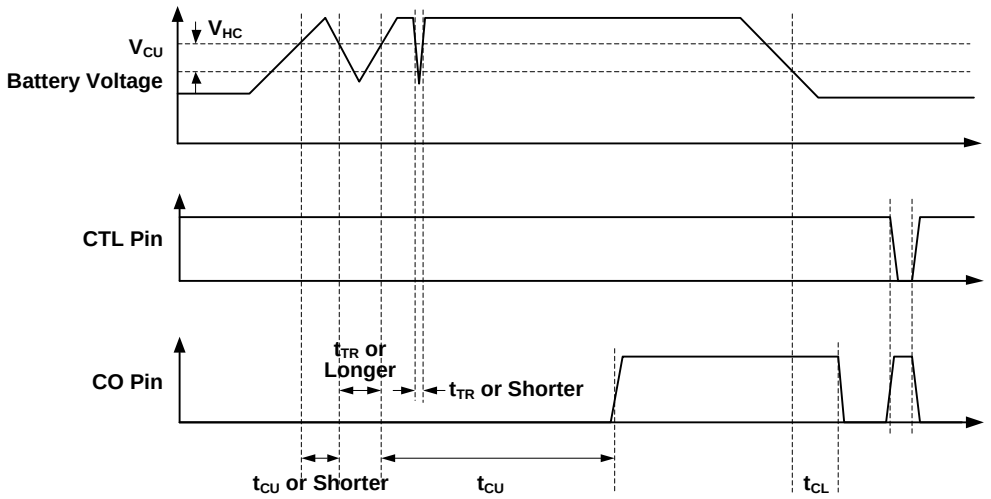


Figure 1. Over-Charge Detection Operation

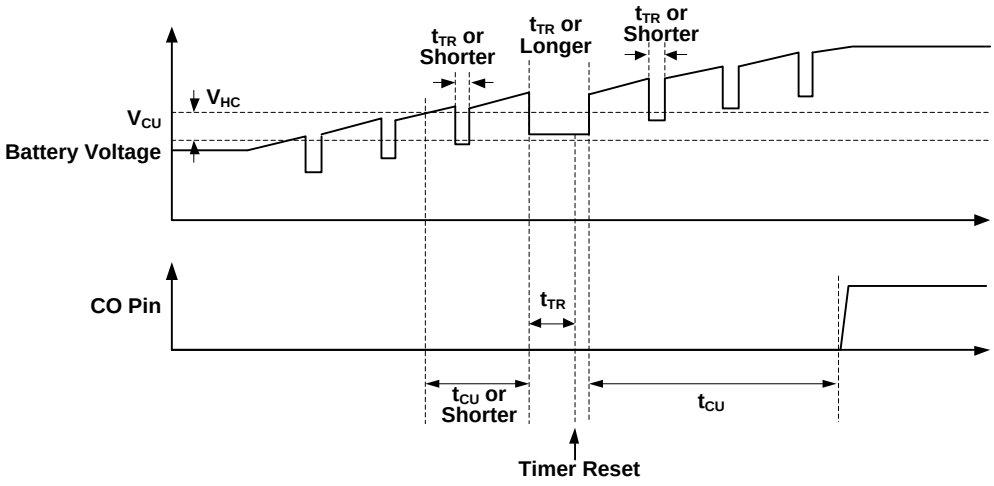


Figure 2. Over-Charge Timer Reset Operation

TYPICAL APPLICATION CIRCUITS

Battery Protection IC Connection Example

- **4-Serial Cell**

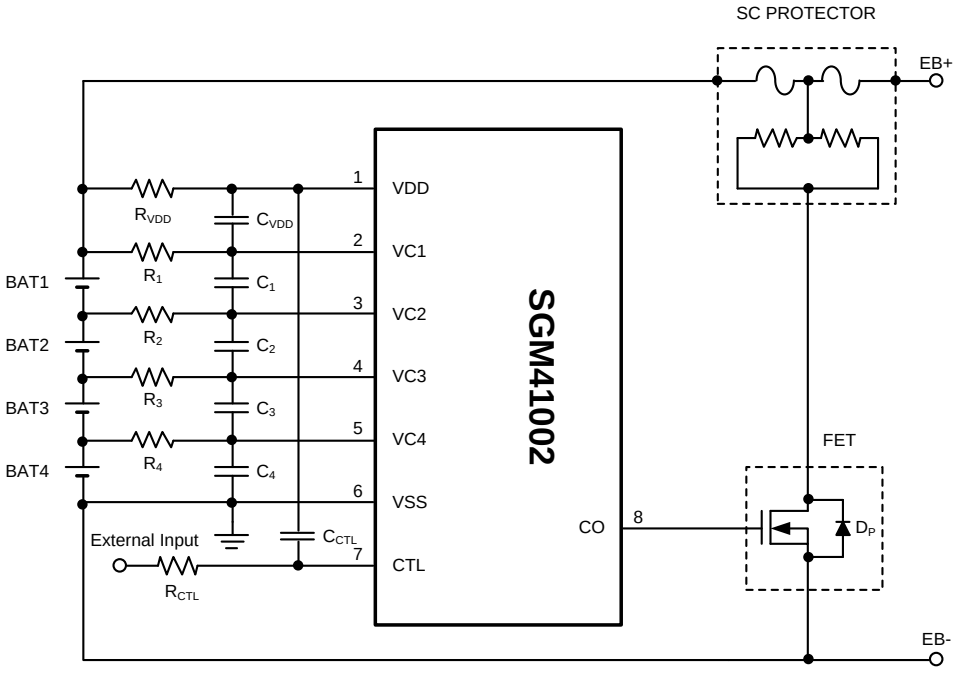


Figure 3. SGM41002 4-Serial Cell Application Circuit

Table 2. Constants for External Components

PART	MIN	TYP	MAX	UNITS
R_1 to R_4	0.1	1	10	kΩ
C_1 to C_4, C_{VDD}	0.01	0.1	1	μF
R_{VDD}	50	100	500	Ω
R_{CTL}	0	100	500	Ω

NOTES:

1. The above constants are subject to change without prior notice.
2. It has not been confirmed whether the operation is normal or not in circuits other than the above example of connection. In addition, the example of connection shown above and the constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.
3. Set the same constants to R_1 to R_4 and to C_1 to C_4 and C_{VDD}.
4. Set R_{VDD}, C_1 to C_4, and C_{VDD} so that the condition (R_{VDD}) × (C_1 to C_4, C_{VDD}) ≥ 5×10^{-6} is satisfied.
5. Set R_1 to R_4, C_1 to C_4, and C_{VDD} so that the condition (R_1 to R_4) × (C_1 to C_4, C_{VDD}) ≥ 1×10^{-4} is satisfied.
6. In the SGM41002, normally input “H” to the external input, and input “L” when setting CO to “H”.
7. Since “H” may be output at CO transiently when the battery is being connected, connect the positive terminal of BAT1 last in order to prevent the three terminal protection fuse from cutoff.

TYPICAL APPLICATION CIRCUITS (continued)

- **3-Serial Cell**

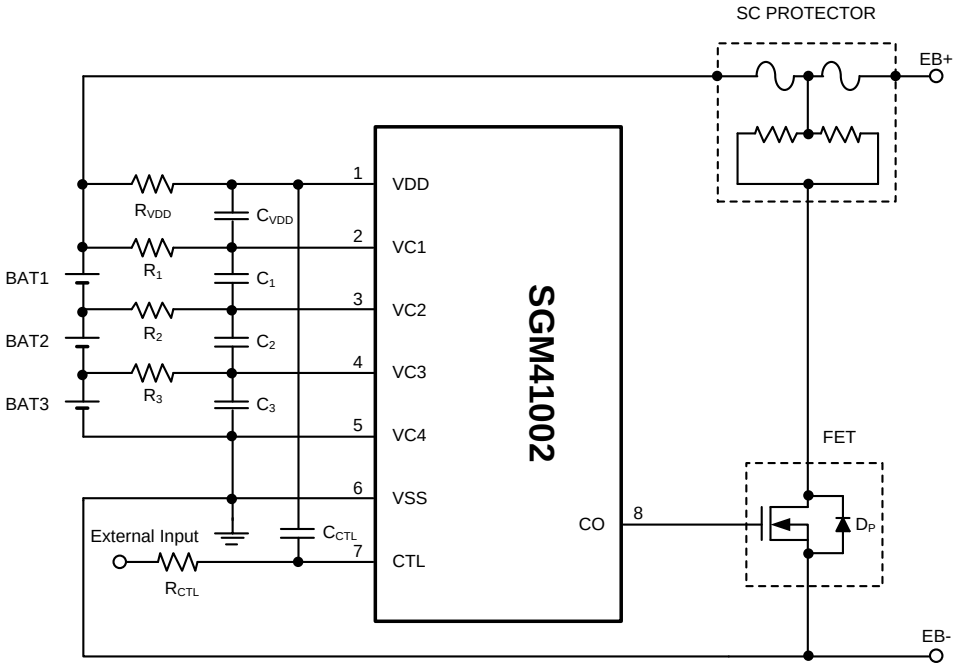


Figure 4. SGM41002 3-Serial Cell Application Circuit

Table 3. Constants for External Components

PART	MIN	TYP	MAX	UNITS
R_1 to R_3	0.1	1	10	kΩ
C_1 to C_3, C_{VDD}	0.01	0.1	1	μF
R_{VDD}	50	100	500	Ω
R_{CTL}	0	100	500	Ω

NOTES:

1. The above constants are subject to change without prior notice.
2. It has not been confirmed whether the operation is normal or not in circuits other than the above example of connection. In addition, the example of connection shown above and the constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.
3. Set the same constants to R_1 to R_3 and to C_1 to C_3 and C_{VDD}.
4. Set R_{VDD}, C_1 to C_3, and C_{VDD} so that the condition (R_{VDD}) × (C_1 to C_3, C_{VDD}) ≥ 5×10^{-6} is satisfied.
5. Set R_1 to R_3, C_1 to C_3, and C_{VDD} so that the condition (R_1 to R_3) × (C_1 to C_3, C_{VDD}) ≥ 1×10^{-4} is satisfied.
6. In the SGM41002, normally input “H” to the external input, and input “L” when setting CO to “H”.
7. Since “H” may be output at CO transiently when the battery is being connected, connect the positive terminal of BAT1 last in order to prevent the three terminal protection fuse from cutoff.

TYPICAL APPLICATION CIRCUITS (continued)

- **2-Serial Cell**

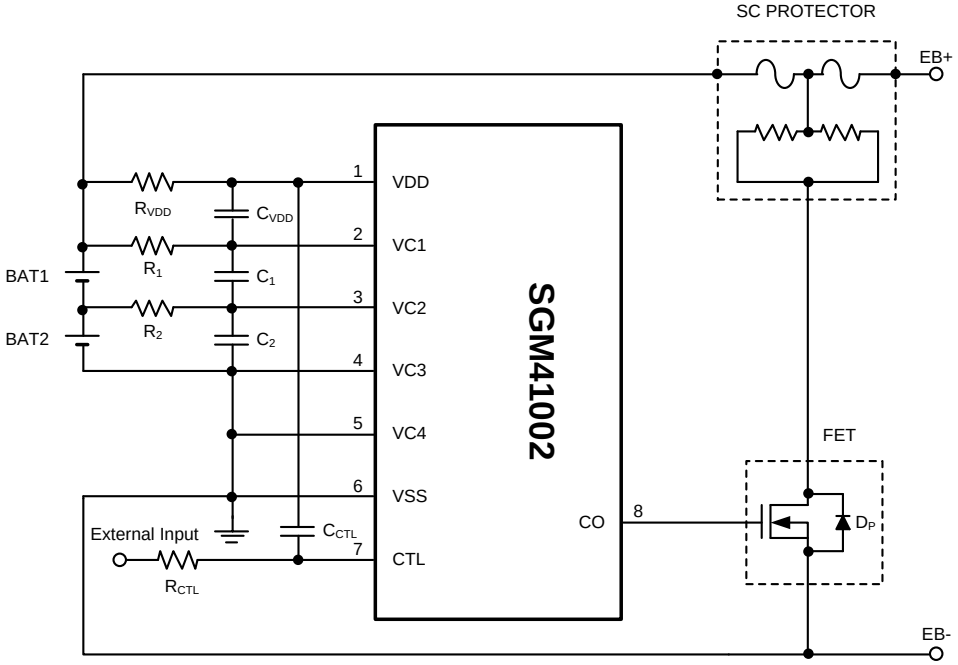


Figure 5. SGM41002 2-Serial Cell Application Circuit

Table 4. Constants for External Components

PART	MIN	TYP	MAX	UNITS
R_1 to R_2	0.1	1	10	kΩ
C_1 to C_2, C_{VDD}	0.01	0.1	1	μF
R_{VDD}	50	100	500	Ω
R_{CTL}	0	100	500	Ω

NOTES:

1. The above constants are subject to change without prior notice.
2. It has not been confirmed whether the operation is normal or not in circuits other than the above example of connection. In addition, the example of connection shown above and the constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.
3. Set the same constants to R_1 to R_2 and to C_1 to C_2 and C_{VDD}.
4. Set R_{VDD}, C_1 to C_2, and C_{VDD} so that the condition (R_{VDD}) × (C_1 to C_2, C_{VDD}) ≥ 5×10^{-6} is satisfied.
5. Set R_1 to R_2, C_1 to C_2, and C_{VDD} so that the condition (R_1 to R_2) × (C_1 to C_2, C_{VDD}) ≥ 1×10^{-4} is satisfied.
6. In the SGM41002, normally input “H” to the external input, and input “L” when setting CO to “H”.
7. Since “H” may be output at CO transiently when the battery is being connected, connect the positive terminal of BAT1 last in order to prevent the three terminal protection fuse from cutoff.

REVISION HISTORY

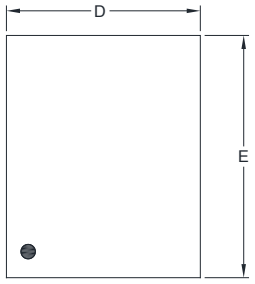
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (SEPTEMBER 2017) to REV.A

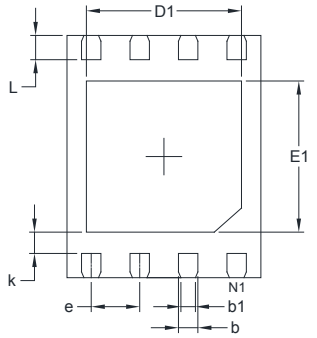
Changed from product preview to production data ..... All

PACKAGE OUTLINE DIMENSIONS

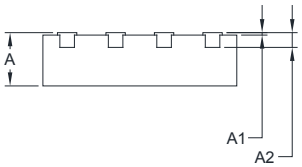
UTDFN-2×2.5-8L



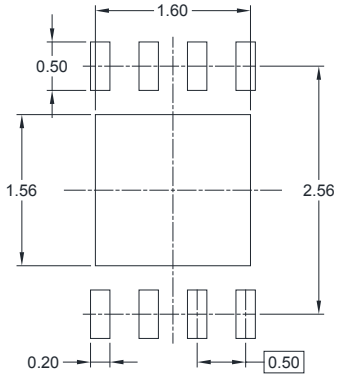
TOP VIEW



BOTTOM VIEW



SIDE VIEW

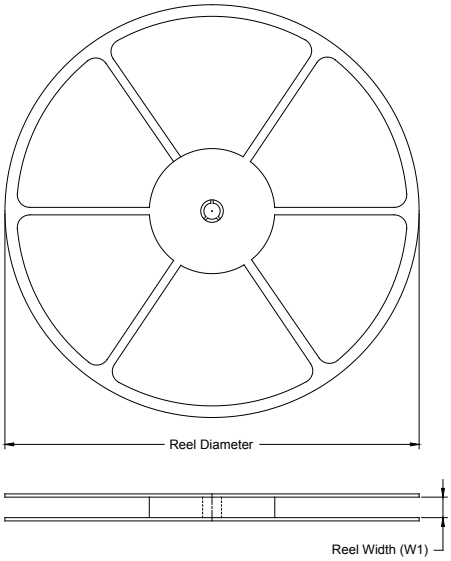


RECOMMENDED LAND PATTERN (Unit: mm)

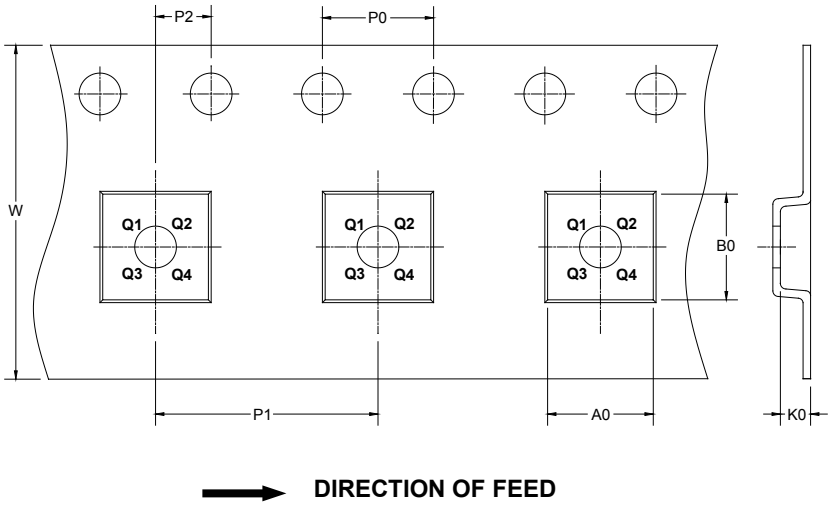
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.500	0.600	0.020	0.024
A1	0.000	0.050	0.000	0.002
A2	0.152 REF		0.006 REF	
D	1.900	2.100	0.075	0.083
D1	1.500	1.700	0.059	0.067
E	2.400	2.600	0.094	0.102
E1	1.460	1.660	0.057	0.065
b	0.150	0.250	0.006	0.010
b1	0.150 REF		0.006 REF	
e	0.500 BSC		0.020 BSC	
k	0.220 REF		0.009 REF	
L	0.174	0.326	0.007	0.013

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



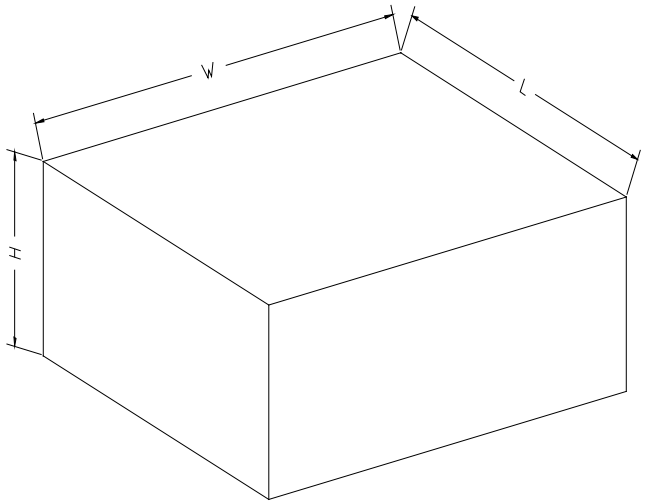
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
UTDFN-2×2.5-8L	7″	9.0	2.25	2.75	0.70	4.0	4.0	2.0	8.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002