SGM40653/SGM40654/SGM40655
High-Current Over-Voltage Protector

GENERAL DESCRIPTION

The SGM40653/4/5 over-voltage protection devices feature a low 62mΩ (TYP, CSP package)/73mΩ (TYP, TDFN package) R_{ON} internal FET and protect low-voltage systems against voltage faults up to +28V_{DC}. An internal clamp also protects the devices from surges up to +120V. When the input voltage exceeds the over-voltage threshold, the internal FET is turned off to prevent damage to the protected downstream components.

The over-voltage protection threshold can be adjusted with optional external resistors to any voltage between 4V and 20V. If the OVLO input is below the external OVLO select voltage, the SGM40653/4/5 automatically choose the internal trip thresholds. The internal over-voltage thresholds (V_{IN_OVLO}) are preset to be 15.39V/6.8V/5.81V typical (SGM40653/4/5). The devices feature an open-drain $\overline{ACOK}$ output indicating a stable supply between minimum supply voltage and V_{OVLO}. The SGM40653/4/5 are also protected against over-current events by an internal thermal shutdown. The SGM40653/4/5 also have enable control to reduce power consumption.

The SGM40653/4/5 are available in Green TDFN-3×3-12L and WLCSP-1.30×1.83-12B packages, and operate over an ambient temperature range of -40℃ to +85℃.

FEATURES

- **Protect High-Power Portable Devices**
  - **Wide Operating Input Voltage Protection from 2.5V to 28V**
  - **Integrated 62mΩ (TYP) N-Channel MOSFET Switch (CSP Package)**
  - **Integrated 73mΩ (TYP) N-Channel MOSFET Switch (TDFN Package)**
- **Flexible Over-Voltage Protection Design**
  - **Adjustable Over-Voltage Protection Trip Level**
  - **Wide Adjustable OVLO Threshold Range from 4V to 20V**
  - **Internal Preset OVLO Thresholds:**
    15.39V (SGM40653)
    6.8V (SGM40654)
    5.81V (SGM40655)
- **Additional Protection Features Increase System Reliability**
  - **Surge Immunity up to +120V**
  - **Soft-Start to Minimize In-Rush Current**
  - **Internal 18.5ms Startup Debounce**
  - **Thermal Shutdown Protection**
- **Enable Function**
- **-40℃ to +85℃ Operating Temperature Range**
- **Available in Green WLCSP-1.30×1.83-12B and TDFN-3×3-12L Packages**

APPLICATIONS

Smart Phones
Tablet PCs
Mobile Internet Devices

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM40653	WLCSP-1.30×1.83-12B	-40℃ to +85℃	SGM40653YG/TR	XXXXX SZ0YG	Tape and Reel, 3000
SGM40654	WLCSP-1.30×1.83-12B	-40℃ to +85℃	SGM40654YG/TR	XXXXX SXDYG	Tape and Reel, 3000
	TDFN-3×3-12L	-40℃ to +85℃	SGM40654YTDF12G/TR	SGM 40654DF XXXXX	Tape and Reel, 4000
SGM40655	WLCSP-1.30×1.83-12B	-40℃ to +85℃	SGM40655YG/TR	XXXXX SZ1YG	Tape and Reel, 3000
	TDFN-3×3-12L	-40℃ to +85℃	SGM40655YTDF12G/TR	SGM 40655DF XXXXX	Tape and Reel, 4000

NOTE: XXXXX = Date Code and Vendor Code.

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

IN (with respect to GND)..... -0.3V to 28V
IN (with respect to GND)..... +120V, 1.2/50μs, 2Ω surge (1) (2)
OUT (with respect to GND).....-0.3V to V_{IN} + 0.3V
OVLO..... -0.3V to 26.4V
$\overline{ACOK}$, $\overline{EN}$ (with respect to GND) ..... -0.3V to 6V
Continuous IN, OUT Current (3)
WLCSP-1.30×1.83-12B Package.....4.5A
TDFN-3×3-12L Package 4.5A
Peak IN, OUT Current (10ms), CSP Package 8A
Package Thermal Resistance
TDFN-3×3-12L, θ_{JA}..... 85℃/W
Junction Temperature.....+150℃
Storage Temperature Range .....-65℃ to +150℃
Lead Temperature (Soldering 10 sec) .....+260℃
ESD Susceptibility
HBM.....4000V
MM.....400V
CDM 1000V

NOTES:
1. Surge pulse in compliance with IEC61000-4-5 specification.
2. Survives burst pulse up to +120V with 2Ω series resistance.
3. Continuous current limited by thermal design.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range .....2.5V to 28V
Operating Temperature Range .....-40℃ to +85℃

OVERSTRESS CAUTION

Stresses beyond those listed may cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ESD SENSITIVITY CAUTION

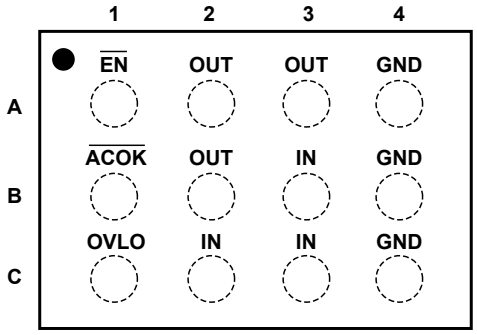
This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time.

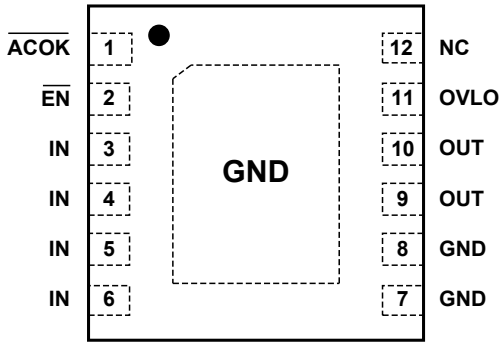
PIN CONFIGURATIONS

SGM40653/4/5 (TOP VIEW)



WLCSP-1.30×1.83-12B

SGM40654/5 (TOP VIEW)



TDFN-3×3-12L

PIN DESCRIPTION

PIN		NAME	FUNCTION
WLCSP-1.30×1.83-12B	TDFN-3×3-12L		
A1	2	$\overline{EN}$	Enable Control. When $\overline{EN}$ = "Low", chip is enabled; when $\overline{EN}$ = "High", chip is in disable status.
A2, A3, B2	9, 10	OUT	Output Voltage. Output of internal switch. Connect OUT pins together for proper operation.
A4, B4, C4	7, 8	GND	Ground. Connect GND pins together for proper operation.
B1	1	$\overline{ACOK}$	Open-Drain Flag Output. $\overline{ACOK}$ is driven low after input voltage is stable between minimum V_{IN} and V_{OVLO} after debounce. Connect a pull-up resistor from $\overline{ACOK}$ to the logic I/O voltage of the host system. $\overline{ACOK}$ is high impedance after thermal shutdown.
B3, C2, C3	3, 4, 5, 6	IN	Input Voltage. Bypass IN with a 0.1μF ceramic capacitor as close as possible to the device. Connect IN pins together for proper operation.
C1	11	OVLO	External OVLO Adjustment. Connect OVLO to GND when using the internal threshold. Connect a resistor-divider to OVLO to set a different OVLO threshold; this external resistor-divider is completely independent of the internal threshold.
–	12	NC	No Connection.

ELECTRICAL CHARACTERISTICS

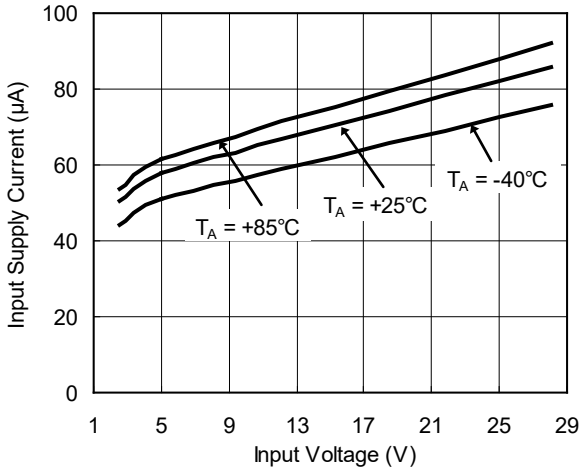
(V_{IN} = 2.5V to 28V, $\overline{EN}$ = 0V, C_{IN} = 0.1μF, T_A = -40℃ to +85℃, typical values are at V_{IN} = 5V, I_{IN} ≤ 3A, T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}			2.5		28	V
Input Clamp Triggering Voltage	V_{IN_CLAMP}	I_{IN} = 10mA limited, T_A = +25℃			28.6		V
Input Supply Current	I_{IN}	V_{IN} = 5V			56	85	μA
OVLO Supply Current	I_{IN_Q}	V_{OVLO} = 3V, V_{IN} = 5V, V_{OUT} = 0V			56	85	μA
Shutdown Current	I_{Q_OFF}	V_{IN} = 5V, $\overline{EN}$ = 2V				1	μA
Internal Over-Voltage Trip Level	V_{IN_OVLO}	V_{IN} rising	SGM40653	14.84	15.39	15.93	V
			SGM40654	6.59	6.8	7.01	
			SGM40655	5.64	5.81	5.98	
		V_{IN} falling	SGM40653	14.45	15.07		
			SGM40654	6.43	6.66		
			SGM40655	5.50	5.69		
V_{BG} Reference	V_{BG}			1.18	1.218	1.26	V
Adjustable OVLO Threshold Range				4		20	V
External OVLO Select Threshold	V_{OVLO_SELECT}			0.22	0.26	0.30	V
Switch On-Resistance	R_{ON}	V_{IN} = 5V, I_{OUT} = 0.5A, T_A = +25℃	WLCSP-1.30×1.83-12B		62	88	mΩ
			TDFN-3×3-12L		73		
OUT Load Capacitance	C_{OUT}	V_{IN} = 5V				1000	μF
OVLO Input Leakage Current	I_{OVLO}	V_{OVLO} = 1.3V			10	100	nA
IN Leakage Voltage by OVLO	V_{IN_LEAK}	V_{OVLO} = 20V, V_{IN} = unconnected, R_{OVLO} = 1MΩ			0.01	0.20	V
Thermal Shutdown					138		℃
Thermal Shutdown Hysteresis					30		℃
DIGITAL SIGNAL ($\overline{ACOK}$)							
$\overline{ACOK}$ Output Low Voltage	V_{OL}	$V_{I/O}$ = 3.3V, I_{SINK} = 1mA, See Figure 1			0.26	0.43	V
$\overline{ACOK}$ Leakage Current	I_{ACOK_LEAK}	$V_{I/O}$ = 3.3V, $\overline{ACOK}$ deasserted, See Figure 1			0.01	1	μA
TIMING CHARACTERISTICS							
Debounce Time	t_{DEB}	Time from V_{IN} > 2.5V to the time V_{OUT} starts rising			18.5		ms
Soft-Start Time	t_{SS}	Time from V_{IN} > 2.5V to soft-start off			37		ms
Switch Turn-On Time	t_{ON}	V_{IN} = 5V, R_L = 100Ω, C_{LOAD} = 100μF, V_{OUT} from 10%, V_{IN} to 90% V_{IN}			8		ms
Switch Turn-Off Time	t_{OFF}	V_{IN} > V_{IN_OVLO} to V_{OUT} = 80% of V_{IN}, R_L = 100Ω, V_{IN} rising at 2V/μs			120		ns
$\overline{EN}$ LOGIC LEVELS							
Logic Low Input Voltage	V_{IL}					0.4	V
Logic High Input Voltage	V_{IH}	The rising rate of $\overline{EN}$ waveform that rises from 0.5V to 1.6V > 2V/ms		1.6			V
Input Low Current	I_{IL}	V_{IN} = 5V, $\overline{EN}$ = 0V				1	μA
Input High Current	I_{IH}	V_{IN} = 5V, $\overline{EN}$ = 5V				2	μA

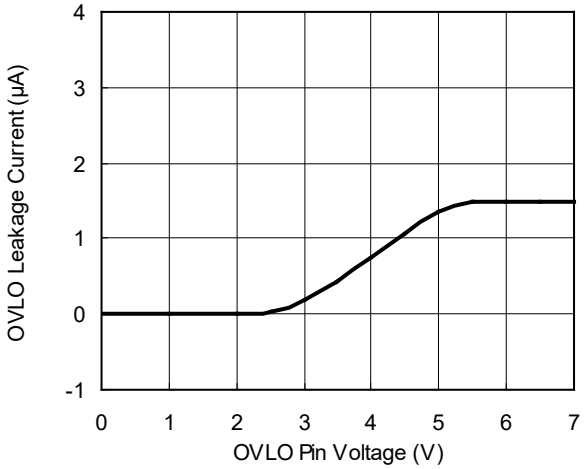
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, $\overline{EN}$ = 0V, C_{IN} = 0.1μF, C_{OUT} = 1μF, T_A = +25℃, unless otherwise noted.

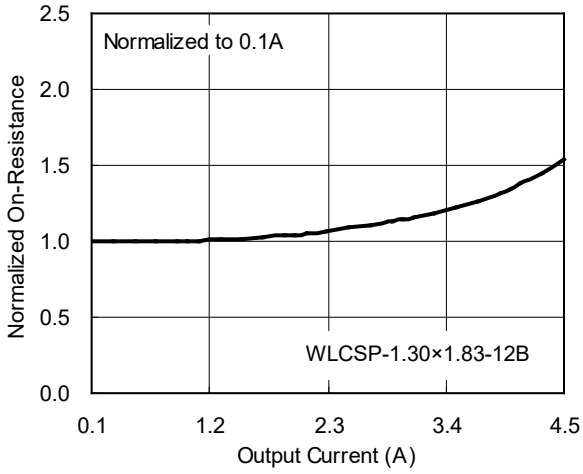
Input Supply Current vs. Input Voltage



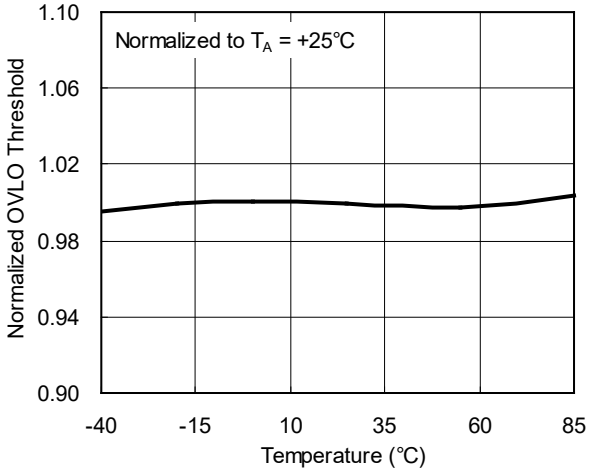
OVLO Leakage Current vs. OVLO Pin Voltage



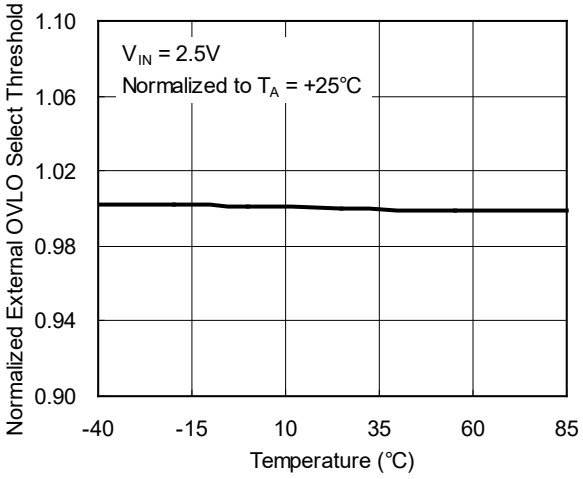
Normalized On-Resistance vs. Output Current



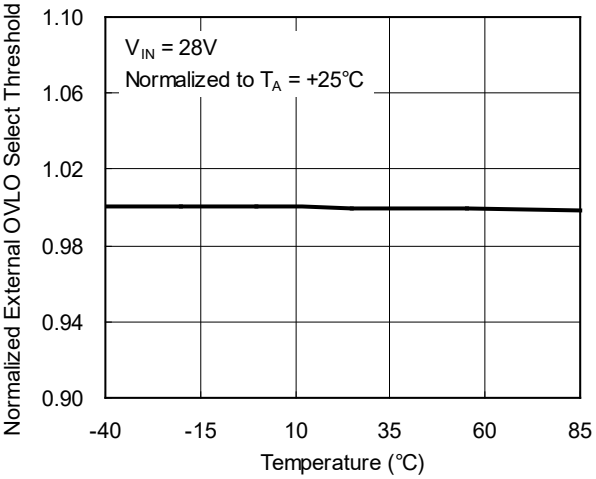
Normalized OVLO Threshold vs. Temperature



Normalized External OVLO Select Threshold vs. Temperature



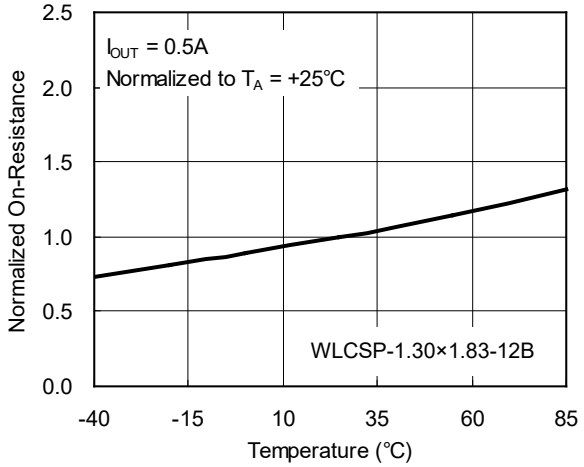
Normalized External OVLO Select Threshold vs. Temperature



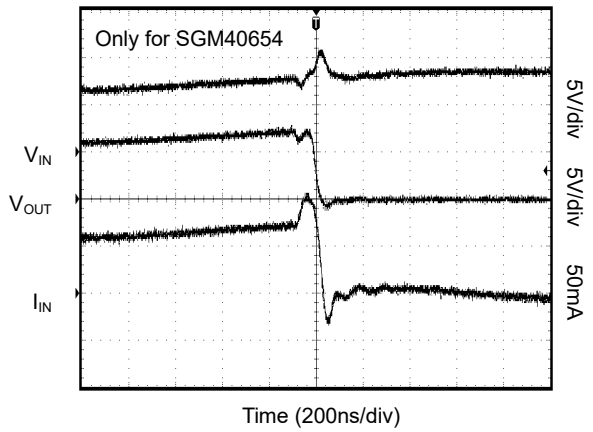
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 5V, $\overline{EN}$ = 0V, C_{IN} = 0.1μF, C_{OUT} = 1μF, T_A = +25℃, unless otherwise noted.

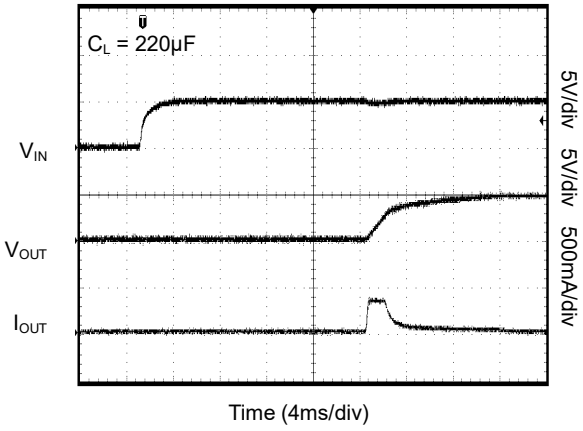
Normalized On-Resistance vs. Temperature



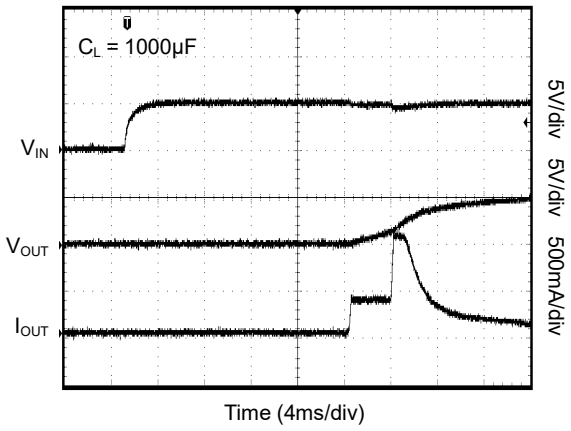
Over-Voltage Fault Response



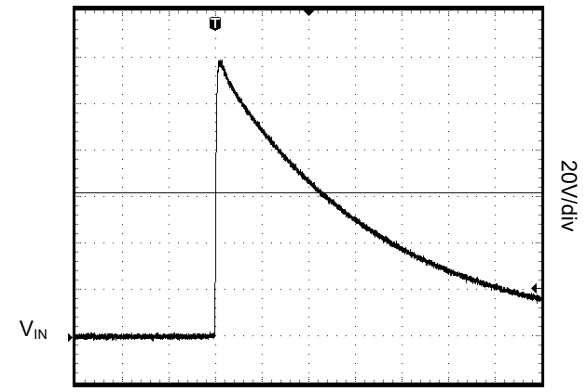
Power-Up Response



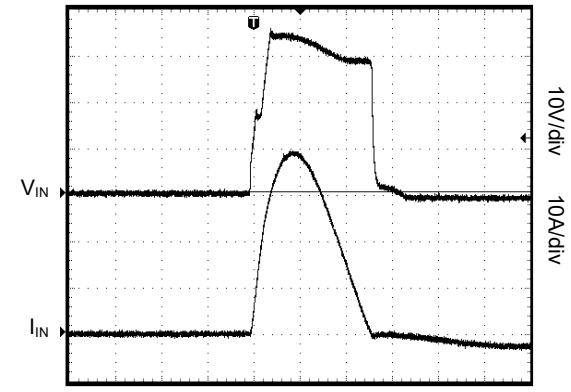
Power-Up Response



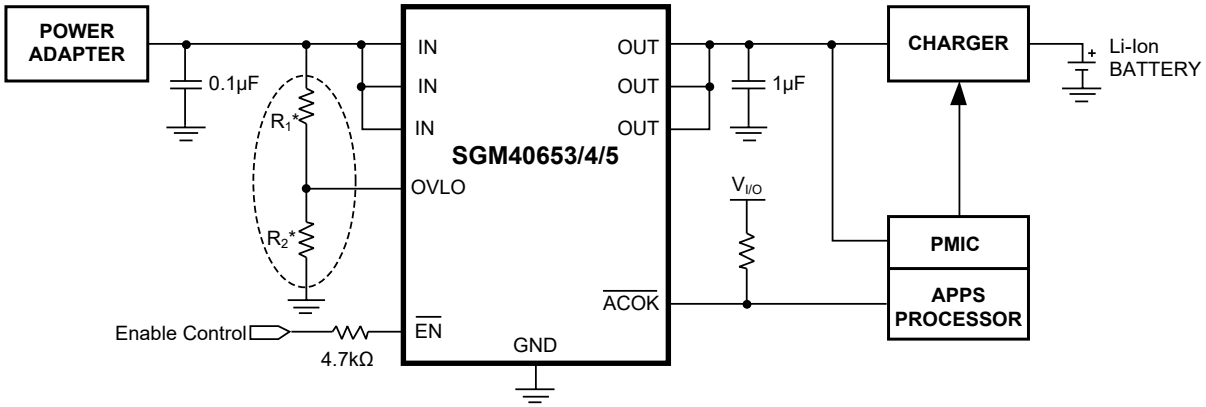
Open Circuit Voltage Waveform without SGM40653/4/5, +120V, 1.2/50μs Surge



IN-GND 120V Surge Discharge Waveforms



TYPICAL APPLICATION



* R_1 and R_2 are only required for adjustable OVLO; otherwise, connect OVLO to GND.

Figure 1. Typical Application Circuit

FUNCTIONAL BLOCK DIAGRAM

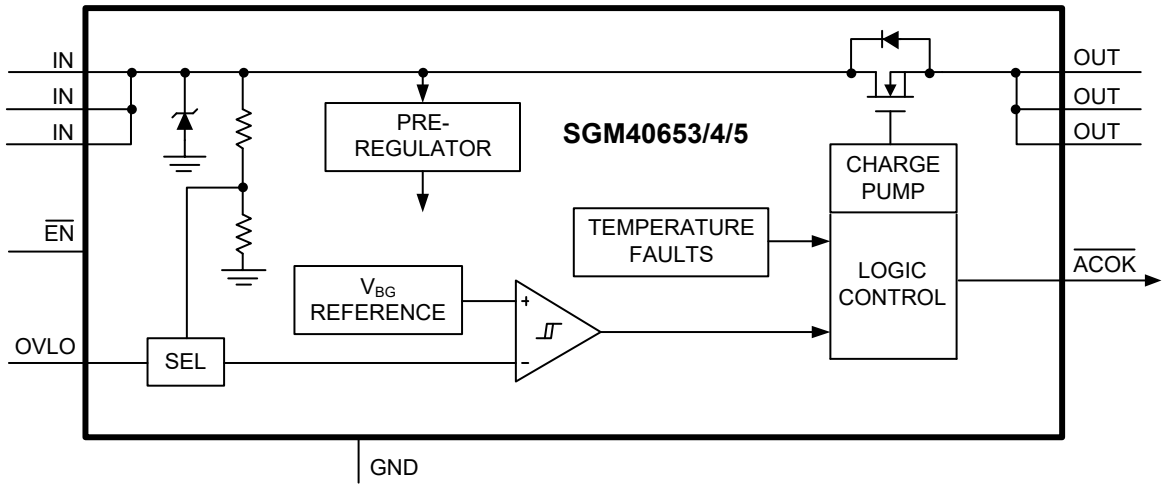
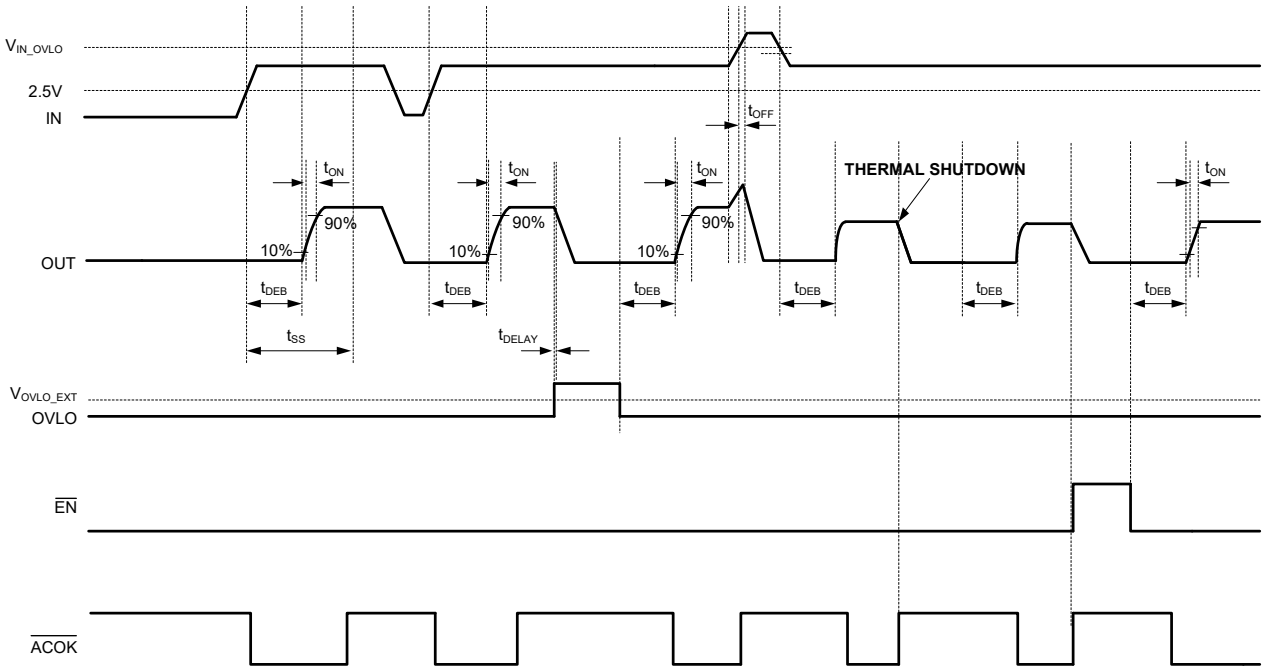


Figure 2. Block Diagram

TIMING DIAGRAM



NOTE: Waveforms are not to scale.

Figure 3. Timing Diagram

SURGE UP TEST CIRCUIT

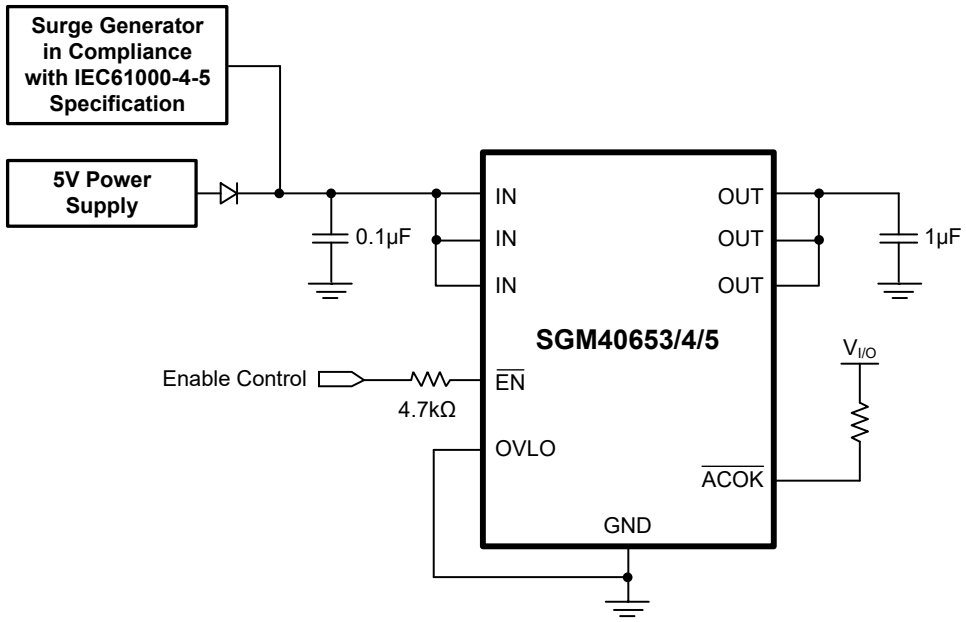


Figure 4. Surge Up Test Circuit

DETAILED DESCRIPTION

The SGM40653/4/5 over-voltage protection devices feature a low on-resistance (R_{ON}) internal FET and protect low-voltage systems against voltage faults up to +28V_{DC}. An internal clamp also protects the devices from surges up to +120V. Surge up tests are operated according to the test circuit in Figure 4. If the input voltage exceeds the over-voltage threshold, the internal FET is turned off to prevent damage to the protected components. A 18.5ms (TYP) debounce time built into the device prevents false turn-on of the internal FET during startup.

Device Operation

The devices contain timing logic that controls the turn-on of the internal FET. The internal charge pump is enabled when V_{IN} < V_{IN_OVLO}, if internal trip thresholds are used or when V_{OVLO} < V_{OVLO_EXT} if external trip thresholds are used. The charge-pump after a 18.5ms (TYP) debounce delay, turns the internal FET on (see Figure 2). After the debounce time, soft-start limits the FET inrush current for 18.5ms (TYP). At any time, if V_{IN} rises above V_{OVLO_THRESH}, OUT is disconnected from IN.

Enable Function

The IC has an enable pin which is used to enable or disable the device. Connect the $\overline{EN}$ pin high to turn off the internal pass FET. Connect the $\overline{EN}$ pin low to turn on the internal pass FET and enter the start-up routine.

Internal Switch

The SGM40653/4/5 incorporate an internal FET with a 62mΩ (TYP, CSP package)/73mΩ (TYP, TDFN package) R_{ON}. The FET is internally driven by a charge pump that generates a necessary gate voltage above IN.

Over-Voltage Lockout (OVLO)

The SGM40653/4/5 has 15.39V/6.8V/5.81V (TYP) over-voltage threshold (OVLO) respectively.

Thermal Shutdown Protection

The SGM40653/4/5 feature thermal shutdown circuitry. The internal FET turns off when the junction temperature exceeds +138℃ (TYP). The device exits thermal shutdown after the junction temperature cools by 30℃ (TYP).

$\overline{ACOK}$ Output

An open-drain $\overline{ACOK}$ output gives the SGM40653/4/5 the ability to communicate a stable power source to the host system. $\overline{ACOK}$ is driven low after input voltage is stable between minimum V_{IN} and V_{OVLO} after debounce. Connect a pull-up resistor from $\overline{ACOK}$ to the logic I/O voltage of the host system. $\overline{ACOK}$ is high impedance after thermal shutdown.

USB OTG Support

When used in an OTG application the SGM40653/4/5 can provide power from OUT to IN. Initially, the OTG voltage applied at OUT will forward-bias the power switch bulk diode and present a voltage drop of approximately 0.7V between OUT and IN. This is purely a transitionary condition as once the voltage at IN exceeds the UVLO voltage of 2.4V (TYP) and the debounce time has elapsed, the main power switch will turn fully on, significantly reducing the voltage drop from OUT to IN. In this mode，the part is able to supply a continuous current up to 2.5A (TDFN package)/3A (CSP package) to the OTG load.

APPLICATION INFORMATION

Bypass Capacitor

For most applications, bypass IN to GND with a 0.1μF ceramic capacitor as close as possible to the device. If the power source has significant inductance due to long lead length, the device clamps the overshoot due to LC tank circuit.

Output Capacitor

The slow turn-on time provides a soft-start function that allows the SGM40653/4/5 to charge an output capacitor up to 1000μF without turning off due to an over-current condition.

External OVLO Adjustment Functionality

If OVLO is connected to ground, the internally set OVLO value will be applied.

If an external resistor-divider is connected to OVLO and V_{OVLO} exceeds the OVLO select voltage, V_{OVLO_SELECT}, the internal OVLO comparator reads the IN fraction fixed by the external resistor divider. R_1 = 1MΩ is a good starting value for minimum current consumption. Since $V_{IN\_OVLO\_EXT}$, V_{BG}, and R_1 are known, R_2 can be calculated from the following formula:

$$V_{IN\_OVLO\_EXT} = V_{BG} \times \left[1 + \frac{R_1}{R_2}\right]$$

This external resistor-divider is completely independent from the internal resistor-divider.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DECEMBER 2017 – REV.B.2 to REV.B.3

Changed Pin Configurations section ..... All

AUGUST 2017 – REV.B.1 to REV.B.2

Changed Electrical Characteristics section 4

JUNE 2017 – REV.B to REV.B.1

Added package thermal resistance 2
Changed Absolute Maximum Ratings section 2

APRIL 2017 – REV.A.4 to REV.B

Changed Package/Ordering Information section 2

JANUARY 2017 – REV.A.3 to REV.A.4

Changed Detailed Description section 9

JANUARY 2017 – REV.A.2 to REV.A.3

Changed Absolute Maximum Ratings section 2
Changed Electrical Characteristics section 4

NOVEMBER 2016 – REV.A.1 to REV.A.2

Added TDFN-3×3-12L package ..... All

AUGUST 2016 – REV.A to REV.A.1

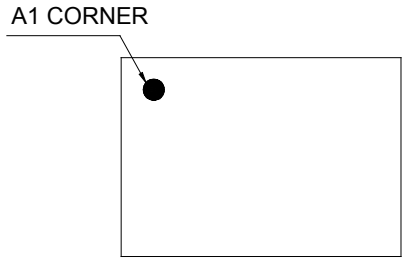
Changed Electrical Characteristics section 4

Changes from Original (FEBRUARY 2016) to REV.A

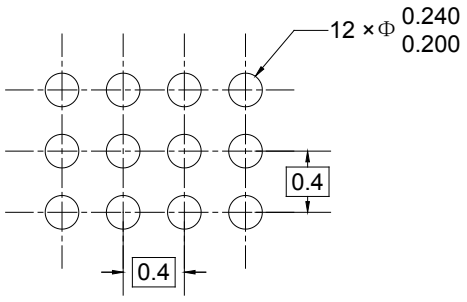
Changed from product preview to production data ..... All

PACKAGE OUTLINE DIMENSIONS

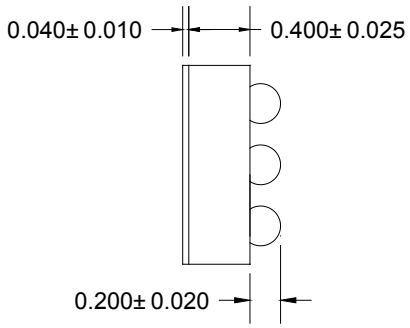
WLCSP-1.30×1.83-12B



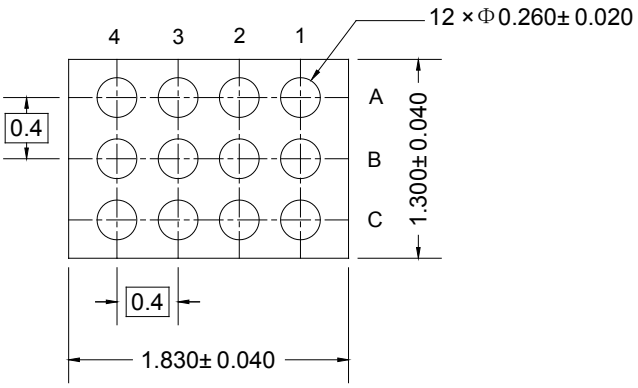
TOP VIEW



RECOMMENDED LAND PATTERN



SIDE VIEW

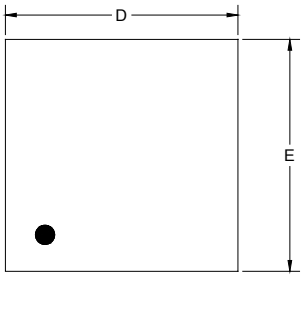


BOTTOM VIEW

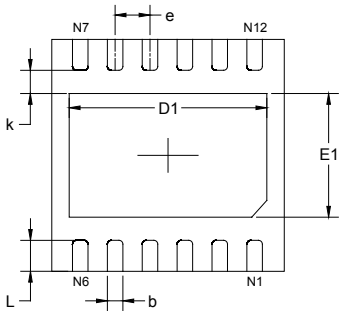
NOTE: All linear dimensions are in millimeters.

PACKAGE OUTLINE DIMENSIONS

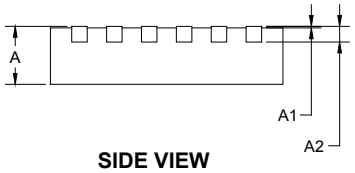
TDFN-3×3-12L



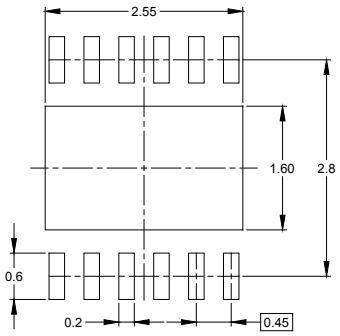
TOP VIEW



BOTTOM VIEW



SIDE VIEW

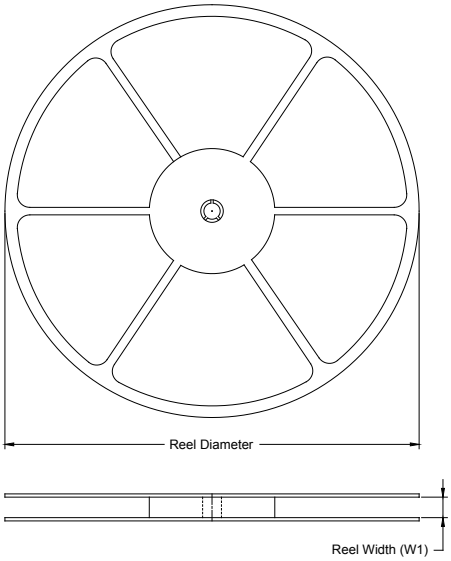


RECOMMENDED LAND PATTERN (Unit: mm)

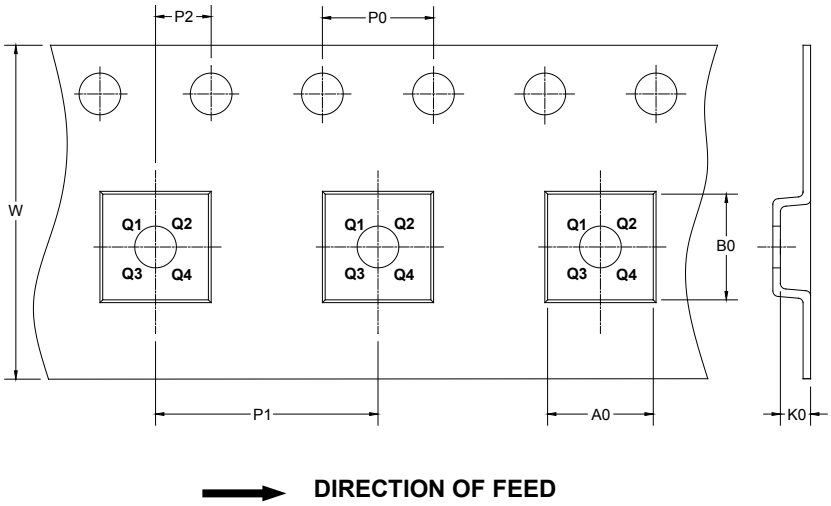
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
D	2.924	3.076	0.115	0.121
D1	2.450	2.650	0.096	0.104
E	2.924	3.076	0.115	0.121
E1	1.500	1.700	0.059	0.067
k	0.200 MIN		0.008 MIN	
b	0.150	0.250	0.006	0.010
e	0.450 TYP		0.018 TYP	
L	0.324	0.476	0.013	0.019

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



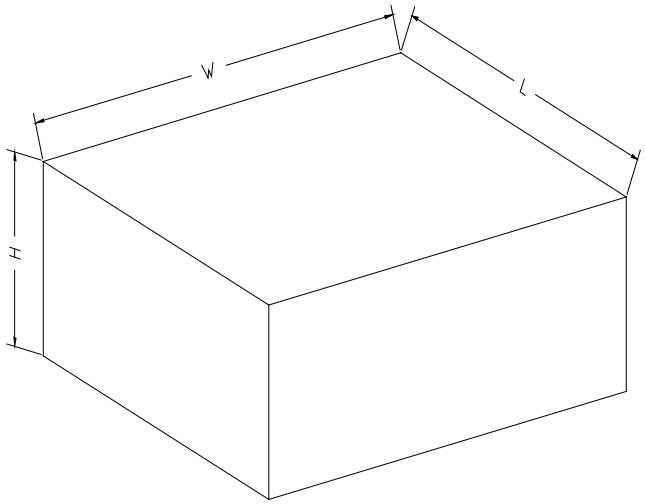
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
WLCSP-1.30×1.83-12B	7″	9.2	1.40	2.00	0.80	4.0	4.0	2.0	8.0	Q2
TDFN-3×3-12L	13″	12.4	3.30	3.30	1.10	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18
13″	386	280	370	5

DD0002