30 V, 2 A, Synchronous PWM Step-down DC/DC Converter

No. EA-370-201203

OVERVIEW

The R1275S is a 36-V synchronous step-down DC/DC converter with built-in drivers. It is designed for industrial equipment, OA equipment and home electronics that require a 24-V input. It operates at a 2-MHz switching frequency, which allows to use a small inductor to ensure a high transient response and to maintain a high efficiency at heavy load condition. Using a spread spectrum clock generator, the EMI noise can be reduced.

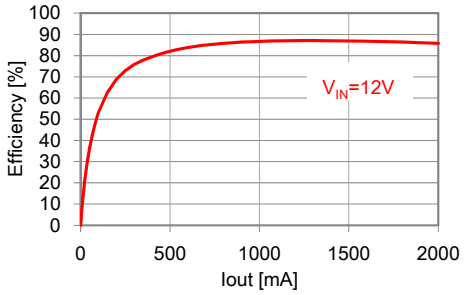
KEY BENEFITS

- **Provides a high switching frequency at 2 MHz with an efficiency of 87%.**
- **Maintains the output voltage constant by reducing a switching frequency to the minimum 1/4 when an input-output voltage difference is small.**
- **Achieves the EMI noise reduction by using a spread spectrum clock generator. (Diffusion Rate: +8%).**

KEY SPECIFICATIONS

- Input Voltage Range (Maximum Ratings): 3.6 V to 30 V (36 V)
- Start-up Voltage: 4.5 V
- Standby Current: Typ. 4 μA
- Output Voltage Range: 3.3 V to 5.0 V
- Feedback Voltage: 0.64 V ±1.0%
- Adjustable Oscillator Frequency Using External Resistors: 2 MHz
- External Synchronous Clock Frequency: 1.8 MHz to 2.2 MHz
- Spread Spectrum Clock Generator (SSCG): Diffusion Rate: Typ. +8%
- Minimum On-time: Typ. 70 ns
- Minimum Off-time: Typ. 120 ns
- Duty-over: Min. 1/4
- Soft-start
- Thermal Shutdown: Tj = 160°C
- Undervoltage Lockout (UVLO): V_{CC} = 3.3 V (Typ.)
- Overvoltage Lockout (OVLO): V_{IN} = 35 V (Typ.)
- Overvoltage Detection (OVD): FB Pin Voltage (V_{FB}) +10%
- LX Current Limiting: Typ. 3 A
- High-side Driver On Resistance: Typ. 0.145 Ω
- Low-side Driver On Resistance: Typ. 0.095 Ω

TYPICAL CHARACTERISTICS



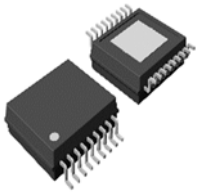
Efficiency (V_{OUT} = 5 V)

OPTIONAL FUNCTIONS

Choose the optional functions from below.

*	Overcurrent Protection	SSCG
A	Hiccup-type	Disable
C	Hiccup-type	Enable

PACKAGE



HSOP-18

5.2mm x 6.2mm x 1.45mm

APPLICATIONS

- Digital Electronics: Digital TVs, DVD Players
- OA Equipment: Printers, Facsimiles
- Portable Communication Equipment, Cameras, Video Cameras
- Battery-powered Equipment

SELECTION GUIDE

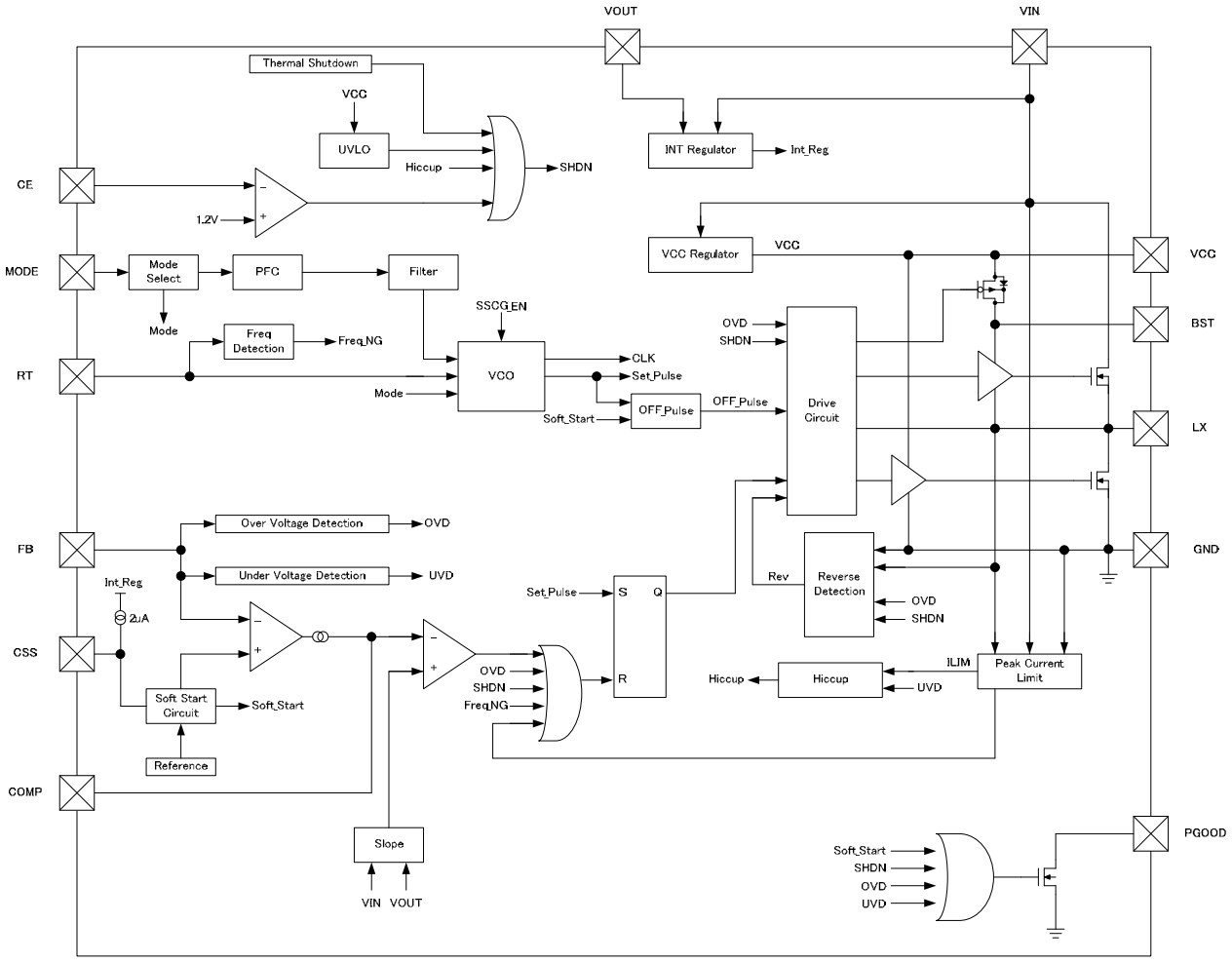
Selection Guide

Product Name	Package	Quantity per Reel	Pb Free	Halogen Free
R1275S003∗-E2-FE	HSOP-18	1,000 pcs	Yes	Yes

∗ : Choose the optional functions from below.

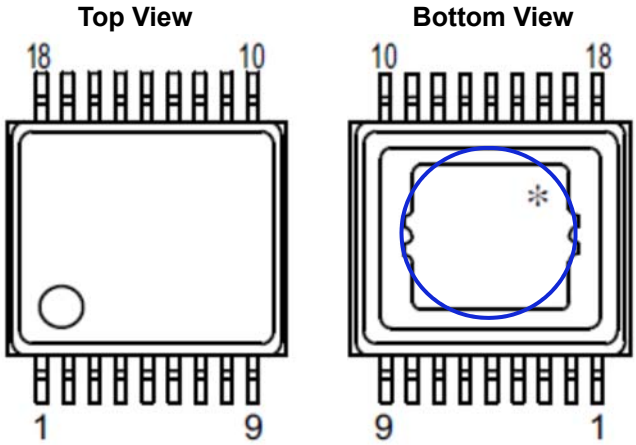
∗	Overcurrent Protection	SSCG
A	Hiccup-type	Disable
C	Hiccup-type	Enable

BLOCK DIAGRAM



R1275S Block Diagram

PIN DESCRIPTION



R1275S (HSOP-18) Pin Configuration

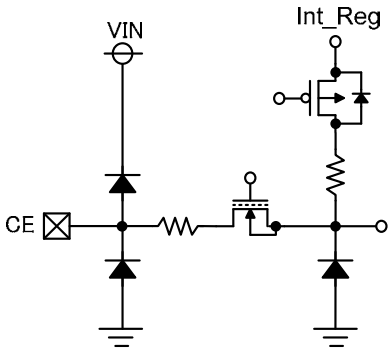
∗ The tab on the bottom of the package is substrate level (GND). The tab must be connected to the ground plane on the board.

R1275S Pin Description

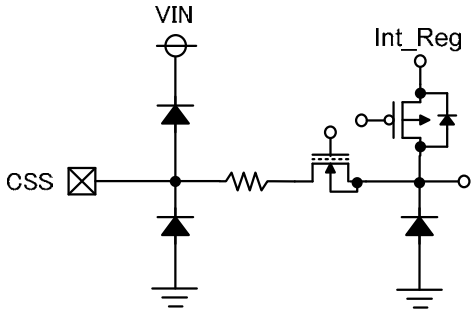
Pin No.	Pin Name	Description
1, 2	VIN(1)	Power Supply Pin
3	NC	Not Connected
4	CE	Chip Enable Pin, Active-high
5	CSS	Soft-start Adjustment Pin
6	COMP	Capacitor Connecting Pin for Error Amplifier's Phase Compensation
7	FB	Feedback Input Pin for Error Amplifier
8	PGOOD	Power Good Output Pin
9	VOUT	Output Voltage Feedback Input Pin
10	MODE(2)	Mode Setting Input Pin
11	RT	Oscillator Frequency Adjustment Pin
12	VCC	VCC Output Pin
13	BST	Bootstrap Pin
14, 15, 16	GND(1)	GND Pin
17	NC	Not Connected
18	LX	Switching Pin

(1) The pins with the same name should be connected together.
(2) This pin should be used with High or with external clock input.

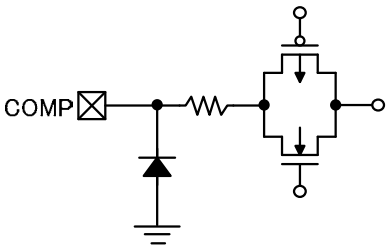
Equivalent Circuits for the Individual Terminals



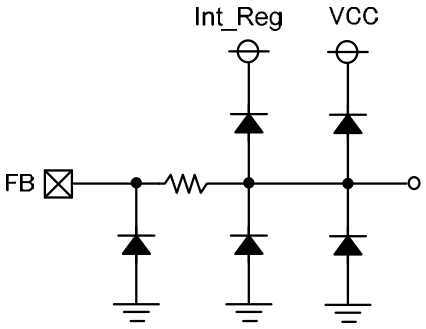
Equivalent Circuit for CE Pin



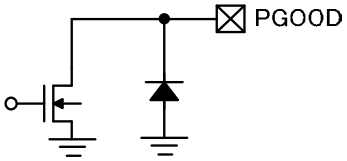
Equivalent Circuit for CSS Pin



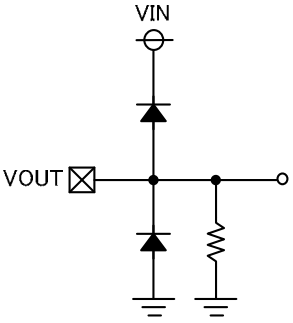
Equivalent Circuit for COMP Pin



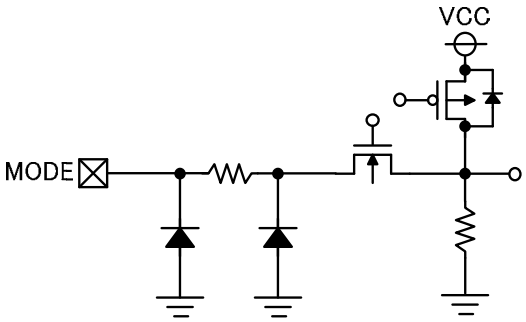
Equivalent Circuit for FB Pin



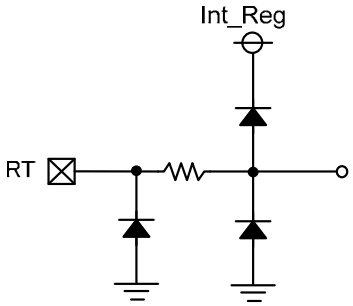
Equivalent Circuit for PGOOD Pin



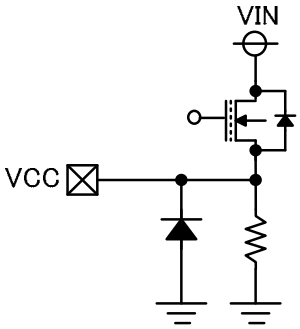
Equivalent Circuit for VOUT Pin



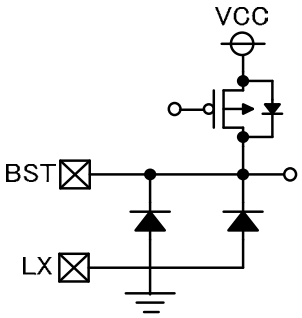
Equivalent Circuit for MODE Pin



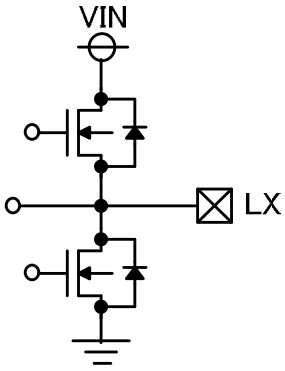
Equivalent Circuit for RT Pin



Equivalent Circuit for VCC Pin



Equivalent Circuit for BST Pin



Equivalent Circuit for LX Pin

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{IN}	VIN Pin Input Voltage	−0.3 to 36	V
V_{CE}	CE Pin Voltage(1)	−0.3 to V_{IN}+0.3 ≤ 36	V
V_{CSS}	CSS Pin Voltage	−0.3 to 3	V
V_{OUT}	VOUT Pin Voltage	−0.3 to 16	V
V_{RT}	RT Pin Voltage	−0.3 to 3	V
V_{COMP}	COMP Pin Voltage(2)	−0.3 to 6	V
V_{FB}	FB Pin Voltage	−0.3 to 3	V
V_{CC}	VCC Pin Voltage	−0.3 to 6	V
	VCC Pin Output Current	Internally Limited	mA
V_{BST}	BST Pin Voltage	LX−0.3 to LX+6	V
V_{LX}	LX Pin Voltage(1)	−0.3 to V_{IN} +0.3 ≤ 36	V
V_{MODE}	MODE Pin Votlage	−0.3 to 6	V
V_{PGOOD}	PGOOD Pin Voltage	−0.3 to 6	V
P_D	Power Dissipation(3) (HSOP-18, JEDEC STD.51-7 Test Land Pattern)	3100	mW
Tj	Junction Temperature Range	−40 to 125	°C
Tstg	Storage Temperature Range	−55 to 125	°C

ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause permanent damage and may degrade the lifetime and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings is not assured.

RECOMMENDED OPERATING CONDITIONS

Recommended Operating Conditions

Symbol	Parameter	Rating	Unit
V_{IN}	Operating Input Voltage	3.6 to 30	V
Ta	Operating Temperature Range	−40 to105	°C

RECOMMENDED OPERATING CONDITIONS

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

(1) It should not exceed V_{IN} + 0.3 V.
(2) It should not exceed V_{CC} + 0.3 V.
(3) Refer to *POWER DISSIPATION* for detailed information.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12 V, CE = V_{IN}, unless otherwise specified.
The specifications surrounded by [ ] are guaranteed by design engineering at −40°C ≤ Ta ≤ 105°C.

R1275S Electrical Characteristics **(Ta = 25°C)**

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit
V_{START}	Start-up Voltage				4.5	V
V_{CC}	VCC Pin Voltage (VCC-GND)	V_{FB} = 0.672 V	4.75	5	5.25	V
$I_{STANDBY}$	Standby Current	V_{IN} = 30 V, CE = 0 V		4	30	μA
I_{VIN1}	VIN Consumption Current 1 at PWM switching stop	V_{FB} = 0.672 V, MODE = 5 V, V_{OUT} = LX = 5 V		1.0	1.35	mA
V_{UVLO1}	Undervoltage Lockout (UVLO) Threshold	V_{CC} Falling	3.2	3.3	3.4	V
V_{UVLO2}		V_{CC} Rising	4.1	4.3	4.5	V
V_{OVLO1}	Overvoltage Lockout (OVLO) Threshold	V_{IN} Rising	33.6	35	36	V
V_{OVLO2}		V_{IN} Falling	32	34		V
V_{FB}	FB Voltage Accuracy	Ta = 25°C	0.6336	0.64	0.6464	V
		−40°C ≤ Ta ≤ 105°C	0.6272		0.6528	
f_{OSC0}	Oscillator Frequency 0	R_{RT} = 14 kΩ	1800	2000	2200	kHz
f_{SYNC}	Synchronizing Frequency		1800		2200	kHz
Δf_{OSC_SSCG}	Oscillator Frequency Spreading Rate for SSCG	V_{FB} = 0.672 V (R1275S003C)		+8		%
t_{SS1}	Soft-start Time 1	C_{SS} = OPEN	0.36		0.75	ms
t_{SS2}	Soft-start Time 2	C_{SS} = 4.7 nF	1.4		2	ms
I_{TSS}	Soft-start Pin Charging Current	C_{SS} = 0 V	1.8	2	2.2	μA
V_{SSEND}	CSS Pin Voltage at soft-start stop		0.635	0.64	0.705	V
R_{DIS_CSS}	CSS Pin Discharge Resistance	V_{IN} = 4.5 V, CE = 0 V, C_{SS} = 3 V		2	5	kΩ
$I_{LXLIMIT}$	LX Current Limiting	High-side Transistor, DC	2.55	3.0	3.45	A
$I_{REVLIMIT}$	Reverse Current Limiting	Low-side Transistor, DC		1.7	3.5	A
V_{CEH}	CE "High" Input Voltage		1.25			V
V_{CEL}	CE "Low" Input Voltage				1.1	V
I_{CEH}	CE "High" Input Current	V_{IN} = CE = 30 V		1.2	2.45	μA
I_{CEL}	CE "Low" Input Current			0	0.1	μA
I_{FBH}	FB "High" Input Current	V_{FB} = 0.672 V	−0.1	0	0.1	μA
I_{FBL}	FB "Low" Input Current	V_{FB} = 0 V	−0.1	0	0.1	μA

All test items listed under Electrical Characteristics are done under the pulse load condition (Tj ≈ Ta = 25°C).

V_{IN} = 12 V, CE = V_{IN}, unless otherwise specified.
The specifications surrounded by ☐ are guaranteed by design engineering at −40°C ≤ Ta ≤ 105°C.

R1275S Electrical Characteristics (Continued) **(Ta = 25°C)**

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit
V_{MODEH}	MODE "High" Input Voltage		1.33			V
I_{MODEH}	MODE "High" Input Current	MODE = 5 V		6.25	14.0	μA
T_{TSD}	Thermal Shutdown Temperature Threshold	Rising	150	160		°C
T_{TSR}		Falling	125	140		°C
$V_{PGOODOFF}$	PGOOD "Low" Output Voltage	V_{IN} = 3.6 V, PGOOD = 1 mA			0.25	V
$I_{PGOODOFF}$	PGOOD Pin Leakage Current	V_{IN} = 30 V, PGOOD = 6 V			100	nA
V_{FBOVD1}	FB Pin Overvoltage Detection (OVD) Threshold	V_{FB} Rising		V_{FB} x1.10	0.730	V
V_{FBOVD2}		V_{FB} Falling	0.650	V_{FB} x 1.07		V
V_{FBUVD1}	FB Pin Undervoltage Detection (UVD) Threshold	V_{FB} Falling	0.556	V_{FB} x 0.90		V
V_{FBUVD2}		V_{FB} Rising		V_{FB} x 0.93	0.625	V

All test items listed under Electrical Characteristics are done under the pulse load condition (Tj ≈ Ta = 25°C).

THEORY OF OPERATION

MODE Pin Function

The R1275S switches the operation mode to either a forced PWM mode or a PLL PWM mode by applying a voltage or a pulse to the MODE pin. By applying 1.33 V or more to the MODE pin, the operation mode goes into the forced PWM mode and operates at PWM regardless of a load current. See *Forced PWM Mode* for more details. See *Frequency Synchronization* for the operation when an external clock is connected.

Frequency Synchronization

The R1275S can synchronize to the external clock frequency sent to the MODE pin by using a PLL (Phase Locked Loop). The synchronizable frequency range is between 1.8 MHz to 2.2 MHz. During the synchronization, the operation mode is a forced PWM. The recommended pulse width of the external clock is 100 ns or more. When starting up the device while the external clock is sent to the MODE pin, the device synchronizes to the external clock while starting up with soft-start. Be aware that if the voltage difference between input and output is reduced and the device goes into the maxduty or duty-over condition, the device starts operating at 1/4 of the synchronous frequency and goes into the asynchronous condition with the MODE pin.

Duty-over

When the input voltage is dropped at cranking, the R1275S linearly changes the operating frequency to 1/4 of the set oscillator frequency in order to maintain the output voltage. This can make the on duty more than the normal maxduty and it can also reduce the voltage difference between input and output. The duty-over starts operating when it detects the minimum off-time in the set oscillator frequency and the external synchronous oscillator frequency.

UVLO (Undervoltage Lockout)

If the VCC pin voltage drops below the UVLO detection threshold of 3.3 V (Typ.) due to the input voltage drop, the R1275S turns the switching off to prevent the malfunction of the device. Due to the switching stop, the output voltage drops according to the load and C_{OUT}. If the VCC pin voltage rises above the UVLO threshold of 4.3 V (Typ.), the device restarts the operation with soft-start. For the R1275S, 4.5 V, the maximum UVLO release voltage, is a start-up voltage.

OVLO (Overvoltage Lockout)

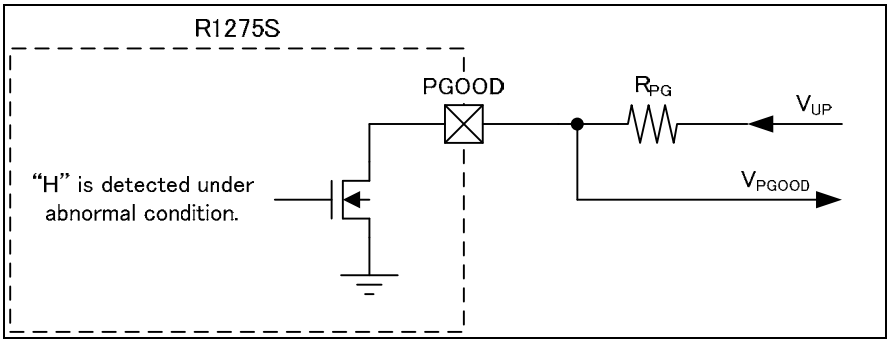
If the input voltage rises above the OVLO detection threshold of 35 V (Typ.), the R1275S turns the switching off to prevent malfunctions of the device or damages on the driver due to overvoltage. Due to the switching stop, the output voltage drops according to the load and C_{OUT} values. If the input voltage drops below the OVLO release threshold of 34 V (Typ.), the device restarts the operation with soft-start. Note that this function does not guarantee the operation above the absolute maximum ratings.

PGOOD (Power Good) Output

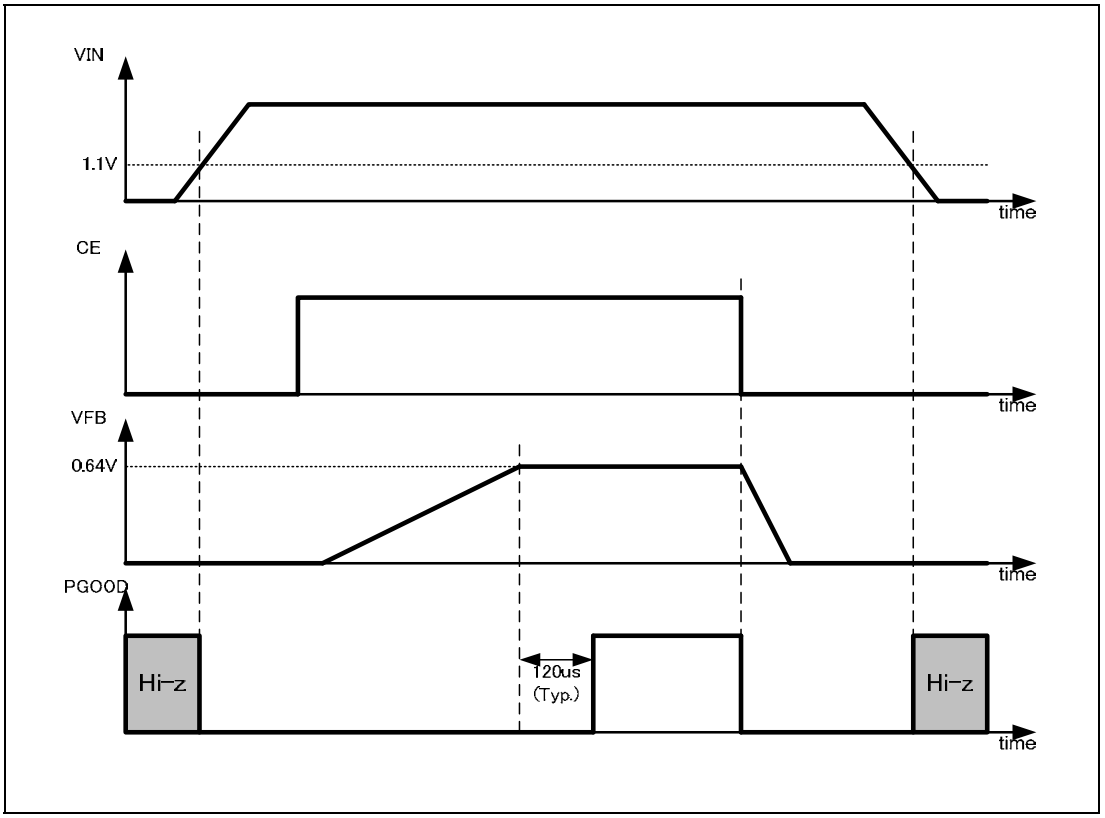
The power good function with using a NMOS open drain output pin can detect the following states of the R1275S. The NMOS turns on and the PGOOD pin becomes “Low” when detecting them. After the device returns to their original state, the NMOS turns off and the PGOOD pin outputs “High” (PGOOD Input Voltage: V_{UP}).

- CE = “Low” (Shut down)
- UVLO
- OVLO
- Thermal Shutdown
- Soft-start
- UVD
- OVD
- Hiccup-type Protection

The PGOOD pin is designed to become 0.25 V or less in “Low” level when the current floating to the PGOOD pin is 1 mA. The use of the PGOOD input voltage (V_{UP}) of 5.5 V or less and the pull-up resistor (R_{PG}) of 10 kΩ to 100 kΩ are recommended. If not using the PGOOD pin, connect it to “Open” or “GND”.



Power Good Circuit



Rising / Falling Sequence of Power Good Circuit

Under Voltage Detection (UVD)

The UVD function indirectly monitors the output voltage with using the FB pin. The PGOOD pin outputs “Low” when the UVD detector threshold is 90% (Typ.) of V_{FB} and V_{FB} is less than the UVD detector threshold for more than 15 µs (Typ.). When V_{FB} is over 93% (Typ.) of 0.64 V, the PGOOD pin outputs “High” after delay time (Typ.120 µs.). And, the hiccup-type overcurrent protection works when detecting a current limiting during the UVD detection.

Overvoltage Detection (OVD)

The OVD function indirectly monitors the output voltage with using the FB pin. Switching stops even if the internal circuit is active state, when detecting the overvoltage of V_{FB}. The PGOOD pin outputs “Low” when the OVD detector threshold is 110% (Typ.) of V_{FB} and V_{FB} is over the OVD detector threshold for more than 15 µs (Typ.). When V_{FB} is under 107% (Typ.) of 0.64 V, which is the OVD released voltage, the PGOOD pin outputs “High” after delay time (Typ.120 µs.). Then, switching is controlled by normal operation.

Hiccup-type Overcurrent Protection

The hiccup-type overcurrent protection can work under the operating conditions that is the UVD can function during the current limiting. The hiccup type protection stops switching releases the circuit after the protection delay time (Typ. 7.5 ms). Since this protection is auto-release, the CE pin switching of “Low”/“High” is unnecessary. And, damage due to the overheating might not be caused because the term to release is long. When the output is shorted to GND, switching of “ON” / “OFF” is repeated until the shorting is released.

Minimum On-Time

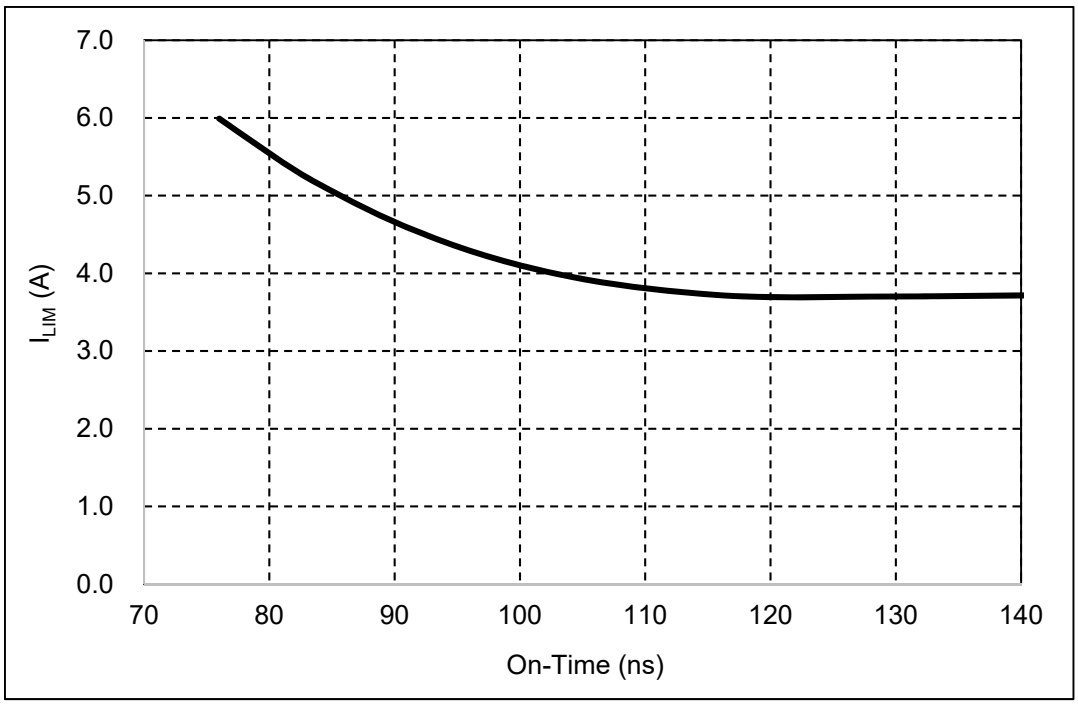
The minimum on-time means the minimum time duration that the R1275S can turn the high-side transistor on during the oscillation period. The minimum on-time of the device (Typ. 70 ns) is determined by the internal circuit. The device cannot generate a pulse width that is less than the pulse width of minimum on-time. Therefore, when setting the output voltage and the oscillator frequency, be careful that the minimum step-down ratio [V_{OUT} / V_{IN} x (1 / f_{OSC})] is not less than the minimum on-time. If they are set to less than the minimum step-down ratio, the pulse skipping occurs, which stabilizes the output voltage but increases the output ripple.

Minimum Off-Time

By the adoption of bootstrap method, the high-side FET, which is used as the R1275S internal circuit for the minimum off-time, is used a NMOS. The voltage sufficient to drive the high-side FET must be charged. Therefore, the minimum off-time is determined from the required time to charge the voltage. By the adoption of the frequency’s reduction method by one-quarter of a set value (Min.), if the input-output difference voltage becomes small or load transients are caused, the OFF period can be caused once in four-cycle period of normal cycle. As a result, the minimum off-time becomes 120 ns (Typ.) substantially, and the maximum duty cycle can be improved.

Current Limit

The output current of the R1275S is limited by the current limit using a peak current method. The current limit is set to 3.0 A (Typ. DC value) and it is fixed inside the IC. The current limit circuit limits the current by monitoring the drain and source voltage of a high-side transistor. The transitional current limit of the inductor current is set to be higher than the DC value. The current limit of the device starts operating after the minimum on-time, so it has to be careful especially when the device is used close to the minimum on-time because the current limit will increase. The following diagram shows the relation between current limit and on-time using our evaluation board. The longer the on-time is, the more the current approaches the current limit value of 3.0 A (Typ. DC value).



R1275S Current Limit vs LX On-Time

Precautions for Operating in Low Input Voltage

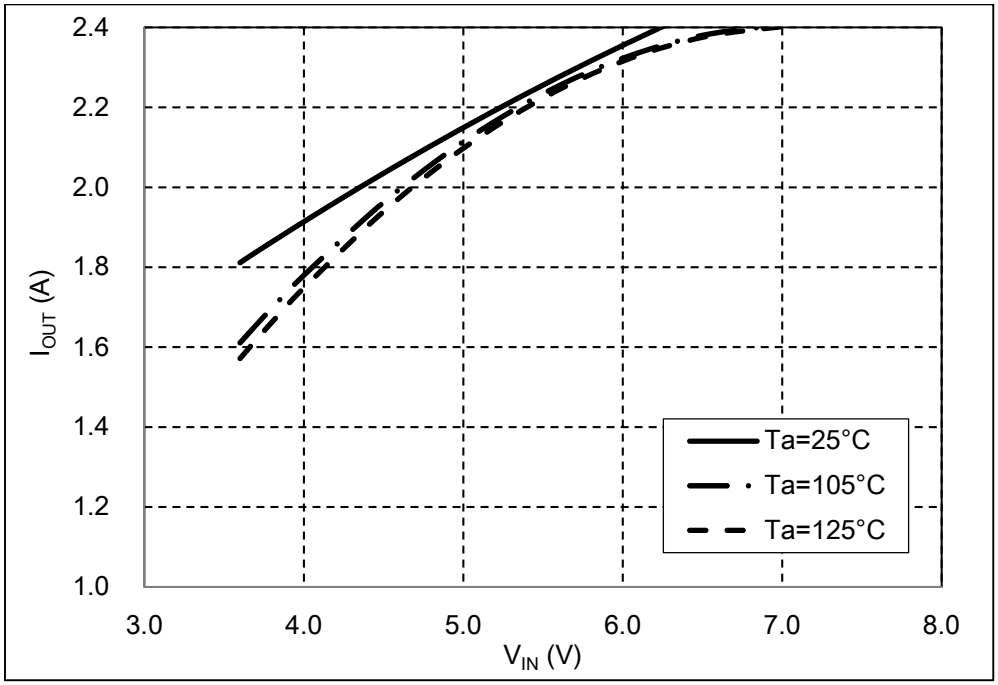
When using the R1275S with V_{IN} = 5 V or less, the load current may be limited in following two cases.

First Case: The device designed to reach current limit by monitoring the voltage difference between VIN and LX. During the low input voltage operation, the driving capability of high-side transistor decreases, so the voltage difference between VIN and LX becomes larger with smaller output current. Therefore, the load current may be limited during the low input voltage operation.

Second Case: During the low input voltage operation, the duty-over function decreases the oscillator frequency. While the oscillator frequency is 1/4 of the set frequency, drawing the load current can cause a voltage difference between the input and output. These make the device to exit from duty-over condition, and as a result, the output voltage drops.

Both cases show that the current limit is depending on the input voltage and load current. Careful consideration is required when applying a heavy load while the input voltage is low. The following graph shows the relation between input voltage and load current.

If the BST voltage between BST and LX drops extremely, the device forcibly turns off the switching to charge the BST voltage. This may occur when V_{IN} is 4.5 V or less and it may affect the output voltage ripple. Also, if V_{IN} is less than 4.5 V and UVD is detected as the output voltage decreases, the hiccup-type overcurrent protection may work due to the protection function inside the IC.



V_{OUT} = 3.3 V Setting

R1275S Output Current vs Input Voltage

Output Voltage Setting

The output voltage (V_{OUT}) can be set by adjustable values of R_{TOP} and R_{BOT}. The value of V_{OUT} can be calculated by Equation 1:

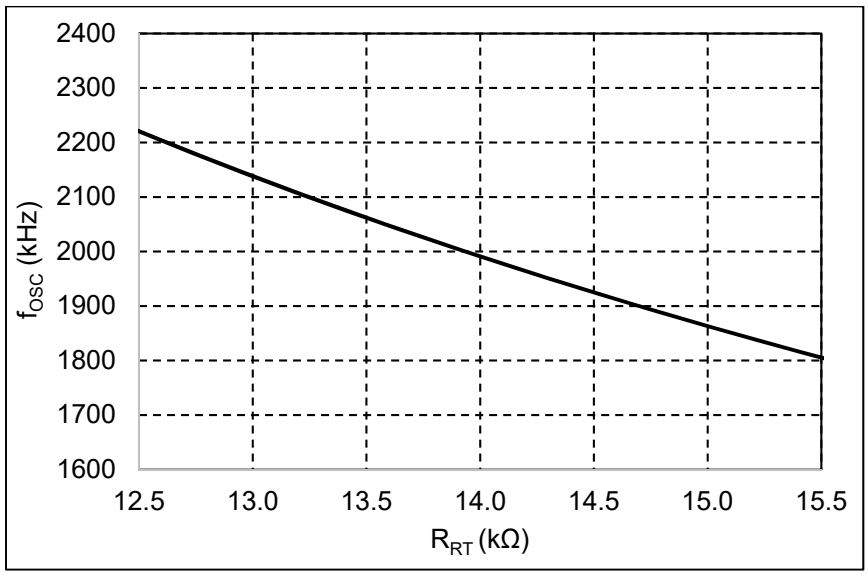
$V_{OUT} = V_{FB} \times (R_{TOP} + R_{BOT}) / R_{BOT}$ ····· Equation 1

For example, when setting V_{OUT} = 3.3 V and setting R_{BOT} = 39 kΩ, R_{TOP} can be calculated by substituting them to Equation 1. As a result of the expanding Equation 2, R_{TOP} can be set to 162 kΩ.
To make 162 kΩ with using the E24 type resistors, the connecting use of 160 kΩ and 2 kΩ resistors in series is required. If the tolerance level of the set output voltage is wide, using a resistor of 160 kΩ to R_{TOP} can reduce the number of components.

R_{TOP} = (3.3 V / 0.64 V - 1) × 39 kΩ
= 162 kΩ ····· Equation 2

Oscillator Frequency Setting

Connecting a 14-kΩ (Typ.) oscillation frequency setting resistor (R_{RT}) between the RT pin and GND can control the oscillation frequency to 2 MHz. The following equation can calculate the variation in resistance of oscillator frequencies. To reduce the variation of oscillator frequencies, it is recommended that a ±1% or less R_{RT} be used. For the SSCG type (R1275S003C), an up-spreading modulation is used (Typ. +8%).



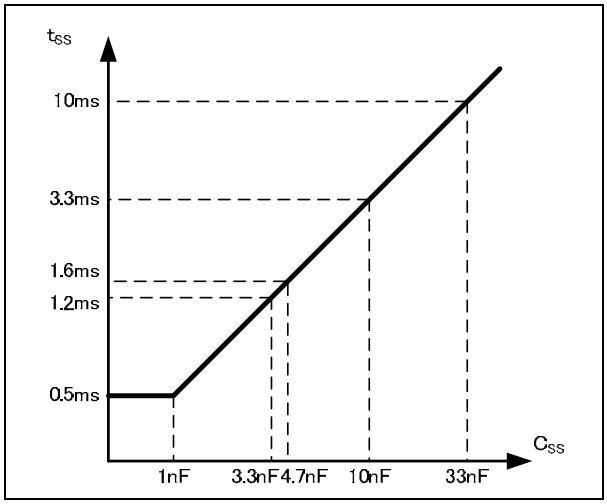
R_{RT} [kΩ] = 37773 × f_{OSC} [kHz] ^ (-1.04)

R1275S Oscillator Frequency vs Oscillator Frequency Setting Resistance

Soft-start Adjustment

The soft-start time is a time between a rising edge (“High” level) of the CE pin and the timing when the output voltage reaches the set output voltage. Connecting a capacitor (C_{SS}) to the CSS pin can adjust the soft-start time (t_{SS}) – provided the internal soft-start time of 500 µs (Typ.) as a lower limit. The adjustable soft-start time (t_{SS2}) is 1.6 ms (Typ.) when connecting an external capacitor of 4.7 nF with the charging current of 2.0 µA (Typ.) and 0.64 V (Typ.). If not required to adjust the soft-start time, set the CSS pin to “Open” to enable the internal soft-start time (t_{SS1}) of 500 µs (Typ.). When a large-capacitance output capacitor is connected, the overcurrent protection may work due to an inflow of large current at startup. Thus, set a longer soft start time to reduce the amount of current and prevent from operating the protections due to the rapid startup.

Each of soft-start time (tss1/ tss2) is guaranteed under the conditions described in the chapter of “Electrical Characteristics”.

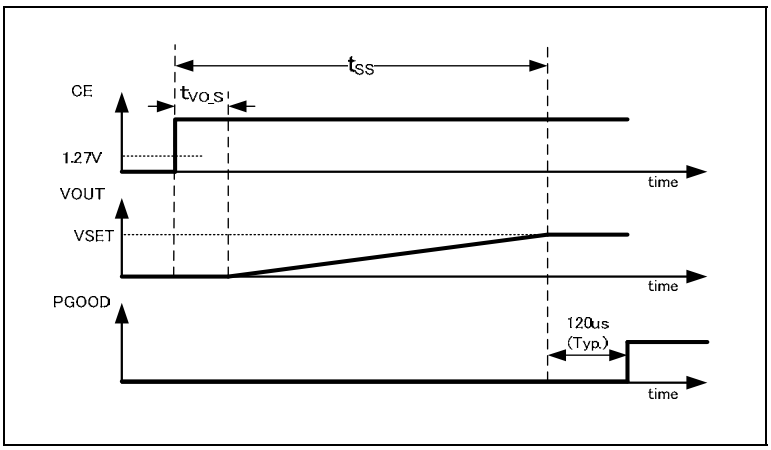


C_{SS} [nF] = (t_{SS} – t_{VO_S}) / 0.64 × 2.0

t_{SS}: Soft-start time (ms)

t_{VO_S}: Time period from CE = “High” to VOUT’s rising (Typ. 0.160 ms)

Soft-start Time Adjustment Capacitor vs Soft-start Time



Soft-start Sequence

Reverse Current Limit

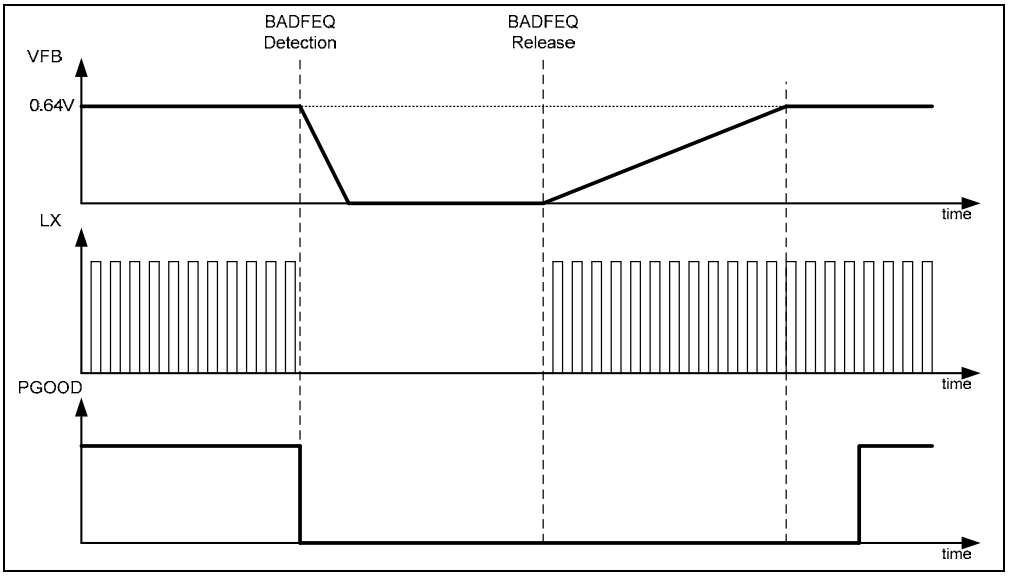
The reverse current limit start operating when the reverse current flowing through the low-side transistor exceeds the set reverse current threshold. It turns off the low-side transistor to control the reverse current. The reverse current limit is 2 A (Typ.). This function operates when the output voltage is pulled up more than the set output voltage due to short-circuiting.

SSCG (Spread Spectrum Clock Generator)

The SSCG function works for EMI reduction at the PWM mode. This function is enabled in the R1275S003C. This function make EMI waveforms decrease in amplitude to generate a ramp waveform within approximately +8.0% (Typ.) of the oscillator frequency (f_{OSC}). The modulation cycle is f_{OSC} / 128. SSCG is enabled only when MODE = High. SSCG is not effective when a clock is externally applied. The oscillator frequencies are not modulated during the soft-start.

Bad Frequency Protection (BADFREQ)

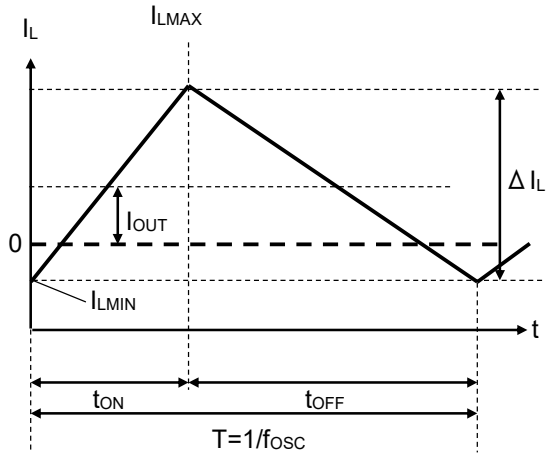
If a current equivalent to 4 MHz (Typ.) or more or 125 kHz (Typ.) or less is applied to the RT pin when the oscillator frequency setting resistor (R_{RT}) of the RT pin is in open / short, the R1275S will stop switching to protect the IC and will cause the internal state to transition to its state before the soft-start. The R1275S will restart under the normal control from the state of soft-start when recover after the abnormal condition.



BADFREQ Detection/ Release Sequence

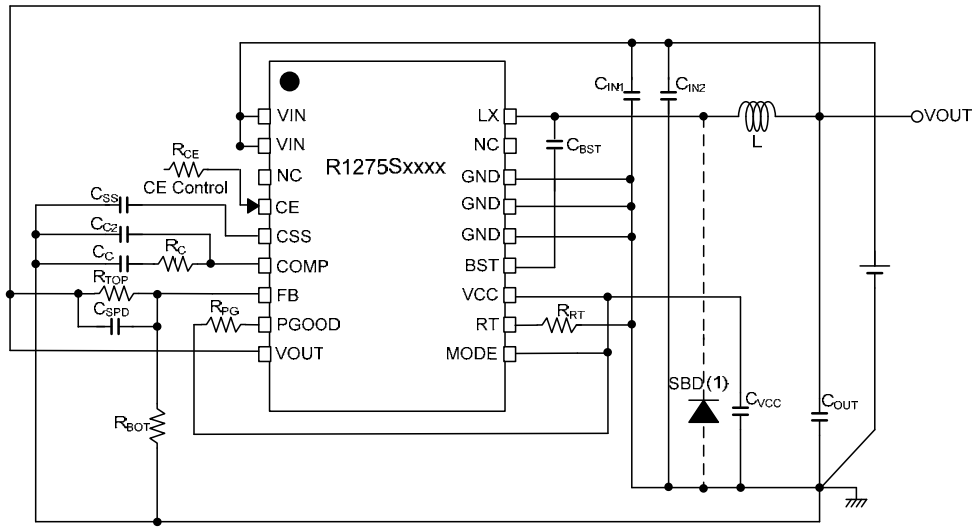
Forced PWM Mode

The R1275S goes into the forced PWM mode by setting the MODE pin high or applying the external clock to the MODE pin. The forced PWM mode operates at fixed switching frequency even during the light load in order to reduce noise. Therefore, when the output current (I_{OUT}) is less than $\Delta I_L / 2$, I_{LMIN} becomes less than "0".



Forced PWM Mode

APPLICATION INFORMATION



R1275S Typical Application Circuit

Recommended Values

V_{OUT}	C_{IN} [µF]	L [µH]	C_{OUT} [µF]	C_{BST} [µF]	C_{VCC} [µF]	C_{SPD} [pF]	R_{TOP} [kΩ]	R_{BOT} [kΩ]	R_{RT} [kΩ]	R_C [kΩ]	C_C [nF]	C_{C2} [pF]
3.3 V	21 (10×2+1)	2.2	48.7 (22×2+4.7)	0.1	1.0	10	162 (150+12)	39	14	8.2	4.7	-
5.0 V	21 (10×2+1)	2.2	48.7 (22×2+4.7)	0.1	1.0	10	267 (220+47)	39	14	12	4.7	-

It is recommended to set 1 kΩ or higher for R_{CE} and between 10 kΩ and 100 kΩ for R_{PG}.

Recommended Parts

Symbol	Capacitance	Specification	Parts Name
C_{IN}	1.0 µF	50 V, 125°C	CGA4J3X7R1H105K (TDK)
	10 µF	50 V, 125°C	CGA6P3X7S1H106K (TDK)
C_{OUT}	4.7 µF	25 V, 125°C	CGA5L1X7R1E475K (TDK)
	22 µF	16 V, 125°C	CGA6P1X7R1C226M (TDK)
C_{BST}	0.1 µF	25 V, 125°C	CGA3E2X7R1E104K (TDK)
C_{VCC}	1.0 µF	16 V, 125°C	CGA3E1X7R1C105K (TDK)

Symbol	Inductance	Specification	Parts Name
L	2.2 µH	5.5 A	CLF7045NIT-2R2-D (TDK)

(1) Connecting a Schottky barrier diode between LX and GND can reduce the LX noise and improve the efficiency.

Precautions for Selecting External Components

Inductor

- Choose an inductor that has small DC resistance, has sufficient allowable current and is hard to cause magnetic saturation. The inductance value must be determined with consideration of load current under the actual condition. If the inductance value of an inductor is extremely small, the peak current of LX may increase along with the load current. As a result, the current limit circuit may start to operate when the peak current of LX reaches to “LX limit current”.

Capacitor

- Choose a capacitor that has a sufficient margin to the drive voltage ratings with consideration of the DC bias characteristics and the temperature characteristics.
- Ceramic capacitors are recommended for the input capacitor (C_{IN}) and the output capacitor (C_{OUT}). The combined use of a ceramic capacitor and an electrolyte capacitor is recommended. Especially, choose the electrolyte capacitor with the lowest possible ESR with consideration of the allowable ripple current rating (I_{RMS}). I_{RMS} can be calculated by the following equation.

  $$I_{RMS} \fallingdotseq I_{OUT} / V_{IN} \times \sqrt{\{ V_{OUT} \times (V_{IN} - V_{OUT}) \}}$$

  The electrolyte capacitor has a characteristic of increasing ESR when it is at a low temperature, so careful consideration is required on the phase characteristics in case of using an electrolyte capacitor for C_{OUT}.

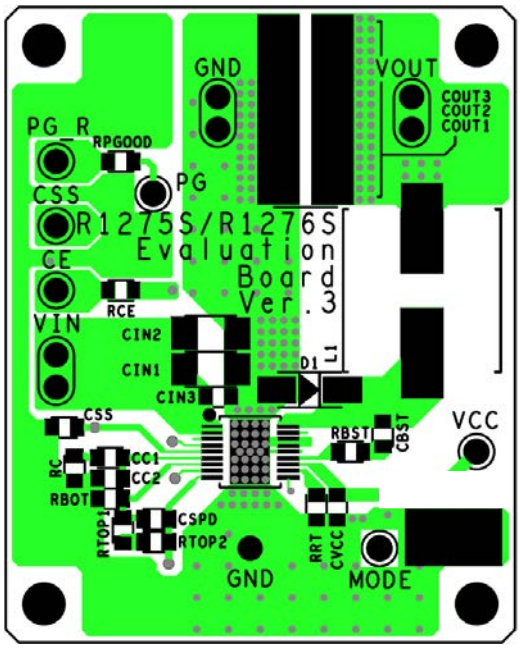
TECHNICAL NOTES

The performance of a power source circuit using this device is highly dependent on a peripheral circuit. A peripheral component or the device mounted on PCB should not exceed a rated voltage, a rated current or a rated power. When designing a peripheral circuit, please be fully aware of the following points. Refer to *PCB Layout* below.

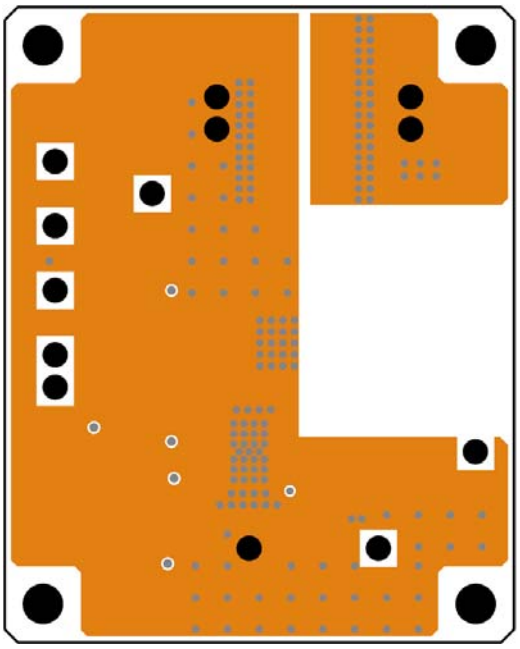
- External components must be connected as close as possible to the ICs and make wiring as short as possible. Especially, the capacitor connected in between VIN pin and GND pin must be wiring the shortest. If their impedance is high, internal voltage of the IC may shift by the switching current, and the operating may be unstable. Make the power supply and GND lines sufficient.
- Place a capacitor (C_{BST}) as close as possible to the LX pin and the BST pin. If controlling slew rate for EMI, a resistor (R_{BST}) should be in series between the BST pin and the capacitor (C_{BST}).
- The tab on the bottom of the HSOP-18 package must be connected to GND when mounted on the board. To improve thermal dissipation on the multilayer board, set via to release the heat to the other layer in the connecting part of the tab on the bottom.
- The NC pin must be set to “Open”.
- The MODE pin requires the high voltages with the high stability when the forced PWM mode (MODE = “High”) is enabled. If the voltage with the high stability cannot be applied, connection to the VCC pin as “High” level is recommended. Avoid the use of the MODE pin being “GND” or “Open”.
- If V_{OUT} is a minus potential, the setup cannot occur.
- Shorten the wiring between the Lx pin and the inductor so that the parasitic capacitance is not provided.
- It is recommended to place the input capacitor (C_{IN}) on the same side as the IC. If it is placed on the different side as the IC by using via, the noise may be increased due to the parasitic inductance component of via.
- Feedback the output voltage near the C_{OUT}.
- Place R_{TOP}, R_{BOT}, and C_{SPD} near FB pin and mount them at a position apart from the inductor, Lx pin, and BST pin to prevent the effect of noise.

PCB LAYOUT

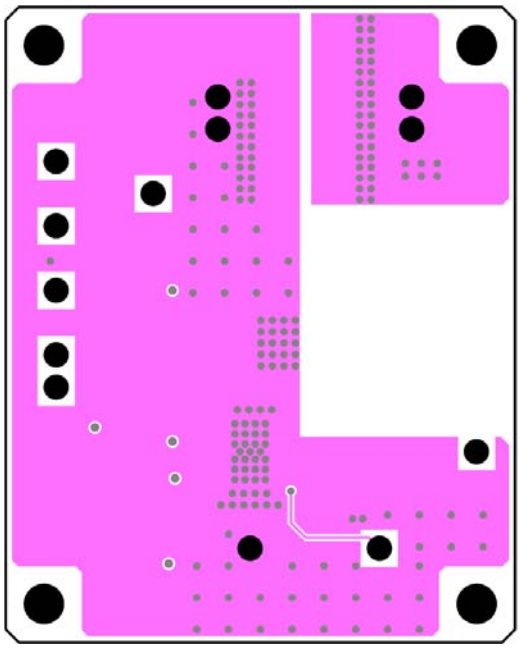
R1275S003x



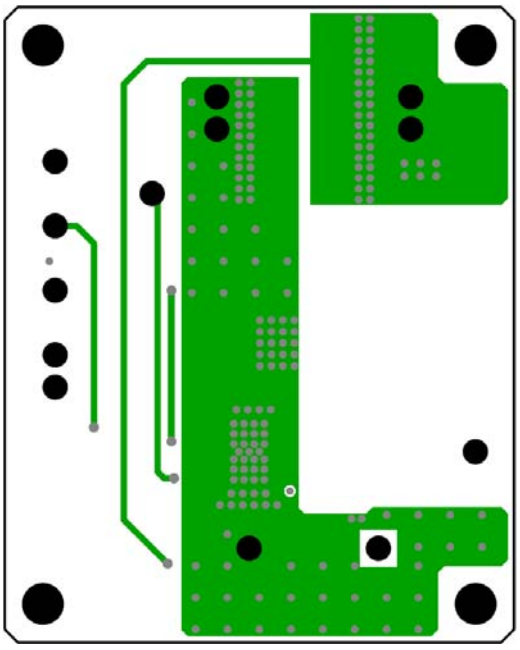
Layer 1 (Top)



Layer 2



Layer 3

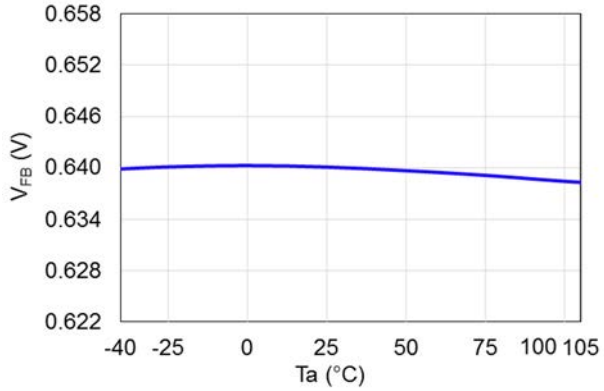


Layer 4 (Bottom)

TYPICAL CHARACTERISTICS

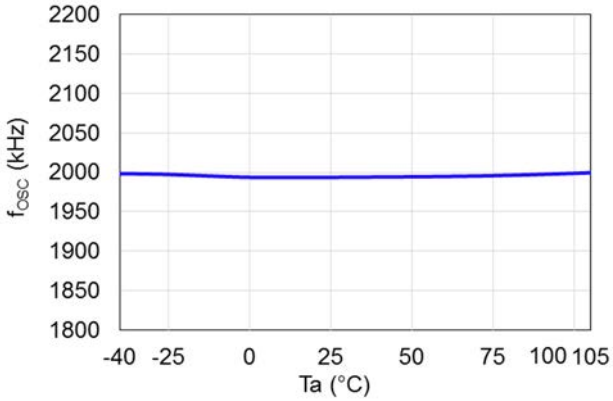
Note: Typical Characteristics are intended to be used as reference data; they are not guaranteed.

1) FB Voltage



2) Oscillator Frequency 0

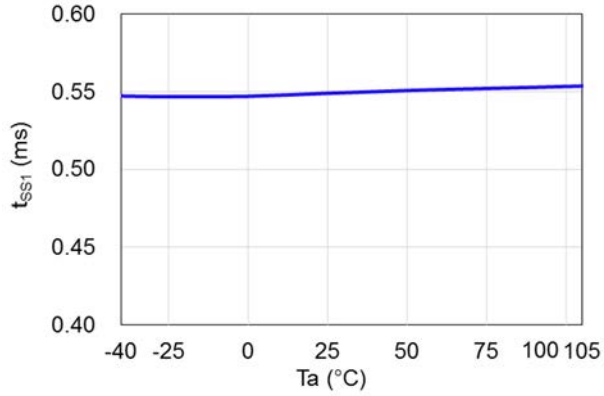
2 MHz (RT = 14 kΩ)



3) Soft-start Time

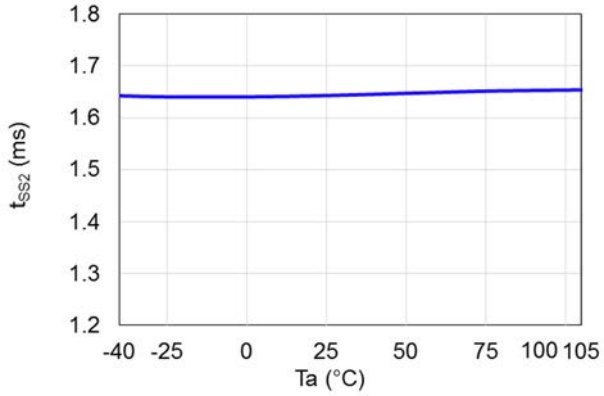
Internally Fixed Soft-start Time

(C_{SS} = Open)

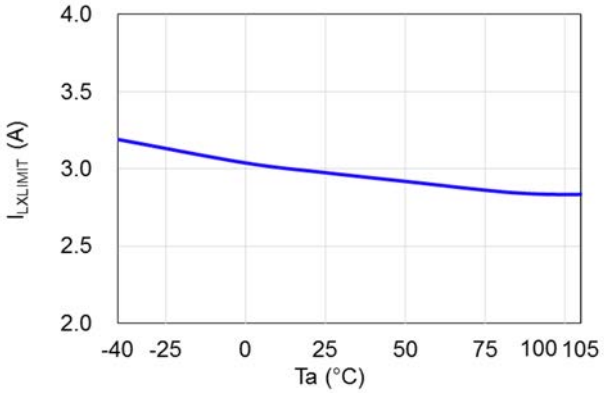


Externally Adjustable Soft-start Time

(C_{SS} = 4.7 nF)

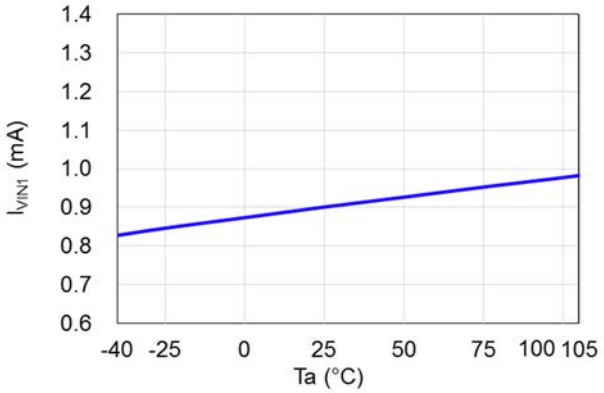


4) LX Limit Current

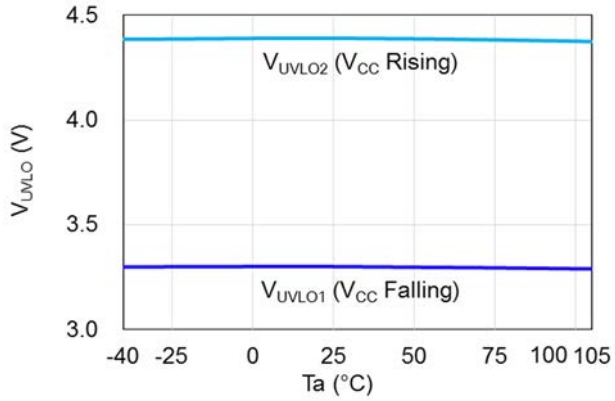


5) VIN Supply Current 1

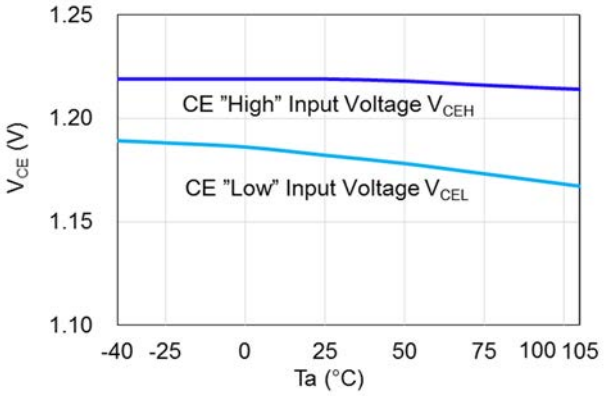
V_{IN} = 12 V, MODE = High



6) UVLO

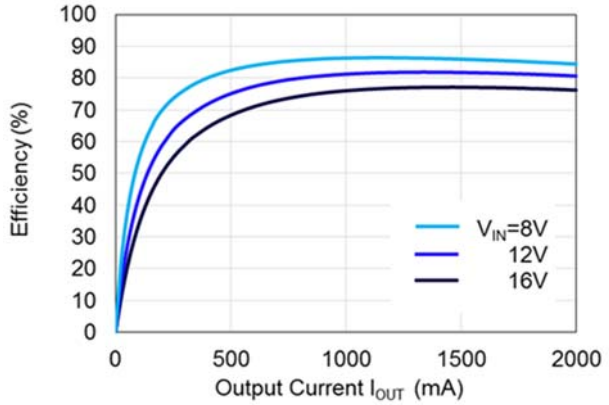


7) CE Input Voltage

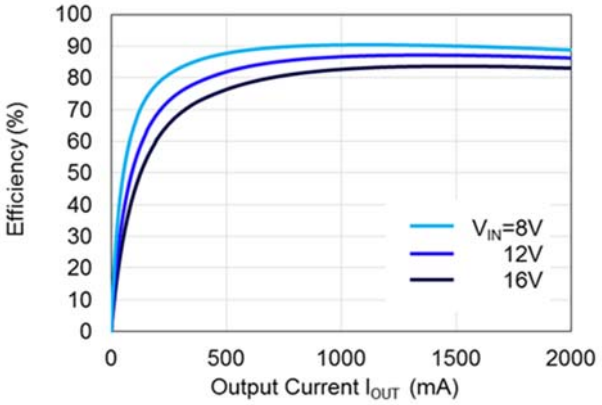


8) Efficiency

V_{OUT} = 3.3 V, f_{OSC} = 2 MHz, Ta = 25°C

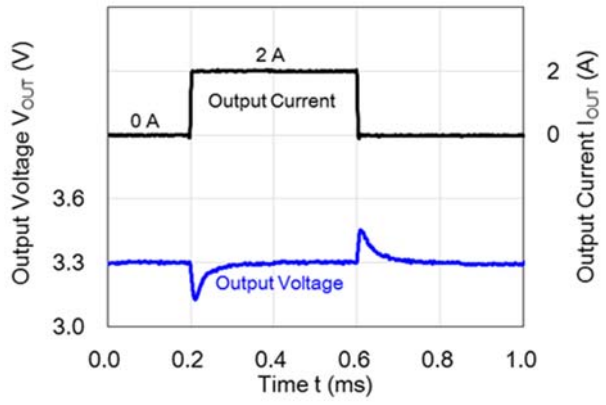


V_{OUT} = 5.0 V, f_{OSC} = 2 MHz, Ta = 25°C



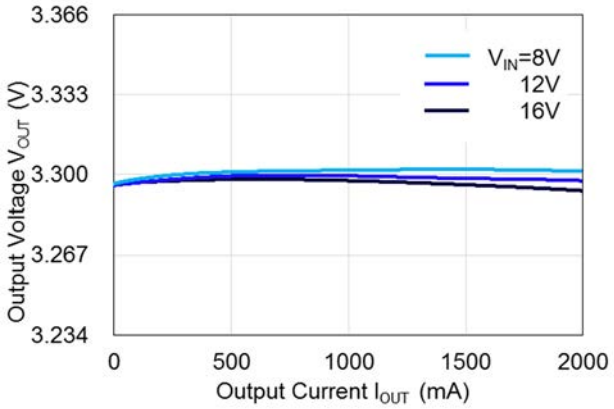
9) Load Transient Response

V_{IN} = 12 V, V_{OUT} = 3.3 V, f_{OSC} = 2 MHz,
MODE = High, Ta = 25°C

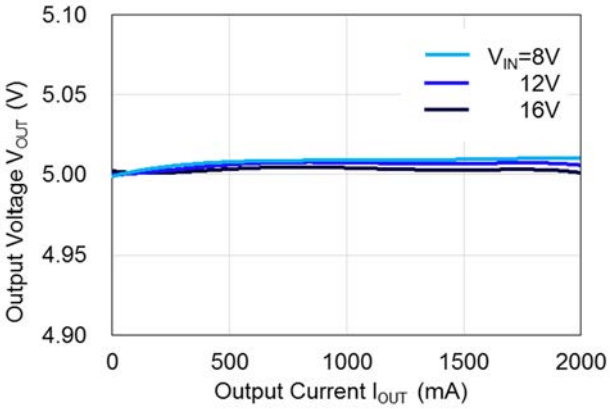


10) Load Regulation

V_{OUT} = 3.3 V, f_{OSC} = 2 MHz, Ta = 25°C



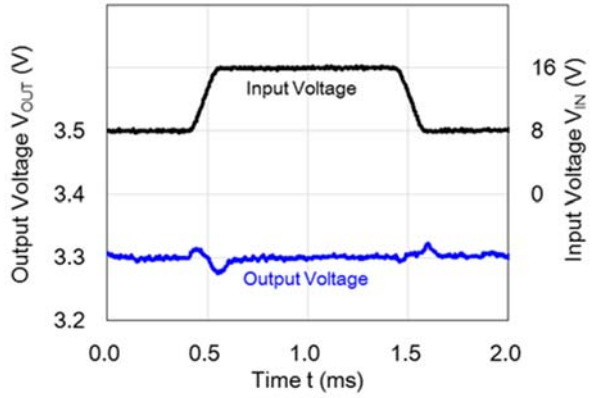
V_{OUT} = 5.0 V, f_{OSC} = 2 MHz, Ta = 25°C



11) Input Voltage Transient Response

V_{IN} = 8 V -> 16 V, tr = tf = 100 µs

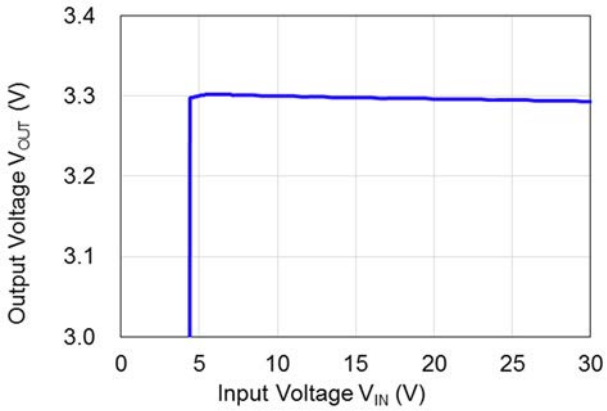
V_{OUT} = 3.3 V, f_{OSC} = 2 MHz, I_{OUT} = 1 A, Ta = 25°C



12) Line Regulation

V_{OUT} = 3.3 V, f_{OSC} = 2 MHz

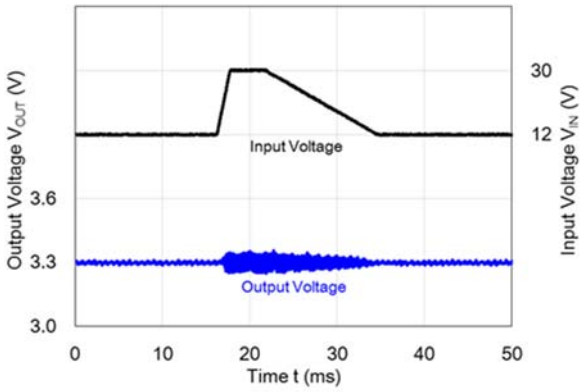
I_{OUT} = 1 A, Ta = 25°C



13) Transient Voltage Surge

V_{OUT} = 3.3 V, f_{OSC} = 2 MHz

I_{OUT} = 100 mA, Ta = 25°C



Ver. C

The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51-7.

Measurement Conditions

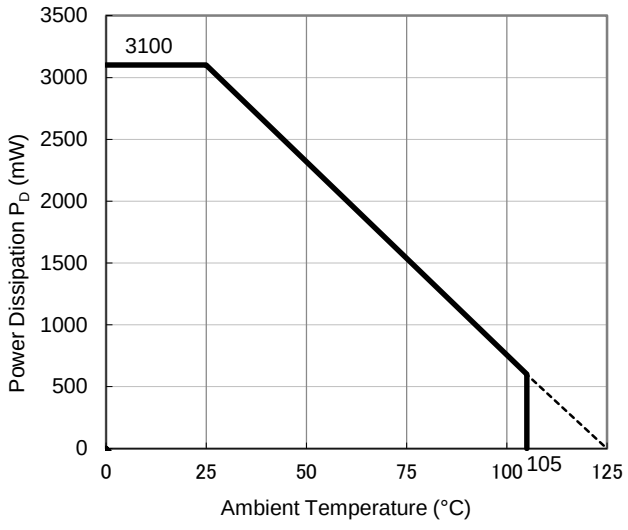
Item	Measurement Conditions
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	76.2 mm × 114.3 mm × 0.8 mm
Copper Ratio	Outer Layer (First Layer): Less than 95% of 50 mm Square Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square Outer Layer (Fourth Layer): Approx. 100% of 50 mm Square
Through-holes	ϕ 0.3 mm × 21 pcs

Measurement Result (Ta = 25°C, Tjmax = 125°C)

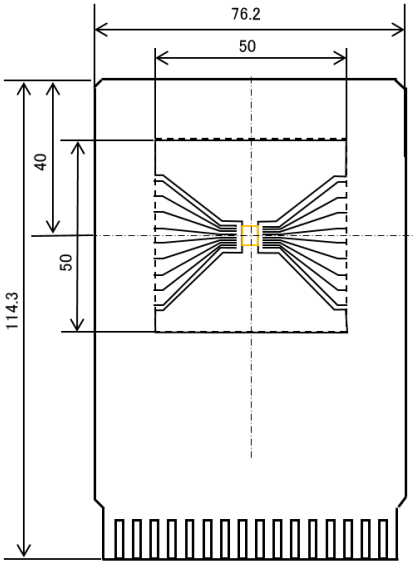
Item	Measurement Result
Power Dissipation	3100 mW
Thermal Resistance (θja)	θja = 32°C/W
Thermal Characterization Parameter (ψjt)	ψjt = 8°C/W

θja: Junction-to-Ambient Thermal Resistance

ψjt: Junction-to-Top Thermal Characterization Parameter

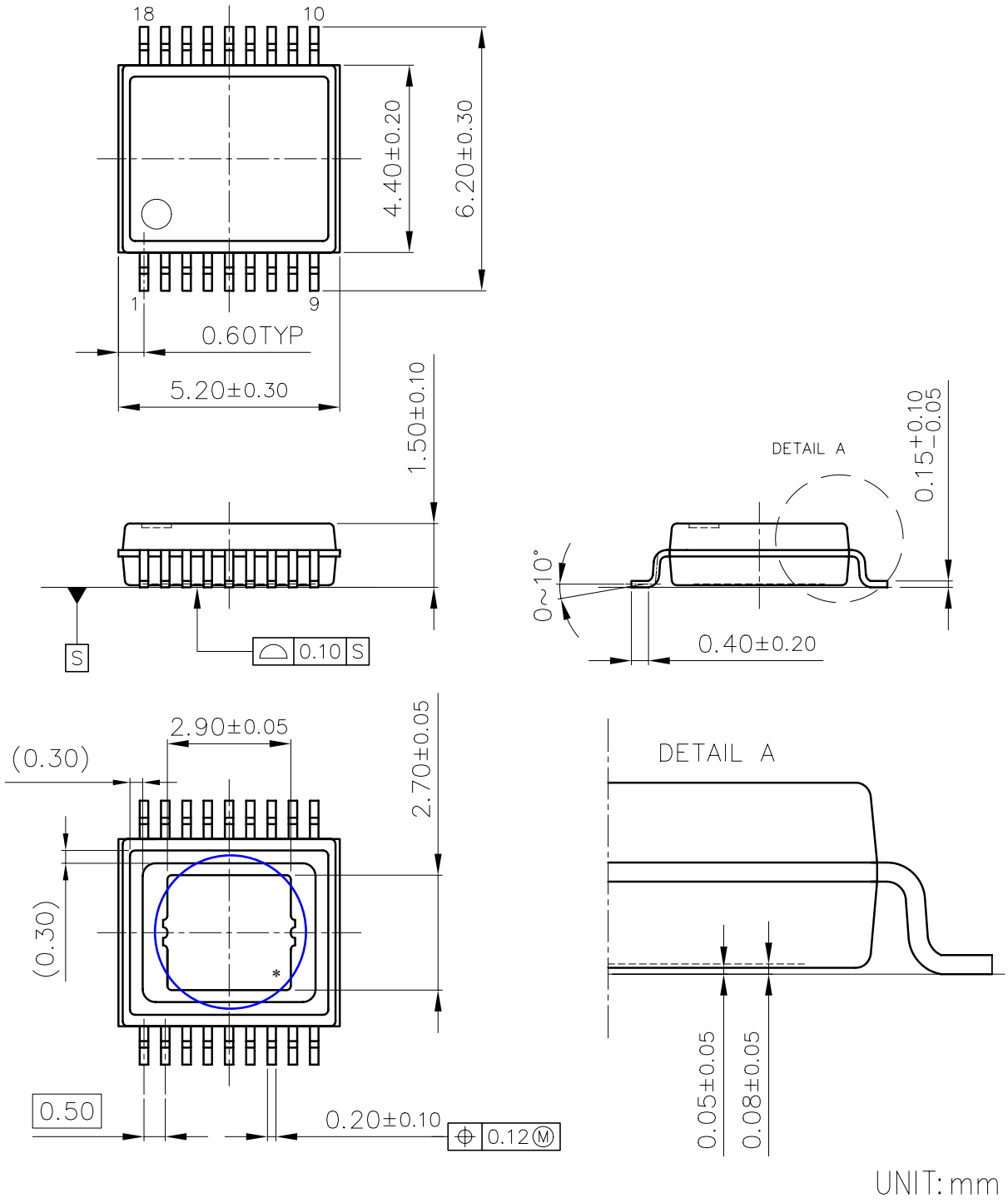


Power Dissipation vs. Ambient Temperature



Measurement Board Pattern

Ver. B



HSOP-18 Package Dimensions

∗ The tab on the bottom of the package is substrate level (GND). It must be connected to the ground plane on the board.

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7. Anti-radiation design is not implemented in the products described in this document.
8. The X-ray exposure can influence functions and characteristics of the products. Confirm the product functions and characteristics in the evaluation stage.
9. WLCSP products should be used in light shielded environments. The light exposure can influence functions and characteristics of the products under operation or storage.
10. There can be variation in the marking when different AOI (Automated Optical Inspection) equipment is used. In the case of recognizing the marking characteristic with AOI, please contact our sales or our distributor before attempting to use AOI.
11. Please contact our sales representatives should you have any questions or comments concerning the products or the technical information.

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