

## OUTLINE

The R1273L is a step-down DC/DC converter which can generate an output voltage of 0.7 V to 5.3 V by driving high- / low-side NMOSs. By the adoption of a unique current mode PWM architecture without an external current sense resistor, the R1273L can make up a stable DC/DC converter with high-efficiency even if adding a low DCR inductor externally. And, by the frequency characteristics optimization with using external phase compensation capacitor, the R1273L can achieve a high-speed response to variations of input voltage and load current. The user-settable oscillation frequency is adjustable over a range of 250 kHz to 1 MHz by external resistors, and also can be synchronized to an external clock in a range of 250 kHz to 1 MHz. The R1273L supports three operating modes: Forced PWM mode, PLL\_PWM mode, and PWM/VFM Auto-switching mode. These modes are selectable according to conditions of the MODE pin. Especially, the PWM/VFM Auto-switching mode can improve efficiency under light load conditions.

The R1273L can minimize the output voltage drop caused by an input voltage drop at cranking, with reducing the operating frequency (the lowest possible limit is a quarter of the frequency) so that the off-duty is reduced. Protection functions include a current limit function, a hiccup-mode short-circuit protection (non-latch type), a thermal shutdown function, an UVLO (Under Voltage Lock Out) function, an OVD (Over Voltage Detection) function, a soft-start function, a low-inductor current shutdown function, and so on. Also, a power good function provides the status of output with using a power good (PGOOD) pin.

For EMI reduction, SSCG (Spread-Spectrum Clock Generator) for diffused oscillation frequency at the PWM operation is optionally available. The R1273L is available in QFN0505-32B package.

## FEATURES

- Operating Voltage (Maximum Rating) ..... 4.0 V to 34 V (36 V)
- Operating Temperature Range ..... -40°C to 125°C
- Start-up Voltage ..... 4.5 V
- Output Voltage Range ..... 0.7 V to 5.3 V
- Feedback Voltage Tolerance ..... 0.64 V  $\pm$ 1%
- Consumption Current at No Load(at VFM mode) ..... Typ.15  $\mu$ A
- Adjustable Oscillation Frequency<sup>(1)</sup>..... 250 kHz to 1 MHz
- Synchronizable Clock Frequency<sup>(1)</sup>..... 250 kHz to 1 MHz
- Minimum On-Time ... ..... Typ.100 ns
- Minimum Off-Time ..... Typ.120 ns (at regulation mode)  
At dropout, actual minimum off-time is reduced.
- Adjustable Soft-start Time<sup>(2)</sup>..... Typ.500  $\mu$ s
- Pre-bias Start-up
- Anti-phase Clock Output
- Thermal Shutdown Function ..... T<sub>j</sub> = 160°C (Typ.)
- Under Voltage Lockout (UVLO) Function..... V<sub>CC</sub> = 3.3V (Typ.)

<sup>(1)</sup> The adjustable oscillation frequency range becomes 250 kHz  $\leq$  f<sub>osc</sub>  $\leq$  600 kHz when 0.7 V  $\leq$  V<sub>OUT</sub> < 1.35V.

<sup>(2)</sup> 500  $\mu$ s(Typ.) as a lower limit with using an external capacitor. Otherwise, available the tracking function through the application of an external voltage.

- Over Voltage Detection (OVD) Function ..... FB pin voltage ( $V_{FB}$ ) + 10% (Typ.)  
Detection/Release Hysteresis ..... FB pin voltage ( $V_{FB}$ ) x 3% (Typ.)
- Under Voltage Detection (UVD) Function ..... FB pin voltage ( $V_{FB}$ ) - 10% (Typ.)  
Detection/Release Hysteresis ..... FB pin voltage ( $V_{FB}$ ) x 3% (Typ.)
- Selectable Over-current Protection ..... Hiccup-mode / Latch mode
- Selectable Current Limit Threshold ..... 50 mV / 70 mV / 100 mV
- High-side / Low-side Tr. On-resistance ..... Typ.11.8 m $\Omega$  / 12.3 m $\Omega$
- Power Good Output ..... NMOS Open-drain Output
- Package ..... QFN0505-32B

## APPLICATIONS

- Power source for car accessories including car audio equipment, car navigation system, and ETC system.

## SELECTION GUIDE

The function and setting for the ICs are selectable at the user's request.

Product Name	Package	Quantity per Reel	Pb Free	Halogen Free
R1273LxxxA-E2-#	QFN0505-32B	1,000	Yes	Yes

xx : Select the combination of processing and function.

xx	Over Current Protection	SSCG	Output Voltage Range
00	Non-latch type hiccup mode	Disable	3.15 V < $V_{OUT}$ $\leq$ 5.3 V
01	Latch mode	Disable	3.15 V < $V_{OUT}$ $\leq$ 5.3 V
03	Latch mode	Enable	3.15 V < $V_{OUT}$ $\leq$ 5.3 V
10	Non-latch type hiccup mode	Disable	0.7 V $\leq$ $V_{OUT}$ $\leq$ 3.15 V
11	Latch mode	Disable	0.7 V $\leq$ $V_{OUT}$ $\leq$ 3.15 V
13	Latch mode	Enable	0.7 V $\leq$ $V_{OUT}$ $\leq$ 3.15 V

If required a version with SSCG function, please contact our sales offices.

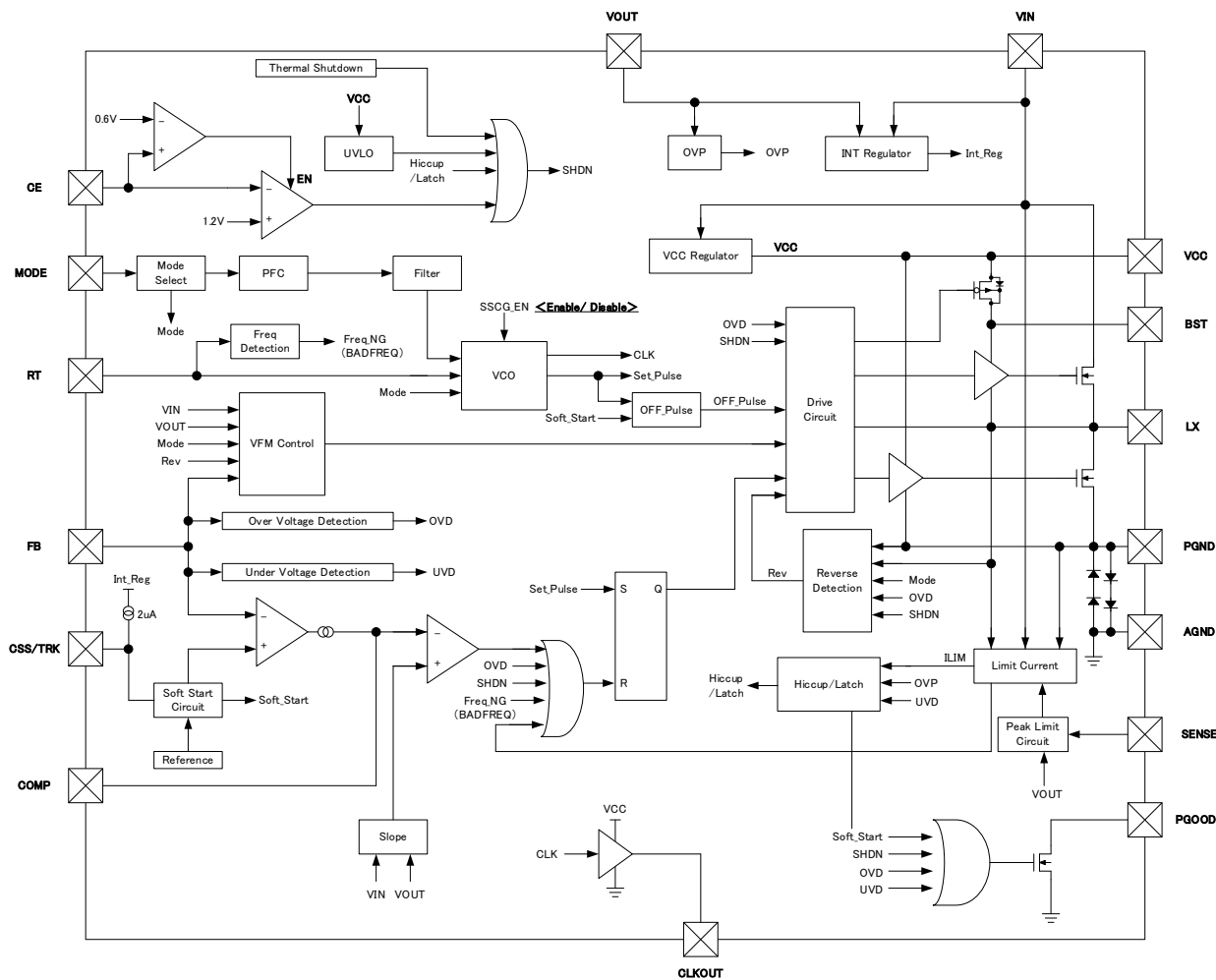
y : Select the current limit threshold voltage.

y	Set Voltage for Current Limit Threshold (Typ.)	Reverse Current Detection Value (Typ.)
1	50 mV	25mV
2	70 mV	35mV
3	100 mV	50mV

# : Specify the quality class.

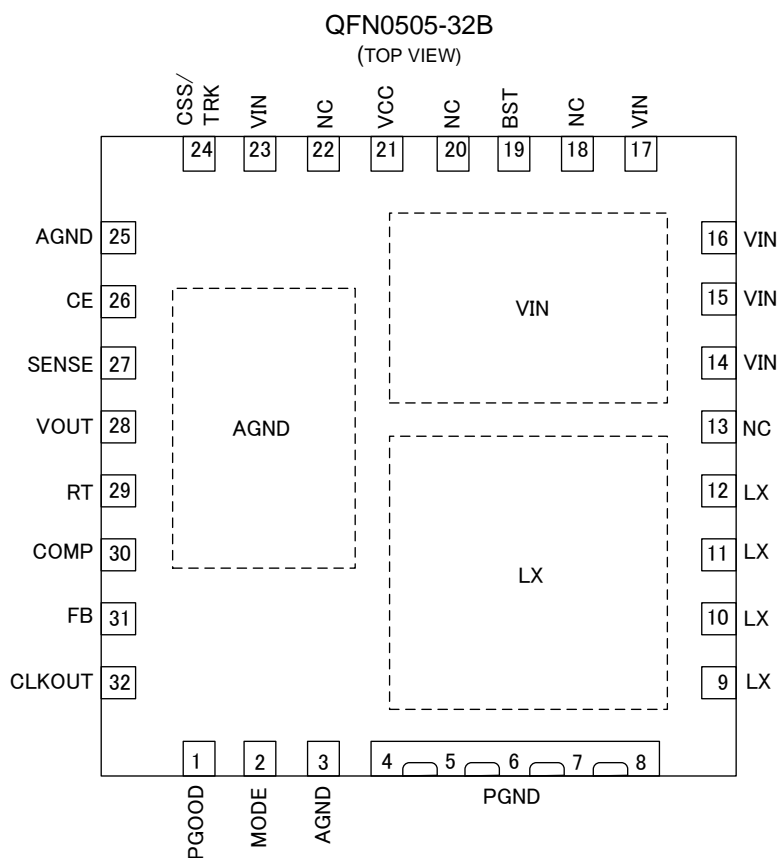
#	Operating Temperature Range	Test Temp.
A	-40°C to 125°C	25°C, High

**BLOCK DIAGRAMS**



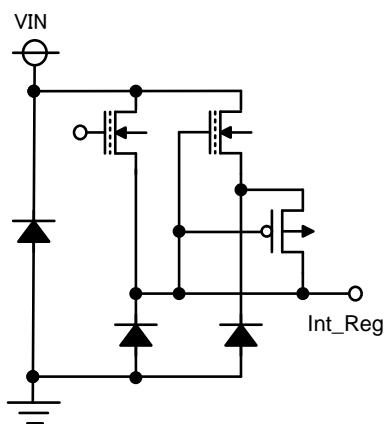
**R1273LxxxA**

## PIN DESCRIPTIONS

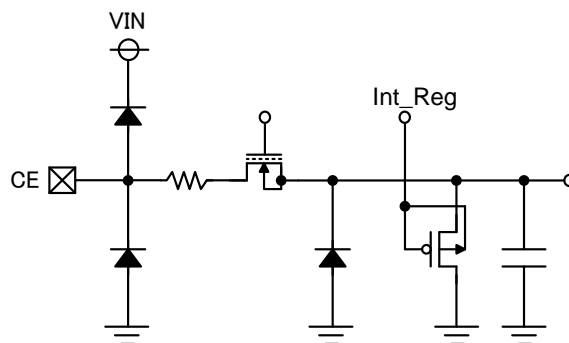


Pin No.	Pin Name	Description
1	PGOOD	Power-good output pin
2	MODE	Mode-set input pin
3, 25	AGND	Analog GND pins
4, 5, 6, 7, 8	PGND	Power GND pins
9, 10, 11, 12	LX	Switching pins
13, 18, 20, 22	NC	No connection
14, 15, 16, 17, 23	VIN	Power supply pins
19	BST	Bootstrap pin
21	VCC	V <sub>cc</sub> output pin
24	CSS/TRK	Soft-start adjustment pin
26	CE	Chip enable pin (Active "H")
27	SENSE	Sense pin for Inductor current
28	VOUT	Output voltage feedback input pin
29	RT	Oscillation adjustment pin
30	COMP	Capacitor connecting pin for Phase compensation of error amplifier
31	FB	Feedback input pin for Error amplifier
32	CLKOUT	Clock output pin

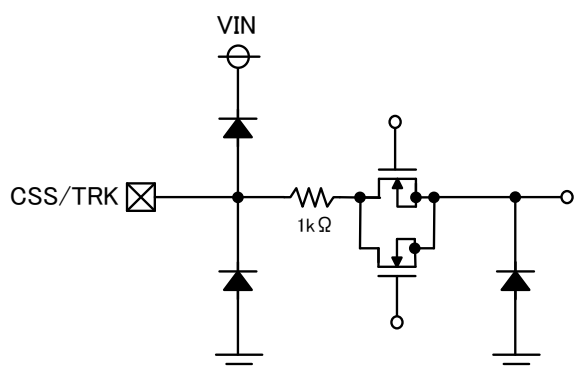
INTERNAL EQUIVALENT CIRCUIT FOR EACH PIN



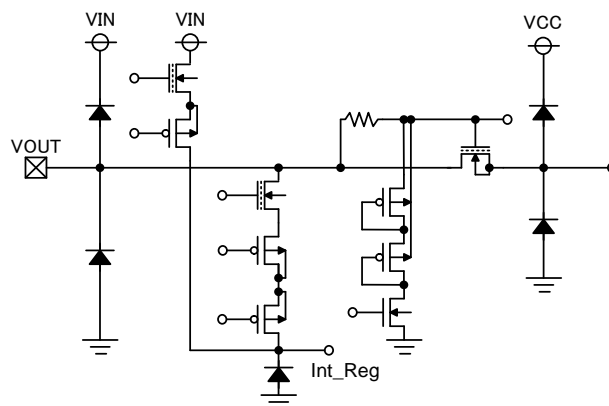
< VIN Pin >



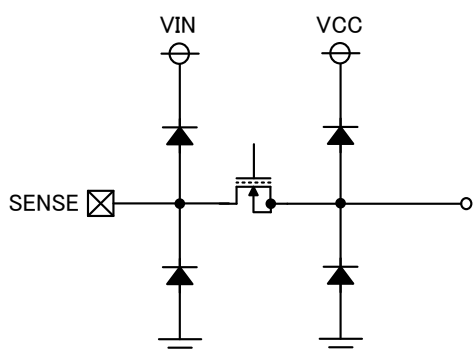
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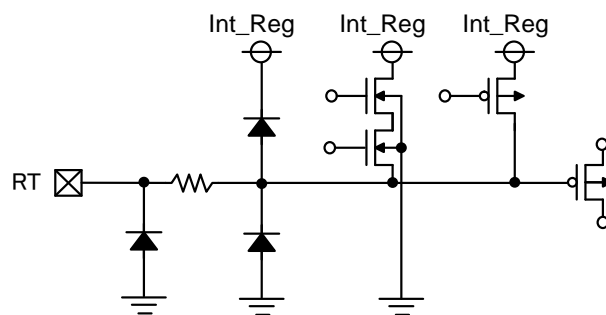
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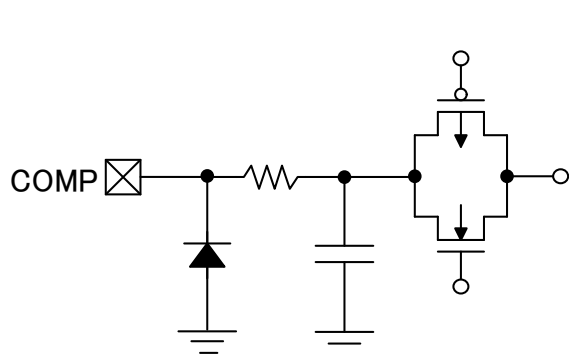
< VOUT Pin >



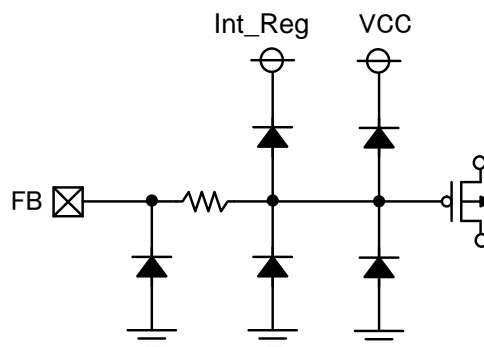
< SENSE Pin >



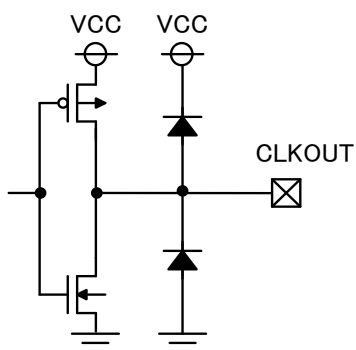
< RT Pin >



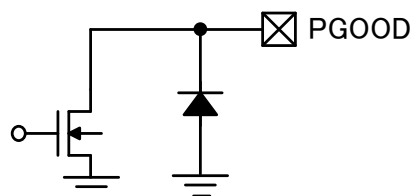
< COMP Pin >



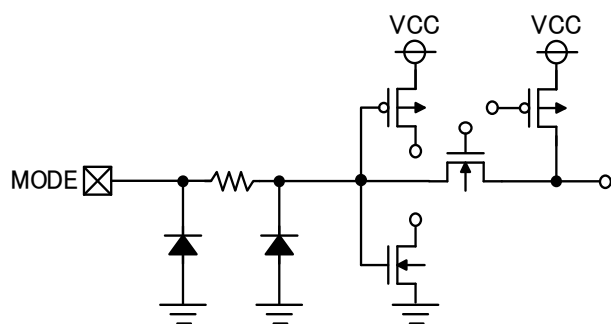
< FB Pin >



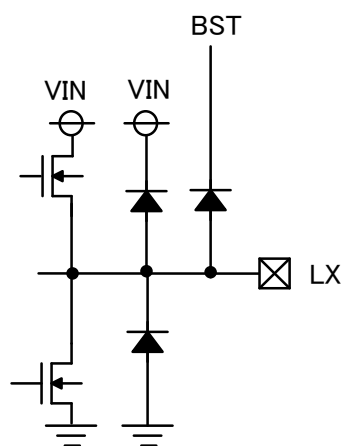
< CLKOUT Pin >



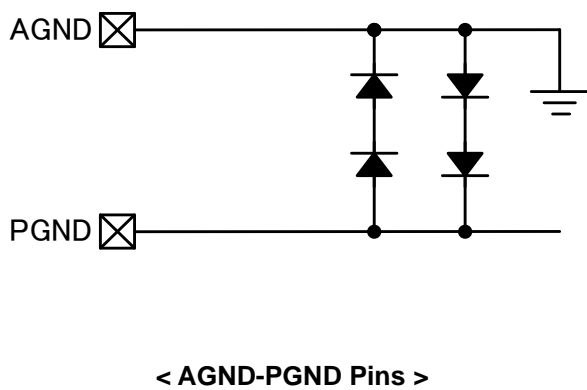
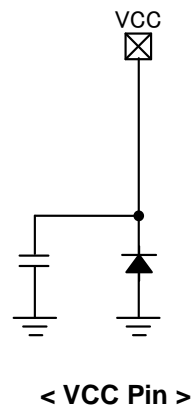
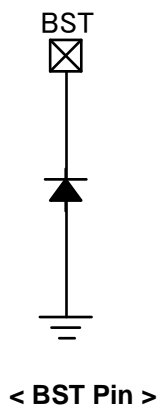
< PGOOD Pin >



< MODE Pin >



< LX Pin >



## ABSOLUTE MAXIMUM RATINGS

Symbol	Item	Rating	Unit
$V_{IN}$	VIN pin voltage	-0.3 to 36	V
$V_{CE}$	CE pin voltage	-0.3 to 36	V
$V_{CSS/TRK}$	CSS/TRK pin voltage	-0.3 to 3	V
$V_{OUT}$	VOUT pin voltage	-0.3 to 6	V
$V_{SENSE}$	SENSE pin voltage	-0.3 to 6	V
$V_{RT}$	RT pin voltage	-0.3 to 3	V
$V_{COMP}$	COMP pin voltage <sup>(1)</sup>	-0.3 to 6	V
$V_{FB}$	FB pin voltage	-0.3 to 3	V
$V_{CC}$	VCC pin voltage	-0.3 to 6	V
	Output current for VCC pin	Internally Limited	mA
$V_{BST}$	BST pin voltage	LX-0.3 to LX+6	V
$V_{LX}$	LX pin voltage <sup>(2)</sup>	-0.3 to 36	V
$V_{MODE}$	MODE pin voltage	-0.3 to 6	V
$V_{PGOOD}$	PGOOD pin voltage	-0.3 to 6	V
$V_{CLKOUT}$	CLKOUT pin voltage <sup>(1)</sup>	-0.3 to 6	V
$P_D$	Power Dissipation <sup>(3)</sup> (QFN0505-32B, JEDEC STD.51-7 Test Land Pattern)	2900	mW
$T_j$	Junction Temperature	-40 to 150	°C
$T_{stg}$	Storage Temperature Range	-55 to 150	°C

### ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause permanent damage and may degrade the life time and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings are not assured.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Item	Rating	Unit
$V_{IN}$	Input Voltage	4.0 to 34	V
$T_a$	Operating Temperature Range	-40 to 125	°C
$V_{OUT}$	Output Voltage Range	0.7 to 5.3	V

### RECOMMENDED OPERATING CONDITIONS

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if they are used over such ratings by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

<sup>(1)</sup> The pin voltage must be prevented from exceeding  $V_{CC} + 0.3V$ .

<sup>(2)</sup> The pin voltage must be prevented from exceeding  $V_{IN} + 0.3V$ .

<sup>(3)</sup> Refer to *POWER DISSIPATION* for detailed information.



## ELECTRICAL CHARACTERISTICS

$V_{IN} = 12\text{ V}$ ,  $CE = V_{IN}$ , unless otherwise specified.

The specifications surrounded by   are guaranteed by design engineering at  $-40^{\circ}\text{C} \leq T_a \leq 125^{\circ}\text{C}$ .

### R1273LxxxA Electrical Characteristics

( $T_a = 25^{\circ}\text{C}$ )

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit
$V_{START}$	Start-up Voltage				<span style="border: 1px solid black; padding: 0 2px;">4.5</span>	
$V_{CC}$	VCC Pin Voltage (VCC - AGND)	$V_{FB} = 0.672\text{ V}$	<span style="border: 1px solid black; padding: 0 2px;">4.9</span>	5.1	<span style="border: 1px solid black; padding: 0 2px;">5.3</span>	V
$I_{STANDBY}$	Standby Current	$V_{IN} = 34\text{ V}$ , $CE = 0\text{ V}$ ,		3	8	$\mu\text{A}$
$I_{VIN1}$	VIN Consumption Current 1 at Switching Stop in PWM mode	R1273L0xx $V_{FB} = 0.672\text{ V}$ , MODE = 5 V, $V_{OUT} = \text{SENSE} = \text{LX} = 5\text{ V}$		1.0	1.15	mA
		R1273L1xx $V_{FB} = 0.672\text{ V}$ , MODE = 5 V, $V_{OUT} = \text{SENSE} = 1.5\text{ V}$ , LX = 5 V		1.15	1.75	
$I_{VIN2}$	VIN Consumption Current 2 at Switching Stop in VFM mode	R1273L0xx $V_{FB} = 0.672\text{ V}$ , MODE = 0 V, $V_{OUT} = \text{SENSE} = \text{LX} = 5\text{ V}$		15	44	$\mu\text{A}$
		R1273L1xx $V_{FB} = 0.672\text{ V}$ , MODE = 0 V, $V_{OUT} = \text{SENSE} = 1.5\text{ V}$ , LX = 5 V		38	99	
$V_{UVLO2}$	UVLO Threshold Voltage	VCC Rising	<span style="border: 1px solid black; padding: 0 2px;">3.85</span>	4.0	<span style="border: 1px solid black; padding: 0 2px;">4.2</span>	V
$V_{UVLO1}$		VCC Falling	<span style="border: 1px solid black; padding: 0 2px;">3.1</span>	3.3	<span style="border: 1px solid black; padding: 0 2px;">3.4</span>	V
$V_{FB}$	FB Voltage Accuracy	$T_a = 25^{\circ}\text{C}$	0.6336	0.64	0.6464	V
		$-40^{\circ}\text{C} \leq T_a \leq 125^{\circ}\text{C}$	<span style="border: 1px solid black; padding: 0 2px;">0.6272</span>		<span style="border: 1px solid black; padding: 0 2px;">0.6528</span>	
$f_{OSC0}$	Oscillation Frequency 0	$R_T = 135\text{ k}\Omega$	<span style="border: 1px solid black; padding: 0 2px;">225</span>	250	<span style="border: 1px solid black; padding: 0 2px;">275</span>	kHz
$f_{OSC1}$	Oscillation Frequency 1	$R_T = 32\text{ k}\Omega$	<span style="border: 1px solid black; padding: 0 2px;">900</span>	1000	<span style="border: 1px solid black; padding: 0 2px;">1100</span>	kHz
$t_{OFF}$	Minimum Off Time	$V_{IN} = 5\text{ V}$ , $V_{OUT} = 5\text{ V}$		120	<span style="border: 1px solid black; padding: 0 2px;">190</span>	ns
$t_{ON}$	Minimum On Time			100	<span style="border: 1px solid black; padding: 0 2px;">120</span>	ns
$f_{SYNC}$	Synchronizing Frequency	$f_{OSC}$ as the reference	<span style="border: 1px solid black; padding: 0 2px;"><math>f_{OSC} \times 0.5</math></span>		<span style="border: 1px solid black; padding: 0 2px;"><math>f_{OSC} \times 1.5</math></span>	kHz
			<span style="border: 1px solid black; padding: 0 2px;">250</span>		<span style="border: 1px solid black; padding: 0 2px;">1000</span>	kHz
$t_{SS1}$	Soft-start Time 1	CSS/TRK = OPEN	<span style="border: 1px solid black; padding: 0 2px;">0.4</span>		<span style="border: 1px solid black; padding: 0 2px;">0.75</span>	ms
$t_{SS2}$	Soft-start Time 2	CSS = 4.7nF	<span style="border: 1px solid black; padding: 0 2px;">1.4</span>		<span style="border: 1px solid black; padding: 0 2px;">2.0</span>	ms
$I_{TSS}$	Charge Current for Soft-start pin	CSS/TRK = 0 V	<span style="border: 1px solid black; padding: 0 2px;">1.8</span>	2	<span style="border: 1px solid black; padding: 0 2px;">2.2</span>	$\mu\text{A}$
$V_{SSEND}$	CSS/TRK pin Voltage at End of Soft-start		$V_{FB}$	$V_{FB} + 0.03$	<span style="border: 1px solid black; padding: 0 2px;"><math>V_{FB} + 0.06</math></span>	V
$R_{DIS\_CSS}$	Discharge Resistance for CSS/TRK pin	$V_{IN} = 4.5\text{ V}$ , $CE = 0\text{ V}$ , CSS/TRK = 3 V	<span style="border: 1px solid black; padding: 0 2px;">2.0</span>	3.0	<span style="border: 1px solid black; padding: 0 2px;">5.0</span>	k $\Omega$

$V_{IN} = 12\text{ V}$ ,  $CE = V_{IN}$ , unless otherwise specified.

The specifications surrounded by   are guaranteed by design engineering at  $-40^{\circ}\text{C} \leq T_a \leq 125^{\circ}\text{C}$ .

## R1273LxxxA Electrical Characteristics Continued

(Ta = 25°C)

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit
V <sub>ILIMIT</sub>	Current Limit Threshold Voltage (SENSE – VOUT)	R1273Lxx1x	<span style="border: 1px solid black; padding: 0 2px;">40</span>	50	<span style="border: 1px solid black; padding: 0 2px;">60</span>	mV
		R1273Lxx2x	<span style="border: 1px solid black; padding: 0 2px;">60</span>	70	<span style="border: 1px solid black; padding: 0 2px;">80</span>	mV
		R1273Lxx3x	<span style="border: 1px solid black; padding: 0 2px;">90</span>	100	<span style="border: 1px solid black; padding: 0 2px;">110</span>	mV
V <sub>IREVLIMIT</sub>	Reverse Current Sense Threshold Voltage (SENSE – VOUT)	MODE = H / CLK R1273Lxx1x	<span style="border: 1px solid black; padding: 0 2px;">-35</span>	-25	<span style="border: 1px solid black; padding: 0 2px;">-15</span>	mV
		MODE = H / CLK R1273Lxx2x	<span style="border: 1px solid black; padding: 0 2px;">-45</span>	-35	<span style="border: 1px solid black; padding: 0 2px;">-25</span>	mV
		MODE = H / CLK R1273Lxx3x	<span style="border: 1px solid black; padding: 0 2px;">-60</span>	-50	<span style="border: 1px solid black; padding: 0 2px;">-40</span>	mV
V <sub>LXSHORTL</sub>	LX Short to GND Detector Threshold Voltage (VIN – LX)		<span style="border: 1px solid black; padding: 0 2px;">0.345</span>	0.43	<span style="border: 1px solid black; padding: 0 2px;">0.520</span>	V
V <sub>LXSHORTH</sub>	LX Short to VCC Detector Threshold Voltage (LX – PGND)		<span style="border: 1px solid black; padding: 0 2px;">0.330</span>	0.43	<span style="border: 1px solid black; padding: 0 2px;">0.515</span>	V
V <sub>CEH</sub>	CE "H" Input Voltage		<span style="border: 1px solid black; padding: 0 2px;">1.27</span>			V
V <sub>CEL</sub>	CE "L" Input Voltage				<span style="border: 1px solid black; padding: 0 2px;">1.14</span>	V
I <sub>CEH</sub>	CE "H" Input Current	CE = 34 V	<span style="border: 1px solid black; padding: 0 2px;">0.20</span>		<span style="border: 1px solid black; padding: 0 2px;">2.45</span>	μA
I <sub>CEL</sub>	CE "L" Input Current	CE = 0 V	<span style="border: 1px solid black; padding: 0 2px;">-1.00</span>	0	<span style="border: 1px solid black; padding: 0 2px;">1.00</span>	μA
I <sub>FBH</sub>	FB "H" Input Current	V <sub>FB</sub> = 3 V	<span style="border: 1px solid black; padding: 0 2px;">-0.1</span>		<span style="border: 1px solid black; padding: 0 2px;">0.1</span>	μA
I <sub>FBL</sub>	FB "L" Input Current	V <sub>FB</sub> = 0 V	<span style="border: 1px solid black; padding: 0 2px;">-0.1</span>		<span style="border: 1px solid black; padding: 0 2px;">0.1</span>	μA
V <sub>MODEH</sub>	MODE "H" Input Voltage		<span style="border: 1px solid black; padding: 0 2px;">1.33</span>			V
V <sub>MODEL</sub>	MODE "L" Input Voltage				<span style="border: 1px solid black; padding: 0 2px;">0.74</span>	V
I <sub>MODEH</sub>	MODE "H" Input Current	MODE = 6 V	<span style="border: 1px solid black; padding: 0 2px;">1.00</span>		<span style="border: 1px solid black; padding: 0 2px;">6.60</span>	μA
I <sub>MODEL</sub>	MODE "L" Input Current	MODE = 0 V	<span style="border: 1px solid black; padding: 0 2px;">-1.0</span>	0	<span style="border: 1px solid black; padding: 0 2px;">1.0</span>	μA
V <sub>CLKOUTH</sub>	Clock Output High Voltage	CLKOUT = Hi-Z	<span style="border: 1px solid black; padding: 0 2px;">4.7</span>		<span style="border: 1px solid black; padding: 0 2px;">VCC</span>	V
V <sub>CLKOUTL</sub>	Clock Output Low Voltage	CLKOUT = Hi-Z	<span style="border: 1px solid black; padding: 0 2px;">0</span>		<span style="border: 1px solid black; padding: 0 2px;">0.1</span>	V
T <sub>TSD</sub>	Temperature at Thermal Shutdown Detection	Ta Rising	<span style="border: 1px solid black; padding: 0 2px;">150</span>	160		°C
T <sub>TSR</sub>	Temperature at Thermal Shutdown Release	Ta Falling	<span style="border: 1px solid black; padding: 0 2px;">125</span>	140		°C
V <sub>PGOODOFF</sub>	PGOOD "Low" Output Voltage	V <sub>IN</sub> = 4.0 V, PGOOD = 1 mA		0.26	<span style="border: 1px solid black; padding: 0 2px;">0.54</span>	V
I <sub>PGOODOFF</sub>	PGOOD Pin Leakage Current	V <sub>IN</sub> = 34 V, PGOOD = 6 V	<span style="border: 1px solid black; padding: 0 2px;">-0.10</span>	0	<span style="border: 1px solid black; padding: 0 2px;">0.10</span>	μA
V <sub>FBOVD1</sub>	FB Pin OVD Threshold Voltage	V <sub>FB</sub> Rising	<span style="border: 1px solid black; padding: 0 2px;">0.680</span>	V <sub>FB</sub> ×1.10	<span style="border: 1px solid black; padding: 0 2px;">0.740</span>	V
V <sub>FBOVD2</sub>		V <sub>FB</sub> Falling	<span style="border: 1px solid black; padding: 0 2px;">0.664</span>	V <sub>FB</sub> ×1.07	<span style="border: 1px solid black; padding: 0 2px;">0.712</span>	V
V <sub>FBUVD1</sub>	FB Pin UVD Threshold Voltage	V <sub>FB</sub> Falling	<span style="border: 1px solid black; padding: 0 2px;">0.556</span>	V <sub>FB</sub> ×0.90	<span style="border: 1px solid black; padding: 0 2px;">0.604</span>	V
V <sub>FBUVD2</sub>		V <sub>FB</sub> Rising	<span style="border: 1px solid black; padding: 0 2px;">0.574</span>	V <sub>FB</sub> ×0.93	<span style="border: 1px solid black; padding: 0 2px;">0.628</span>	V
gm (EA)	Trans Conductance Amplifier	COMP = 1.5 V	<span style="border: 1px solid black; padding: 0 2px;">0.35</span>	1	<span style="border: 1px solid black; padding: 0 2px;">1.55</span>	mS

All test items listed under Electrical Characteristics are done under the pulse load condition (T<sub>J</sub> ≈ T<sub>a</sub> = 25°C).

## OPERATING DESCRIPTIONS

### MODE Pin Function

The R1273L operating mode is switched among the forced PWM mode, PWM/VFM auto-switching mode and PLL\_PWM mode, by a voltage or a pulse applied to MODE pin. The forced PWM mode is selected when the voltage of the MODE pin is more than 1.33 V, and the PWM works regardless of a load current. The PWM/VFM auto-switching mode is selected when it is less than 0.74 V, and control is switched between a PWM mode and a VFM mode depending on the load current.

See *Forced PWM mode and VFM mode* for details. And see *Frequency Synchronization Function* for the operation on connecting an external clock.

### Frequency Synchronization Function

The R1273L can synchronize to the external clock being inputted via the MODE pin, with using a PLL (Phase-locked loop). The forced PWM mode is selected during synchronization. The external clock with a pulse-width of 100 ns or more is required. The allowable range of oscillation frequency is 0.5 to 1.5 times of the set frequency<sup>(1)</sup>, and the operating guaranteed frequency is in the 250 kHz to 1 MHz range<sup>(2)</sup>. The R1273L can synchronize to the external clock even if the soft-start works. That is, the R1273L executes the soft-start and the synchronization functions at a time if having started up while inputting an external clock to the MODE pin. When the maxduty or the duty\_over state is caused by reduction in differential between input and output voltages, the device runs at asynchronous to the MODE pin, and it operates in the frequency reduced until one-fourth of the external clock frequency. Likewise, the CLKOUT pin becomes asynchronous to the MODE pin. If making synchronization to the MODE pin, take notice in use under a reduced input voltage.

### Duty\_over Function

When the input voltage is reduced at cranking, the operating frequency is reduced until one-fourth of the set frequency with being linearly proportional to time in order to maintain the output voltage. Exploiting the ON duty to exceed the maxduty value at normal operation can make the differential between input and output voltages small.

### PGOOD (Power Good) Output Function

The power good function with using a NMOS open drain output pin can detect the following states of the R1273L. The NMOS turns on and the PGOOD pin becomes “Low” when detecting them. After the R1273L returns to their original state, the NMOS turns off and the PGOOD pin outputs “High” (PGOOD Input Voltage:  $V_{UP}$ ).

- CE = “L” (Shut down)
- UVLO (Shut down)

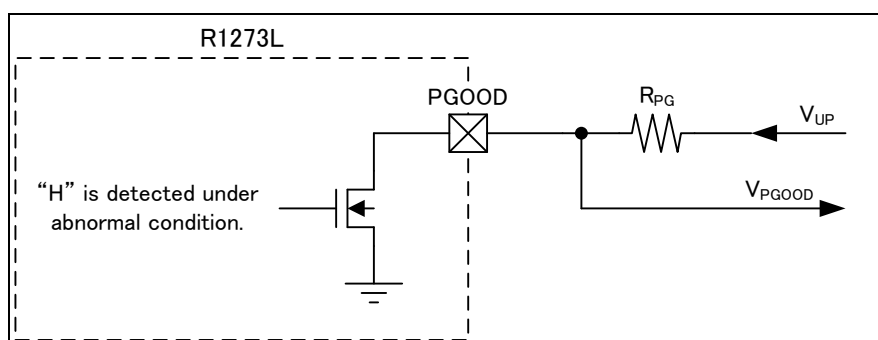
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<sup>(1)</sup> See *Oscillation Frequency Setting* for details of the set frequency.

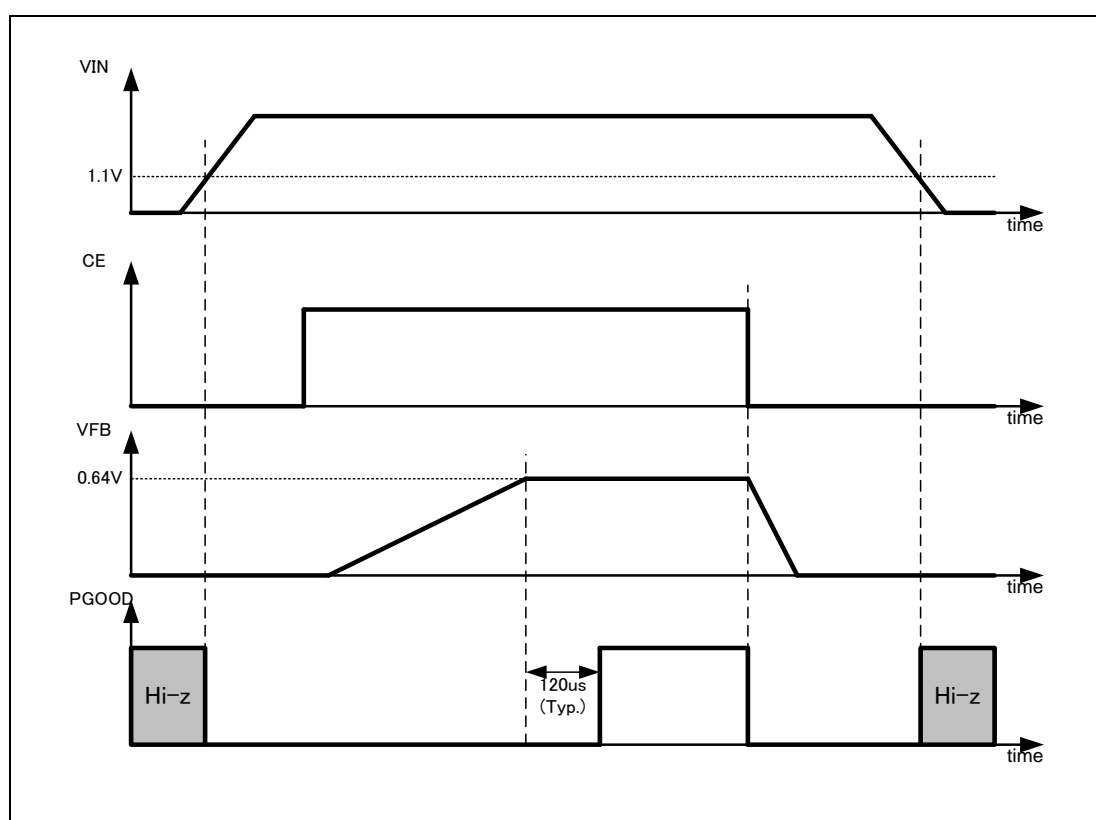
<sup>(2)</sup> The adjustable oscillation frequency range becomes  $250 \text{ kHz} \leq f_{osc} \leq 600 \text{ kHz}$  when  $0.7 \text{ V} \leq V_{OUT} < 1.35 \text{ V}$ .

- Thermal Shutdown
- Soft-start time
- at UVD Threshold Voltage Detection
- at OVD Threshold Voltage Detection
- at hiccup-type Protection (when hiccup mode is selected)
- at latch-type Protection (when latch mode is selected)

The PGOOD pin is designed to become 0.54 V or less in “Low” level when the current floating to the PGOOD pin is 1 mA. The use of the PGOOD input voltage ( $V_{UP}$ ) of 5.5 V or less and the pull-up resistor ( $R_{PG}$ ) of 10 k $\Omega$  to 100 k $\Omega$  are recommended. If not using the PGOOD pin, connect it to “Open” or “GND”.



PGOOD Output Pin Connecting Diagram



Rising / Falling Sequence of Power Good Circuit

### **Under Voltage Detection (UVD)**

The UVD function indirectly monitors the output voltage with using the FB pin. The PGOOD pin outputs “L” when the UVD detector threshold is 90% (Typ.) of  $V_{FB}$  and  $V_{FB}$  is less than the UVD detector threshold for more than 30  $\mu$ s (Typ.). When  $V_{FB}$  is over 93% (Typ.) of 0.64 V, the PGOOD pin outputs “H” after delay time (Typ.120  $\mu$ s.). And, the hiccup- / latch-type overcurrent protection works when detecting an overcurrent, an LX power supply protection, or an over voltage protection during the UVD detection.

### **Over Voltage Detection (OVD)**

The OVD function indirectly monitors the output voltage with using the FB pin. Switching stops even if the internal circuit is active state, when detecting the over voltage of  $V_{FB}$ . The PGOOD pin outputs “L” when the OVD detector threshold is 110% (Typ.) of  $V_{FB}$  and  $V_{FB}$  is over the OVD detector threshold for more than 30  $\mu$ s (Typ.). When  $V_{FB}$  is under 107% (Typ.) of  $V_{FB}$ , which is the OVD released voltage, the PGOOD pin outputs “H” after delay time (Typ.120  $\mu$ s.). Then, switching is controlled by normal operation. The over voltage protection works when an error is caused by a feedback resistor in peripheral circuits for the FB pin.

### **Over Voltage Protection (OVP)**

The OVP function monitors the voltage of VOUT pin to reduce an over voltage, when an error is caused in peripheral circuits for the FB pin. Switching stops even if the internal circuit is active state, when  $V_{OUT}$  is over the OVP detector threshold. When  $V_{OUT}$  is under the OVP detector threshold, switching is controlled by normal operation. If the UVD for FB pin occur during the OVP detect state, an error will occur and hiccup- / latch-type protection will work. However, the operation under this function is not guaranteed because the OVP detector threshold is set to the absolute maximum rating and more for the VOUT pin.

### **LX Power Supply (VIN Short) / GND (GND Short ) Protection**

In addition to normal current limit, the R1273L provides the LX power supply / GND short protection to monitor the voltage between the transistor’s drain and source. Since the current limit function is controlled with an external inductor’s DCR or a sense resistance, the current limit function cannot work when a through-current is flowed through the transistor and when an overcurrent is generated by shorting the LX pin to VDD/GND. The detecting current is determined by LX shot to VDD/GND detector threshold voltage ( $Tr\_ON$ -Resistance x Current, Typ.0.43 V).

### **Hiccup-type / Latch-type Overcurrent Protection**

The hiccup-type / latch-type overcurrent protection can work under the operating conditions that is the UVD can function during the current limit or OVP and the LX GND short protection. The latch-type protection can release the circuit by setting the CE pin to “L” or by reducing  $V_{IN}$  to be less than the UVLO detector threshold, when the output is latched off. The hiccup type protection stops switching releases the circuit after the protection delay time (Typ. 3.5 ms). Since this protection is auto-release, the CE pin switching of “L” / “H” is unnecessary. And, damage due to the overheating might not be caused because the term to release is long. When the output is shorted to GND, switching of “ON” / “OFF” is repeated until the shorting is released.

## Current Limit Function

The current limit function can be to limit the current by the peak current method to turn the high-side transistor off that the potential differences is over the current limit threshold voltage. The threshold voltage is selectable among 50 mV / 70 mV / 100 mV. And, the two following detection methods can be selected by external components connected.

### A. Detecting Method with $R_{SENSE}$

The current limit value is detected with the voltage across the inductor that a sense resistance is connected in series. By connecting a resistance with low level of variation, the current limit with high accuracy can achieve. As a result, be caution that the power loss is caused from the current and  $R_{SENSE}$ . The peak current in the current limit inductor can be calculated by the following equation.

$$\text{Peak current in Current limit inductor (A)} = \text{Current limit threshold voltage (mV)} / R_{SENSE} \text{ (m}\Omega\text{)}$$

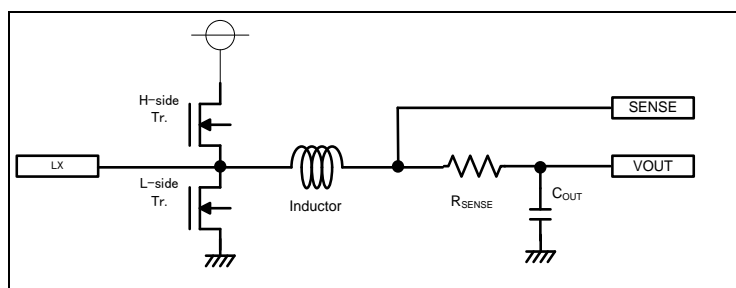


Figure A Detection with Sense Resistance

### B. Detecting Method with DCR of Inductor

The current limit value is detected with the DCR of the inductor. The reduction of the loss is minimized since the inductor is in no need of a resistance. But, the SENSE pin requires to connect a resistor and a capacitor to each end of the inductor. Because a constant slope is caused depending on the inductance and the capacitance. Factors causing the poor accuracy of current limit value include the variation in production of the inductor's DCR and the temperature characteristics.  $R_s$  and  $C_s$  can be calculated by the following equation.

$$\text{Peak current in Current limit inductor (A)} = \text{Current limit threshold voltage (mV)} / \text{Inductor's DCR (m}\Omega\text{)}$$

$$C_s = L / (\text{DCR} \times R_s)$$

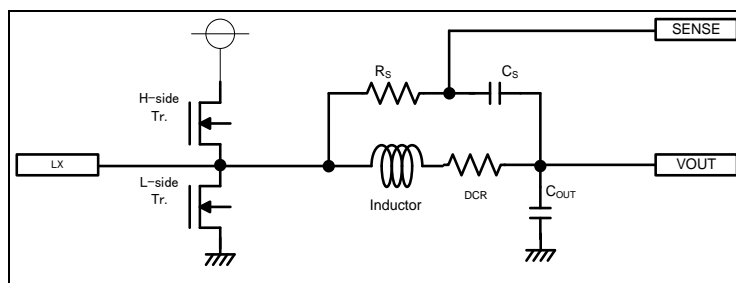


Figure B Detecting with Inductor's DCR

## Output Voltage Setting

The output voltage ( $V_{OUT}$ ) can be set by adjustable values of  $R_{TOP}$  and  $R_{BOT}$ . The value of  $V_{OUT}$  can be calculated by Equation 1 :

$$V_{OUT} = V_{FB} \times (R_{TOP} + R_{BOT}) / R_{BOT} \quad \text{..... Equation 1}$$

For example, when setting  $V_{OUT} = 3.3 \text{ V}$  and setting  $R_{BOT} = 22 \text{ k}\Omega$ ,  $R_{TOP}$  can be calculated by substituting them to Equation 1. As a result of the expanding Equation 2,  $R_{TOP}$  can be set to  $91.4 \text{ k}\Omega$ .

To make  $91.4 \text{ k}\Omega$  with using the E24 type resistors, the connecting use of  $91 \text{ k}\Omega$  and  $0.39 \text{ k}\Omega$  resistors in series is required. If the tolerance level of the set output voltage is wide, using a resistor of  $91 \text{ k}\Omega$  to  $R_{TOP}$  can reduce the number of components.

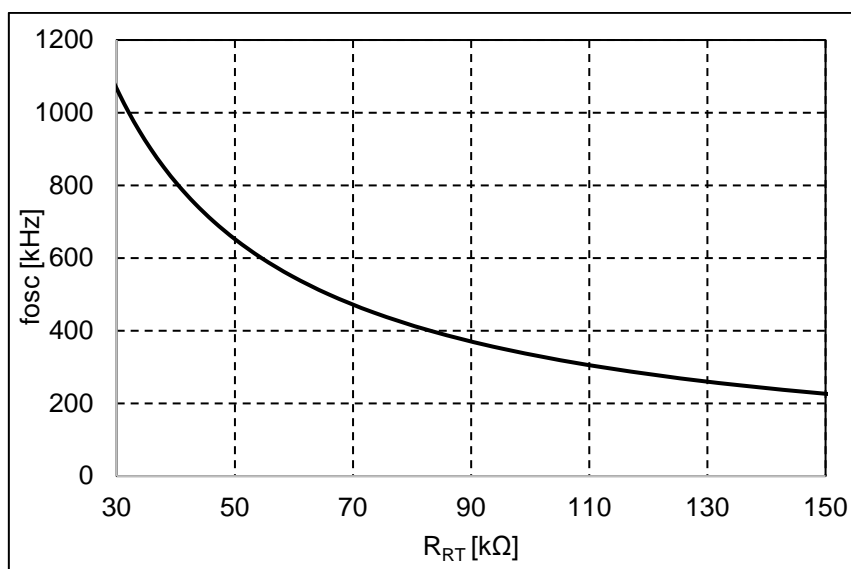
$$\begin{aligned} R_{TOP} &= (3.3 \text{ V} / 0.64 \text{ V} - 1) \times 22 \text{ k}\Omega \\ &= 91.4 \text{ k}\Omega \quad \text{..... Equation 2} \end{aligned}$$

As to R1273L00x, R1273L01x and R1273L03x,  $R_{TOP}$  and  $R_{BOT}$  should be selected to meet the required output voltage ( $V_{OUT}$ ) > 2.91 V with a variation in resistance taken into account.

## Oscillation Frequency Setting

Connecting the oscillation frequency setting resistor ( $R_{RT}$ ) between the RT pin and GND can control the oscillation frequency in the range of 250 kHz to 1 MHz<sup>(1)</sup>. For example, using the resistor of  $66 \text{ k}\Omega$  can set the frequency of about 500 kHz.

The Electrical Characteristics guarantees the oscillation frequency under the conditions stated below for  $f_{OSC0}$  (at  $R_{RT} = 135 \text{ k}\Omega$ ) and  $f_{OSC1}$  (at  $R_{RT} = 32 \text{ k}\Omega$ ).



$$R_{RT} [\text{k}\Omega] = 41993 \times f_{OSC} [\text{kHz}]^{-1.039}$$

R1273L001A Oscillation Frequency Setting Resistor ( $R_{RT}$ ) vs. Oscillation Frequency ( $f_{osc}$ )

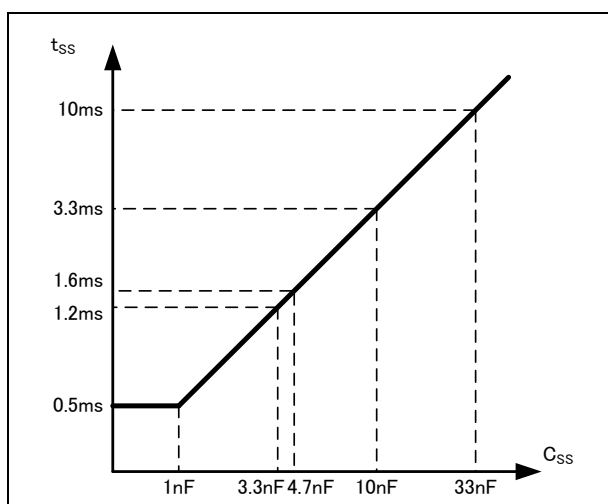
<sup>(1)</sup> The adjustable oscillation frequency range becomes  $250 \text{ kHz} \leq f_{osc} \leq 600 \text{ kHz}$  when  $0.7 \text{ V} \leq V_{OUT} < 1.35 \text{ V}$ .

## Soft-start Function

The soft-start time is a time between a rising edge (“H” level) of the CE pin and the timing when the output voltage reaches the set output voltage. Connecting a capacitor ( $C_{SS}$ ) to the CSS / TRK pin can adjust the soft-start time ( $t_{SS}$ ) – provided the internal soft-start time of 500  $\mu$ s (Typ.) as a lower limit. The adjustable soft-start time ( $t_{SS2}$ ) is 1.6 ms (Typ.) when connecting an external capacitor of 4.7 nF with the charging current of 2.0  $\mu$ A (Typ.). If not required to adjust the soft-start time, set the CSS / TRK pin to “Open” to enable the internal soft-start time ( $t_{SS1}$ ) of 500  $\mu$ s (Typ.).

If connecting a large capacitor to an output signal, the overcurrent protection or the LX GND short protection might run. To avoid these protections caused by starting abruptly when reducing the amount of power current, soft-start time must be set as long as possible.

Each of soft-start time ( $t_{SS1}$ /  $t_{SS2}$ ) is guaranteed under the conditions described in the chapter of “Electrical Characteristics”.

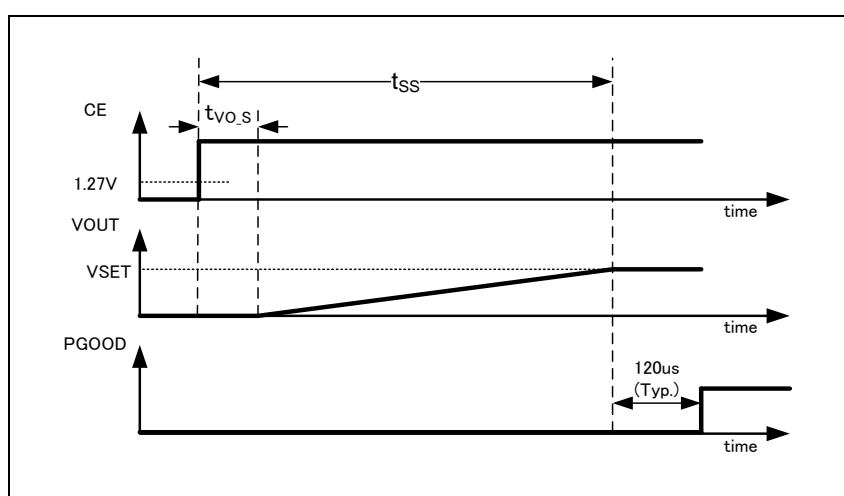


$$C_{SS} [\text{nF}] = (t_{SS} - t_{VO\_S}) / 0.64 \times 2.0$$

$t_{SS}$ : Soft-start time (ms)

$t_{VO\_S}$ : Time period from CE = “H” to VOUT’s rising (Typ. 0.160 ms)

Soft-start Time Adjustable Capacitor ( $C_{SS}$ ) vs. Soft-start Time ( $t_{SS}$ )

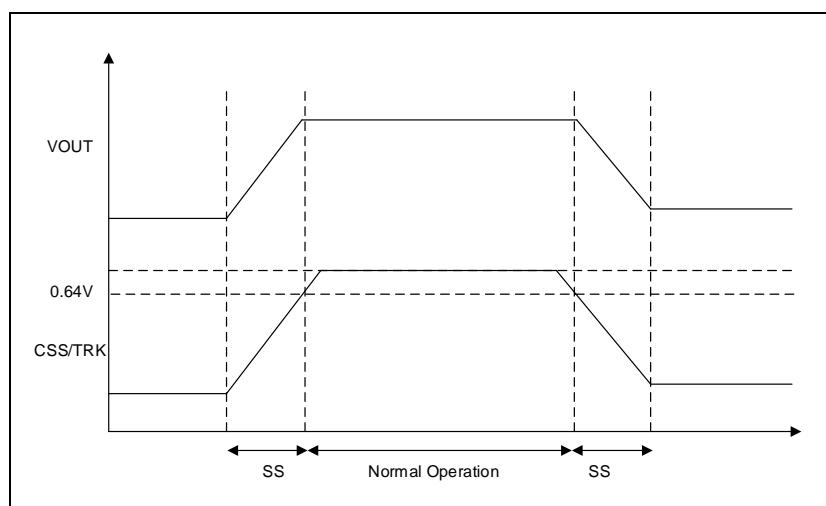


Soft-start Sequence



## Tracking Function

Applying an external tracking voltage to the CSS / TRK pin can control the soft-start sequence – provided that the lowest internal soft-start time is limited to 500  $\mu$ s (Typ.). Since  $V_{FB}$  becomes nearly equal to  $V_{CSS/TRK}$  at tracking, the complex start timing and soft-start can be easily designed. The available voltage at tracking is between 0 V and 0.64 V. If the tracking voltage is over 0.64 V, the internal reference voltage of 0.64 V is enabled. Also, an arbitrary falling waveform can be generated by reducing  $V_{CSS/TRK}$  to 0.64 V (Typ.) or less, because the R1273L supports both of up- and down- tracking.



Tracking Sequence

## Min. ON-time

The min. ON time (Max. 120 ns), which is determined in the R1273L internal circuit, is a minimum time to turn high-side transistor on. The R1273L cannot generate a pulse width less than the min. ON time. Therefore, settings of the output set voltage and the oscillator frequency are required so that the minimum step-down ratio [ $V_{OUT}/V_{IN} \times (1 / f_{OSC})$ ] does not stay below 120ns. If staying below 120 ns, the pulse skipping will operate to stabilize the output voltage. However, the ripple current and the output voltage ripple will be larger.

## Min. OFF-time

By the adoption of bootstrap method, the high-side transistor, which is used as the R1273L internal circuit for the min. OFF time, is used a NMOS. The voltage sufficient to drive the high-side transistor must be charged. Therefore, the min. OFF time is determined from the required time to charge the voltage. By the adoption of the frequency's reduction method by one-quarter of a set value (Min.), if the input-output difference voltage becomes small or load transients are caused, the OFF period can be caused once in four-cycle period of normal cycle. As a result, the min. OFF time becomes 30 ns (Typ.) substantially, and the maximum duty cycle can be improved.

## Reverse Current Limit Function

The reverse current limit function works when the output voltage is pulled up more than the set output voltage by shorting. When the current is over the threshold current to detect the reverse current, the low-side transistor is turned OFF to control the reverse current. As with the current limit value, the reverse current limit value is determined by the voltage between the VOUT pin and the SENSE pin. The detector threshold is one half of the current limit value.

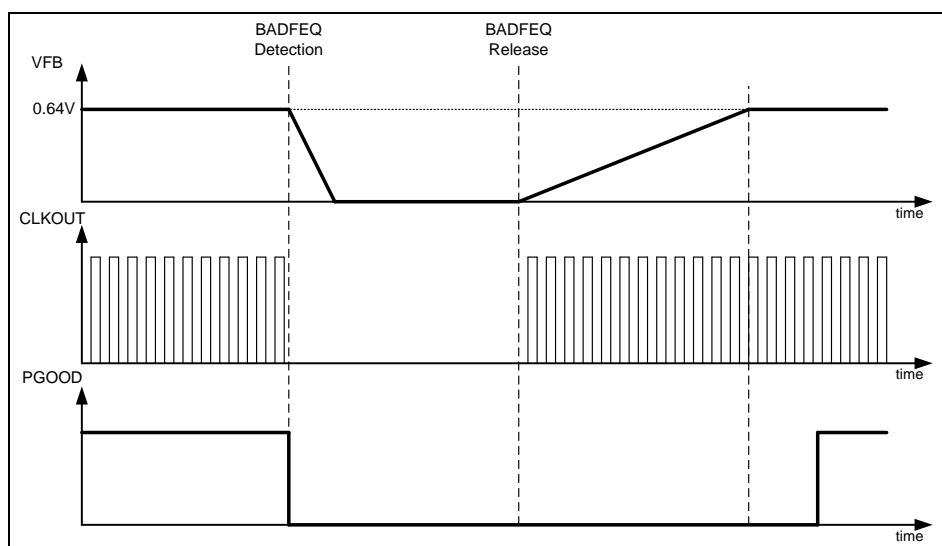
## SSCG (Spread Spectrum Clock Generator)

The SSCG function works for EMI reduction at the PWM mode. This function is enabled in the R1273L03xA/13xA.

This function makes EMI waveforms decrease in amplitude to generate a ramp waveform within approximately  $\pm 3.6\%$  (Typ.) of the oscillator frequency ( $f_{osc}$ ). The modulation cycle is  $f_{osc} / 128$ . At the VFM mode, the SSCG is disabled.

## Bad Frequency (BADFREQ) Protection

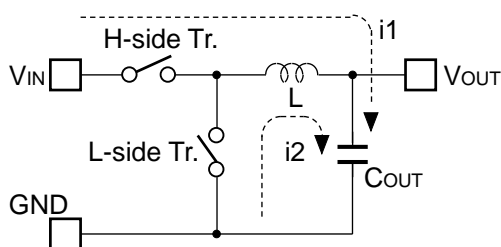
If a current equivalent to 2 MHz (Typ.) or more or 125 kHz (Typ.) or less is applied to the RT pin when the resistor of the RT pin is in open / short, the R1273L will stop switching to protect the IC and will cause the internal state to transition to its state before the soft-start. The CLKOUT pin is fixed to "L" while the bad frequency as above is detected. The R1273L will restart under the normal control from the state of soft-start when recover after the abnormal condition.



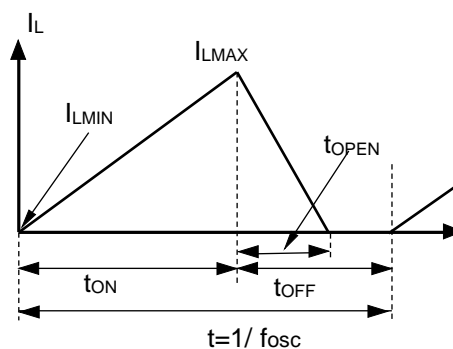
**BADFREQ Detection / Release Sequence**

## Operation of the Step-down Converter

A basic step-down DC/DC converter circuit is illustrated in the following figures. This DC/DC converter charges energy in the inductor when the high-side transistor turns on, and discharges the energy from the inductor when the high-side transistor turns off and controls with less energy loss, so that a lower output voltage than the input voltage is obtained.



**Basic Circuit**



**Current Through Inductor**

Step1. The high-side transistor turns on and current  $I_L (= i_1)$  flows, and energy is charged into  $C_{OUT}$ . At this moment,  $I_L$  increases from  $I_{LMIN} (= 0)$  to reach  $I_{LMAX}$  in proportion to the on-time period ( $t_{ON}$ ) of the high-side transistor turns on and current  $I_L (= i_1)$  flows, and energy is charged into  $C_{OUT}$ . At this moment,  $I_L$  increases from  $I_{LMIN} (= 0)$  to reach  $I_{LMAX}$  in proportion to the on-time period ( $t_{ON}$ ) of the high-side transistor.

Step2. When the high-side transistor turns off, the low-side transistor turns on in order to maintain  $I_L$  at  $I_{LMAX}$ , and current  $I_L (= i_2)$  flows.

Step3. When  $MODE = L$  (VFM/PWM Auto-switching mode),  $I_L (= i_2)$  decreases gradually and reaches  $I_L = I_{LMIN} = 0$  after a time period of  $t_{OPEN}$ , and the low-side transistor turns off. This case is called as discontinuous mode. The VFM mode is switched if go to the discontinuous mode. If the output current is increased, a time period of  $t_{OFF}$  runs out prior to reach of  $I_L = I_{LMIN} = 0$ . The result is that the high-side transistor turns on and the low-side transistor turns off in the next cycle. This case is called continuous mode.

When  $MODE = H$  (Forced PWM mode),  $MODE = External Clock$  (PLL\_PWM mode),

Since the continuous mode works at all time, the low-side transistor turns on until going to the next cycle. That is, the low-side transistor must keep "On" to meet  $I_L = I_{LMIN} < 0$ , when reaches  $I_L = I_{LMIN} = 0$  after a time period of  $t_{OPEN}$ .

In the PWM mode, the output voltage is maintained constant by controlling  $t_{ON}$  with the constant switching frequency ( $f_{osc}$ ).

## Forced PWM Mode and VFM Mode

The output voltage control methods are selectable between the PWM / VFM Auto-switching mode and the forced PWM mode by using the MODE pin.

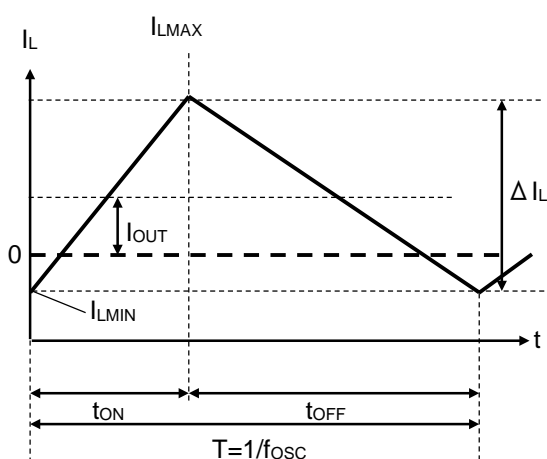
### Forced PWM Mode

Forced PWM mode is selected when setting the MODE pin to "H". This mode can reduce the output noise, since the frequency is fixed during light load conditions. Thus,  $I_{LMIN}$  becomes less than "0" when  $I_{OUT}$  is less than  $\Delta I_L/2$ . That is, the electric charge, which is charged to  $C_{OUT}$ , is discharged via transistor for the durations – when  $I_L$  reaches "0" from  $I_{LMIN}$  during the  $t_{ON}$  periods and when  $I_L$  reaches  $I_{LMIN}$  from "0" during  $t_{OFF}$  periods. But, pulses are skipped to prevent the overvoltage when high-side transistor is set to ON under the condition that the output voltage being more than the set output voltage.

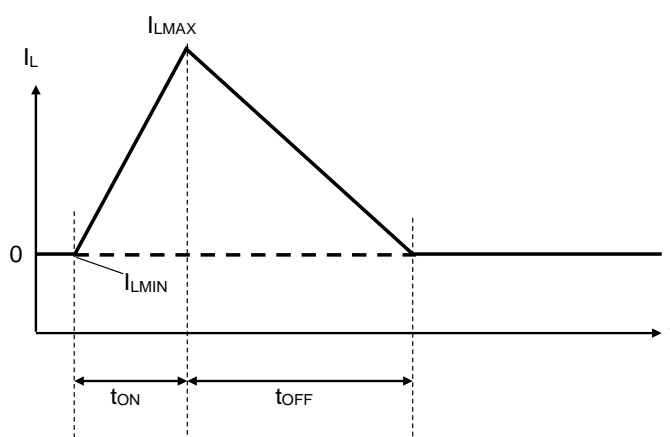
### VFM Mode

PWM / VFM Auto-switching mode is selected when setting the MODE pin to "L". This mode can automatically switch from PWM to VFM to achieve a high-efficiency during light load conditions. By the VFM mode architecture, the high-side transistor is turned on for  $t_{ON} \times 1.54$  (typ.) at the PWM mode under the same condition as the VFM mode when the VFB pin voltage drops below the internal reference voltage (Typ.0.64 V). After the On-time, the high-side transistor is turned off and the low-side transistor is turned on. When the inductor current of 0 A is detected, the low-side transistor is turned off and the switching operation is stopped (Both of hi- and low-side transistors are OFF). The switching operation restarts when the VFB pin voltage becomes less than 0.64 V.

The On-time at the PWM mode is determined by a resistance, input and output voltages, which are connected to the RT pin. Refer to "Calculation of VFM Ripple" for detailed description on the On-time at the VFM mode.



Forced PWM Mode



VFM Mode

### Calculation of VFM Ripple

Calculation example of output ripple voltage ( $V_{OUT\_VFM}$ ) is described.  $V_{OUT\_VFM}$  can be calculated by Equation 1. And, the maximum value of inductor current ( $I_{L\_VFM}$ ) can be calculated by Equation 2.

$$V_{OUT\_VFM} = R_{COUT\_ESR} \times (I_{L\_VFM}) + C_{COEF\_TON\_VFM} \times (I_{L\_VFM} / 2) / f_{OSC} / C_{OUT\_EFF} \dots\dots\dots \text{Equation 1}$$

$$I_{L\_VFM} = ((V_{IN} - V_{OUT}) / L) \times C_{COEF\_TON\_VFM} \times V_{OUT} / V_{IN} / f_{OSC} \dots\dots\dots \text{Equation 2}$$

$V_{OUT\_VFM}$  : Output ripple

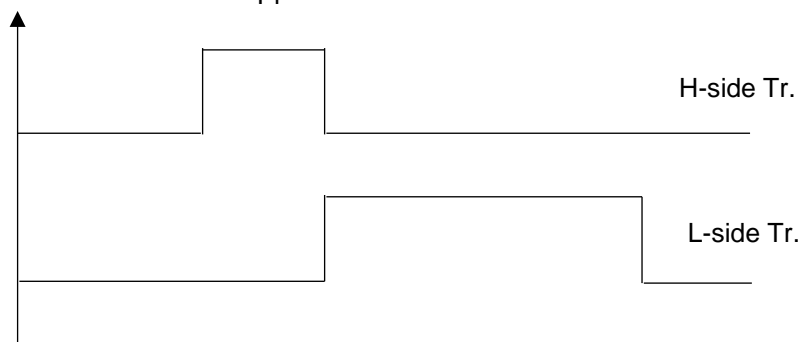
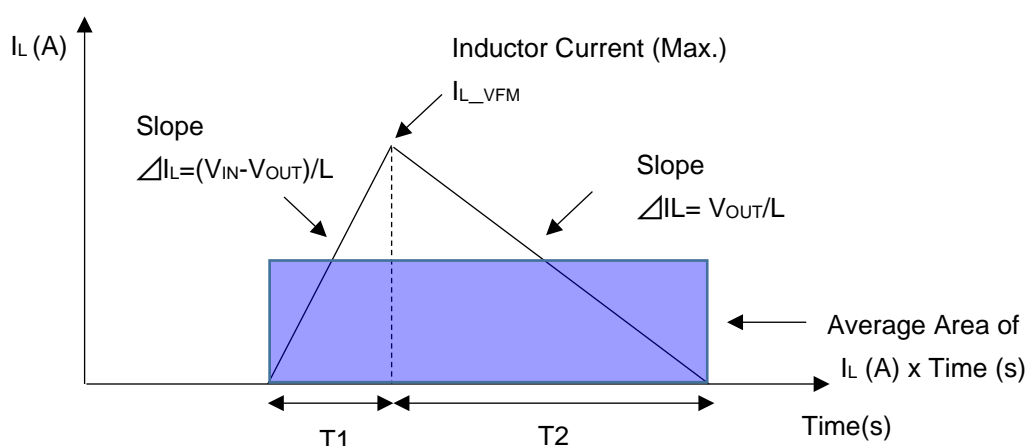
$R_{COUT\_ESR}$  : ESR of output capacitor

$I_{L\_VFM}$  : Maximum current of inductor

$C_{COEF\_TON\_VFM}$  : Scaling factor of On-time - Typ.1.54X (Design value)

$(V_{IN}-V_{OUT}) / L$  : Slope of inductor current

$C_{COEF\_TON\_VFM} \times V_{OUT} / V_{IN} / f_{OSC}$  : On-time



Inductor Current Waveform at VFM Mode

Output voltage can be calculated by the following simple equation.

$$V_{OUT} = I \times T/C$$

I : Current, C : Capacitance, T : Time

Since I is represented by  $1/2 \times I_{L\_VFM}$  as the average current, the time of current passing at the VFM mode can be expressed by the following equation.

$$T = C_{OEF\_TON\_VFM} / f_{OSC}$$

And, the output ripple voltage ( $V_{OUT\_VFM}$ ) is superimposed a voltage for  $ESR \times I$ , and Equation 1 is determined. But, ESR is so small that it may be ignored if ceramic capacitors are connected in parallel.

The amount of charge to the output capacitor can be calculated by Equation 3.

$$(High\text{-}side\ Tr.\ On\text{-}time\ (T1) + Low\text{-}side\ Tr.\ On\text{-}time\ (T2)) \times \text{Average amount of current} \dots\dots\dots \text{Equation 3}$$

Then, T1 and T2 can be calculated by the following equations, and the time of current passing can be determined.

$$\begin{aligned} T1 &= C_{OEF\_TON\_VFM} / f_{OSC} \times V_{OUT} / V_{IN} \dots\dots (On\text{-}time\ at\ VFM) \\ T2 &= (V_{IN}/V_{OUT}-1) \times T1 \quad (0 = I_{L\_VFM} - V_{OUT}/L \times T2) \\ T &= T1 + T2 \\ &= V_{IN} / V_{OUT} \times T1 \\ &= C_{OEF\_TON\_VFM} / f_{OSC} \end{aligned}$$

And then, the amount of charge can be determined as Equation 4.

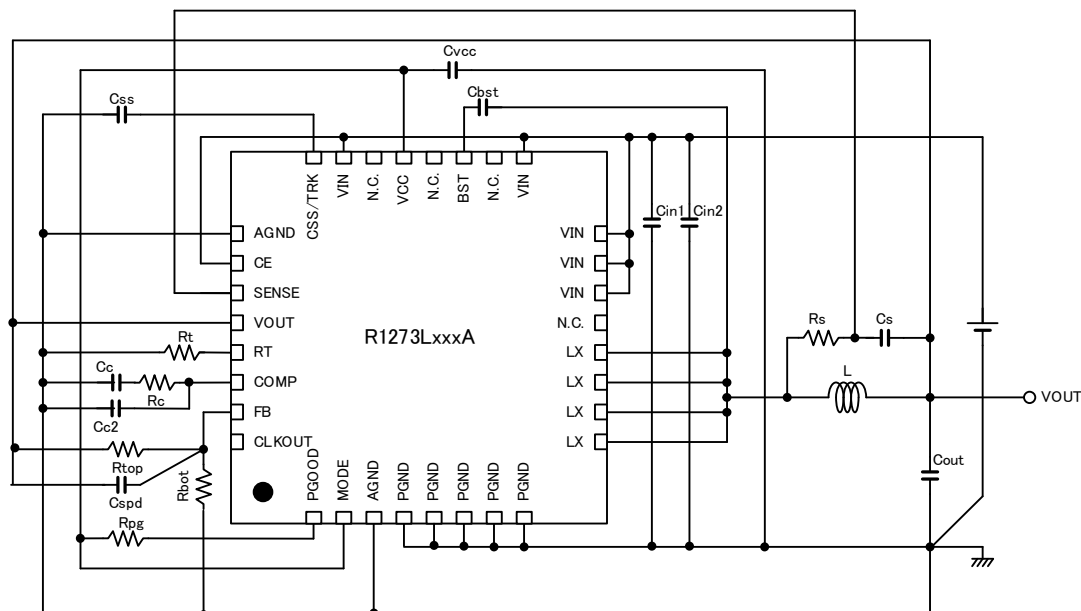
$$T \times I_{L\_VFM} / 2 = C_{OEF\_TON\_VFM} / f_{OSC} \times I_{L\_VFM} / 2 \dots\dots\dots \text{Equation 4}$$

With using above-equations, the output ripple voltage ( $V_{OUT\_VFM}$ ) can be calculated by Equation 5.

$$V = IT/C = C_{OEF\_TON\_VFM} / f_{OSC} \times I_{L\_VFM} / 2 / C_{OUT\_EFF} \dots\dots\dots \text{Equation 5}$$

## APPLICATION INFORMATION

## Typical Application Circuit



R1273LxxxA Typical Application Circuit

## Recommended External Components

Symbol	Input Voltage (V <sub>IN</sub> )	Spec.	Product Name
C <sub>IN</sub>	≤ 16 V	4.7 μF, 25 V, 125°C	GRM32ER71H106KA12L (Murata)
		10μF, 25 V, 125°C	CGA6P1X7R1E106K (TDK)
	4.0 V ~ 34 V	4.7 μF, 25 V, 125°C	CGA6P3X7R1H475K (TDK)
		10 μF, 50 V, 125°C	CGA6P3X7S1H106K (TDK)
C <sub>OUT</sub>	4.0 V ~ 34 V	22 μF, 6.3 V, 125°C	CGA5L1X7R0J226M (TDK)
		22 μF, 16 V, 125°C	CGA6P1X7R1C226M (TDK)
		47 μF, 10 V, 125°C	GRM32ER71A476KE15L (Murata)
		100μF, 16 V, 125°C	CKG57NX7S1C107M (TDK)
Symbol	Inductance	Spec.	Product Name
L	0.56 μH	32 A	FDU1250C-H-R56M (TOKO)
		20 A	CLF12555T-1R0M-D (TDK)
	1.5 μH	26 A	VLM13580T-1R5M-D1 (TDK)
		16.4 A	CLF12555T-1R5M-D (TDK)
	2.2 μH	20 A	VLM13580T-2R2M-D1 (TDK)
		13.1 A	CLF12555T-2R2M-D (TDK)
	3.3 μH	18 A	VLM13580T-3R3M-D1 (TDK)
		11.4 A	CLF12555T-3R3M-D (TDK)

## Selection of External Components

External components and its value required for R1273L are described. Each value is reference value at initial. Since inductor's variations and output capacitor's effective value may lead a drift of phase characteristics, adjustment to a unity-gain and phase characteristics may be required by evaluation on the actual unit.

### 1. Determination of Requirements

Determine the frequency, the output capacitor, and the input voltage required. For reference values, parameters listed in the following table will be used to explain each equation.

Parameter	Value
Output Voltage ( $V_{OUT}$ )	3.3 V
Output Current ( $I_{OUT}$ )	10 A
Input Voltage ( $V_{IN}$ )	12 V
Input Voltage Range	8 V to 16 V
Frequency ( $f_{OSC}$ )	500 kHz
ESR of Output Capacitor ( $R_{COUT\_ESR}$ )	3 m $\Omega$

### 2. Selection of Unity-gain frequency ( $f_{UNITY}$ )

The unity-gain frequency ( $f_{UNITY}$ ) is determined by the frequency that the loop gain becomes "1" (zero dB). It is recommended to select within the range of one-sixth to one-tenth of the oscillator frequency ( $f_{OSC}$ ). Since the  $f_{UNITY}$  determines the transient response, the higher the  $f_{UNITY}$ , the faster response is achieved, but the phase margin will be tight. Therefore, it is required that the  $f_{UNITY}$  can secure the adequate stability. As for the reference, the  $f_{UNITY}$  is set to 70 kHz.

### 3. Selection of Inductor

After the input and the output voltages are determined, a ripple current ( $\Delta I_L$ ) for the inductor current is determined by an inductance (L) and an oscillator frequency ( $f_{OSC}$ ). The ripple current ( $\Delta I_L$ ) can be calculated by Equation 1.

$$\Delta I_L = (V_{OUT} / L / f_{OSC}) \times (1 - V_{OUT} / V_{IN\_MAX}) \dots \dots \dots \text{Equation 1}$$

$V_{IN\_MAX}$  : Maximum input voltage

The core loss in the inductor and the ripple current of the output voltage become small when the ripple current ( $\Delta I_L$ ) is small. But, a large inductance is required as shown by Equation 1. The inductance can be calculated by Equation 2 when a reference value of  $\Delta I_L$  assumes 30% of  $I_{OUT}$  is appropriate value.

$$L = (V_{OUT} / \Delta I_L / f_{OSC}) \times (1 - V_{OUT} / V_{IN\_MAX}) \dots \dots \dots \text{Equation 2}$$

$$= (V_{OUT} / (I_{OUT} \times 0.3) / f_{OSC}) \times (1 - V_{OUT} / V_{IN\_MAX})$$

The inductance can be calculated by substituting each parameter to Equation 2.

$$L = (3.3 \text{ V} / 3 \text{ A} / 500 \text{ kHz}) \times (1 - 3.3 \text{ V} / 16 \text{ V})$$

$$= 1.75 \text{ } \mu\text{H}$$



When selecting the inductor of 2.2μH as an approximate value of the above calculated value,  $\Delta I_L$  can be shown as below.

$$\begin{aligned}\Delta I_L &= (3.3 \text{ V} / 2.2 \text{ } \mu\text{H} / 500 \text{ kHz}) \times (1 - 3.3 \text{ V} / 16 \text{ V}) \\ &= 2.38 \text{ A}\end{aligned}$$

#### 4. Setting of Output Capacitance

The output capacitance ( $C_{OUT}$ ) must be set to meet the following conditions.

##### ■ Calculation based on phase margin

To secure the adequate stability, it is recommended that the pole frequency ( $f_{P\_OUT}$ ) is set to become equal or below one-fourteenth of the unity-gain frequency. The pole frequency ( $f_{P\_OUT}$ ) can be calculated by Equation 3.

$$f_{P\_OUT} = 1 / (2 \times \pi \times C_{OUT\_EFF} \times ((R_{OUT\_MIN} \times 2 \times \pi \times f_{OSC} \times L) / (R_{OUT\_MIN} + 2 \times \pi \times f_{OSC} \times L) + R_{COUT\_ESR})) \dots\dots\dots \text{Equation 3}$$

$C_{OUT\_EFF}$  : Output capacitance (effective value)

$R_{OUT\_MIN}$  : Output resistance at maximum output current

$$\begin{aligned}R_{OUT\_MIN} &= V_{OUT} / I_{OUT} \\ &= 3.3 \text{ V} / 10 \text{ A} \\ &= 0.33 \text{ } \Omega\end{aligned}$$

Equation 4 can be expressed by substituting  $f_{P\_OUT} = f_{UNITY} / 14$  to Equation 3.

$$C_{OUT\_EFF} = 14 / (2 \times \pi \times f_{UNITY} \times ((R_{OUT\_MIN} \times 2 \times \pi \times f_{OSC} \times L) / (R_{OUT\_MIN} + 2 \times \pi \times f_{OSC} \times L) + R_{COUT\_ESR})) \dots\dots\dots \text{Equation 4}$$

Then, the output capacitance (effective value) can be calculated by substituting each parameter to Equation 4.

$$\begin{aligned}C_{OUT\_EFF} &= 14 / (2 \times \pi \times 70 \text{ kHz} \times ((0.33 \text{ } \Omega \times 2 \times \pi \times 500 \text{ kHz} \times 2.2 \text{ } \mu\text{H}) / (0.33 \text{ } \Omega + 2 \times \pi \times 500 \text{ kHz} \times 2.2 \text{ } \mu\text{H}) + 3 \text{ m}\Omega)) \\ &= 100.1 \text{ } \mu\text{F}\end{aligned}$$

It is recommended that the output capacitance is set to become equal or over the effective value calculated by Equation 4.

The output capacitance (effective value), which is derated depending on the DC voltage applied, can be calculated by Equation 5. Refer to “*Capacitor Manufacture’s Datasheet*” for details about derating.

$$C_{OUT\_EFF} = C_{OUT\_SET} \times (V_{CO\_AB} - V_{OUT}) / V_{CO\_AB} \dots\dots\dots \text{Equation 5}$$

$C_{OUT\_SET}$  : Output capacitor’s spec

$V_{CO\_AB}$  : Capacitor’s voltage rating

With using Equation 5, the effective value is calculated to become 100.1  $\mu\text{F}$  or more. The output voltage ( $C_{\text{OUT}}$ ) can be shown as below when  $V_{\text{CO\_AB}}$  is 10 V.

$$\begin{aligned} C_{\text{OUT\_SET}} &> C_{\text{OUT\_EFF}} / ((V_{\text{CO\_AB}} - V_{\text{OUT}}) / V_{\text{CO\_AB}}) \\ C_{\text{OUT\_SET}} &> 100.1\mu\text{F} / ((10 - 3.3) / 10) \\ C_{\text{OUT}} &> 149.4 \mu\text{F} \end{aligned}$$

As the calculated result,  $C_{\text{OUT}}$  selects a capacitor of 150  $\mu\text{F}$  (the effective value is 100.5  $\mu\text{F}$ ).

#### ■ Calculation based on ripple at VFM mode

With using the calculated value of  $C_{\text{OUT}}$ , the amount of ripple at the VFM mode can be shown as Equations 6 and Equation 7.

$$I_{\text{L\_VFM}} = ((V_{\text{IN\_MAX}} - V_{\text{OUT}}) / L) \times C_{\text{COEF\_TON\_VFM}} \times V_{\text{OUT}} / V_{\text{IN\_MAX}} / f_{\text{OSC}} \dots\dots\dots \text{Equation 6}$$

$$V_{\text{OUT\_VFM}} = R_{\text{COUT\_ESR}} \times (I_{\text{L\_VFM}}) + C_{\text{COEF\_TON\_VFM}} \times (I_{\text{L\_VFM}} / 2) / f_{\text{OSC}} / C_{\text{OUT\_EFF}} \dots\dots\dots \text{Equation 7}$$

$I_{\text{L\_VFM}}$  : Maximum current of inductor

$C_{\text{COEF\_TON\_VFM}}$  : On-time scaling (multiples of PWM\_ON time)

$V_{\text{OUT\_VFM}}$  : Maximum output ripple

$C_{\text{COEF\_TON\_VFM}}$  can be calculated by 1.54 times (Typ.) as the design value. The ripple value can be calculated by substituting each parameter to Equations 6 and Equation 7.

$$\begin{aligned} I_{\text{L\_VFM}} &= ((16 \text{ V} - 3.3 \text{ V}) / 2.2 \mu\text{H}) \times 1.54 \times 3.3 \text{ V} / 16 \text{ V} / 500 \text{ kHz} \\ &= 3.67 \text{ A} \end{aligned}$$

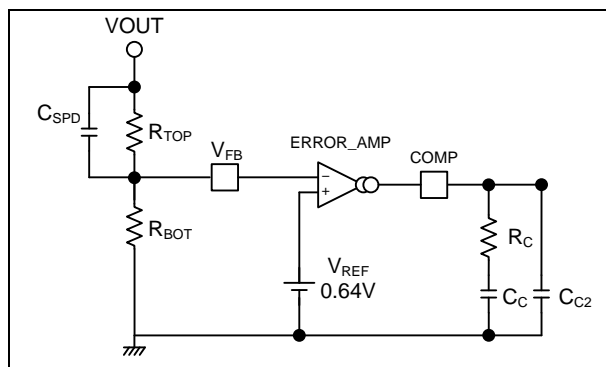
$$\begin{aligned} V_{\text{OUT\_VFM}} &= 3 \text{ m}\Omega \times 3.67 \text{ A} + 1.54 \times (3.67 \text{ A} / 2) / 500 \text{ kHz} / 100.5 \mu\text{F} \\ &= 67.2 \text{ mV} \end{aligned}$$

$V_{\text{OUT\_VFM}}$  must be set to become the target ripple value or less. If  $V_{\text{OUT\_VFM}}$  is over the target value, the output capacitance must be calculated by Equation 8.

$$C_{\text{OUT\_EFF}} = 1.54 \times (I_{\text{L\_VFM}} / 2) / f_{\text{OSC}} / (V_{\text{OUT\_VFM}} - R_{\text{COUT\_ESR}} \times (I_{\text{L\_VFM}})) \dots\dots\dots \text{Equation 8}$$

## 5. Designation of Phase Compensation

Since the current amplifier for the voltage feedback is output via the COMP pin, the phase compensation is achieved with using external components. The phase compensation is able to secure stable operation with using an external ceramic capacitor and the phase compensation circuit.



Connection Example for External Phase Compensation Circuit

### ■ Calculation of $R_C$

The phase compensation resistance ( $R_C$ ) to set the calculated unity-gain frequency can be calculated by Equation 9.

$$R_C = 2 \times \pi \times f_{\text{UNITY}} \times V_{\text{OUT}} \times C_{\text{OUT\_EFF}} / (g_{m\_ea} \times V_{\text{REF}} \times g_{m\_pwr}) \dots\dots\dots \text{Equation 9}$$

$g_{m\_ea}$  : Error amplifier of  $g_m$   
 $V_{\text{REF}}$  : Reference voltage (0.64 V)  
 $g_{m\_pwr}$  : power level of  $g_m$

$$\begin{aligned} g_{m\_pwr} \times \Delta V_s &= \Delta I_L \\ g_{m\_ea} / \Delta V_s &= 0.05 \times 10^{-6} \times f_{\text{OSC}} / V_{\text{OUT}} \\ g_{m\_ea} \times g_{m\_pwr} &= 0.05 \times 10^{-6} \times \Delta I_L \times f_{\text{OSC}} / V_{\text{OUT}} \dots\dots\dots \text{Equation 10} \end{aligned}$$

$\Delta V_s$  : Output amplitude of the slope circuit

$R_C$  can be calculated by substituting Equation 10 to Equation 9.

$$\begin{aligned} R_C &= 2 \times \pi \times f_{\text{UNITY}} \times V_{\text{OUT}} \times C_{\text{OUT\_EFF}} / (V_{\text{REF}} \times 0.05 \times 10^{-6} \times \Delta I_L \times f_{\text{OSC}} / V_{\text{OUT}}) \\ &= 2 \times \pi \times 70 \text{ kHz} \times 3.3 \text{ V} \times 100.5 \mu\text{F} / (0.64 \times 0.05 \times 10^{-6} \times 2.38\text{A} \times 500 \text{ kHz} / 3.3 \text{ V}) \\ &= 12.63 \approx 13 \text{ k}\Omega \end{aligned}$$

#### ■ Calculation of $C_C$

$C_C$  must be calculated by Equation 11 so that the zero frequency of the error amplifier meets the highest pole frequency ( $f_{P\_OUT}$ ). Then,  $f_{P\_OUT} = 5.0$  kHz is determined by calculation of Equation 3.

$$\begin{aligned} C_C &= 1 / (2 \times \pi \times R_C \times f_{P\_OUT}) \dots\dots\dots \text{Equation 11} \\ &= 1 / (2 \times 3.14 \times 13 \text{ k}\Omega \times 5.0 \text{ kHz}) \\ &= 2.45 \approx 2.7 \text{ nF} \end{aligned}$$

#### ■ Calculation of $C_{C2}$

$C_{C2}$  can be calculated by two different calculation methods to vary from the zero frequency ( $f_{Z\_ESR}$ ) depending on the ESR of a capacitor.  $f_{Z\_ESR}$  can be calculated by Equation 12.

$$\begin{aligned} f_{Z\_ESR} &= 1 / (2 \times \pi \times R_{COUT\_ESR} \times C_{OUT\_EFF}) \dots\dots\dots \text{Equation 12} \\ &= 528 \text{ kHz} \end{aligned}$$

[When the zero frequency is lower than  $f_{OSC} / 2$ ]

$C_{C2}$  sets the pole to  $f_{Z\_ESR}$ .

$$C_{C2} = R_{COUT\_ESR} \times C_{OUT\_EFF} / R_C \dots\dots\dots \text{Equation 13}$$

[When the zero frequency is higher  $f_{OSC} / 2$ ]

$C_{C2}$  sets the pole to  $f_{OSC} / 2$  so as to be a noise filter for the COMP pin.

$$\begin{aligned} f_{OSC} / 2 &= 1 / (2 \times \pi \times R_C \times C_{C2}) \\ C_{C2} &= 2 / (2 \times \pi \times R_C \times f_{OSC}) \dots\dots\dots \text{Equation 14} \end{aligned}$$

In the reference example,  $C_{C2}$  is used as the noise filter for the COMP pin because of being higher than  $f_{OSC}/2$ .

$$C_{C2} = 49 \approx 47 \text{ pF}$$

#### ■ Calculation of $C_{SPD}$

$C_{SPD}$  sets the zero frequency to meet the unity-gain frequency.

$$\begin{aligned} R_{TOP} &= R_{BOT} \times (V_{OUT} / V_{REF} - 1) \\ C_{SPD} &= 1 / (2 \times \pi \times f_{UNITY} \times R_{TOP}) \dots\dots\dots \text{Equation 15} \end{aligned}$$

$$\begin{aligned} \text{When } R_{BOT} &= 22 \text{ k}\Omega, \\ R_{TOP} &= 22 \text{ k} \times (3.3 \text{ V} / 0.64 \text{ V} - 1) \\ &= 91.4 \text{ k}\Omega \end{aligned}$$

$$\begin{aligned} C_{SPD} &= 1 / (2 \times \pi \times 70 \text{ kHz} \times 91.4 \text{ k}\Omega) \\ &= 24.8 \approx 27 \text{ pF} \end{aligned}$$

## Cautions in Selecting External Components

### Inductor

- Choose an inductor that has small DC resistance, has sufficient allowable current and is hard to cause magnetic saturation. The inductance value must be determined with consideration of load current under the actual condition. If the inductance value of an inductor is extremely small, the peak current of LX may increase along with the load current. As a result, the current limit circuit may start to operate when the peak current of LX reaches to “LX limit current”.

### Capacitor

- Choose a capacitor that has a sufficient margin to the drive voltage ratings with consideration of the DC bias characteristics and the temperature characteristics.
- The use of a ceramic capacitor for C<sub>IN</sub> is recommended. If combined use of a ceramic and an electrolyte capacitors, the stable operation will improve since the margin becomes bigger. Choose the electrolyte capacitor with the lowest possible ESR with consideration of the allowable ripple current rating (I<sub>RMS</sub>). I<sub>RMS</sub> can be calculated by the following equation.

$$I_{RMS} \doteq I_{OUT} / V_{IN} \times \sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}$$

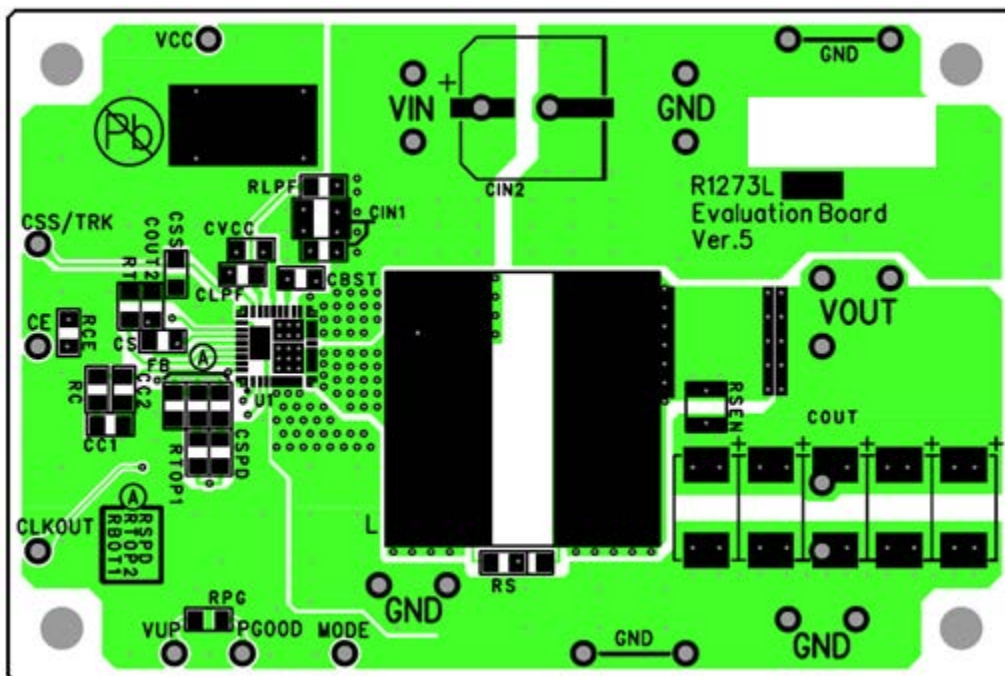
## TECHNICAL NOTES

The performance of power source circuits using this IC largely depends on peripheral circuits. When selecting the peripheral components, please consider the conditions of use. Do not allow each component, PCB pattern or the IC to exceed their respected rated values (voltage, current, and power) when designing the peripheral circuits. Refer to the PCB layouts as reference design.

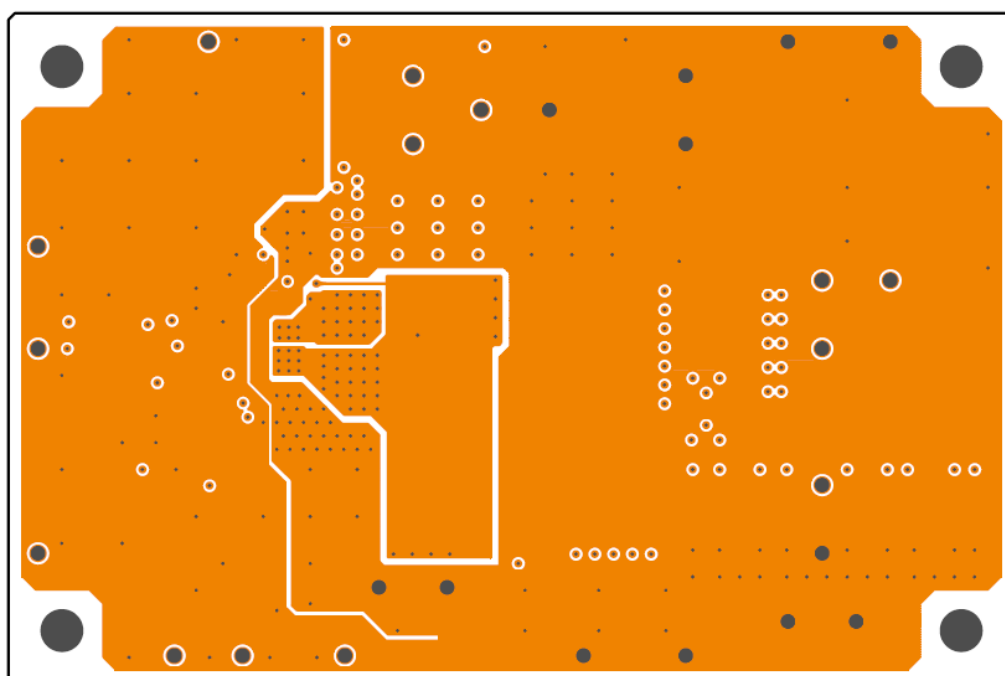
- External components must be connected as close as possible to the ICs and make wiring as short as possible. Especially, the capacitor connected in between VIN pin and GND pin must be wiring the shortest. If their impedance is high, internal voltage of the IC may shift by the switching current, and the operating may be unstable. Make the power supply and GND lines sufficient.
- Place a capacitor ( $C_{OUT}$ ) to keep a distance between  $C_{IN}$  and  $C_{OUT}$  in order to avoid the high-frequency noise by input.
- AGND and PGND must be wired to the GND line at the low impedance point of the same layer with  $C_{IN}$  and  $C_{OUT}$ .
- Place a capacitor ( $C_{BST}$ ) as close as possible to the LX pin and the BST pin. If controlling a slew rate of the high-side transistor for EMI, a resistor ( $R_{BST}$ ) should be in series between the BST pin and the capacitor ( $C_{BST}$ ).
- The NC pin must be set to "Open".
- The MODE pin requires the H / L voltages with the high stability when the forced PWM mode (MODE = "H") or the VFM mode (MODE = "L") is enabled. If the voltage with the high stability cannot be applied, connection to the VCC pin as "H" level or the AGND pin as "L" level is recommended. If connecting to the PGND pin as noisy, a malfunction may occur. Avoid the use of the MODE pin being "Open".
- If  $V_{OUT}$  is a minus potential, the setup cannot occur.

Reference PCB Layouts

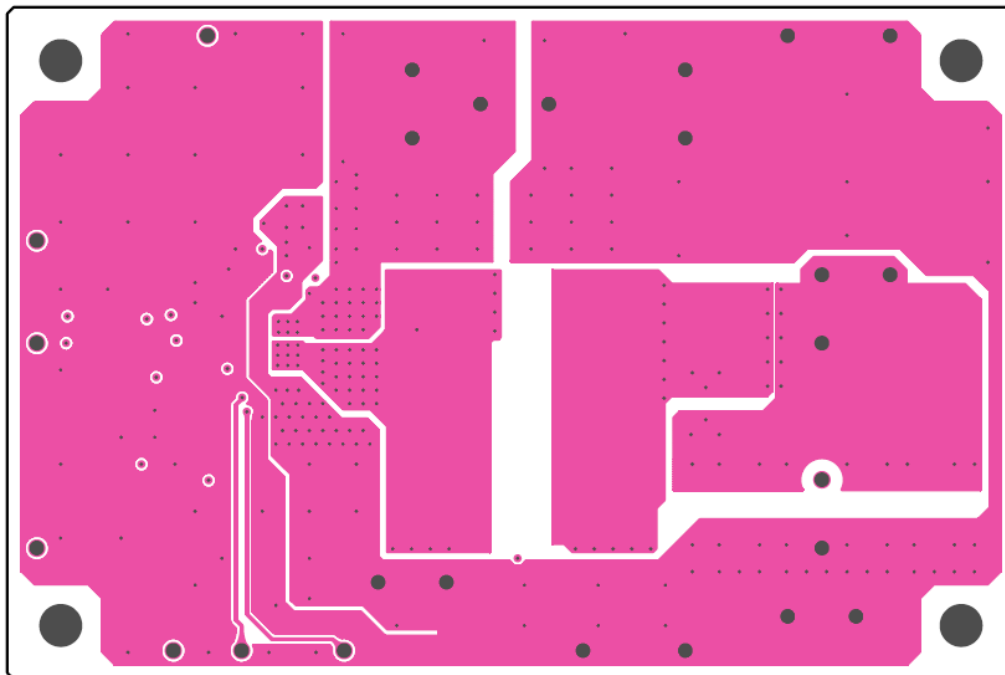
R1273LxxxA



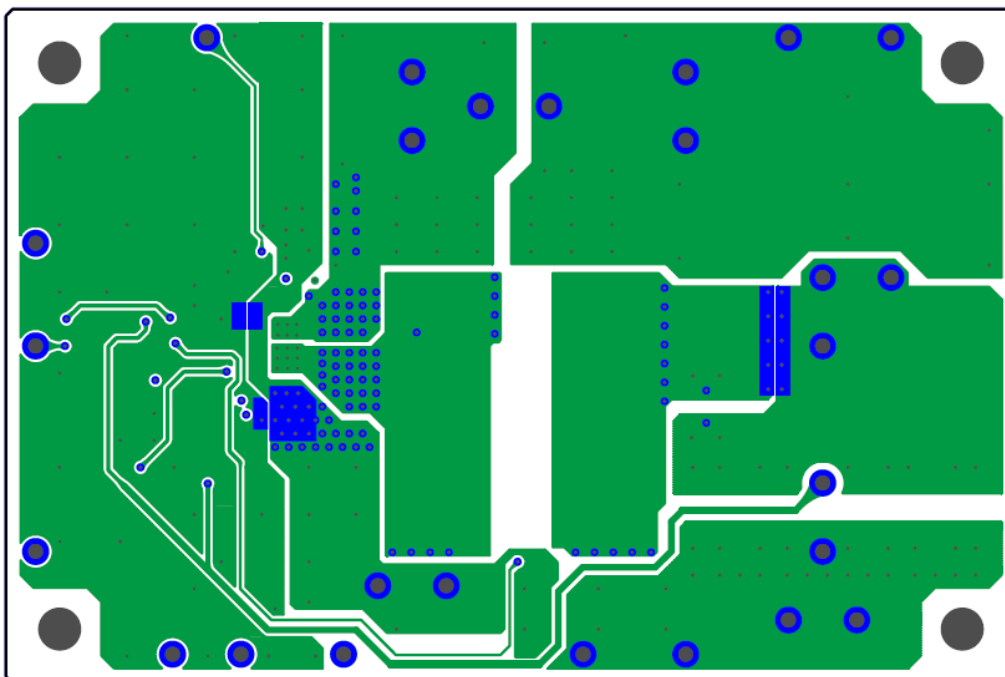
PCB Layout – 1<sup>st</sup> Layer (Top Layer)



PCB Layout – 2<sup>nd</sup> Layer



PCB Layout - 3<sup>rd</sup> Layer



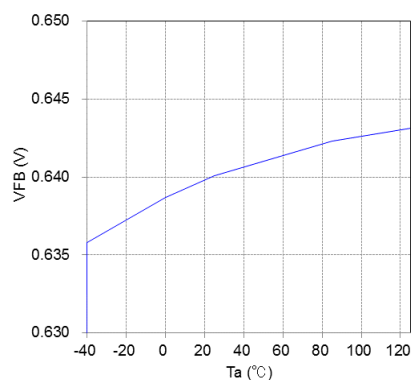
PCB Layout - 4<sup>th</sup> Layer (Bottom Layer)



## TYPICAL CHARACTERISTICS

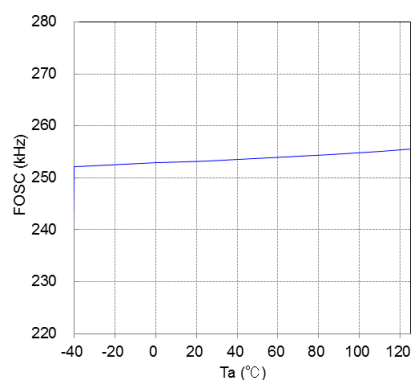
Typical Characteristics are intended to be used as reference data, they are not guaranteed.

### 1) FB Voltage vs. Temperature

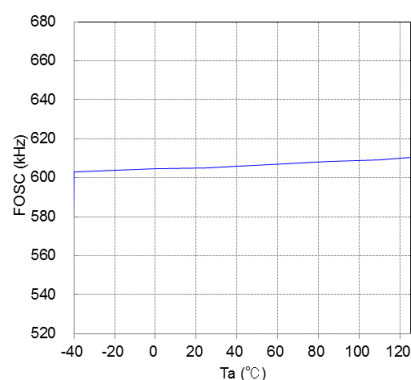


### 2) Oscillation Frequency vs. Temperature

250 kHz (RT = 135 kΩ)



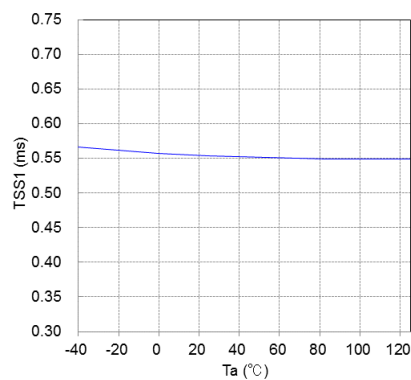
600 kHz (RT = 55 kΩ)



### 3) Soft-start time 1 vs. Temperature

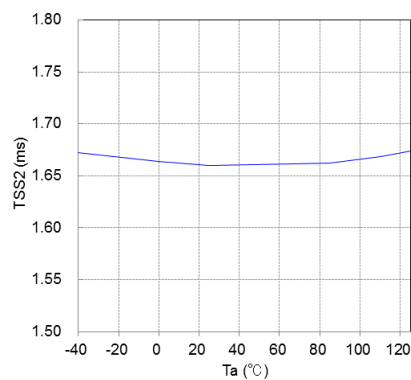
Fixed soft-start time

(C<sub>SS</sub> = Open)



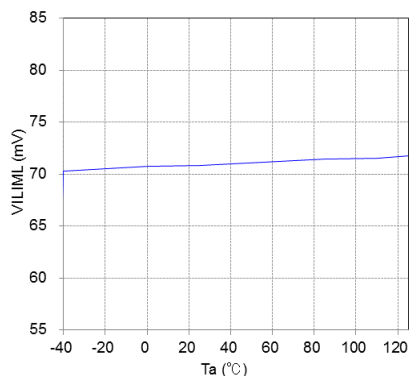
Adjustable soft-start time

(C<sub>SS</sub> = 4.7 nF)

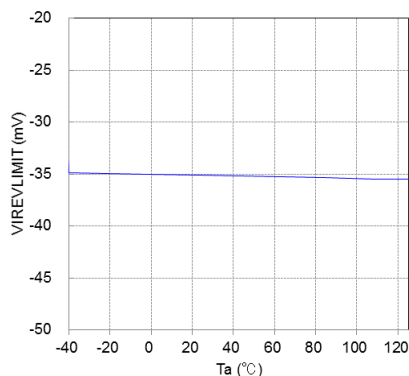


**4) Current limit threshold voltage vs. Temperature**

Current limit threshold voltage  
(R1273Lxx2x)

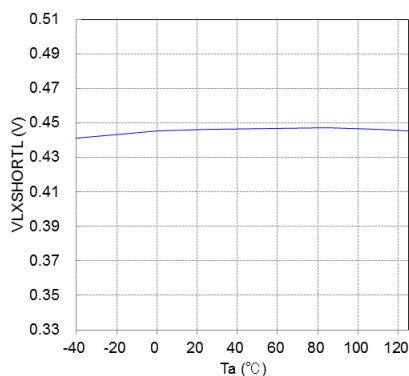


Overcurrent limit threshold voltage  
(R1273Lxx2x)

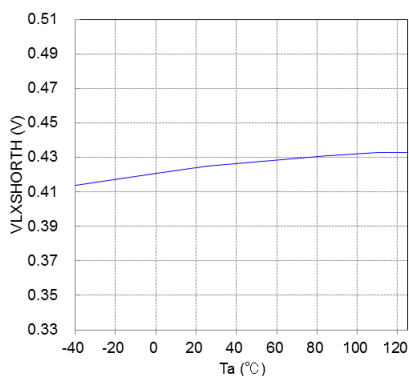


**5) LX GND/VIN short threshold voltage vs. Temperature**

LX GND short threshold voltage  
(VIN-LX)

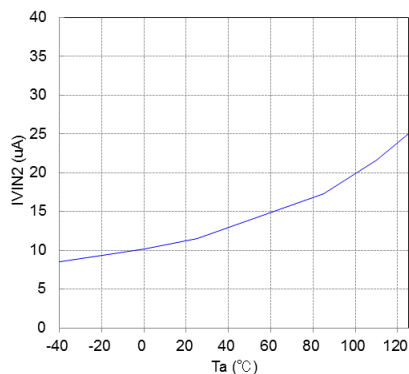


LX VIN short threshold voltage  
(LX-PGND)

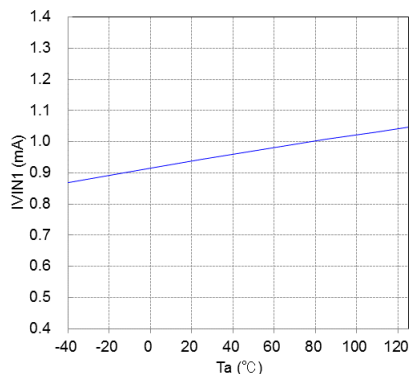


**6) Current consumption vs. Temperature**

Current consumption (VFM)  
(VIN = 12V)

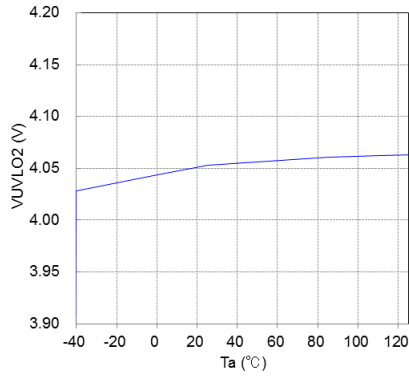


Current consumption (PWM)  
(VIN = 12V)

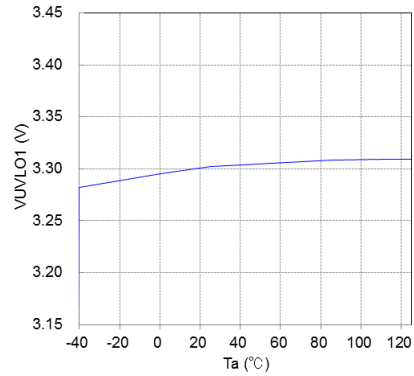


**7) UVLO vs. Temperature**

UVLO release voltage

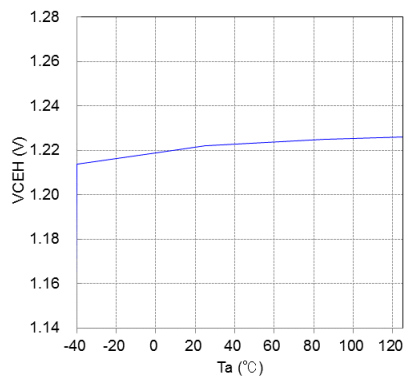


UVLO threshold voltage

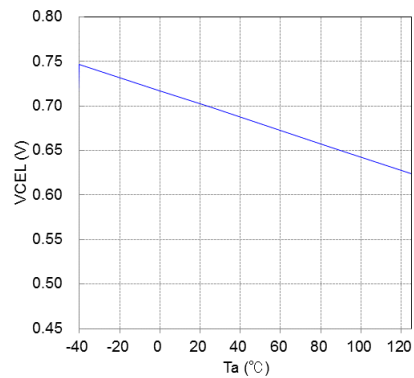


**8) CE input voltage vs. Temperature**

CE "H" input voltage

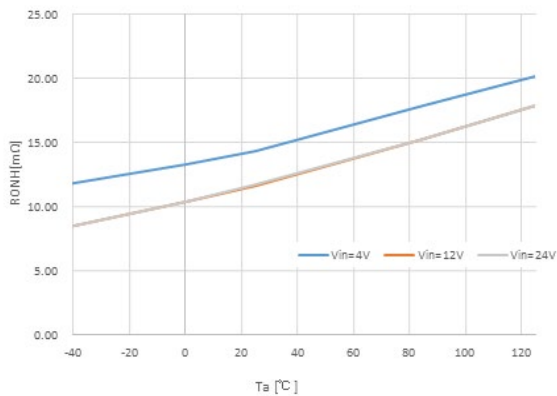


CE "L" input voltage

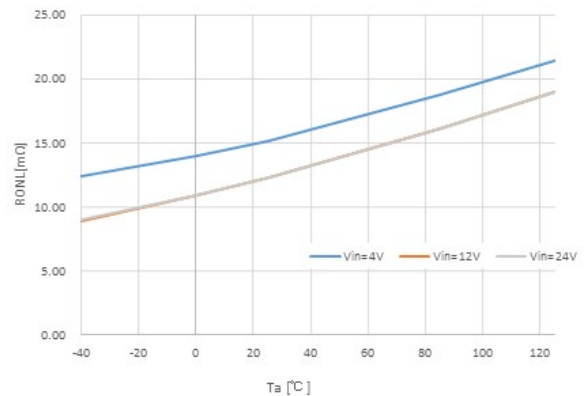


**9) Driver On-resistance**

High-side Driver On-resistance



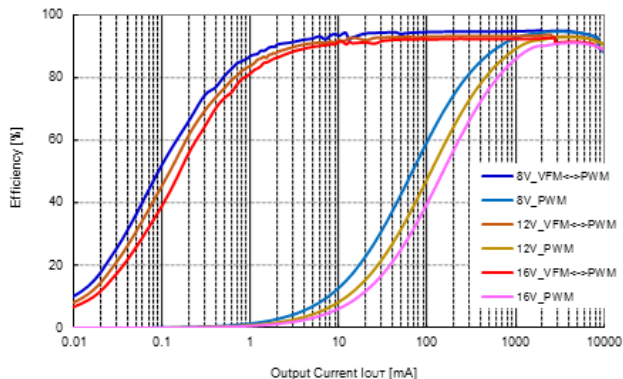
Low-side Driver On-resistance



**10) Output current vs. Efficiency**

$V_{OUT} = 3.3V$

$f_{OSC} = 500kHz / V_{IN} = 8V/12V/16V$



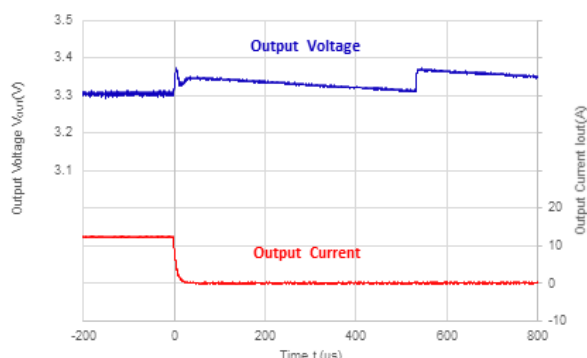
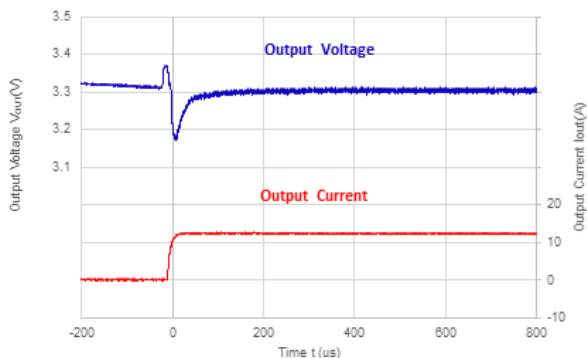
**11) Load transient response**

$V_{IN} = 12V / V_{OUT} = 3.3V$

$f_{OSC} = 500kHz / MODE = L$  VFM/PWM auto-switching

$V_{IN} = 12V / V_{OUT} = 3.3V$

$f_{OSC} = 500kHz / MODE = L$  VFM/PWM auto-switching

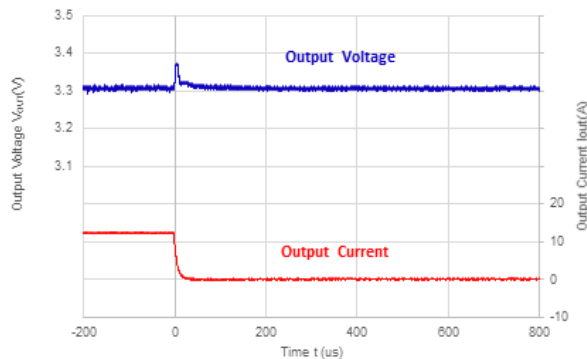
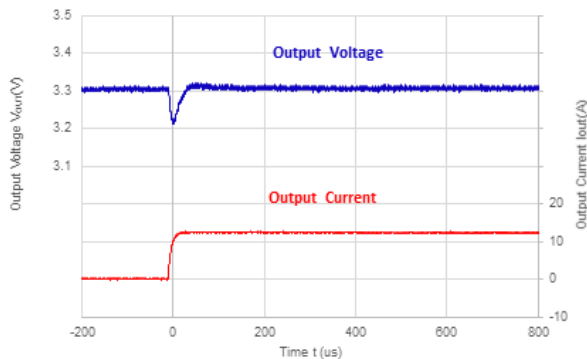


$V_{IN} = 12V / V_{OUT} = 3.3V$

$f_{OSC} = 500kHz / MODE = H$  Forced PWM

$V_{IN} = 12V / V_{OUT} = 3.3V$

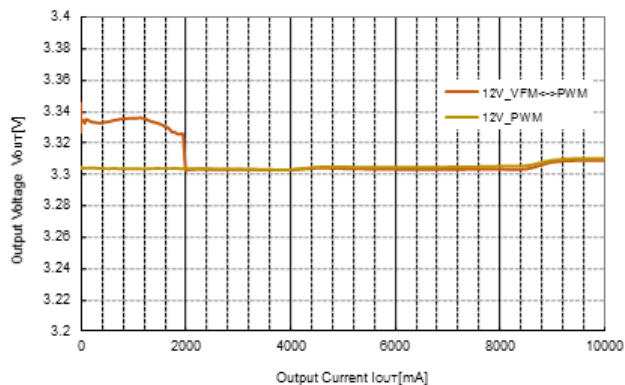
$f_{OSC} = 500kHz / MODE = H$  Forced PWM



**12) Output voltage vs. Output current**

$V_{OUT} = 3.3V$

$f_{OSC} = 500kHz / V_{IN}=12V$



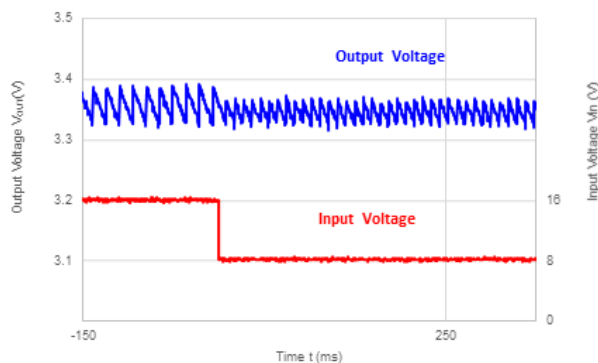
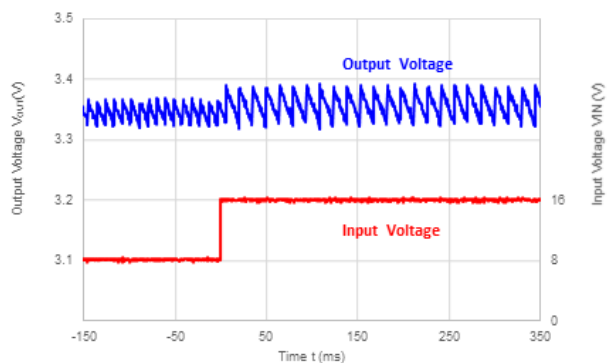
**13) Input transient response**

$V_{OUT} = 3.3V$

$f_{OSC} = 500kHz / MODE = L$  VFM/PWM auto-switching  
 $I_{OUT}=0.1A$  VFM mode

$V_{OUT} = 3.3V$

$f_{OSC} = 500kHz / MODE = L$  VFM/PWM auto-switching  
 $I_{OUT}=0.1A$  VFM mode

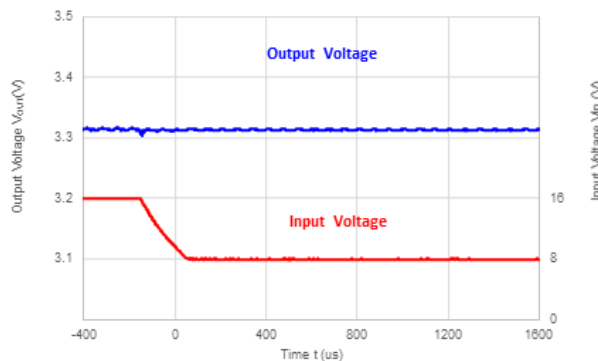
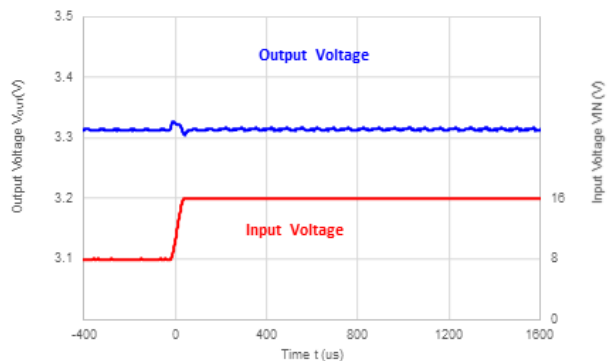


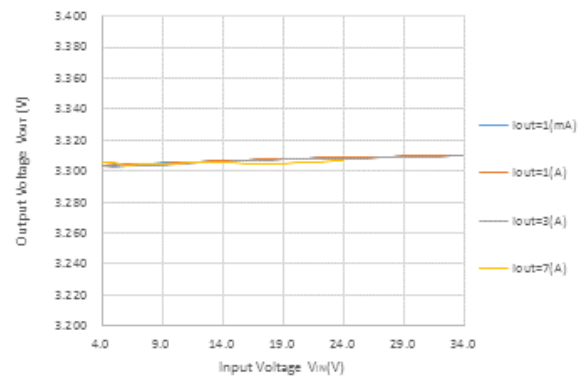
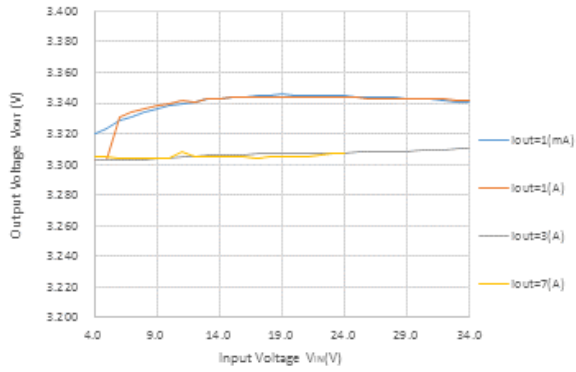
$V_{OUT} = 3.3V$

$f_{OSC} = 500kHz / MODE = H$  Forced PWM  
 $I_{OUT}=1A$  PWM mode

$V_{OUT} = 3.3V$

$f_{OSC} = 500kHz / MODE = H$  Forced PWM  
 $I_{OUT}=1A$  PWM mode



**14) Input voltage vs. Output voltage** $V_{OUT} = 3.3V$  $f_{osc} = 500kHz$  / MODE = L VFM/PWM auto-switching $V_{OUT} = 3.3V$  $f_{osc} = 500kHz$  / MODE = H Forced PWM

# POWER DISSIPATION

# QFN0505-32B

PD-QFN0505-32B-(125150)-JE-A

The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51-7.

## Measurement Conditions

Item	Measurement Conditions
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	76.2 mm × 114.3 mm × 0.8 mm
Copper Ratio	Outer Layer (First Layer and Fourth Layer): Less than 95% of 50 mm Square Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square
Through-holes	φ 0.3 mm × 6 pcs

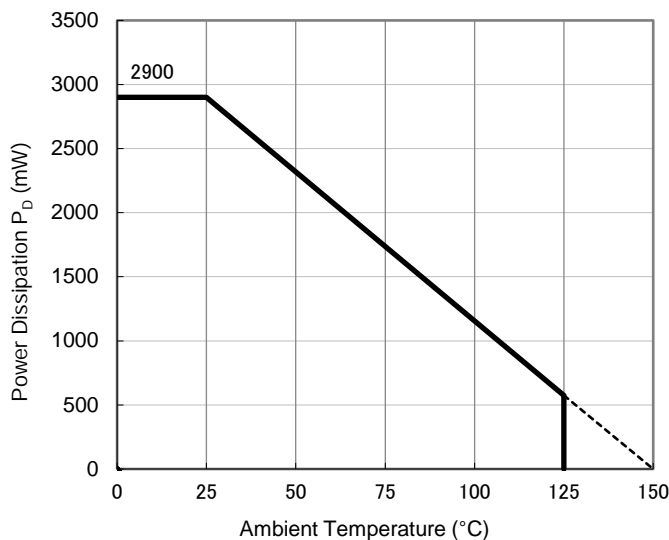
## Measurement Result

(Ta = 25°C, Tjmax = 150°C)

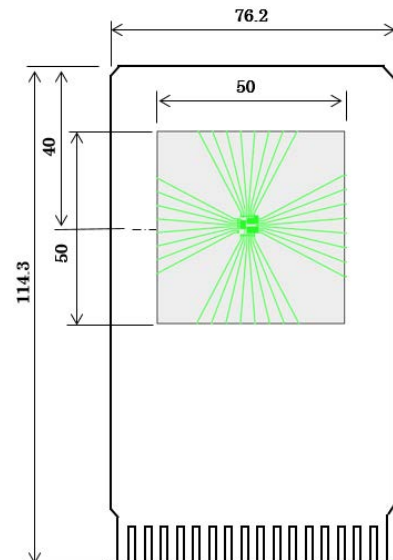
Item	Measurement Result
Power Dissipation	2900 mW
Thermal Resistance ( $\theta_{ja}$ )	$\theta_{ja} = 43^{\circ}\text{C/W}$
Thermal Characterization Parameter ( $\psi_{jt}$ )	$\psi_{jt} = 9^{\circ}\text{C/W}$

$\theta_{ja}$ : Junction-to-Ambient Thermal Resistance

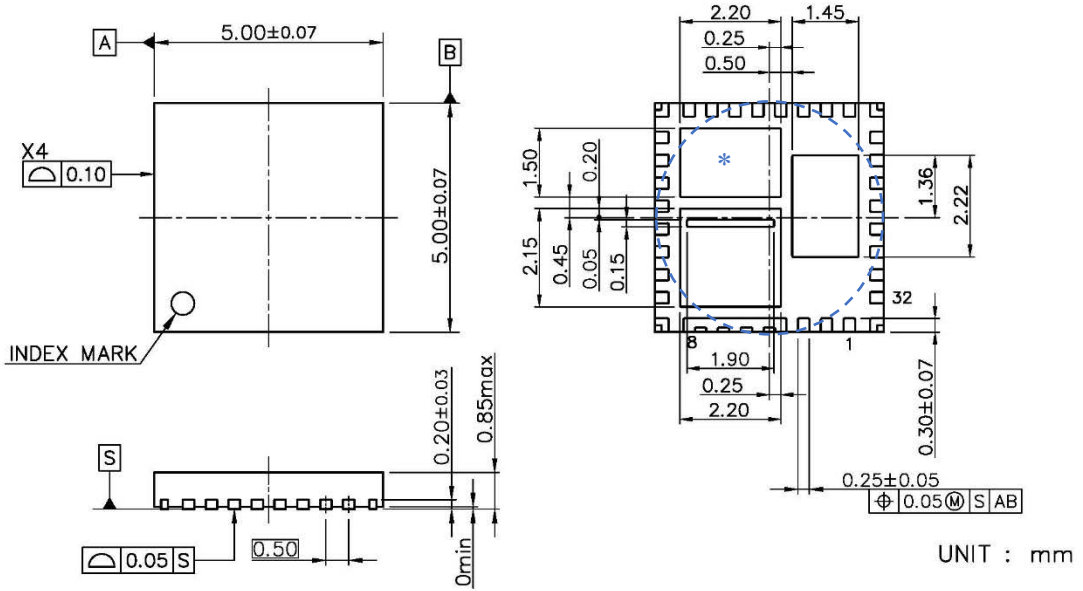
$\psi_{jt}$ : Junction-to-Top Thermal Characterization Parameter



Power Dissipation vs. Ambient Temperature



Measurement Board Pattern



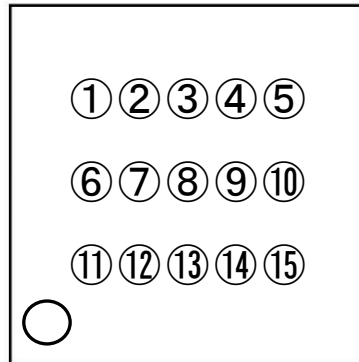
**QFN0505-32B Package Dimensions (Unit: mm)**

\* The tabs for VIN, LX, and AGND pins on the bottom of the package, shown by blue circle, should be connected to the same potential of each tab.



①②③④⑤⑥⑦⑧⑨⑩ : Product Code ... **Refer to the following table**

⑪⑫⑬⑭⑮ : Lot Number ... Alphanumeric Serial Number



**QFN0505-32B Marking Specification**

**NOTICE**

There can be variation in the marking when different AOI (Automated Optical Inspection) equipment is used. In the case of recognizing the marking characteristic with AOI, please contact our sales or our distributor before attempting to use AOI.

**R1273LxxxA Marking List**

Product Name	①②③④⑤⑥⑦⑧⑨⑩
R1273L001A	R 1 2 7 3 L 0 0 1 A
R1273L002A	R 1 2 7 3 L 0 0 2 A
R1273L003A	R 1 2 7 3 L 0 0 3 A
R1273L011A	R 1 2 7 3 L 0 1 1 A
R1273L012A	R 1 2 7 3 L 0 1 2 A
R1273L013A	R 1 2 7 3 L 0 1 3 A
R1273L031A	R 1 2 7 3 L 0 3 1 A
R1273L032A	R 1 2 7 3 L 0 3 2 A
R1273L033A	R 1 2 7 3 L 0 3 3 A

Product Name	①②③④⑤⑥⑦⑧⑨⑩
R1273L101A	R 1 2 7 3 L 1 0 1 A
R1273L102A	R 1 2 7 3 L 1 0 2 A
R1273L103A	R 1 2 7 3 L 1 0 3 A
R1273L111A	R 1 2 7 3 L 1 1 1 A
R1273L112A	R 1 2 7 3 L 1 1 2 A
R1273L113A	R 1 2 7 3 L 1 1 3 A
R1273L131A	R 1 2 7 3 L 1 3 1 A
R1273L132A	R 1 2 7 3 L 1 3 2 A
R1273L133A	R 1 2 7 3 L 1 3 3 A

This document provides a Design Failure Modes and Effects Analysis (DFMEA) for the device under the failure conditions.

● Pin Short-Circuit to Neighboring Pin

( $V_{IN} = 24\text{ V} / 34\text{ V}$ )

Pin Name	State	Comments
VIN – CSS/TRK	Startup	Startup by a set time for internal soft-start.
	PWM mode	Normal operation.
	VFM mode	
AGND – CE	Startup	Device is disabled.
	PWM mode	
	VFM mode	
CE – SENSE	Startup	Overcurrent protection in hiccup mode runs.
	PWM mode	Operation at short-circuit vary by the CE pin voltage. 1) $V_{CE} > V_{OUT} + V_{LIMIT}$ → Overcurrent protection in hiccup mode runs. 2) $V_{OUT} - V_{IREVLIMIT} \leq V_{CE} \leq V_{OUT} + V_{LIMIT}$ → Normal operation. 3) $V_{CE} < V_{OUT} - V_{IREVLIMIT}$ → The body diode for the low-side transistor can provide function such as rectifier diode.
	VFM mode	Normal operation.
VOUT – SENSE	Startup	Overcurrent and reverse-current protections become disabled.
	PWM mode	
	VFM mode	
VOUT – RT	Startup	Switching is stopped.
	PWM mode	
	VFM mode	VFM ripple value increases. After detecting the overvoltage, Device goes into PWM mode and stops switching.
RT – COMP	Startup	Switching is stopped after detecting an opened RT.
	PWM mode	
	VFM mode	VFM ripple is varied.
COMP – VFB	Startup	Switching is stopped.
	PWM mode	
	VFM mode	
VFB – CLKOUT	Startup	Switching is stopped.
	PWM mode	
	VFM mode	

## ● Pin Short-Circuit to Neighboring Pin (Continued)

(V<sub>IN</sub> = 24 V / 34 V)

Pin Name	State	Comments
PGOOD – MODE	Startup	PGOOD pin outputs an improper value under the influence of MODE pin.
	PWM mode	
	VFM mode	
MODE – AGND	Startup	Device goes into the VFM / PWM auto-switching mode.
	PWM mode	
	VFM mode	
AGND – PGND	Startup	Normal operation.
	PWM mode	
	VFM mode	

## ● Pin Left Open

(V<sub>IN</sub> = 24 V / 34 V)

Pin Name	State	Comments
VIN	Startup	VIN pin is biased to VIN via the diode of CE pin.
	PWM mode	
	VFM mode	
CSS / TRK	Startup	Device starts by internal soft-start function.
	PWM mode	Normal operation.
	VFM mode	
AGND	Startup	Device operates under AGND = PGND ± 2V <sub>f</sub> by a pair of back-to-back diodes connected with PGND.
	PWM mode	
	VFM mode	
CE	Startup	When CE pin is “Low”, CE pin is stored as “Low”. Once CE pin becomes “High” by noise, CE pin is stored as “High”.
	PWM mode	Normal operation. CE pin is stored as “High”.
	VFM mode	
SENSE	Startup	Overcurrent and reverse-current protections become enabled.
	PWM mode	
	VFM mode	Normal operation.
VOUT	Startup	By switching, overcurrent protection in hiccup mode runs.
	PWM mode	
	VFM mode	VFM mode is shifted to PWM mode. Device runs in PWM mode.

## ● Pin Left Open (Continued)

(V<sub>IN</sub> = 24 V / 34 V)

Pin Name	State	Comments
RT	Startup	Device detects abnormal frequency and stops switching.
	PWM mode	
	VFM mode	After detecting the overvoltage, Device goes into PWM mode and runs it.
COMP	Startup	It becomes a cause of abnormal switching, but not causing an overvoltage.
	PWM mode	
	VFM mode	Normal operation.
VFB	Startup	Switching is stopped by internal pull-up resistor.
	PWM mode	
	VFM mode	
VCC	Startup	A noise of VCC pin voltage rises. But the switching runs.
	PWM mode	
	VFM mode	
BST	Startup	A lack of voltage driven the high-side transistor causes unstable output voltage, even if the high-side transistor is turned ON.
	PWM mode	
	VFM mode	
LX	Startup	Once the high-side transistor is turned ON, it will never be turned OFF, and overvoltage and overcurrent would be caused.
	PWM mode	
	VFM mode	
PGND	Startup	Device operates under PGND = AGND ± 2Vf by a pair of back-to-back diodes connected with PGND.
	PWM mode	
	VFM mode	
MODE	Startup	Device operates in the VFM / PWM auto-switching mode.
	PWM mode	
	VFM mode	
PGOOD	Startup	Normal operation.
	PWM mode	
	VFM mode	
CLKOUT	Startup	Normal operation.
	PWM mode	
	VFM mode	

● VOUT/LX Pins Short-Circuit to Supply Voltage / GND (V<sub>IN</sub> = 24 V / 34 V)

Pin Name	State		Comments
VOUT	Short-circuit to GND	Startup	Current is limited by overcurrent protection, and device goes into the hiccup mode.
		PWM mode	
		VFM mode	Device's operation goes from VFM mode to PWM mode, and Device runs the PWM mode.
	Short-circuit to Supply Voltage (VIN)	Startup	When V <sub>OUT</sub> exceed V <sub>FBOVD</sub> , High- / Low-side transistors stop. V <sub>IN</sub> becomes equal to V <sub>OUT</sub> finally. But, device will not be damaged by clamped voltage.
		PWM mode	
		VFM mode	After detecting the overvoltage, device's operation goes from VFM mode to PWM mode, and runs the PWM mode.
LX	Short-circuit to GND	Startup	After detecting the LX pin shorted to GND, the high-side transistor becomes OFF. Then, device goes into the hiccup mode by detecting the undervoltage.
		PWM mode	
		VFM mode	Device's operation goes from VFM mode to PWM mode, and device runs the PWM mode.
	Short-circuit to Supply Voltage (VIN)	Startup	When V <sub>OUT</sub> exceed V <sub>FBOVD</sub> , High- / Low-side transistors stop. But, device will not be damaged by clamped voltage.
		PWM mode	
		VFM mode	After detecting the overvoltage, device's operation goes from VFM mode to PWM mode, and runs the PWM mode.

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  - Various Safety Devices
  - Traffic control system
  - Combustion equipment

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