

#### **General Description**

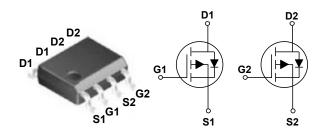
These P-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

BV <sub>DSS</sub>	R <sub>DS(ON)</sub>	Ι <sub>D</sub>
-30 V	16 mΩ	-10 A

#### **Features**

- -30V, -10A,  $R_{DS(ON)} \le 16m\Omega@V_{GS} = -10V$
- · Fast switching
- Green Device Available
- Suit for -4.5V Gate Drive Applications

### SOP-8 Pin Configuration



### **Applications**

- · MB / VGA / Vcore
- LED Application
- · Load Switch
- POL Applications

osolute Maximum Ratings T <sub>C</sub> =25°C unless otherwise noted						
Symbol	Parameter	Rating	Units			
V <sub>DS</sub>	Drain-Source Voltage	-30	V			
$V_{GS}$	Gate-Source Voltage (base on I <sub>GSS1</sub> condition)	±20	V			
$V_{GS}$	Gate-Source Voltage (base on I <sub>GSS2</sub> condition)	±25	V			
1	Drain Current - Continuous (T <sub>C</sub> =25°C)	-10	Α			
I <sub>D</sub>	Drain Current - Continuous (T <sub>C</sub> =100°C)	-6.3	A			
I <sub>DM</sub>	Drain Current - Pulsed (NOTE 1)	-40	Α			
$P_{D}$	Power Dissipation (T <sub>C</sub> =25°C)	2.1	W			
гЪ	Power Dissipation - Derate above 25°C	0.017	W/°C			
T <sub>J</sub>	Operating Junction Temperature Range	-50 to 150	°C			
T <sub>STG</sub>	Storage Temperature Range	-50 to 150	°C			
Marking Code		PC016A, DS3805				

Thermal Characteristics				
Symbol	Parameter	Тур.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction to Ambient		60	°C/W





### Electrical Characteristics (T<sub>J</sub>=25°C, unless otherwise noted)

#### **Off Characteristics**

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS}$ = 0V , $I_D$ = -250uA	-30			V
1	IDrain-Source Leakage Current	$V_{DS}$ = -30V , $V_{GS}$ = 0V , $T_{J}$ =25°C			-1	uA
I <sub>DSS</sub>		$V_{DS}$ = -24V , $V_{GS}$ = 0V , $T_{J}$ =125°C			-10	uA
I <sub>GSS1</sub>	Gate-Source Leakage Current	$V_{GS}$ = ±20V , $V_{DS}$ = 0V			±100	nA
$I_{GSS2}$	Gate-Source Leakage Current	$V_{GS}$ = ±25V , $V_{DS}$ = 0V			±1	mA

#### **On Characteristics**

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
R <sub>DS(ON)</sub>	IStatic Drain-Source On-Resistance	$V_{GS}$ = -10V , $I_D$ = -8A		12	16	- mΩ
		$V_{GS}$ = -4.5V , $I_D$ = -6A		18	26	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = -250 uA$	-1.2	-1.6	-2.5	V
gfs	Forward Transconductance	$V_{DS}$ = -10V , $I_{D}$ = -8A		10.5		S

#### **Dynamic and switching Characteristics**

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
$Q_g$	Total Gate Charge	V <sub>DS</sub> = -15V , V <sub>GS</sub> = -4.5V ,		14.6	21	
$Q_{gs}$	Gate-Source Charge	I <sub>D</sub> = -8A		4.1	6	nC
$Q_{gd}$	Gate-Drain Charge	(NOTE 2 \ 3)		6.3	9	
$T_{d(on)}$	Turn-On Delay Time	45)/		9	17	
$T_r$	Rise Time	$V_{DD}$ = -15V , $V_{GS}$ = -10V , $R_{G}$ =6 $\Omega$ , $I_{D}$ = -1A		21.8	41	nS
$T_{d(off)}$	Turn-Off Delay Time			59.8	114	113
T <sub>f</sub>	Fall Time	(10122 0)		14.4	27	
C <sub>iss</sub>	Input Capacitance			1730	2510	
C <sub>oss</sub>	Output Capacitance	$V_{DS}$ = -15V , $V_{GS}$ = 0V , F= 1MHz		180	260	pF
C <sub>rss</sub>	Reverse Transfer Capacitance			125	180	

#### **Drain-Source Diode Characteristics and Ratings**

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
Is	Continuous Source Current	V <sub>G</sub> = V <sub>D</sub> = 0V,Force Current			-7	Α
I <sub>SM</sub>	Pulsed Source Current		-		-14	Α
$V_{SD}$	Diode Forward Voltage	$V_{GS}$ = 0V , $I_{S}$ = -1A , $T_{J}$ = 25 $^{\circ}$ C			-1	V

#### NOTES:

- 1. Repetitive Rating: Pulsed width limited by maximum junction temperature.
- 2. The data tested by pulsed , pulse width  $\leq$  300us , duty cycle  $\leq$  2%.
- 3. Essentially independent of operating temperature.





#### **Characteristics Curves**

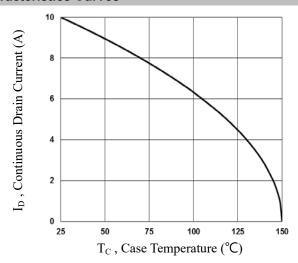


Fig.1 Continuous Drain Current vs. Tc

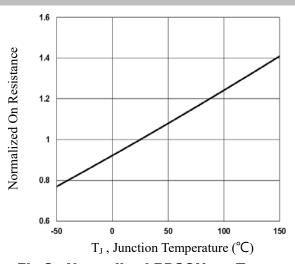


Fig.2 Normalized RDSON vs. T,

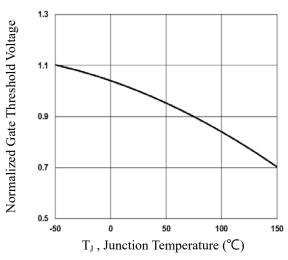


Fig.3 Normalized  $V_{th}$  vs.  $T_J$ 

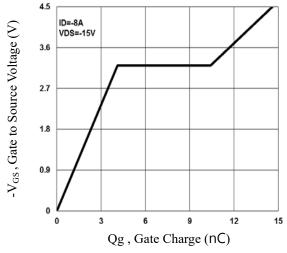


Fig.4 Gate Charge Waveform

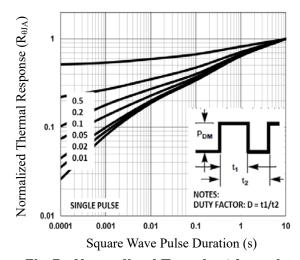


Fig.5 Normalized Transient Impedance

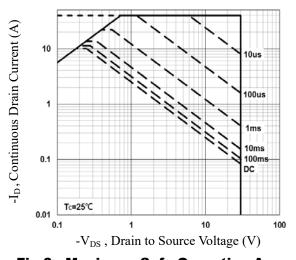
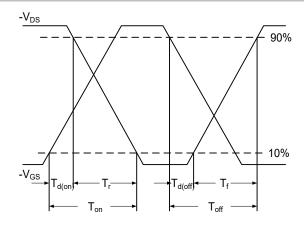


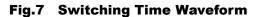
Fig.6 Maximum Safe Operation Area





#### **Characteristics Curves**





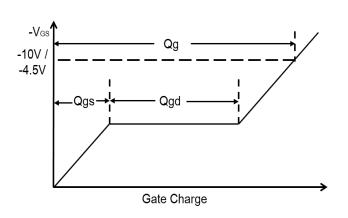
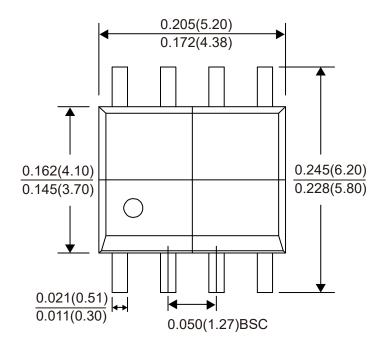
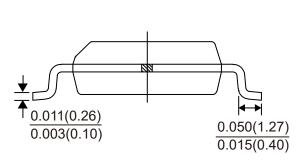
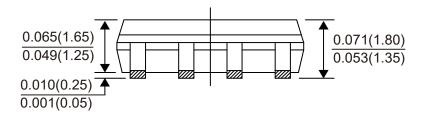


Fig.8 Gate Charge Waveform

### **Package Outline Dimensions**







**SOP-8**Dimensions in inches and (millimeters)





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