



# 30V Dual N-Channel MOSFETs

## General Description

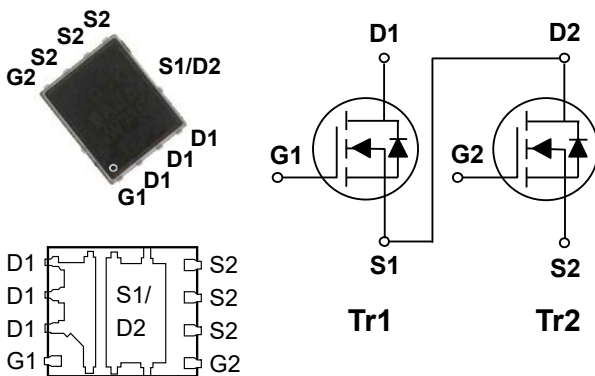
These N-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

$BV_{DSS}$	$R_{DS(ON)}$	$I_D$
30 V	9 mΩ	30 A

## Features

- Improved dv/dt capability
- Fast switching
- Green Device Available

PPAK5x6 Asymmetric Dual Pin Configuration



## Applications

- MB / VGA / Vcore
- POL Applications
- SMPS 2<sup>nd</sup> SR

## Absolute Maximum Ratings $T_C=25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	30	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D$	Drain Current - Continuous ( $T_C=25^\circ\text{C}$ )	30	A
	Drain Current - Continuous ( $T_C=100^\circ\text{C}$ )	18.9	A
$I_{DM}$	Drain Current - Pulsed (NOTE 1)	120	A
EAS	Single Pulse Avalanche Energy (NOTE 2)	31	mJ
IAS	Single Pulse Avalanched Current (NOTE 2)	25	A
$P_D$	Power Dissipation ( $T_C=25^\circ\text{C}$ )	33.5	W
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
Marking Code		NC9P0	

## Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction to Ambient	---	62	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance Junction to Case	---	3.73	$^\circ\text{C/W}$



## 30V Dual N-Channel MOSFETs

Electrical Characteristics ( $T_J=25^\circ\text{C}$ , unless otherwise noted)

## Off Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	30	---	---	V
$I_{DSS}$	Drain-Source Leakage Current	$V_{DS}=24V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	1	$\mu A$
$I_{GSS}$	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	$\pm 100$	nA

## On Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=10V, I_D=15A$	---	---	9	m $\Omega$
		$V_{GS}=4.5V, I_D=8A$	---	---	12	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\mu A$	1.2	1.6	2.5	V
gfs	Forward Transconductance	$V_{DS}=10V, I_D=8A$	---	5.6	---	S

## Dynamic and switching Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$Q_g$	Total Gate Charge	$V_{DS}=15V, V_{GS}=10V, I_D=1A$	---	23.2	---	nC
$Q_{gs}$	Gate-Source Charge		---	3.2	---	
$Q_{gd}$	Gate-Drain Charge		---	3.7	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=10V, V_{GS}=10V, R_{GEN}=2.7\Omega, I_D=30A$	---	7	---	nS
$T_r$	Rise Time		---	76.6	---	
$T_{d(off)}$	Turn-Off Delay Time		---	27.1	---	
$T_f$	Fall Time		---	52.6	---	
$C_{iss}$	Input Capacitance	$V_{DS}=15V, V_{GS}=0V, F=1\text{MHz}$	---	1180	---	pF
$C_{oss}$	Output Capacitance		---	177	---	
$C_{rss}$	Reverse Transfer Capacitance		---	132	---	
$R_g$	Gate Resistance	$V_{GS}=0V, V_{DS}=0V, F=1\text{MHz}$	---	3.2	---	$\Omega$

## Drain-Source Diode Characteristics and Ratings

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$I_S$	Continuous Source Current	$V_G=V_D=0V, \text{Force Current}$	---	---	30	A
$I_{SM}$	Pulsed Source Current		---	---	60	A
$V_{SD}$	Diode Forward Voltage	$V_{GS}=0V, I_S=1A, T_J=25^\circ\text{C}$	---	---	1	V

## NOTES :

1. Repetitive Rating : Pulsed width limited by maximum junction temperature.
2.  $V_{DD}=25V, V_{GS}=10V, L=0.1\text{mH}, I_{AS}=25A, R_G=25\Omega, \text{Starting } T_J=25^\circ\text{C}$ .
3. The data tested by pulsed , pulse width  $\leq 300\mu s$  , duty cycle  $\leq 2\%$ .
4. Essentially independent of operating temperature.
5. It is the same characteristics for Tr1 and Tr2.



Characteristics Curves

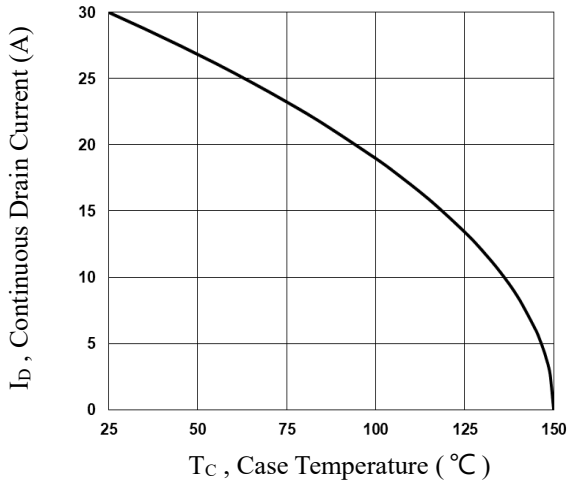


Fig.1 Continuous Drain Current vs.  $T_C$

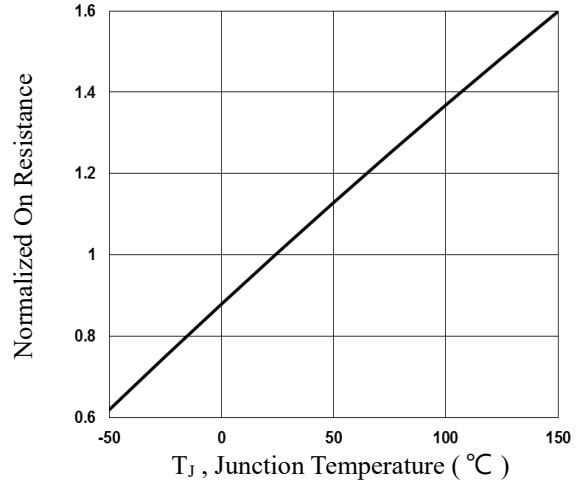


Fig.2 Normalized  $R_{DS(on)}$  vs.  $T_J$

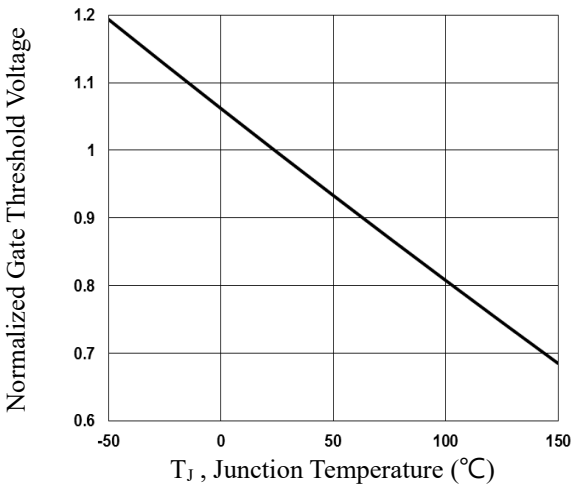


Fig.3 Normalized  $V_{th}$  vs.  $T_J$

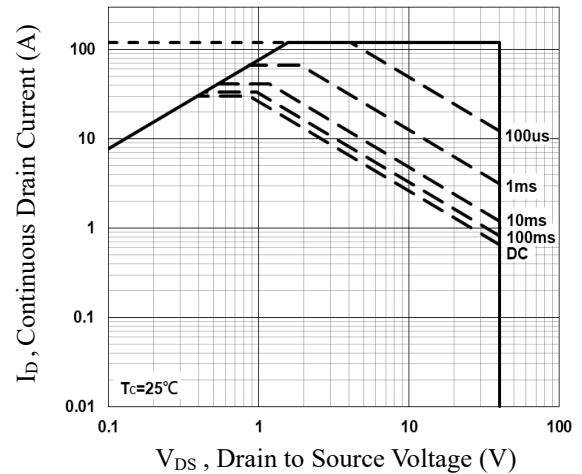


Fig.4 Maximum Safe Operation Area

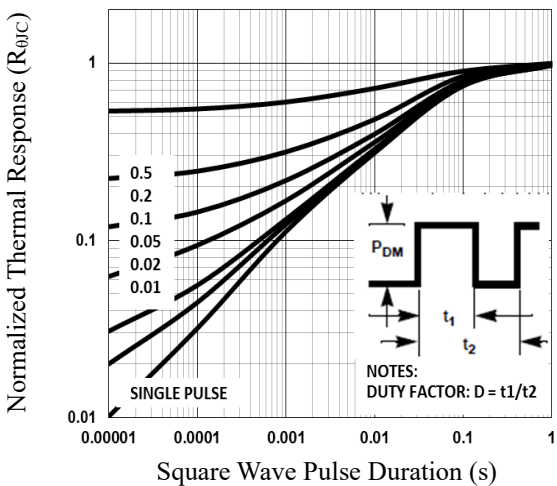


Fig.5 Normalized Transient Impedance

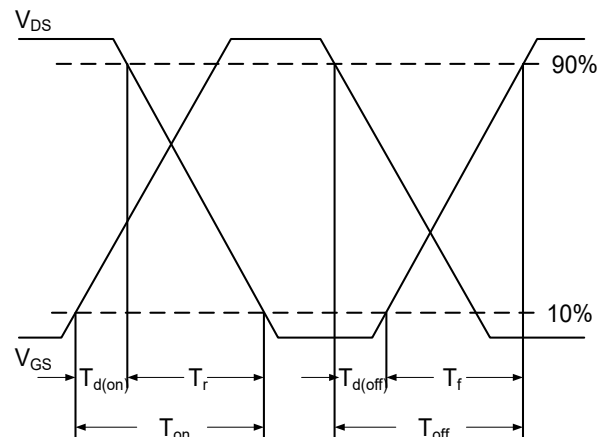


Fig.6 Switching Time Waveform



### Characteristics Curves

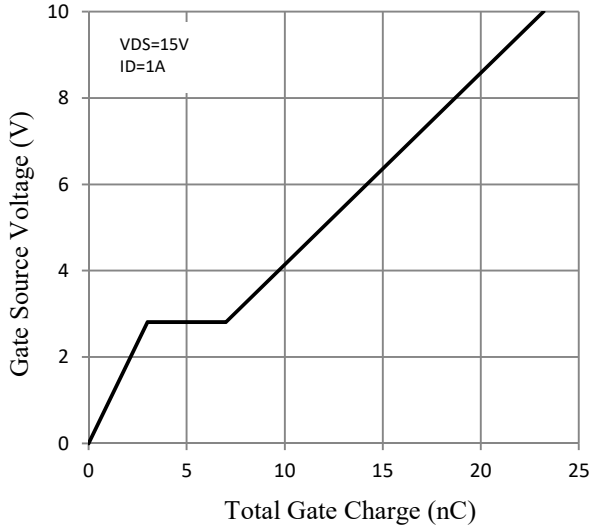
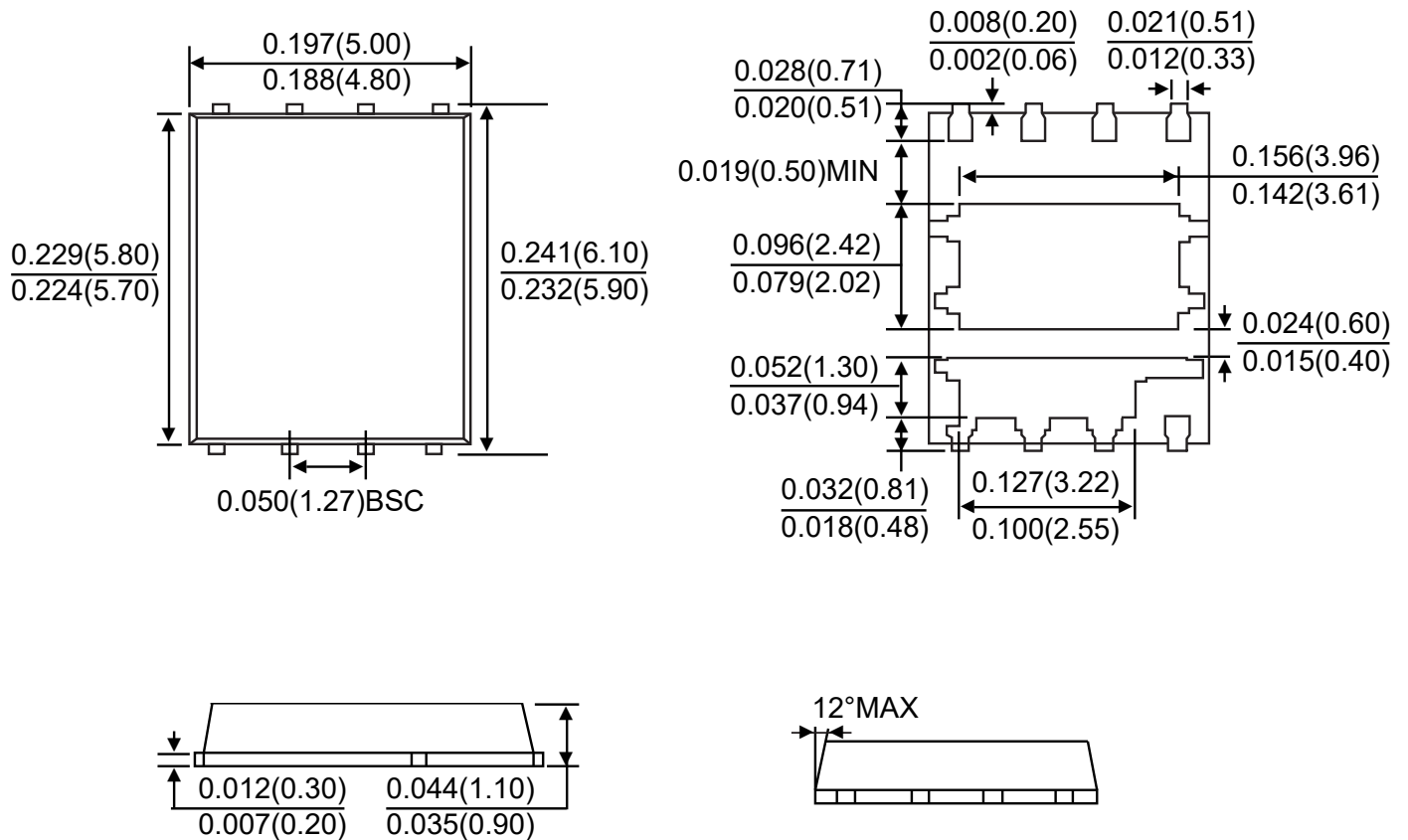


FIG. 7 Gate Charge Characteristics

### Package Outline Dimensions



### PPAK5x6 Asymmetric Dual

Dimensions in inches and (millimeters)



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