



### **General Description**

These P-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

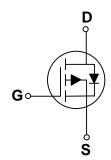
BV <sub>DSS</sub>	R <sub>DS(ON)</sub>	$I_D$
-20 V	2.3 mΩ	-90 A

#### **Features**

- $R_{DS(ON)} \leq 2.3 m\Omega@V_{GS}$ = -10V
- · Fast switching
- · Green Device Available
- · Improved dv/dt capability

### PPAK5X6 Pin Configuration





## **Applications**

- Notebook
- Networking
- · Hand-Held Instruments
- · Load Switch

Absolute Maximum Ratings T <sub>C</sub> =25°C unless otherwise noted							
Symbol	Rating	Units					
$V_{DS}$	Drain-Source Voltage	-20	V				
$V_{GS}$	Gate-Source Voltage	±12	V				
I-	Drain Current - Continuous (T <sub>C</sub> =25°C)	-90	Α				
I <sub>D</sub>	Drain Current - Continuous (T <sub>C</sub> =100°C)	-54	Α				
I <sub>DM</sub>	Drain Current - Pulsed (NOTE 1)	-360	Α				
$P_{D}$	Power Dissipation (T <sub>C</sub> =25°C)	41.67	W				
ı D	Power Dissipation - Derate above 25°C	0.33	W/°C				
$T_J$	Operating Junction Temperature Range	-55 to 150	°C				
T <sub>STG</sub>	Storage Temperature Range	-55 to 150	°C				
Marking Code		PB2P3					

Thermal Characteristics					
Symbol	nbol Parameter Typ.				
$R_{\theta JA}$	Thermal Resistance Junction to Ambient		62	°C/W	
$R_{ heta JC}$	R <sub>eJC</sub> Thermal Resistance Junction to Case		3	°C/W	





## Electrical Characteristics (T<sub>J</sub>=25°C, unless otherwise noted)

#### **Off Characteristics**

	Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
	$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}$ =0V , $I_D$ = -250uA	-20			V
1	Drain-Source Leakage Current	$V_{DS}$ = -20V , $V_{GS}$ =0V , $T_J$ =25 $^{\circ}$ C			-1	uA	
	I <sub>DSS</sub>	Diain-Source Leakage Current	$V_{DS}$ = -16V , $V_{GS}$ =0V , $T_{J}$ =125°C			-30	uA
I	$I_{GSS}$	Gate-Source Leakage Current	$V_{GS}$ = ±12V , $V_{DS}$ =0V			±500	nA

#### On Characteristics

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
	Static Drain-Source On-Resistance	$V_{GS}$ = -10V , $I_D$ = -20A		1.8	2.3	
R <sub>DS(ON)</sub>		$V_{GS}$ = -4.5V , $I_{D}$ = -20A		2.1	2.6	mΩ
		$V_{GS}$ = -2.5V , $I_{D}$ = -20A		2.7	3.6	
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{GS}=V_{DS}$ , $I_D=-250uA$	-0.4	-0.6	-1.0	V
gfs	Forward Transconductance	$V_{DS}$ = -10V , $I_{S}$ = -3A		30		S

#### **Dynamic and switching Characteristics**

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
$Q_g$	Total Gate Charge	V = 46V V = 4.5V		149	225	
$Q_{gs}$	Gate-Source Charge	V <sub>DS</sub> = -16V , V <sub>GS</sub> = -4.5V , I <sub>D</sub> = -5A (NOTE 2 \ 3)		14.4	22	nC
$Q_{gd}$	Gate-Drain Charge	1B- 3/(1/372 2 3)		42.8	65	
$T_{d(on)}$	Turn-On Delay Time			21.2	42	
T <sub>r</sub>	Rise Time	$V_{DD}$ = -15V , $V_{GS}$ = -4.5V , $R_{G}$ = 25 $\Omega$ , $I_{D}$ = -1A		20.6	40	nS
$T_{d(off)}$	Turn-Off Delay Time	(NOTE 2 \ 3)		26	52	110
$T_f$	Fall Time			400	600	
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = -15V , V <sub>GS</sub> = 0V , F= 1MHz		14000	21000	
C <sub>oss</sub>	Output Capacitance			1670	2500	pF
C <sub>rss</sub>	Reverse Transfer Capacitance			730	1100	
Rg	Gate resistance	$V_{GS}$ = 0V , $V_{DS}$ = 0V , F=1MHz		2.6		Ω

### **Drain-Source Diode Characteristics and Ratings**

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
Is	Continuous Source Current	$V_G = V_D = 0V$ , Force Current			-90	Α
I <sub>SM</sub>	Pulsed Source Current				-180	Α
$V_{SD}$	Diode Forward Voltage	V <sub>GS</sub> = 0V , I <sub>S</sub> = -1A , T <sub>J</sub> =25°C			-1	V

#### NOTES:

- 1. Repetitive Rating: Pulsed width limited by maximum junction temperature.
- 2. The data tested by pulsed , pulse width  $\leq$  300us , duty cycle  $\leq$  2%.
- 3. Essentially independent of operating temperature.





#### **Characteristics Curves**

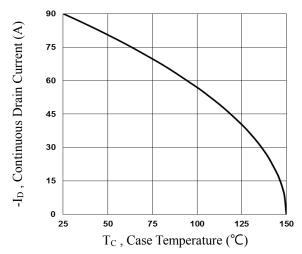


Fig.1 Continuous Drain Current vs.  $T_c$ 

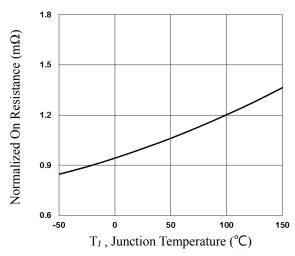


Fig.2 Normalized RDSON vs. TJ

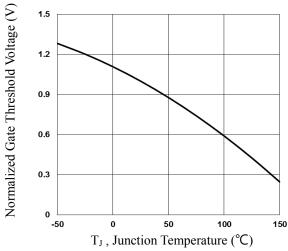


Fig.3 Normalized V<sub>th</sub> vs. T<sub>J</sub>

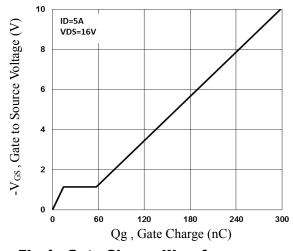


Fig.4 Gate Charge Waveform

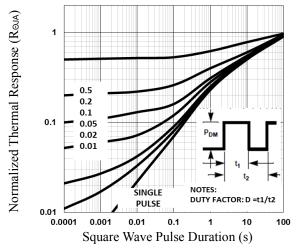


Fig.5 Normalized Transient Response

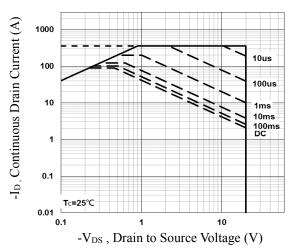
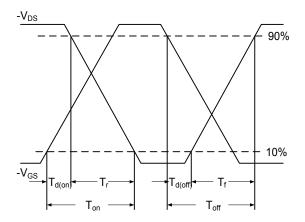


Fig.6 Maximum Safe Operation Area





#### **Characteristics Curves**





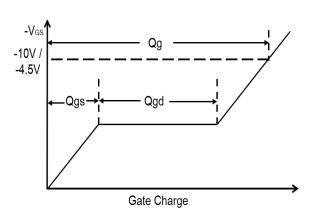
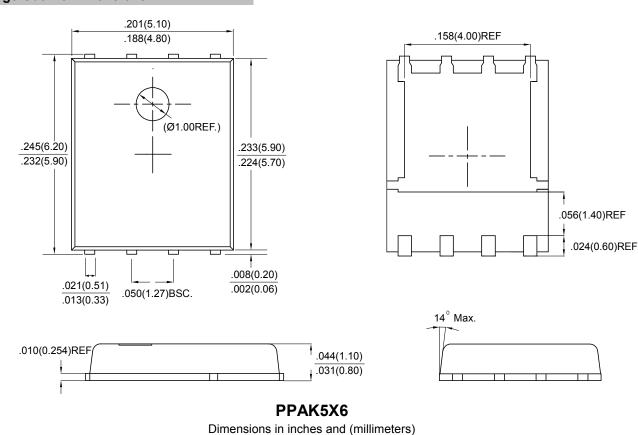


Fig.8 Gate Charge Waveform

### **Package Outline Dimensions**







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