



# P3MNM9P8



## 100V N-Channel MOSFETs

### General Description

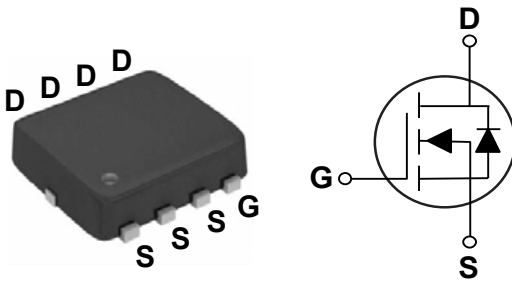
These N-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

$BV_{DSS}$	$R_{DS(ON)}$	$I_D$
100 V	9.8 m $\Omega$	48 A

### Features

- $R_{DS(ON)} \leq 9.8m\Omega @ V_{GS}=10V$
- Improved dv/dt Capability
- Fast Switching
- Green Device Available

PPAK3X3 Pin Configuration



### Applications

- Networking
- Load Switch
- LED applications

### Absolute Maximum Ratings $T_C=25^\circ C$ unless otherwise noted

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	100	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D$	Drain Current - Continuous ( $T_C=25^\circ C$ )	48	A
	Drain Current - Continuous ( $T_C=100^\circ C$ )	30	A
$I_{DM}$	Drain Current - Pulsed (NOTE 1)	88	A
EAS	Single Pulse Avalanche Energy (L=0.1mH)	36	mJ
IAS	Single Pulse Avalanche Current (L=0.1mH)	27	A
$P_D$	Power Dissipation ( $T_C=25^\circ C$ )	26.3	W
$T_J$	Operating Junction Temperature Range	-50 to 150	$^\circ C$
$T_{STG}$	Storage Temperature Range	-50 to 150	$^\circ C$
Marking Code		NM9P8	

### Thermal Characteristics

Symbol	Parameter	Rating	Unit
$R_{\theta JC}$	Thermal Resistance Junction to Case	4.75	$^\circ C/W$

**Electrical Characteristics (T<sub>j</sub>=25°C, unless otherwise noted)****Off Characteristics**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	100	---	---	V
I <sub>DSS</sub>	Drain-Source Leakage Current	V <sub>DS</sub> =80V, V <sub>GS</sub> =0V	---	---	1	uA
I <sub>GSS</sub>	Gate-Source Leakage Current	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	---	---	±100	nA

**On Characteristics**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =15A	---	---	9.8	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =10A	---	---	14	
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =250uA	1.0	---	3.0	V
g <sub>fs</sub>	Forward Transconductance	V <sub>DS</sub> =10V, I <sub>D</sub> =5A	---	22.3	---	S

**Dynamic and switching Characteristics (NOTE 3)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =50V, V <sub>GS</sub> =10V, I <sub>D</sub> =20A	---	39.9	---	nC
Q <sub>gs</sub>	Gate-Source Charge		---	8.92	---	
Q <sub>gd</sub>	Gate-Drain Charge		---	10.4	---	
T <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DS</sub> =50V, V <sub>GS</sub> =10V, R <sub>GEN</sub> =6Ω, I <sub>D</sub> =1A	---	9.2	---	nS
T <sub>r</sub>	Rise Time		---	17.6	---	
T <sub>d(off)</sub>	Turn-Off Delay Time		---	32.2	---	
T <sub>f</sub>	Fall Time		---	69.9	---	
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =50V, V <sub>GS</sub> =0V, F=1MHz	---	1910	---	pF
C <sub>oss</sub>	Output Capacitance		---	506	---	
C <sub>rss</sub>	Reverse Transfer Capacitance		---	36	---	
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, F=1MHz	---	0.8	---	Ω

**Drain-Source Diode Characteristics and Ratings**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V <sub>SD</sub>	Diode Forward Voltage	V <sub>GS</sub> =0V, I <sub>S</sub> =10A	---	---	1.1	V
t <sub>rr</sub>	Reverse Recovery Time	I <sub>F</sub> =10A, V <sub>R</sub> =50V,	---	37	---	nS
Q <sub>rr</sub>	Reverse Recovery Charge	dI/dt=100A/us	---	35	---	nC

**NOTES :**

1. Repetitive Rating : Pulsed width limited by maximum junction temperature.
2. The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%.
3. Guaranteed by design, not subject to production testing.



Characteristics Curves

FIG. 1- On-Resistance vs.  $I_D$

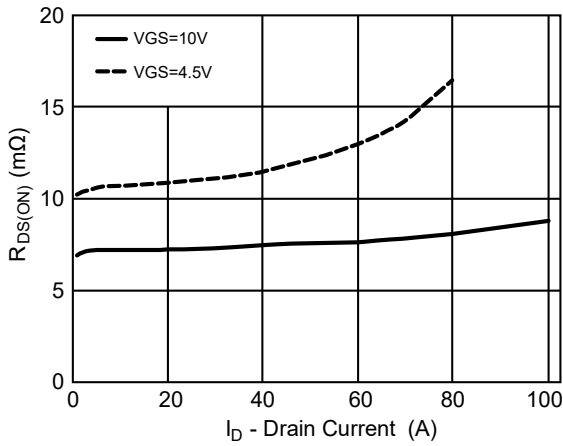


FIG. 2- Gate Threshold Voltage

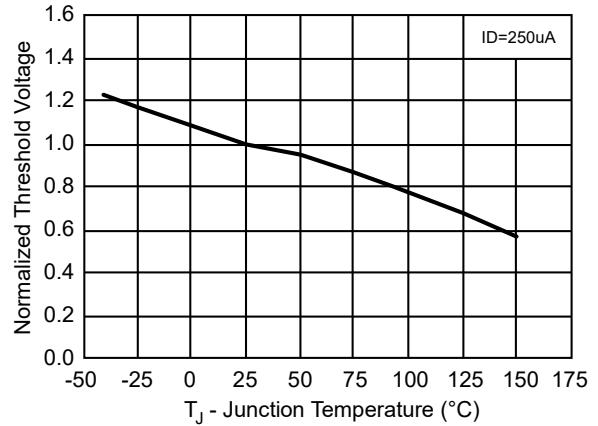


FIG. 3- Gate Charge Characteristics

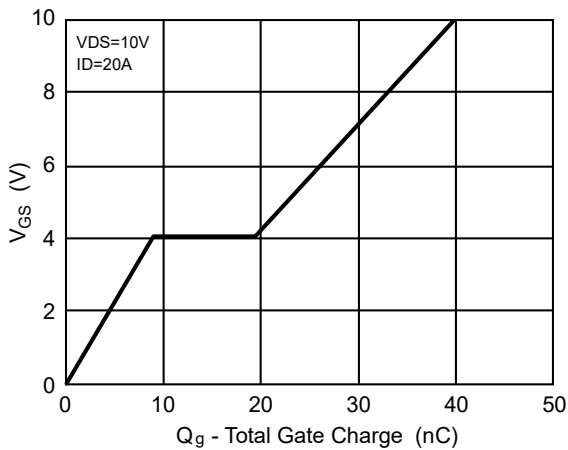


FIG. 4- Drain Current

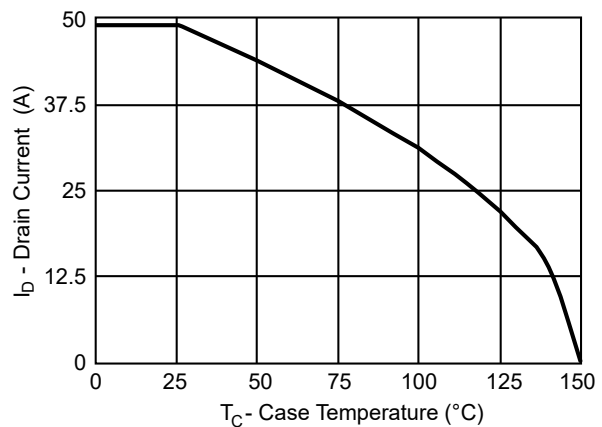


FIG. 5- Safe Operating Area

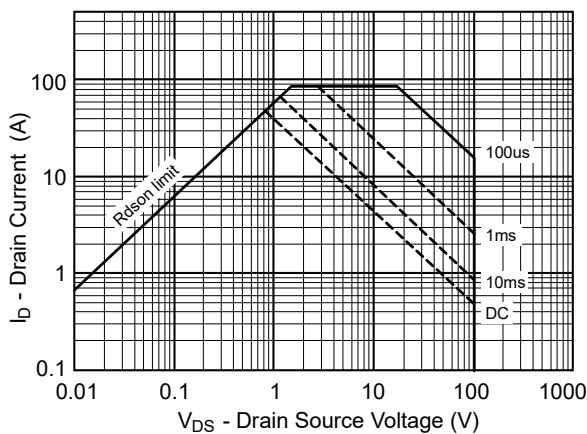
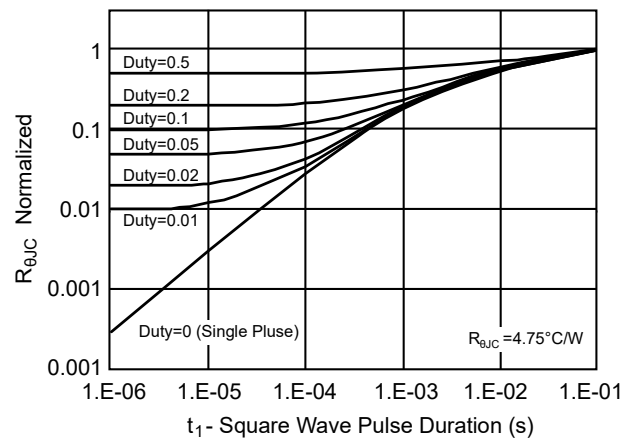


FIG. 6-  $R_{\theta JC}$  Transient Thermal Impedance



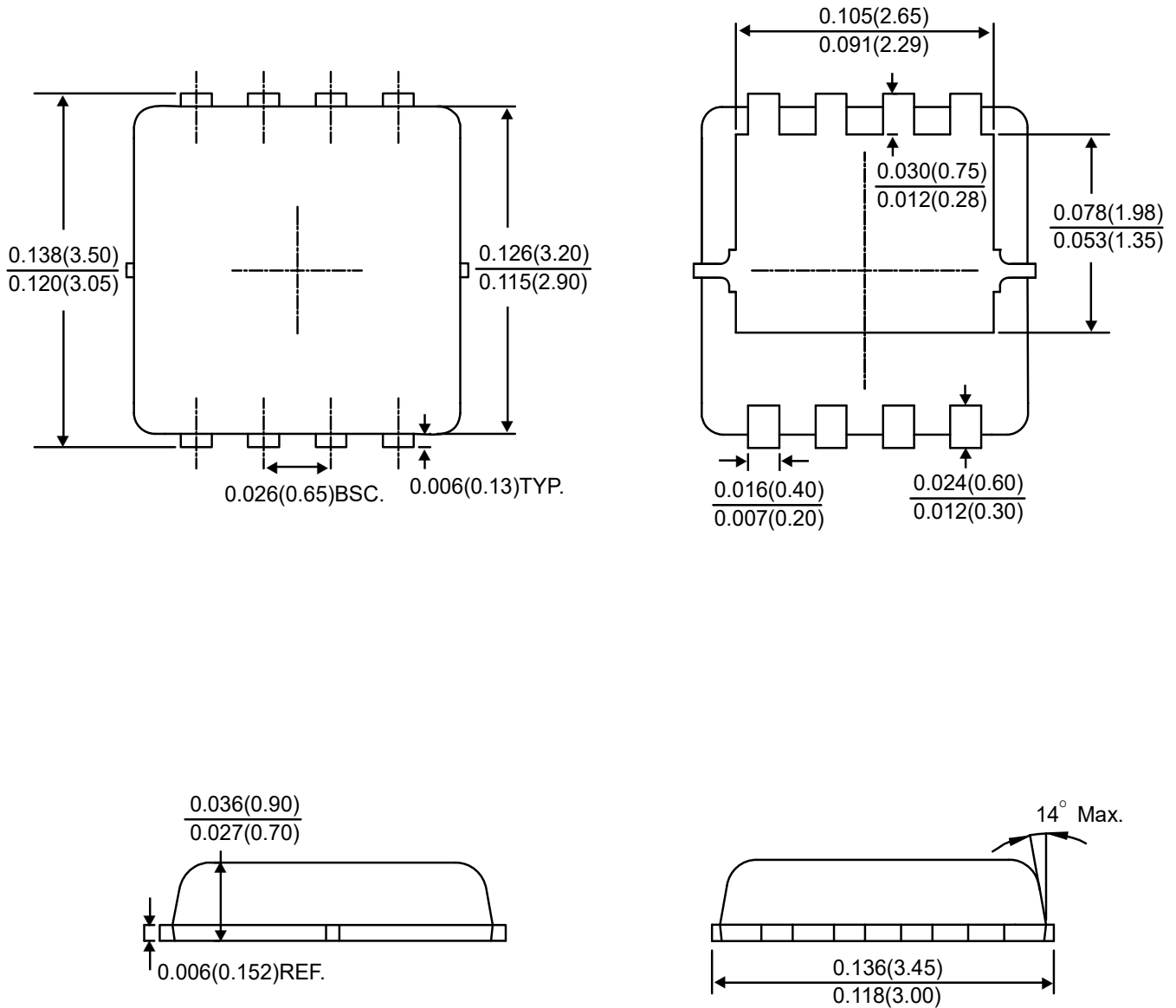


# P3MNM9P8



## 100V N-Channel MOSFETs

### Package Outline Dimensions



### PPAK3X3

Dimensions in inches and (millimeters)



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