

High Voltage $I_o=500\text{mA}$ Low Dropout Regulator

■ GENERAL DESCRIPTION

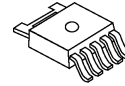
The NJW4185 is a high voltage and low current consumption low dropout regulator.

It has two product type: A version (built-in ON/OFF function type) and B version (3-terminal / compatible with 78M series)

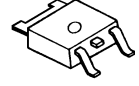
NJW4185 is mounted to TO-252-3/-5 packages and corresponded to Low ESR capacitor (MLCC).

The wide input range makes NJW4185 suitable for Automotive applications, Industrial supplies, Multiple cell battery equipment and various applications.

■ PACKAGE OUTLINE



NJW4185DL3



NJW4185DL1

■ FEATURES

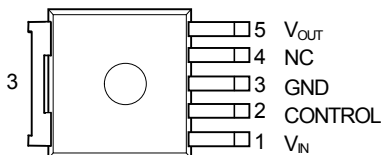
- Wide Operating Voltage Range 4.0V to 40V
- Low Current Consumption 55 μA typ. (A version)
48 μA typ. (B version)
- High Precision Output $V_o \pm 1.0\%$
- Output Current $I_o(\text{min.})=500\text{mA}$
- Output Voltage Range 2.0V to 15.0V
- Correspond to Low ESR capacitor (MLCC)
- ON/OFF Function (apply only the A ver.)
- Internal Thermal Overload Protection
- Internal Over Current Protection
- Package Outline A version: TO-252-5
B version: TO-252-3

■ PRODUCT CLASSIFICATION

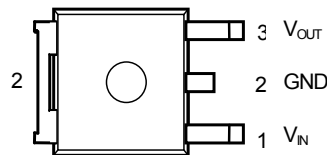
Device Name	Version	ON/OFF Function	Package
NJW4185DL3-xxA	A	Yes	TO-252-5
NJW4185DL1-xxB	B	-	TO-252-3

xx=Output Voltage ex) 33=3.3V 05=5.0V

■ PIN CONFIGURATION



NJW4185DL3-A

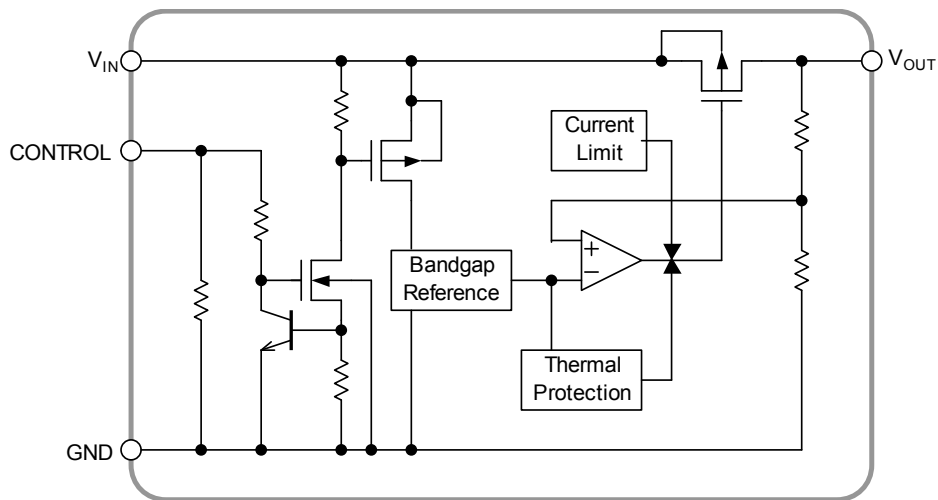


NJW4185DL1-B

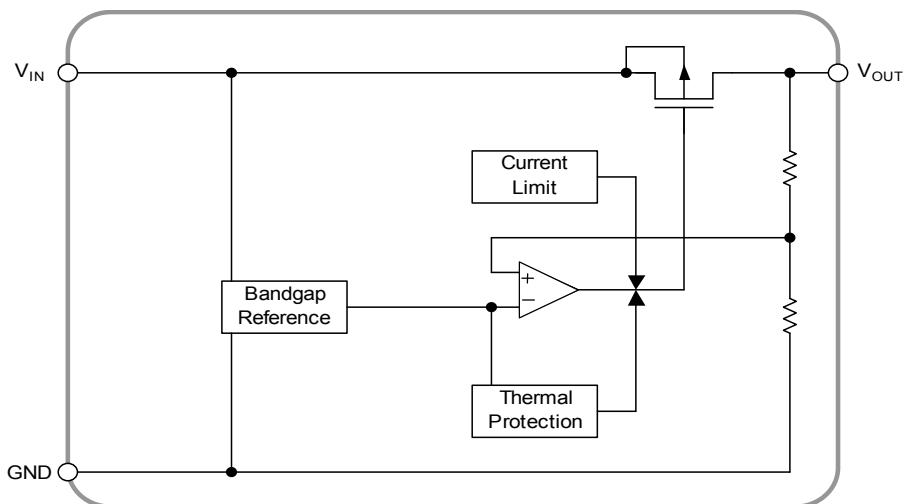
NJW4185

■ BLOCK DIAGRAM

· A version



· B version



■ OUTPUT VOLTAGE RANK LIST

· A version

Device Name	Output Voltage
NJW4185DL3-33A	3.3V
NJW4185DL3-05A	5.0V
NJW4185DL3-08A	8.0V
NJW4185DL3-15A	15.0V

· B version

Device Name	Output Voltage
NJW4185DL1-33B	3.3V
NJW4185DL1-05B	5.0V
NJW4185DL1-08B	8.0V
NJW4185DL1-15B	15.0V

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Input Voltage	V _{IN}	-0.3 to +45	V
Control Voltage(*1)	V _{CONT}	-0.3 to +45	V
Output Voltage	V _{OUT}	-0.3 to V _{IN} ≤ +17	V
Power Dissipation	P _D	1190 (*2) 3125 (*3)	mW
Junction Temperature	T _j	-40 to +150	°C
Operating Temperature	T _{opr}	-40 to +125	°C
Storage Temperature	T _{stg}	-40 to +150	°C

(*1): Apply only the A version.

(*2): Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard size, 2Layers, Cu area 100mm²)

(*3): Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard, 4Layers)

(For 4Layers: Applying 74.2 x 74.2mm inner Cu area and thermal via hole to a board based on JEDEC standard JESD51-5)

■ INPUT VOLTAGE RANGE

V_{IN}=4.0V to 40V

■ ELECTRICAL CHARACTERISTICS

Unless otherwise noted, V_{IN}=V_O+1V, C_{IN}=1.0μF, C_O=2.2μF, Ta=25°C

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
Output Voltage	V _O	I _O =30mA	-1.0%	-	+1.0%	V	
Quiescent Current	I _Q	A version, I _O =0mA, except I _{CONT}	-	55	90	μA	
		B version, I _O =0mA	-	48	83		
Quiescent Current at Control OFF (*4)	I _{Q(OFF)}	V _{CONT} =0V	-	-	1	μA	
Output Current	I _O	V _O × 0.9	500	-	-	mA	
Line Regulation	ΔV _O /ΔV _{IN}	V _{IN} = V _O +1V to 40V, I _O =30mA	-	-	0.03	%/V	
Load Regulation	ΔV _O /ΔI _O	I _O =0mA to 500mA	-	-	0.006	%/mA	
Ripple Rejection	RR	V _{IN} = V _O +1V, e _{in} =200mVrms, f=1kHz, I _O =10mA	V _O =3.3V	-	62	-	dB
			V _O =5.0V	-	60	-	
			V _O =8.0V	-	55	-	
			V _O =15V	-	50	-	
Dropout Voltage (*5)	ΔV _{I_O}	I _O =300mA	-	0.27	0.42	V	
Average Temperature Coefficient of Output Voltage	ΔV _O /ΔTa	Ta =0 to 85°C, I _O =30mA	-	±50	-	ppm/°C	
Control Current (*4)	I _{CONT}	V _{CONT} =1.6V	-	1	3	μA	
Control Voltage for ON-state (*4)	V _{CONT(ON)}		1.6	-	-	V	
Control Voltage for OFF-state (*4)	V _{CONT(OFF)}		-	-	0.6	V	

(*4): Apply only the A version.

(*5): Except Output Voltage Rank less than 3.8V

The above specification is a common specification for all output voltages.

Therefore, it may be different from the individual specification for a specific output voltage.

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■ THERMAL CHARACTERISTICS

PARAMETER	SYMBOL	VALUE	UNIT
Junction-to-Ambient thermal resistance	θ_{ja}	105 (*6) 40 (*7)	$^{\circ}\text{C/W}$
Junction-to-Top of package characterization parameter	ψ_{jt}	17 (*6) 12 (*7)	$^{\circ}\text{C/W}$

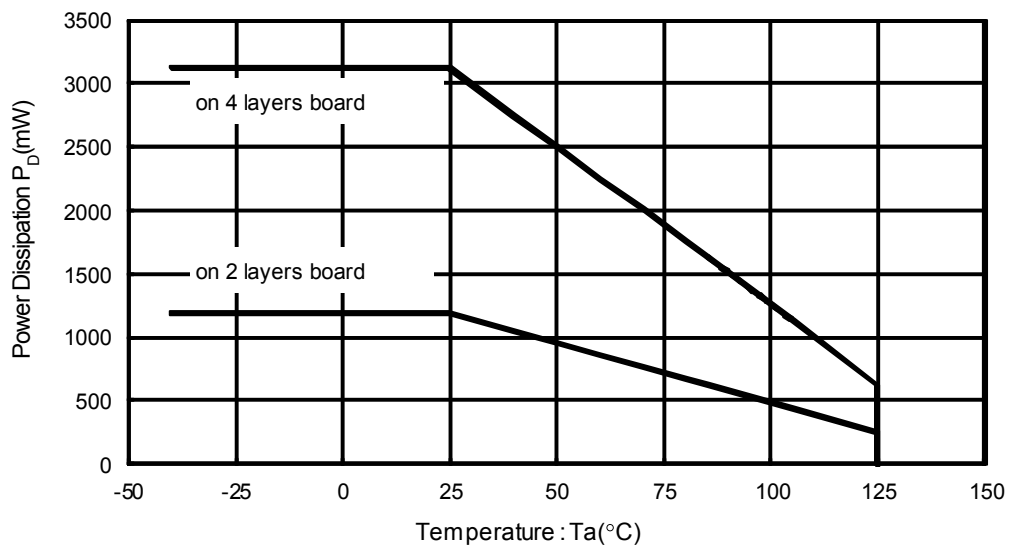
(*6): Mounted on glass epoxy board. (76.2 × 114.3 × 1.6mm:based on EIA/JDEC standard size, 2Layers, Cu area 100mm²)

(*7): Mounted on glass epoxy board. (76.2 × 114.3 × 1.6mm:based on EIA/JDEC standard, 4Layers)

(For 4Layers: Applying 74.2 × 74.2mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5)

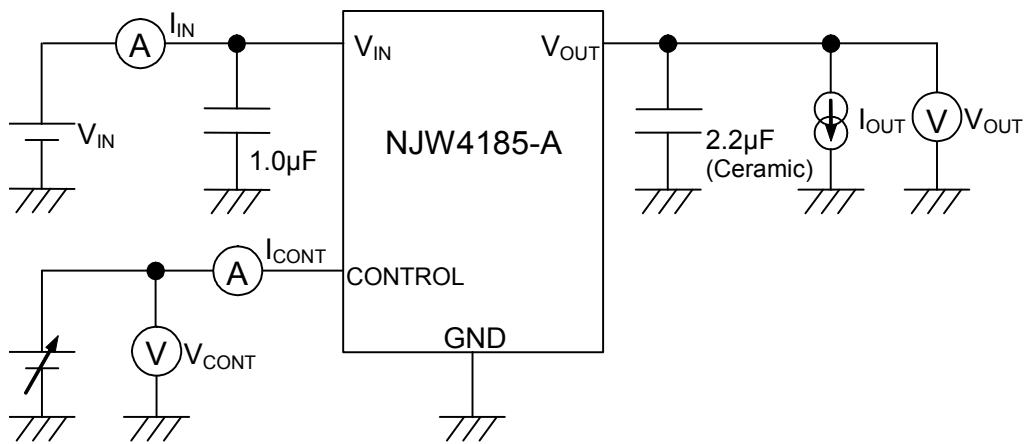
■ POWER DISSIPATION vs. AMBIENT TEMPERATURE

NJW4185DL1/DL3 PowerDissipation
(Topr=-40~+125°C, Tj=150°C)

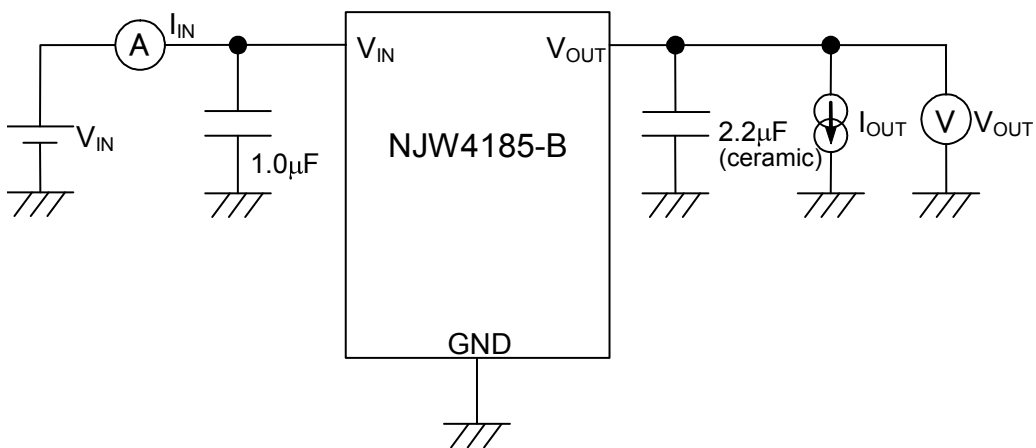


■ TEST CIRCUIT

·A version



·B version

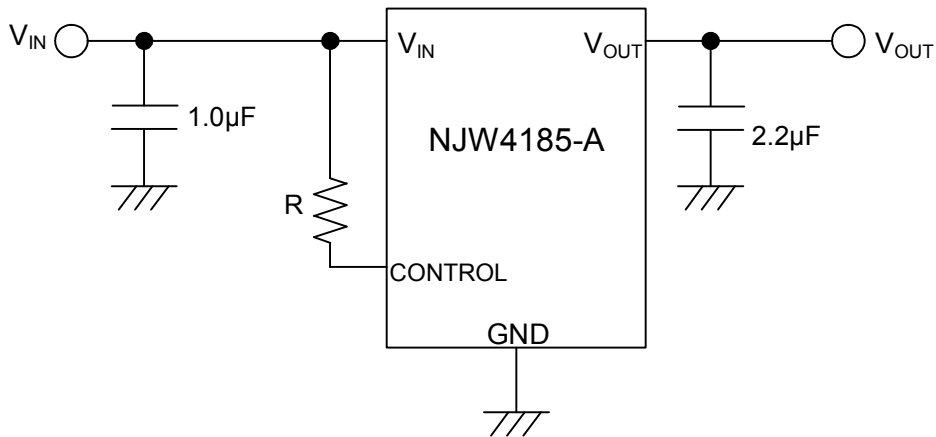


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■ TYPICAL APPLICATION

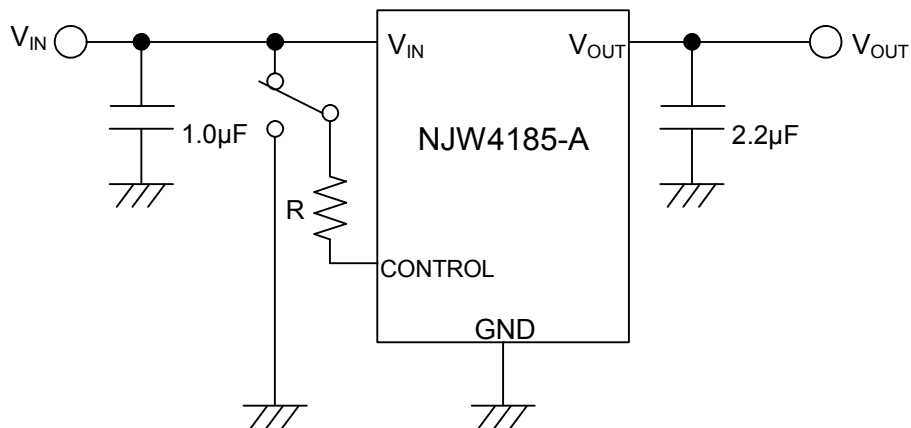
· A version

1. In the case where ON/OFF Control is not required



Connect control pin to V_{IN} pin

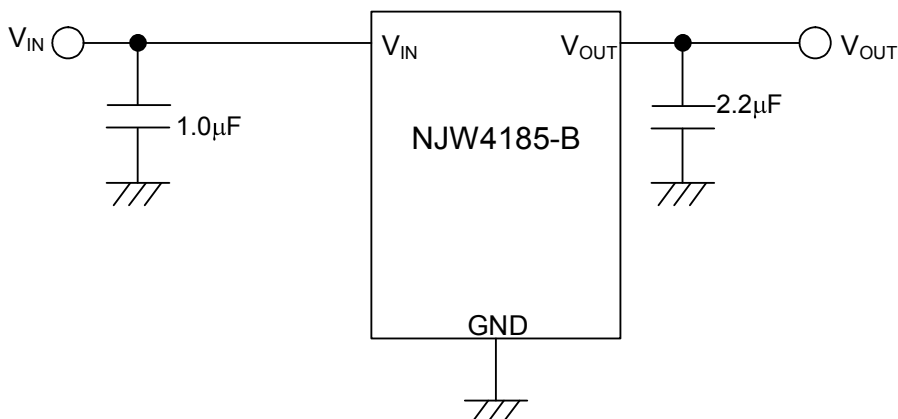
2. In use of ON/OFF CONTROL



State of control pin:

- "H" → output is enabled.
- "L" or "open" → output is disabled.

· B version



*In the case of using a resistance "R" between V_{IN} and control.

If this resistor is inserted, it can reduce the control current when the control voltage is high.

The applied voltage to control pin should set to consider voltage drop through the resistor "R" and the minimum control voltage for ON-state.

The $V_{CONT(ON)}$ and I_{CONT} have temperature dependence as shown in the "Control Current vs. Temperature" and "Control Voltage vs. Temperature" characteristics. Therefore, the resistance "R" should be selected to consider the temperature characteristics.

*Input Capacitor C_{IN}

Input Capacitor C_{IN} is required to prevent oscillation and reduce power supply ripple for applications when high power supply impedance or a long power supply line.

Therefore, use the recommended C_{IN} value (refer to conditions of ELECTRIC CHARACTERISTIC) or larger and should connect between GND and V_{IN} as shortest path as possible to avoid the problem.

*Output Capacitor C_O

The output capacitor C_O will be required for a phase compensation of the internal error amplifier.

The capacitance and the equivalent series resistance (ESR) influence to stable operation of the regulator.

Use of a smaller C_O may cause excess an output noise or an oscillation of the regulator due to lack of the phase compensation.

On the other hand, use of a larger C_O reduces an output noise and a ripple output, and also improves an output transient response when load rapidly changes.

Therefore, use the recommended C_O value (refer to conditions of ELECTRIC CHARACTERISTIC) or larger and should connect between GND and V_{OUT} as shortest path as possible for stable operation.

The recommended capacitance depends on the output voltage rank. Especially, a low voltage regulator requires larger C_O value.

In addition, you should consider varied characteristics of capacitor (a frequency characteristic, a temperature characteristic, a DC bias characteristic and so on) and unevenness peculiar to a capacitor supplier enough.

When selecting C_O , recommend that have withstand voltage margin against an output voltage and superior temperature characteristic.

*Transient response characteristic of Output Voltage

In general, overshoot or undershoot of output voltage may occur due to the transient response characteristic of an internal error amplifier.

Especially, low current consumption regulator may have overshoot or undershoot due to slow feedback caused by current saving design.

Therefore, design validation is important in the following cases:

1. Input voltage or output current change sharply
2. Output capacitors is small
3. Output load is light
4. A regulator starts up with very low dropout voltage operation.

Increasing the value of input and/or output capacitor is a common countermeasure for improving a transient response characteristic.

A transient response characteristic may vary with operating conditions and external components value.

Please check it with the actual environment.

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*The notes of the evaluation when output pin is shorted to GND

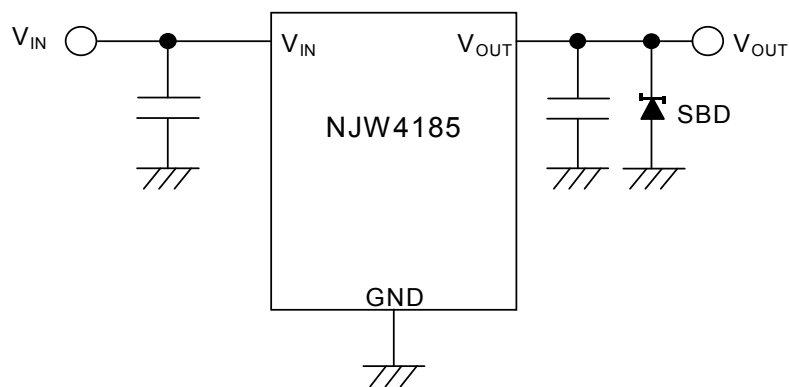
When evaluate short circuit test, the IC may break down because of regenerated energy by the parasitic inductance included in wiring pattern.

It phenomenon appears conspicuously when an output voltage is higher($V_o=8.0V$ or more) or connected to inductive load.

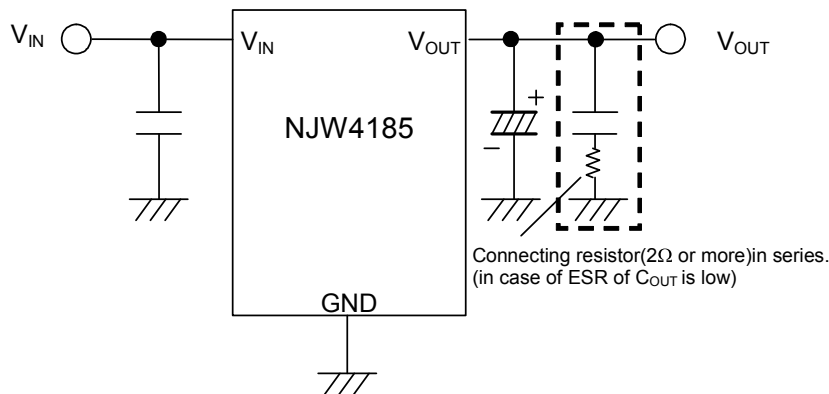
In case of short circuit in actual application, not likely to destruction of the IC because of some of Resistance exist between load.

If happened above phenomenon by the short circuit test with the actual application, recommend connecting schottky barrier diode(SBD) between V_o pin and GND or using output capacitors that have ESR more than 2Ω like a tantalum or aluminum electrolytic capacitor.(see below figure)

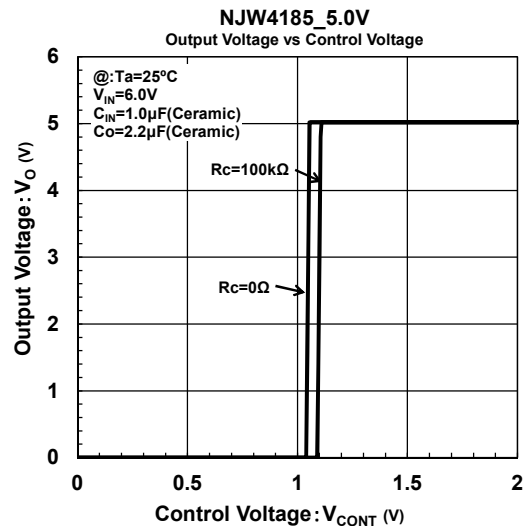
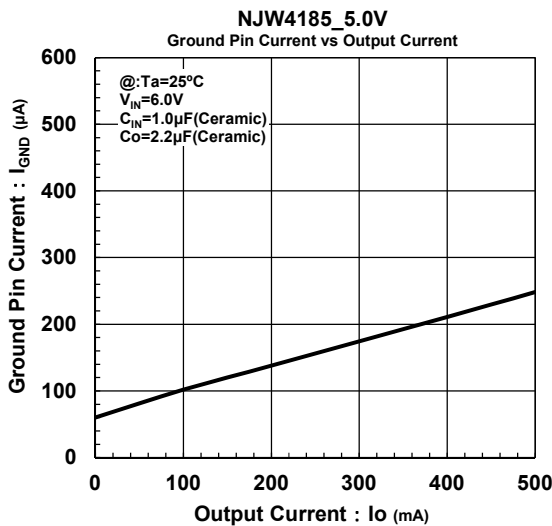
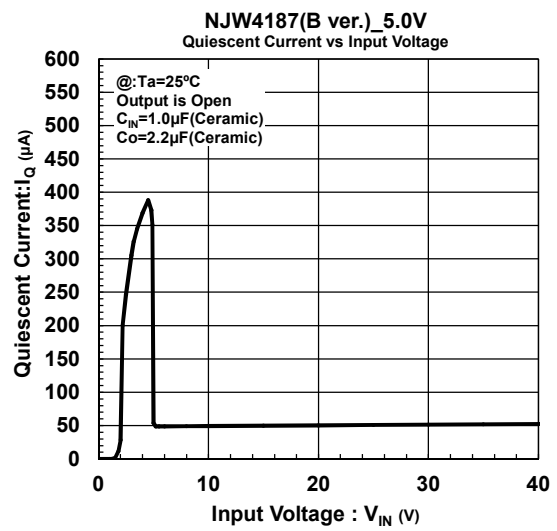
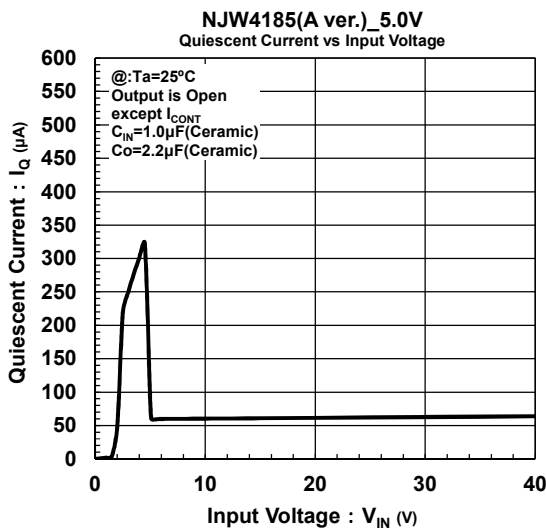
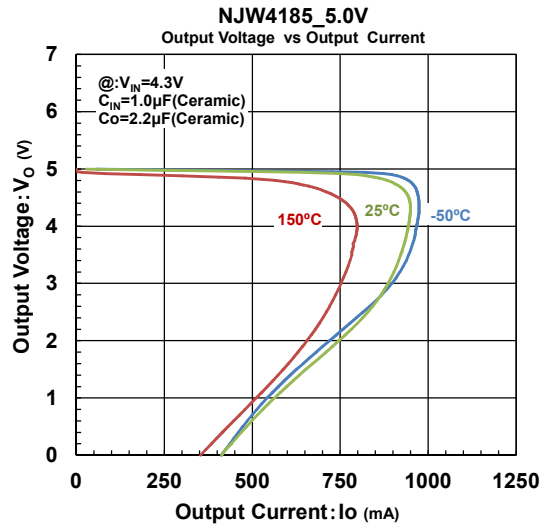
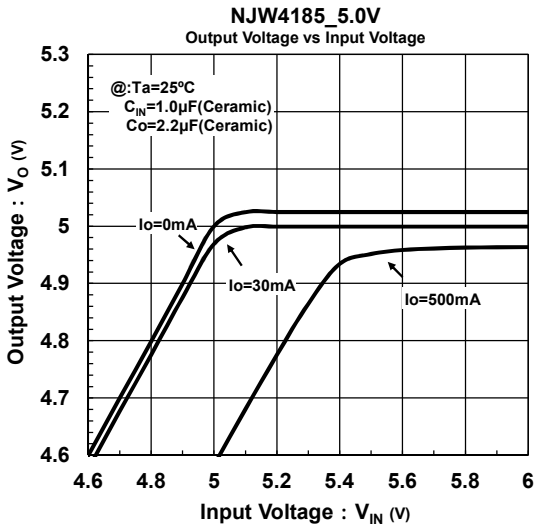
(a) In case of insert Schottky barrier diode between output pin - GND

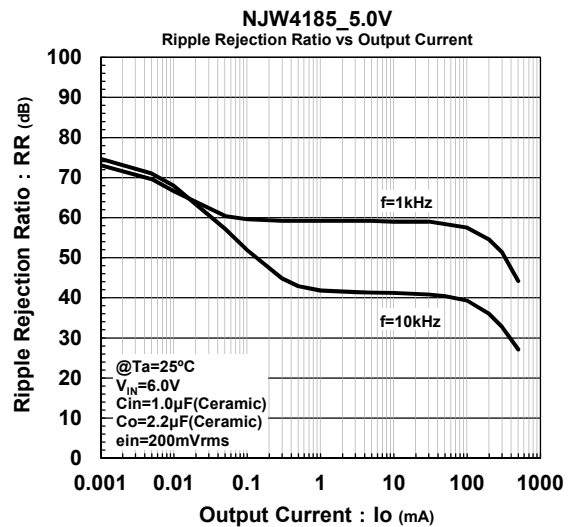
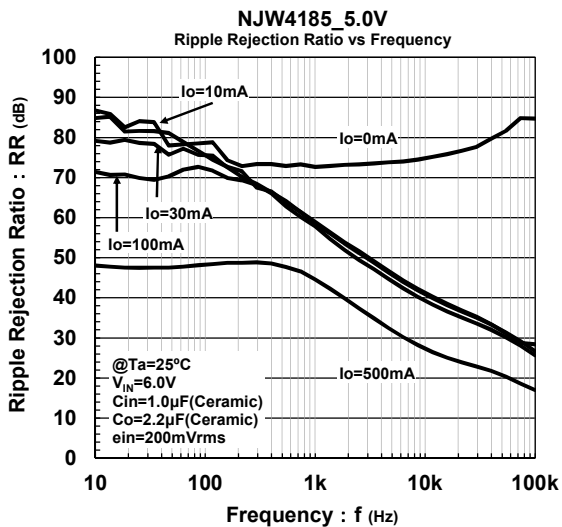
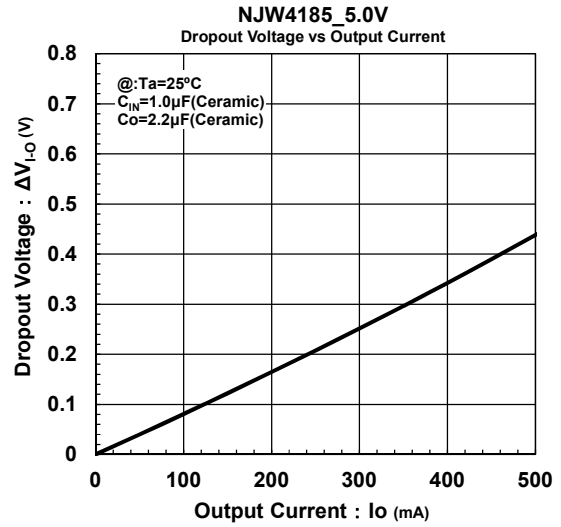
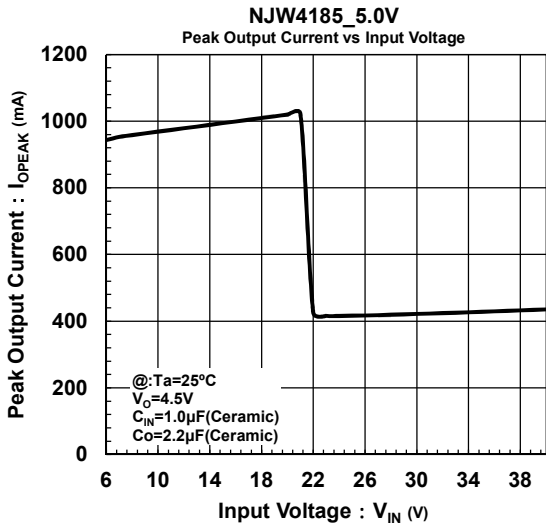
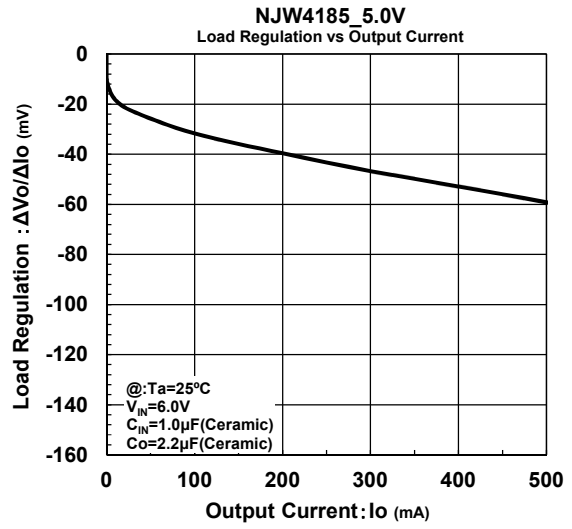
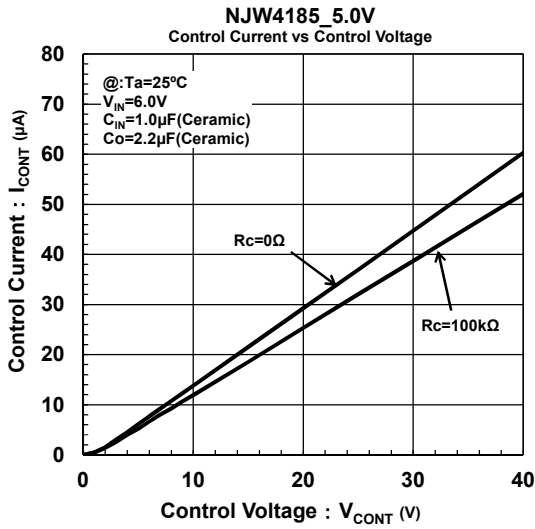


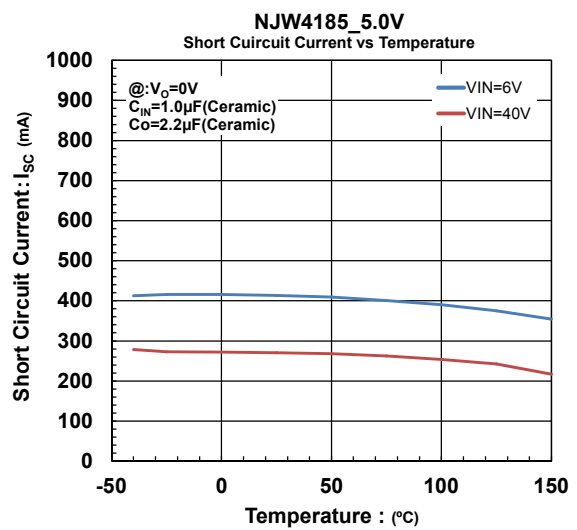
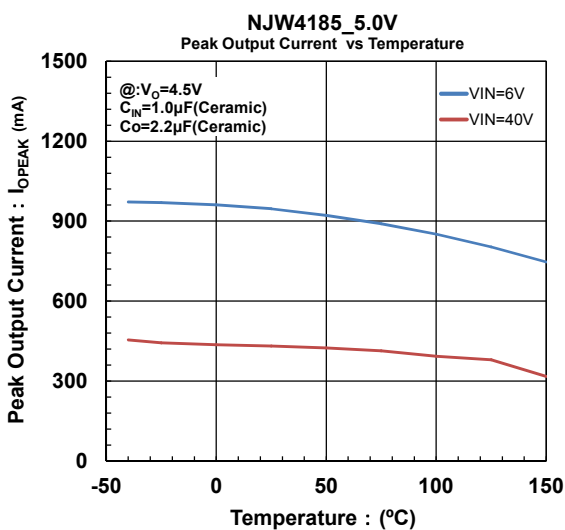
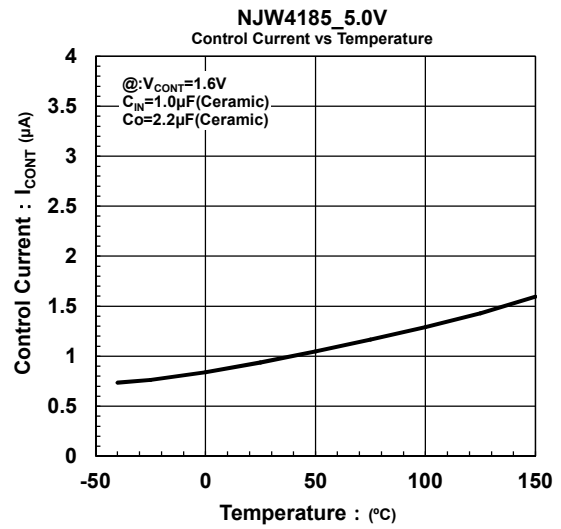
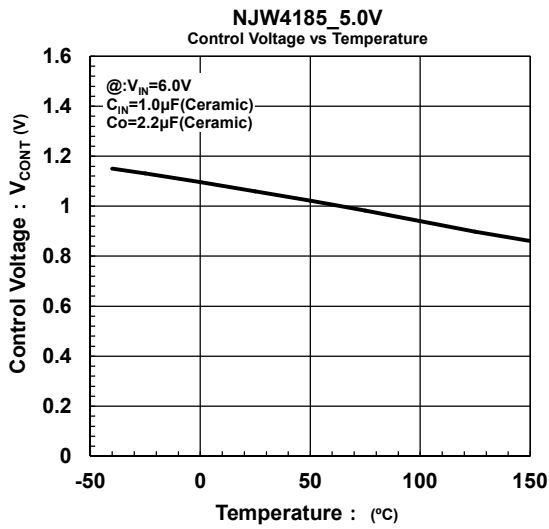
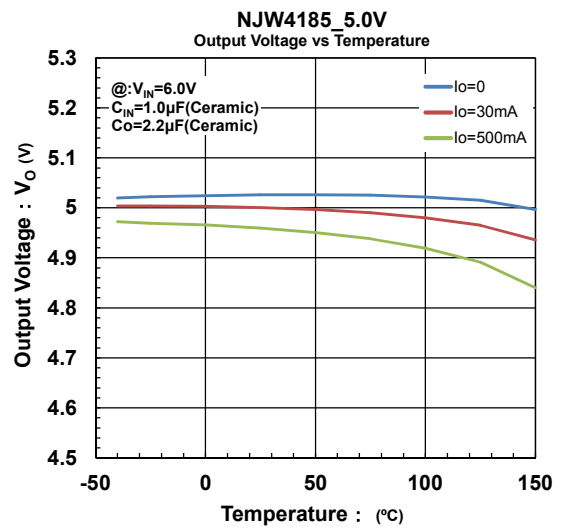
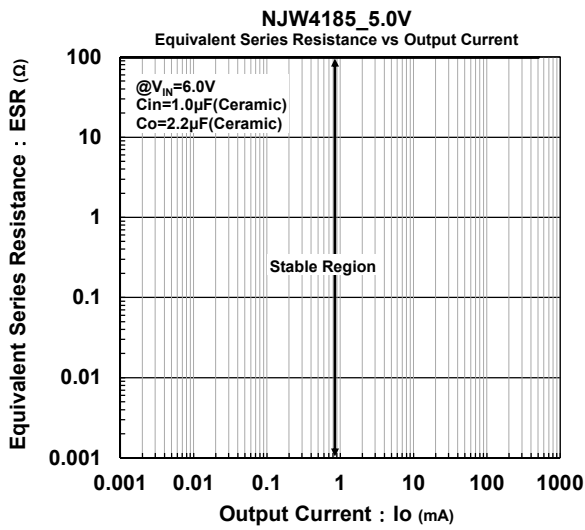
(b) In case of using the electrolytic capacitor or insert series resistor



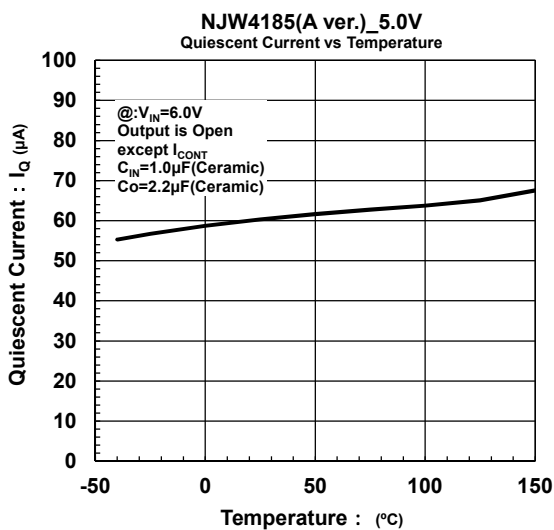
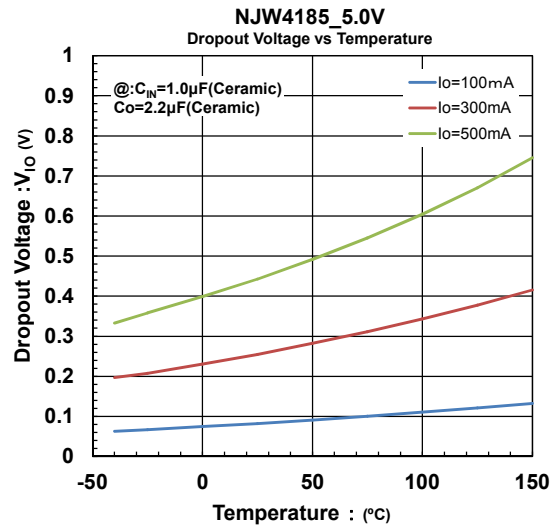
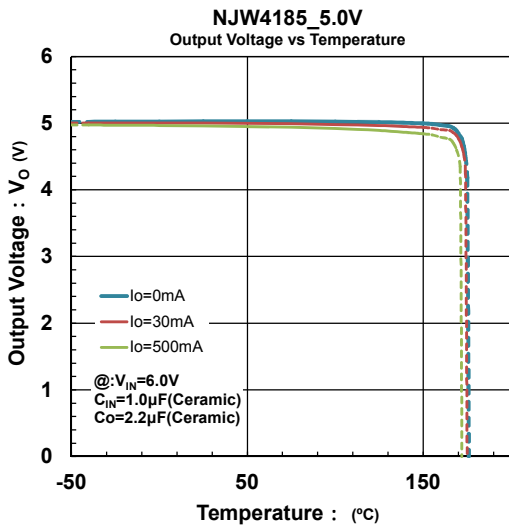
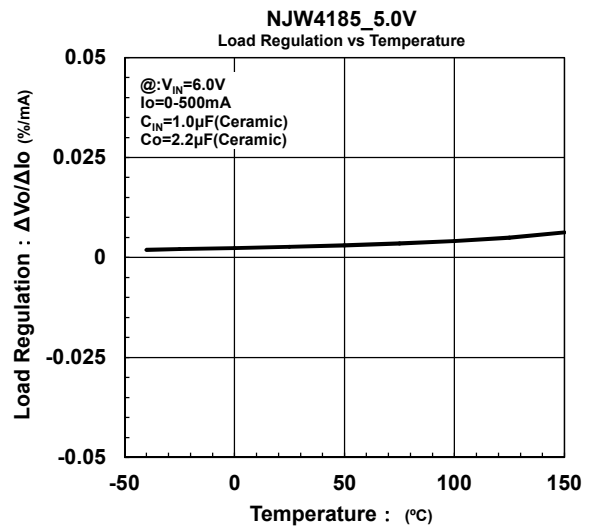
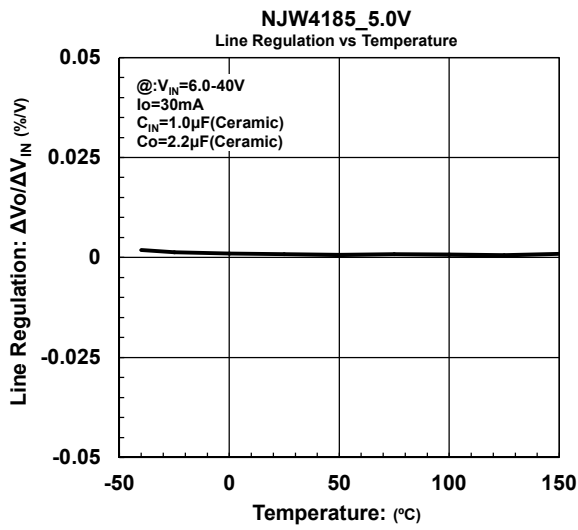
TYPICAL CHARACTERISTICS



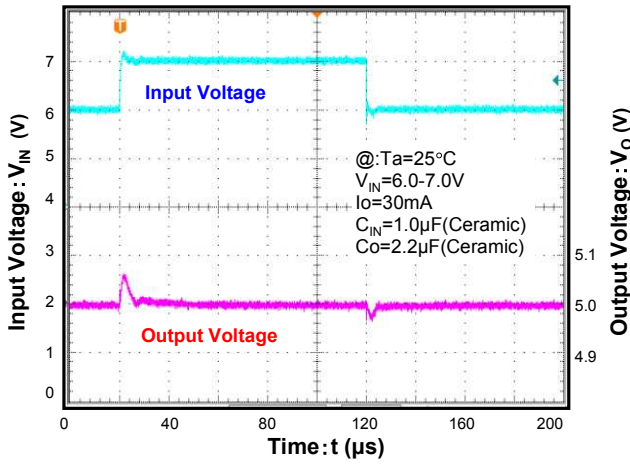




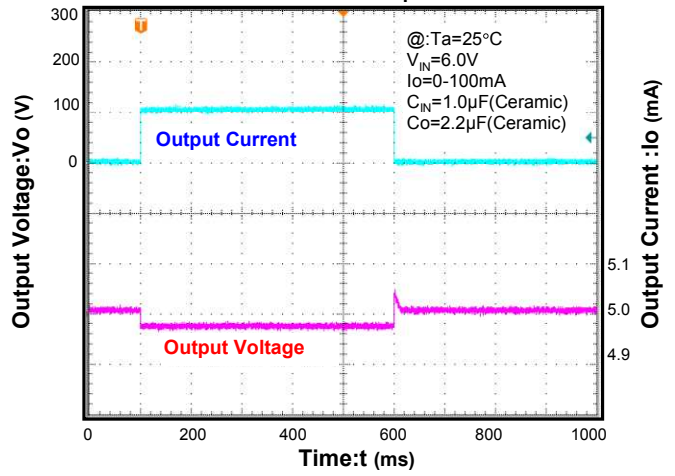
NJW4185



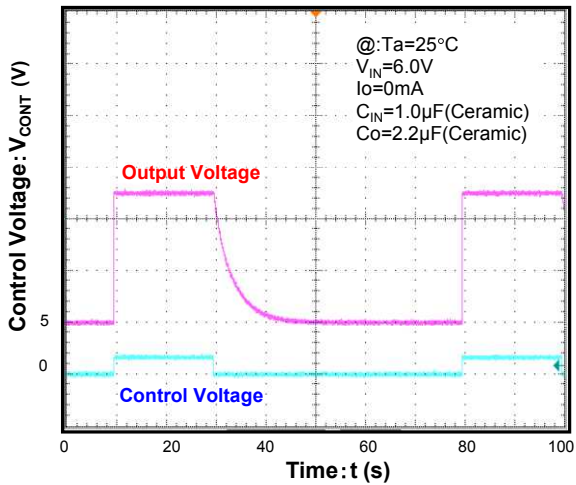
NJW4185_5.0V
Input Transient Response



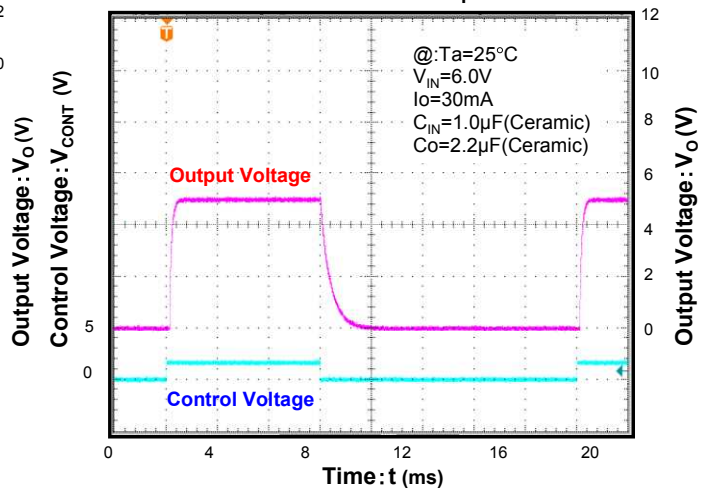
NJW4185_5.0V
Load Transient Response



NJW4185(A ver.)_5.0V
ON/OFF Transient Response without Load



NJW4185(A ver.)_5.0V
ON/OFF Transient Response



[CAUTION]
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