Switching Regulator IC for Buck Converter

External MOSFET driving

■ GENERAL DESCRIPTION

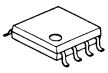
The **NJW4160** is a MOSFET Drive switching regulator IC for Buck Converter that operates wide input range from 3.0V to 35V. It can provide large current application because of built-in highly effective Pch MOSFET drive circuit.

Built-in pulse-by-pulse current detecting type over current protection limits the output current at over load.

It is suitable for logic voltage generation from high voltage that Car Accessory, Office Automation Equipment, Industrial Instrument and so on.

■ PACKAGE OUTLINE

NJW4160R
(MSOP8(VSP8))

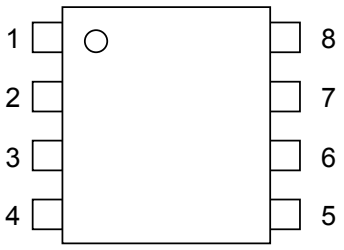


NJW4160M
(DMP8)

■ FEATURES

● Pch MOSFET Driving	Driving Voltage V^+-5.35V(typ.)
● Wide Operating Voltage Range	3V to 35V
● PWM Control	
● Wide Oscillating Frequency	50kHz to 1MHz
● Over Current Protection	
● UVLO (Under Voltage Lockout)	
● Standby Function	
● Package Outline	NJW4160M: DMP8 NJW4160R: MSOP8(VSP8) *MEETJEDEC MO-187-DA

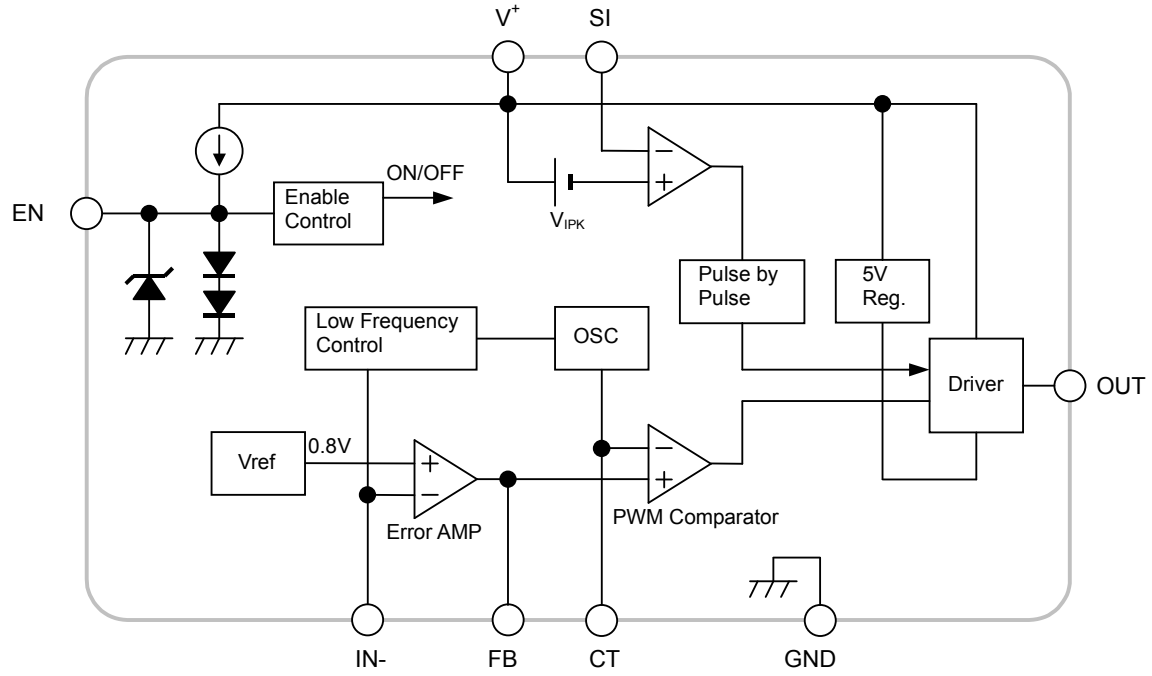
■ PIN CONFIGURATION



NJW4160R
NJW4160M

PIN FUNCTION
1. OUT
2. SI
3. V^+
4. EN
5. IN-
6. FB
7. CT
8. GND

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

PARAMETER	SYMBOL	MAXIMUM RATINGS	UNIT
Supply Voltage	V^+	+40	V
OUT pin Voltage	V_{OUT}	V^+-6 to V^+	V
EN pin sink Current	I_{EN}	500	μA
IN- pin Voltage	V_{IN-}	+6	V
CT pin Voltage	V_{CT}	+6 (*1)	V
Power Dissipation	P_D	MSOP8(VSP8) : 595 (*2) DMP8: 530 (*2)	mW
Operating Temperature Range	T_{opr}	-40 to +85	°C
Storage Temperature Range	T_{stg}	-40 to +150	°C

(*1): When Supply voltage is less than +6V, the absolute maximum voltage is equal to the Supply voltage.

(*2): Mounted on glass epoxy board based on EIA/JEDEC. (76.2 × 114.3 × 1.6mm: 2-Layers)

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V^+	3	–	35	V
Timing Capacitor	C_T	120	–	3,300	pF
Oscillating Frequency	f_{OSC}	50	–	1,000	kHz

■ ELECTRICAL CHARACTERISTICS

(Unless otherwise noted, V^+=12V, V_{EN} is connected to V^+ via 200kΩ pull-up, C_T=470pF, Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Oscillator Block						
Oscillation Frequency	f_{OSC}	C_T=470pF	270	300	330	kHz
Charge Current	I_{chg}		180	200	220	μA
Discharge Current	I_{dis}		180	200	220	μA
Voltage amplitude	V_{OSC}		–	0.6	–	V
Frequency Supply Voltage Deviation	f_{DV}	V^+=3V to 35V	–	1	–	%
Frequency Temperature Deviation	f_{DT}	Ta=-40°C to +85°C	–	5	–	%
Oscillation Frequency (Low Frequency Control)	f_{OSC_LOW}	V_{IN-}=0.3V, V_{FB}=0.7V	–	100	–	kHz
Error Amplifier Block						
Reference Voltage	V_B		-1.0%	0.8	+1.0%	V
Input Bias Current	I_B		-0.1	–	+0.1	μA
Open Loop Gain	A_V		–	80	–	dB
Gain Bandwidth	G_B		–	1	–	MHz
Output Source Current	I_{OM+}	V_{FB}=1V, V_{IN-}=0.7V	50	90	140	μA
Output Sink Current	I_{OM-}	V_{FB}=1V, V_{IN-}=0.9V	6	13	20	mA
PWM Comparate Block						
Input Threshold Voltage (FB pin)	V_{T_0}	Duty=0%, V_{IN-}=0.6V	0.32	0.4	0.48	V
	V_{T_50}	Duty=50%, V_{IN-}=0.6V	0.63	0.7	0.77	V
Maximum Duty Cycle	$M_{AX}D_{UTY}$	V_{FB}=1.2V	100	–	–	%
Current Limit Detection Block						
Current Limit Detection Voltage	V_{IPK}		95	120	145	mV
Delay Time	T_{DELAY}		–	100	–	ns
Output Block						
Output High Level ON Resistance	R_{OH}	I_O=-50mA	–	3.5	7	Ω
Output Low Level ON Resistance	R_{OL}	I_O=+50mA	–	9	–	Ω
Output Sink Current	I_{OL}	OUT pin= V^+ - 4.8V	20	30	45	mA
Output pin Limiting Voltage	V_{OLIM}		V^+-5.5V	V^+-5.35V	V^+-5.0V	V
Under Voltage Lockout Block						
ON Threshold Voltage	V_{T_ON}	V^+= L → H	2.65	2.8	2.95	V
OFF Threshold Voltage	V_{T_OFF}	V^+= H → L	2.4	2.55	2.7	V

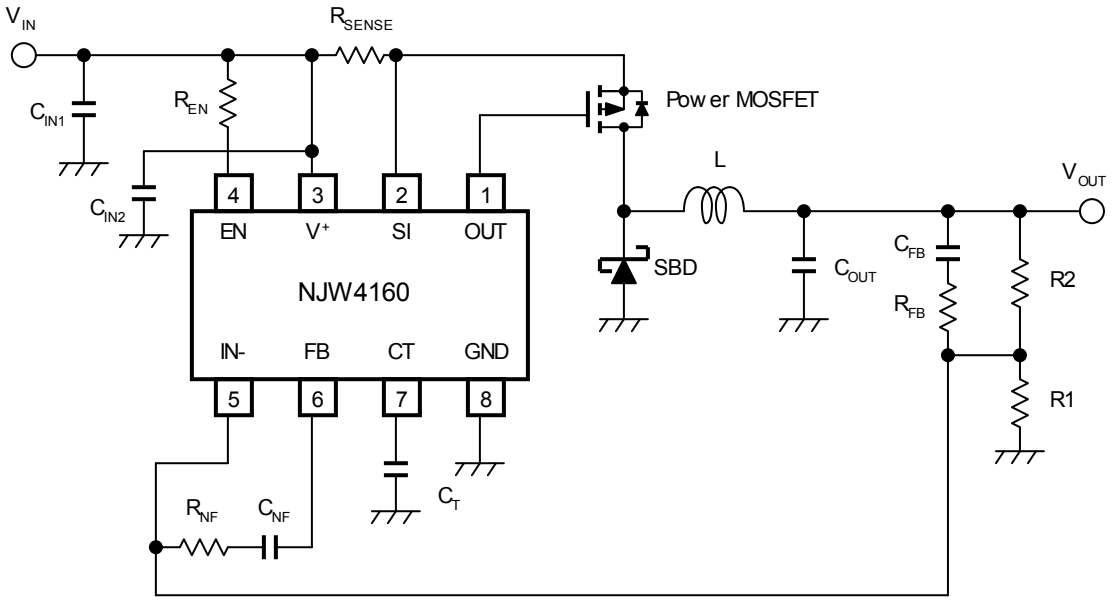
■ ELECTRICAL CHARACTERISTICS

(Unless otherwise noted, V^+=12V, V_{EN} is connected to V^+ via 200kΩ pull-up, C_T=470pF, Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Enable Control Block						
ON Control Voltage	V_{ON}	V_{EN}= L → H	1.6	–	V_{Z_EN}	V
OFF Control Voltage	V_{OFF}	V_{EN}= H → L	0	–	0.5	V
EN pin Voltage at Open	V_{EN_OPEN}		1.5	1.8	2.0	V
EN pin Zener Voltage	V_{Z_EN}	I_{EN}= 450μA	4.8	5.2	–	V
EN pin Source Current	I_{EN_SOURCE}	V_{EN}= 0V	0.6	2.0	6.0	μA
EN pin Sink Current	I_{EN_SINK}	V_{EN}= 4.8V	–	20	40	μA
General Characteristics						
Quiescent Current	I_{DD}	R_L=no load, V_{IN-}=0.7V, V_{FB}=0.7V	–	1.1	1.5	mA
Standby Current	I_{DD_STB}	V_{EN}=0V	–	3.5	6	μA

■ APPLICATION EXAMPLE

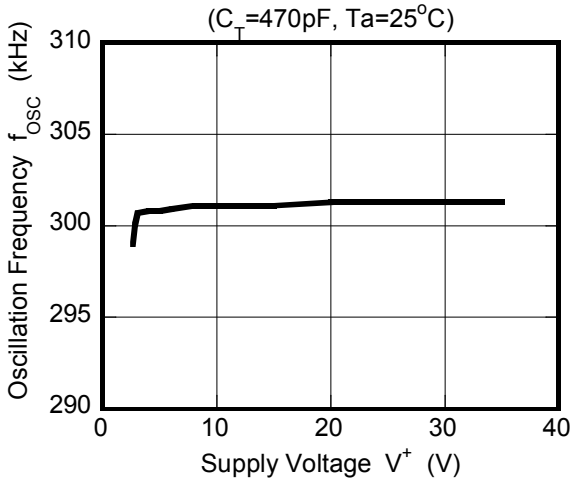
Non-isolated Buck Converter



■ CHARACTERISTICS

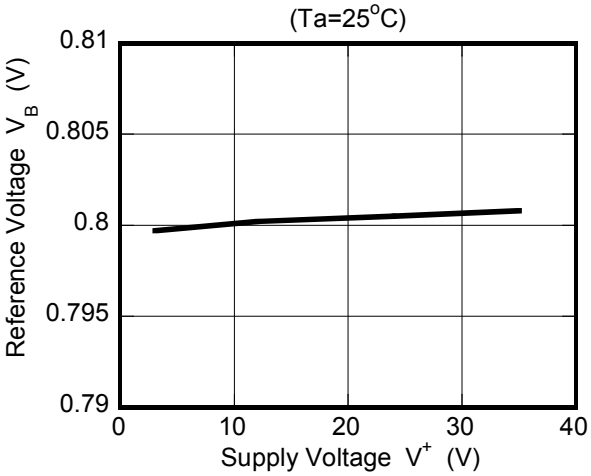
Oscillation Frequency vs. Supply Voltage

(C_T=470pF, Ta=25°C)



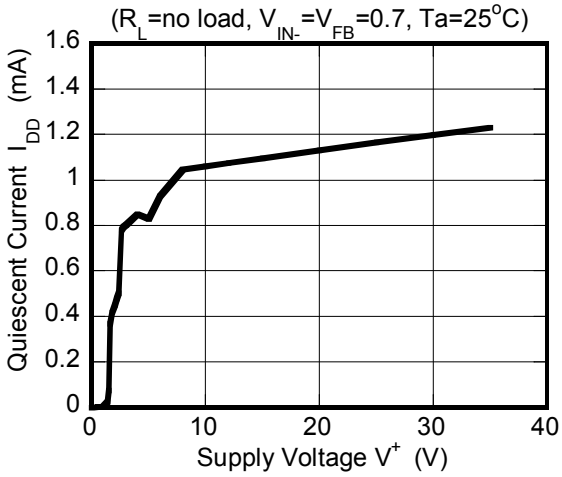
Reference Voltage vs. Supply Voltage

(Ta=25°C)



Quiescent Current vs. Supply Voltage

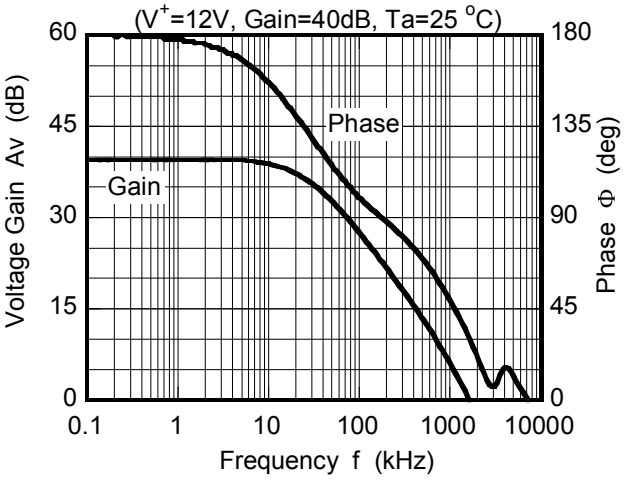
(R_L=no load, V_{IN-}=V_{FB}=0.7, Ta=25°C)



Error Amplifier Block

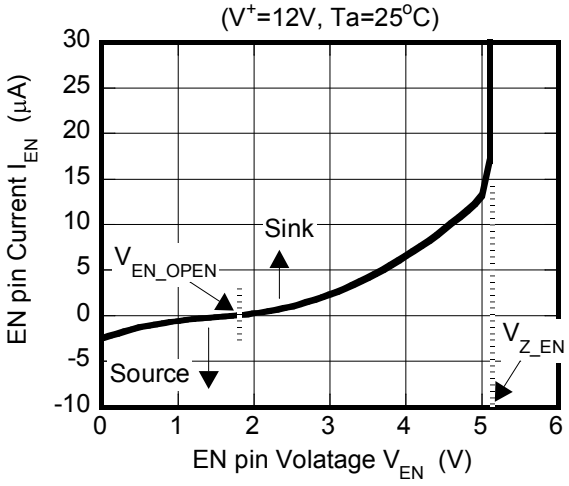
Voltage Gain, Phase vs. Frequency

(V^+=12V, Gain=40dB, Ta=25 °C)



EN pin Current vs.EN pin Voltage

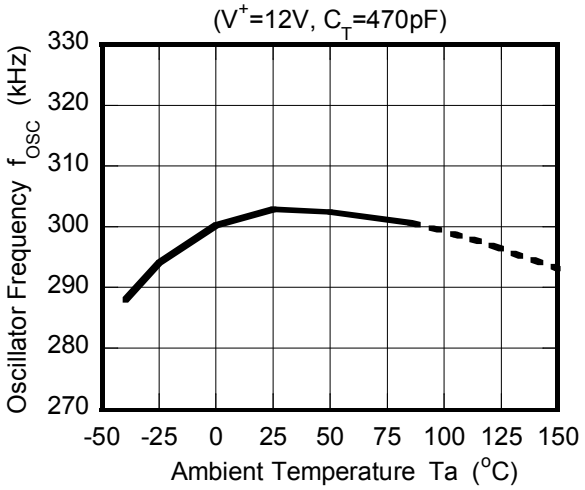
(V^+=12V, Ta=25°C)



■ CHARACTERISTICS

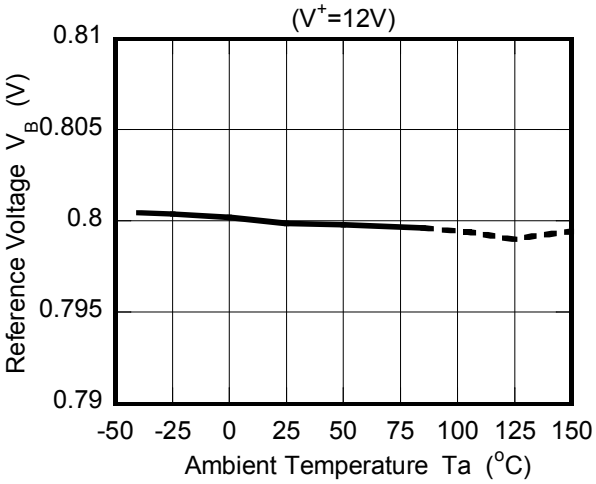
Oscillator Frequency vs. Temperature

(V^+=12V, C_T=470pF)



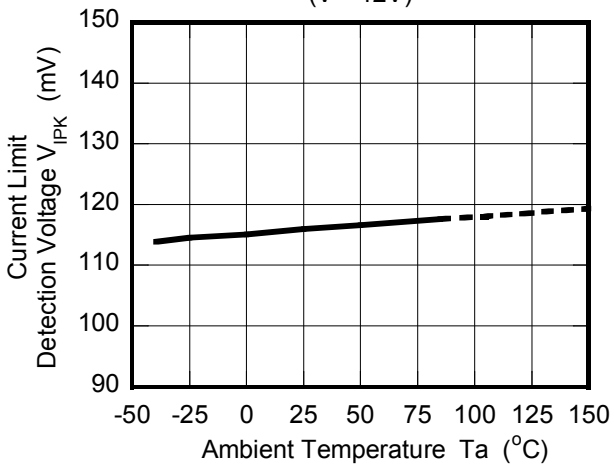
Reference Voltage vs. Temperature

(V^+=12V)



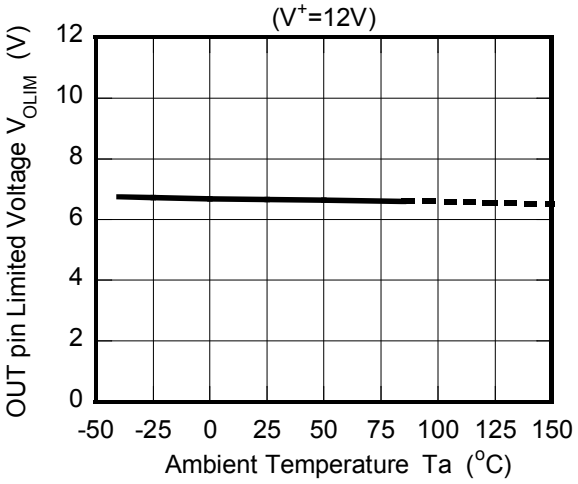
Current Limit Detection Votage vs.Temperature

(V^+=12V)



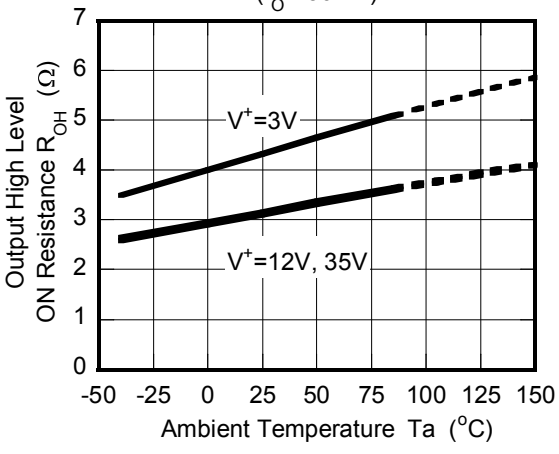
OUT pin Limited Voltage vs.Temperature

(V^+=12V)



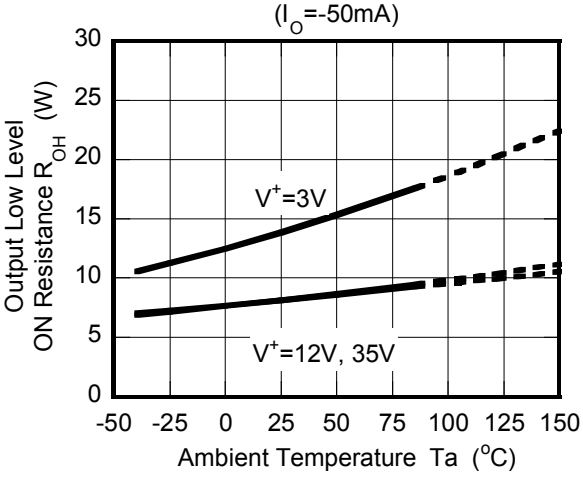
Output High Level ON Resistance vs.Temperature

(I_O=-50mA)



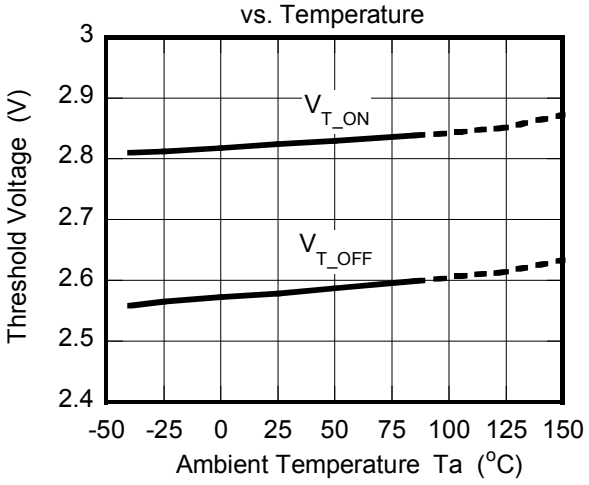
Output Low Level ON Resistance vs.Temperature

(I_O=-50mA)

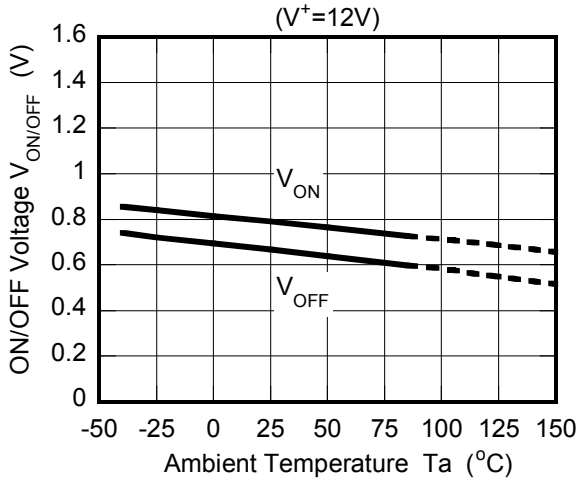


■ CHARACTERISTICS

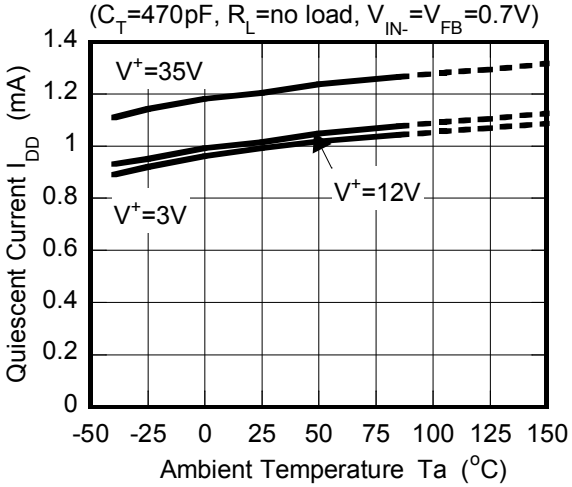
Under Voltage Lockout Voltage vs. Temperature



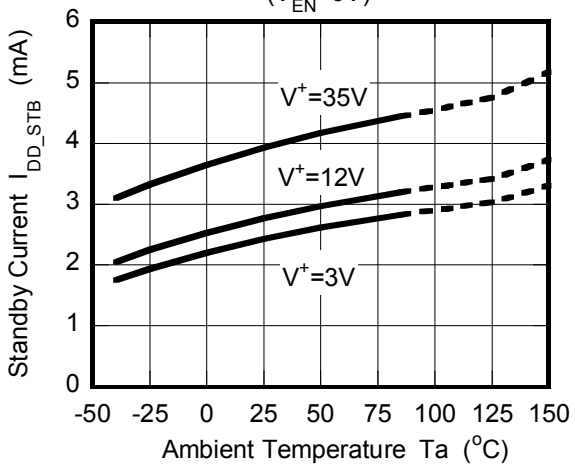
Enable Control ON/OFF Voltage vs.Temperature (V^+=12V)



Quiescent Current vs. Temperature (C_T=470pF, R_L=no load, V_{IN-}=V_{FB}=0.7V)



Standby Current vs. Temperature (V_{EN}=0V)



■ PIN DESCRIPTIONS

PIN NUMBER	PIN NAME	FUNCTION
1	OUT	Output pin for Power MOSFET Driving The OUT pin Voltage is clamped with V^+ -5.35V(typ.) at the time of Low level, in order to protect a gate of Pch MOSFET.
2	SI	Current Sensing pin When difference voltage between the V^+ pin and the SI pin exceeds 120mV(typ.), over current protection operates.
3	V^+	Power Supply pin
4	EN	ON/OFF Control pin Normal Operation at the time of High Level. Standby Mode at the time of Low Level.
5	IN-	Output Voltage Detecting pin Connects output voltage through the resistor divider tap to this pin in order to voltage of the IN- pin become 0.8V.
6	FB	Feedback Setting pin The feedback resistor and capacitor are connected between the FB pin and the IN- pin.
7	CT	Oscillating Frequency Setting pin by Timing Capacitor Oscillating Frequency should set between 50kHz and 1MHz.
8	GND	GND pin

■ Description of Block Features

● Error Amplifier Section (ER·AMP)

0.8V±1% precise reference voltage is connected to the non-inverted input of this section.

To set the output voltage, connects converter's output to inverted input of this section (IN- pin). If requires output voltage over 0.8V, inserts resistor divider.

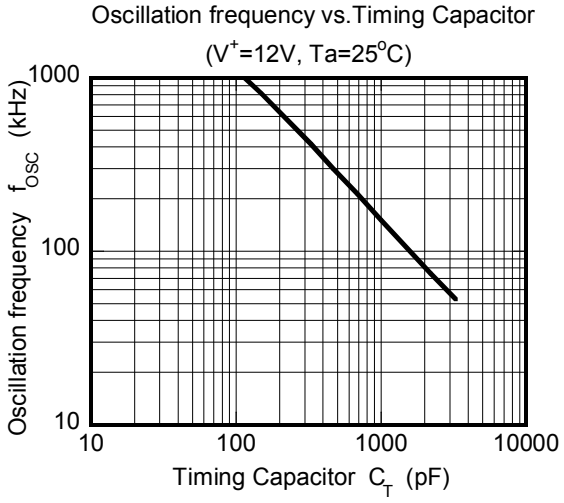
This AMP section has high gain and external feedback pin (FB pin). It is easy to insert a feedback resistor and a capacitor between the FB pin and the IN- pin, making possible to set optimum loop compensation for each type of application.

● Oscillation Circuit Section (OSC)

Oscillation frequency can be set by inserting capacitor between the CT pin and GND. Referring to the sample characteristics in "Timing Capacitor and Oscillation Frequency", set oscillation frequency between 50kHz and 1MHz.

The triangular wave of the oscillating circuit is generated in the IC, having amplitude between 0.4V and 1.0V at C_T=470pF(ref.).

If voltage of the IN- pin becomes less than 0.3V, the oscillation frequency decreases to one third (33%) and the energy consumption is suppressed.



● PWM Comparator Section (PWM)

This section controls the switching duty ratio.

PWM comparator receives the signal of the error amplifier and the triangular wave, and controls the duty ratio between 0% and 100%. The timing chart is shown in Fig.1.

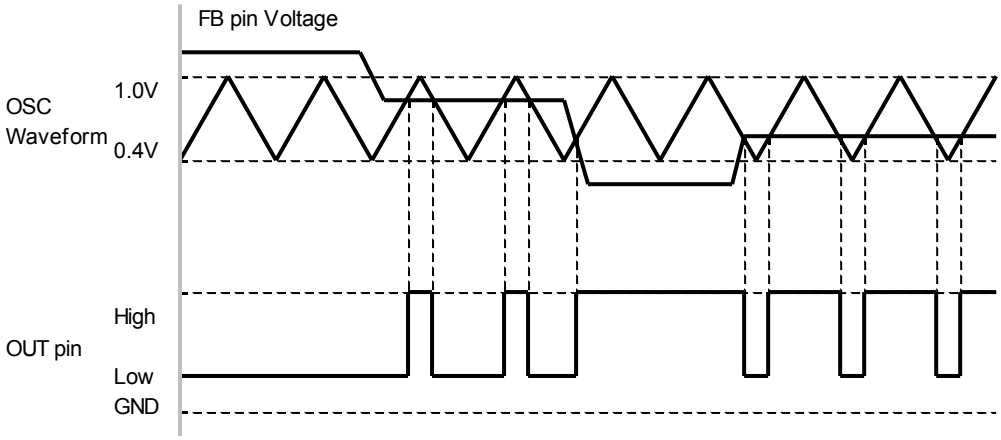


Fig. 1. Timing Chart PWM Comparator and OUT pin

■ Description of Block Features (Continued)

● Driver Section (Driver)

The output driver circuit is configured a totem pole type, it can efficiently drive a Pch MOSFET switching device. When the output is low level, the OUT pin voltage is clamped with V+ -5.35V (typ.) by the internal regulator to protect gate of Pch MOSFET. (Ref. Fig.2. OUT pin)

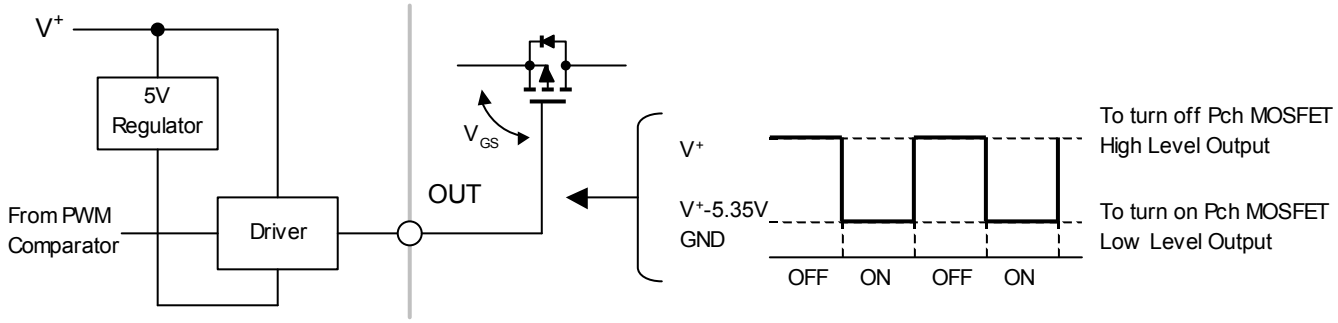


Fig. 2. Driver Circuit and the OUT pin Voltage

When supply voltage is decreasing, gate drive voltage output from the OUT pin is also decreasing. Although the OUT pin voltage is kept gate drive voltage by bypassing the internal regulator around supply voltage 5V. Fig.3. shows the example of the OUT pin voltage vs. supply voltage characteristic

The optimum drive ability of MOSFET depends on the oscillation frequency and the gate capacitance of MOSFET.

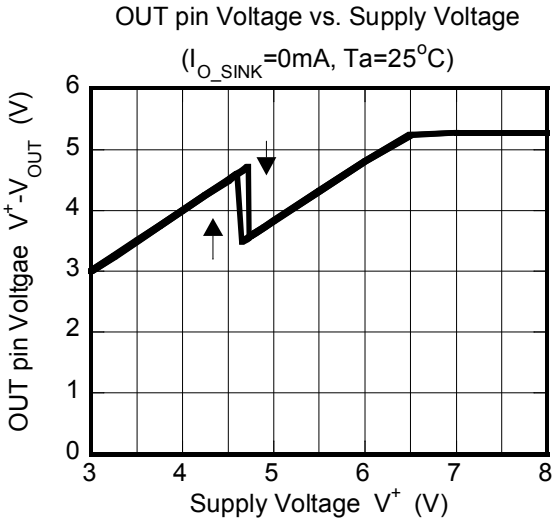


Fig. 3. OUT pin Voltage vs. Supply Voltage Characteristic

■ Description of Block Features (Continued)

● Power Supply, GND pin (V^+, GND)

In line with MOSFET drive, current flows into the IC according to frequency. If the power supply impedance provided to the power supply circuit is high, it will not be possible to take advantage of IC performance due to input voltage fluctuation. Therefore insert a bypass capacitor close to the V^+ pin – the GND pin connection in order to lower high frequency impedance.

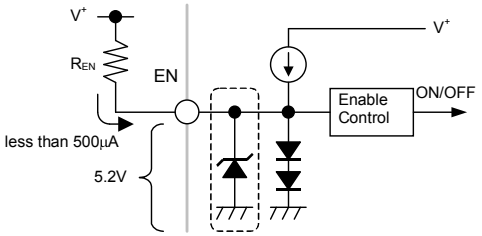
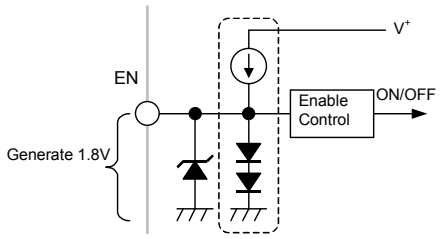
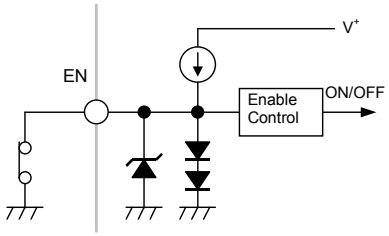
● Under Voltage Lockout Function (UVLO)

The UVLO circuit operating is released above V^+=2.8V(typ.) and IC operation starts. When power supply voltage is low, IC does not operate because the UVLO circuit operates. There is 250mV width hysteresis voltage at rise and decay of power supply voltage. Hysteresis prevents the malfunction at the time of UVLO operating and releasing.

● Enable Function (Enable Control)

With the voltage of the EN pin, the operation of NJW4160 can be set as in Table1.

Table1. EN pin voltage and NJW4160 status

State of NJW4160	Condition of applied voltage to EN pin	Example of connecting EN pin
Normal Mode	1.6V to V_{Z_EN}* *Internal Zener Voltage	The EN pin voltage is clamped to V_{Z_EN}=5.2V (typ.) with the internal Zener diode. You should adjust the flow current into the Zener diode to less than 500μA. 
	The EN pin OPEN	When the EN pin is open, V_{EN_OPEN}=1.8V (typ.) is generated with the internal current source and two diodes. 
Standby Mode	0V to 0.5V	Connect to GND 

■ Description of Block Features (Continued)

● Over Current Protection Circuit

At when the potential difference between the V^+ pin and the SI pin becomes 120mV or more, the over current protection circuit is stopped the switch output. The switching current is detected by inserted current sensing resistor (Rsc) between the V^+ pin and the SI pin. Fig.4. shows the timing chart of the over current protection detection.

The switching output holds low level until next pulse output at OCP operating. The NJW4160 output returns automatically along with release from the over current condition because the OCP is pulse-by-pulse type.

If voltage of the IN- pin becomes less than 0.3V, the oscillation frequency decreases to one third (33%) and the energy consumption is suppressed.

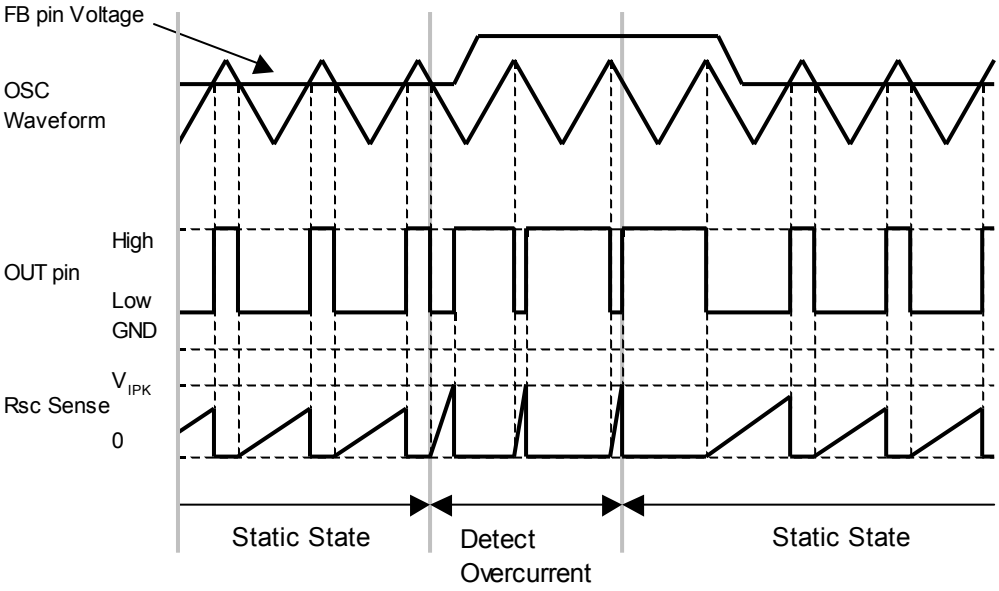


Fig. 4. Timing Chart at Over Current Detection

The current waveform contains high frequency superimposed noises due to the parasitic elements of MOSFET, the inductor and the others. Depending on the application, inserting RC low-pass filter between current sensing resistor (R_{SENSE}) and the SI pin to prevent the malfunction due to such noise. The time constant of RC low-pass filter should be equivalent to the spike width ($T \leq R_{S1} \times C_{S1}$) as a rough guide (Fig. 5).

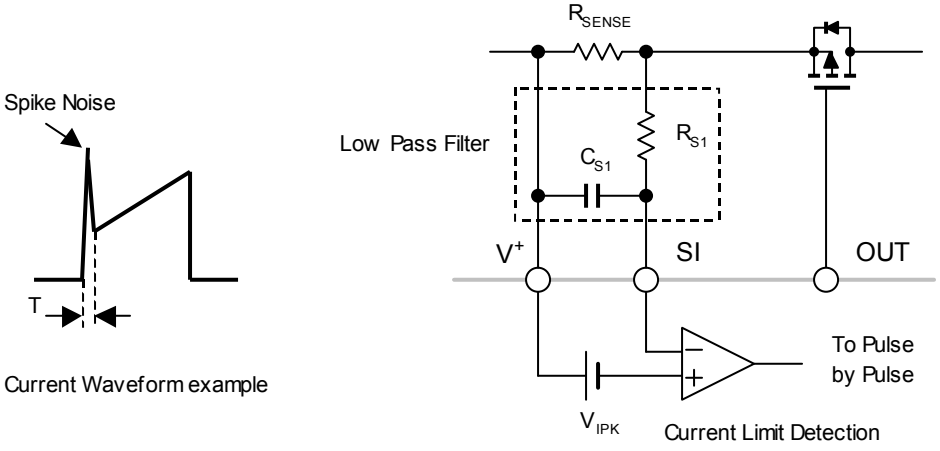


Fig. 5. Current Waveform and Filter Circuit

■ Application Information

● Inductors

Large currents flow into inductor, therefore you must provide current capacity that does not saturate.

Reducing L, the size of the inductor can be smaller. However, peak current increases and adversely affecting efficiency.

On the other hand, increasing L, peak current can be reduced at switching time. Therefore conversion efficiency improves, and output ripple voltage reduces. Above a certain level, increasing inductance windings increases loss (copper loss) due to the resistor element.

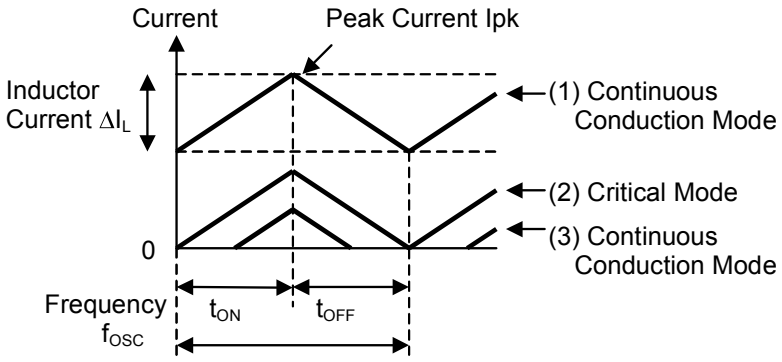


Fig. 6. Inductor Current State Transition

Ideally, the value of L is set so that inductance current is in continuous conduction mode. However, as the load current decreases, the current waveform changes from (1) CCM: Continuous Conduction Mode → (2) Critical Mode → (3) DCM: Discontinuous Conduction Mode (Fig. 6.).

In discontinuous mode, peak current increases with respect to output current, and conversion efficiency tend to decrease. Depending on the situation, increase L to widen the load current area to maintain continuous mode.

● Catch Diode

When the switch element is in OFF cycle, power stored in the inductor flows via the catch diode to the output capacitor. Therefore during each cycle current flows to the diode in response to load current. Because diode's forward saturation voltage and current accumulation cause power loss, a Schottky Barrier Diode (SBD), which has a low forward saturation voltage, is ideal.

An SBD also has a short reverse recovery time. If the reverse recovery time is long, through current flows when the switching transistor transitions from OFF cycle to ON cycle. This current may lower efficiency and affect such factors as noise generation.

● Switching Element

You should use a switching element (Pch MOSFET) that is specified for use as a switch. And select sufficiently low R_{ON} MOSFET at less than V_{GS}=5V because the NJW4160 OUT pin voltage is clamped V^+-5.35V (typ.).

However, when the supply voltage of the NJW4160 is low, the OUT pin voltage becomes low. You should select a suitable MOSFET according to the supply voltage specification. (Ref. Driver section)

Large gate capacitance is a source of decreased efficiency. That is charge and discharge from gate capacitance delays switching rise and fall time, generating switching loss.

The spike noise might occur at the time of charge/discharge of gate by the parasitic inductance element. You should insert resistance between the OUT pin and the gate and limit the current for gate protection when gate capacitance is small. However, it should be noted that the efficiency might decrease because the shape of waves may become duller when resistance is too large. The last fine-tuning should be done on the actual device and equipment.

■ Application Information (Continued)

● Input Capacitor

Transient current flows into the input section of a switching regulator responsive to frequency. If the power supply impedance provided to the power supply circuit is large, it will not be possible to take advantage of the NJW4160 performance due to input voltage fluctuation. Therefore insert an input capacitor as close to the MOSFET as possible.

● Output Capacitor

An output capacitor stores power from the inductor, and stabilizes voltage provided to the output.

When selecting an output capacitor, you must consider Equivalent Series Resistance (ESR) characteristics, ripple current, and breakdown voltage.

Also, the ambient temperature affects capacitors, decreasing capacitance and increasing ESR (at low temperature), and decreasing lifetime (at high temperature). Concerning capacitor rating, it is advisable to allow sufficient margin.

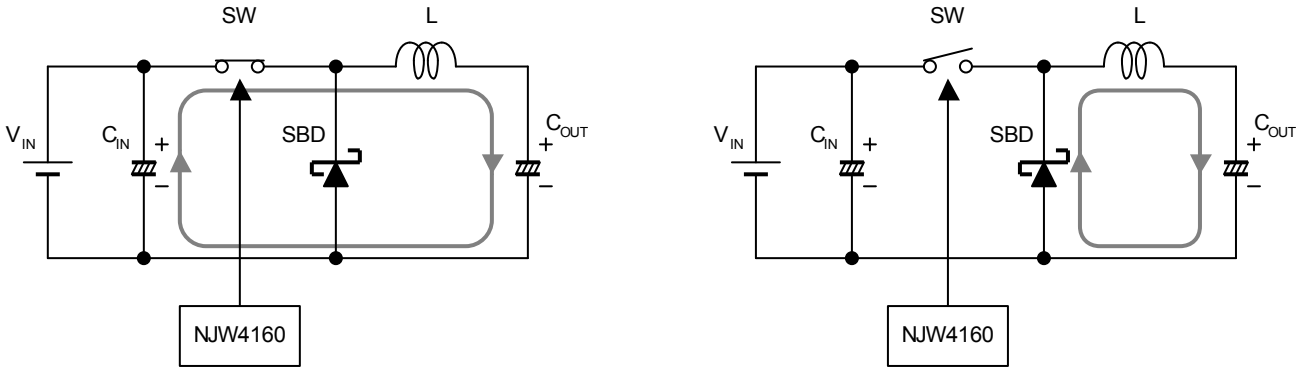
Output capacitor ESR characteristics have a major influence on output ripple noise. A capacitor with low ESR can further reduce ripple voltage. Be sure to note the following points; when ceramic capacitor is used, the capacitance value decreases with DC voltage applied to the capacitor.

■ Application Information (Continued)

● Board Layout

In the switching regulator application, because the current flow corresponds to the oscillation frequency, the substrate (PCB) layout becomes an important.

You should attempt the transition voltage decrease by making a current loop area minimize as much as possible. Therefore, you should make a current flowing line thick and short as much as possible. Fig.7. shows a current loop at step-down converter.



(a) Buck Converter SW ON (b) Buck Converter SW OFF

Fig. 7. Current Loop at Buck Converter

Concerning the GND line, it is preferred to separate the power system and the signal system, and use single ground point.

The voltage sensing feedback line should be as far away as possible from the inductance. Because this line has high impedance, it is laid out to avoid the influence noise caused by flux leaked from the inductance.

Fig. 8. shows example of wiring at buck converter.

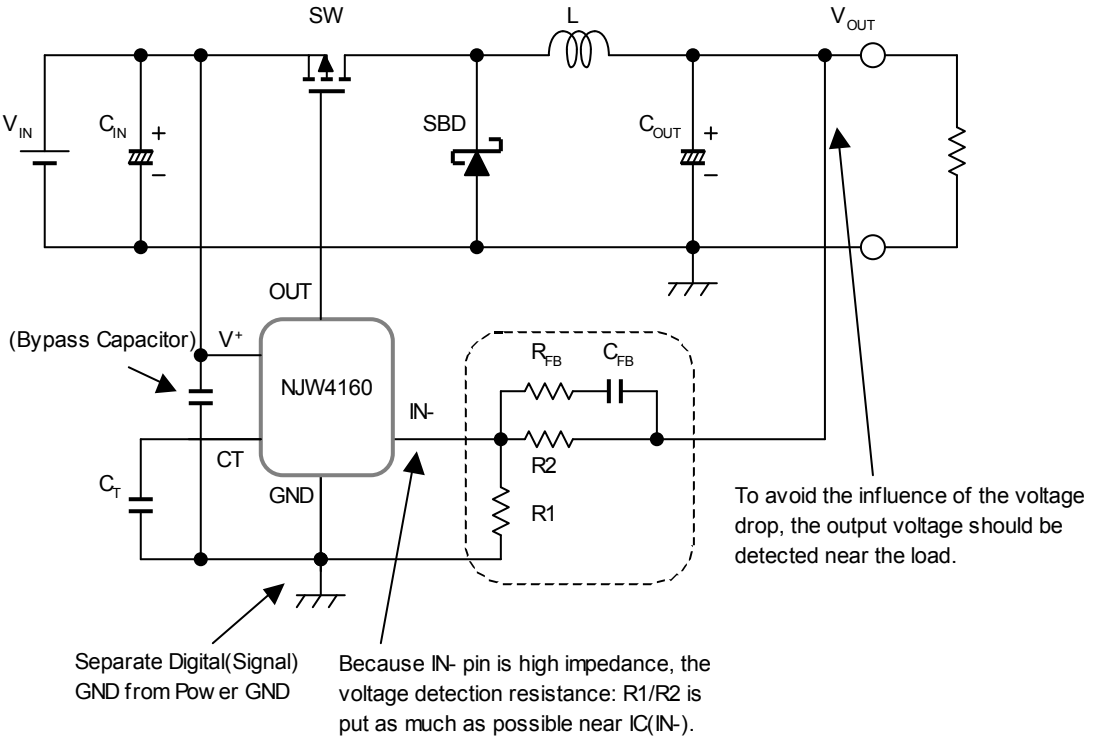


Fig. 8. Board Layout at Buck Converter

■ Calculation of Package Power

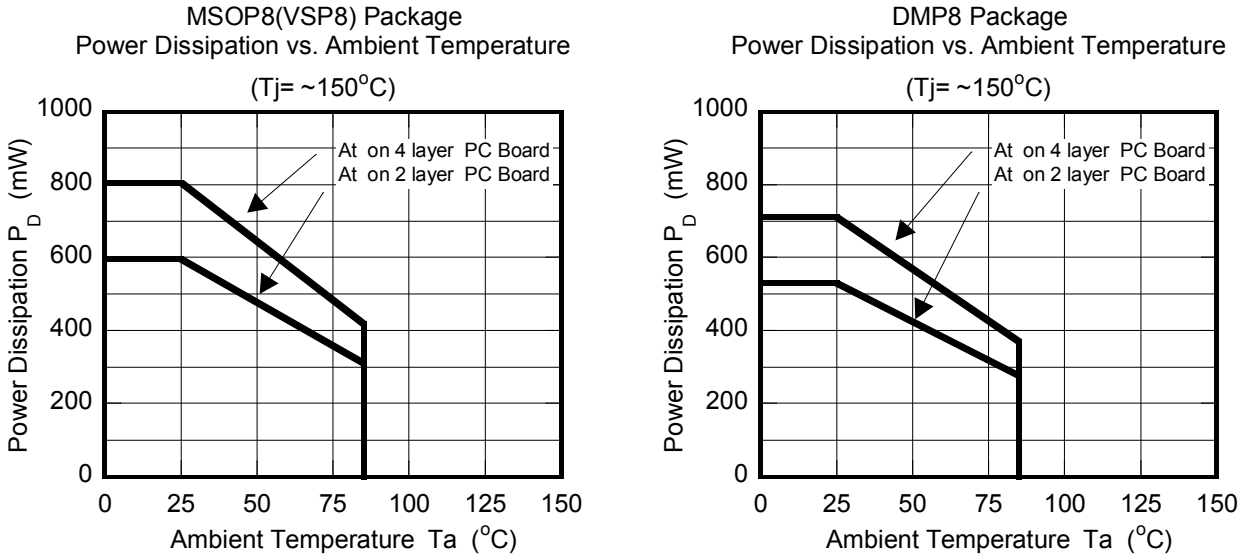
You should consider derating power consumption under using high ambient temperature.
Moreover, you should consider the power consumption that occurs in order to drive the switching element.

Supply Voltage:	V^+
Quiescent Current:	I_{DD}
Oscillation Frequency:	f_{OSC}
ON time:	ton
Gate charge amount:	Qg

The gate of MOSFET has the character of high impedance. The power consumption increases by quickening the switching frequency due to charge and discharge the gate capacitance. Power consumption: P_D is calculated as follows.

$$P_D = (V^+ \times I_{DD}) + (V^+ \times Qg \times f_{OSC}) \text{ [W]}$$

You should consider temperature derating to the calculated power consumption: P_D.
You should design power consumption in rated range referring to the power dissipation vs. ambient temperature characteristics (Fig. 9).



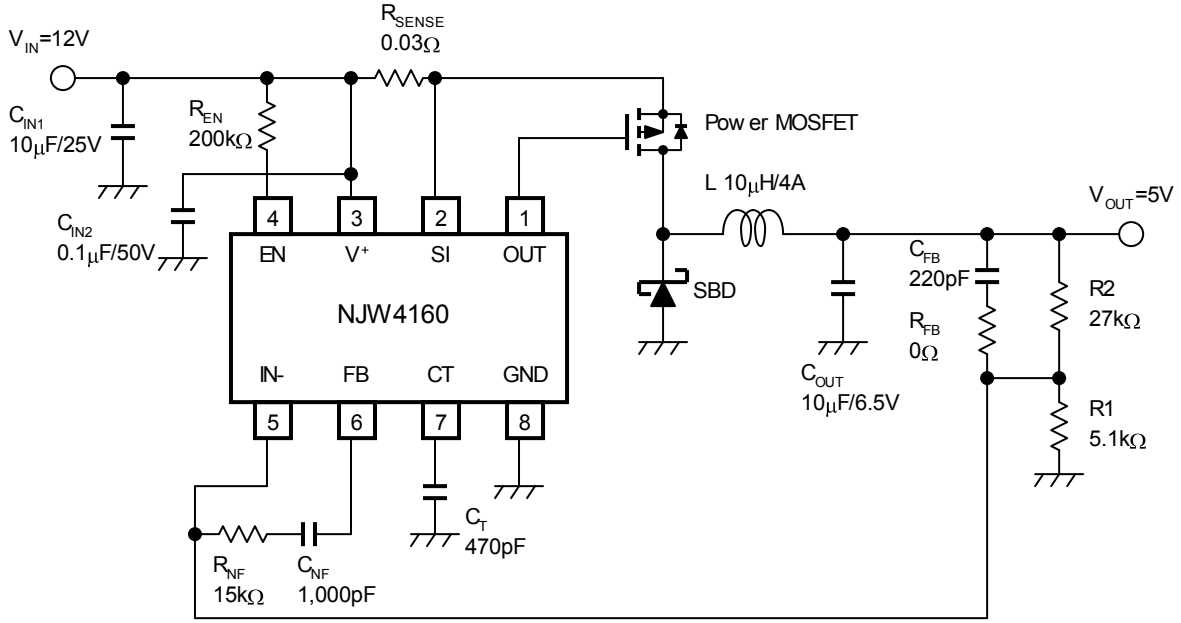
Mounted on glass epoxy board. (76.2×114.3×1.6mm:EIA/JDEC standard size, 2Layers)
Mounted on glass epoxy board. (76.2×114.3×1.6mm:EIA/JDEC standard size, 4Layers),
internal Cu area: 74.2×74.2mm

Fig. 9. Power Dissipation vs. Ambient Temperature Characteristics

■ Application Design Examples

● Step-Down Application Circuit

Input Voltage : V_{IN}=12V
Output Voltage : V_{OUT}=5V
Output Current : I_{OUT}=3A
Oscillation frequency : fosc=300kHz
Output Ripple Voltage : $V_{ripple(P-P)}$=less than 20mV



■ Application Design Examples (Continued)

● Setting Oscillation Frequency

From the Oscillation frequency vs. Timing Capacitor Characteristic, C_T=470 [pF], t=3.33[μs] at fosc=300kHz.

Step-down converter duty ratio is shown with the following equation.

$$Duty = \frac{V_{OUT} + V_F}{V_{IN}} \times 100 = \frac{5 + 0.4}{12} \times 100 = 45\,[\%]$$

Therefore, t_{ON}=1.50 [μs], t_{OFF}=1.83 [μs]

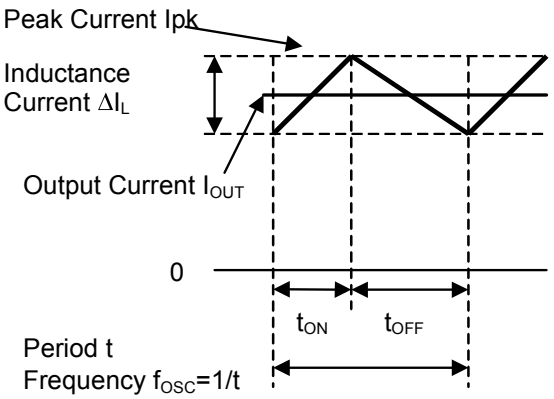


Fig. 10. Inductor Current Waveform

● Selecting Inductance

ΔIL is Inductance ripple current. When to ΔIL= output current 34%:

$\Delta I_L = 0.34 \times I_{OUT} = 0.34 \times 3 = 1.02$ [A]

This obtains inductance L. V_{DS_RON} is drop voltage by MOSFET on resistance.

$$L = \frac{V_{IN} - V_{DS-RON} - V_{OUT}}{\Delta I_L} \times t_{ON} = \frac{12 - 0.2 - 5}{1.02} \times 1.5\mu = 10\,[\mu H]$$

Inductance L is a theoretical value. The optimum value varies according such factors as application specifications and components. Fine-tuning should be done on the actual device.

This obtains the peak current Ipk at switching time.

$$Ipk = I_{OUT} + \frac{\Delta I_L}{2} = 3 + \frac{1.02}{2} = 3.51\,[A]$$

The current that flows into the inductance provides sufficient margin for peak current at switching time.

In the application circuit, use L=10μH/4A.

● Setting Over Current Detection

In this application, current limitation value: I_{LIMIT} is set to Ipk=4A.

$I_{LIMIT} = V_{IPK} / R_{SC}$ = 120mV / 30mΩ =4 [A]

The limit value increases slightly according to response time from the overcurrent detection with the SI pin to the OUT pin stop.

$$I_{LIMIT\_DELAY} = I_{LIMIT} + \frac{V_{IN}}{L} \times T_{DELAY} = 4.0 + \frac{12}{10\mu} \times 100n = 4.12\,[A]$$

■ Application Design Examples (Continued)

● Selecting the Input Capacitor

The input capacitor corresponds to the input of the power supply. It is required to adequately reduce the impedance of the power supply. The input capacitor selection should be determined by the input ripple current and the maximum input voltage of the capacitor rather than its capacitance value.

The effective input current can be expressed by the following formula.

$$I_{RMS} = I_{OUT} \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}} [A]$$

In the above formula, the maximum current is obtained when $V_{IN} = 2 \times V_{OUT}$, and the result in this case is $I_{RMS} = I_{OUT\,(MAX)} \div 2$.

When selecting the input capacitor, carry out an evaluation based on the application, and use a capacitor that has adequate margin.

● Selecting the Output Capacitor

The output capacitor is an important component that determines output ripple noise. Equivalent Series Resistance (ESR), ripple current, and capacitor breakdown voltage are important in determining the output capacitor.

The output ripple noise can be expressed by the following formula.

$$ESR = \frac{V_{ripple(p-p)}}{\Delta I_L}$$

When selecting output capacitance, select a capacitor that allows for sufficient ripple current.
The effective ripple current that flows in a capacitor (I_{rms}) is obtained by the following equation.

$$I_{rms} = \frac{\Delta I_L}{2\sqrt{3}} = \frac{1.02}{2\sqrt{3}} = 294\,[mArms]$$

Consider sufficient margin, and use a capacitor that fulfills the above spec.
In the application circuit, use C_{OUT}=10μF/6.3V,.

● Setting Output Voltage

The output voltage V_{OUT} is determined by the relative resistances of R1, R2. The current that flows in R1, R2 must be a value that can ignore the bias current that flows in ER AMP.

$$V_{OUT} = \left(\frac{R2}{R1} + 1\right) \times V_B = \left(\frac{27k}{5.1k} + 1\right) \times 0.8 = 5.04\,[V]$$

■ Compensation design example

A switching regulator requires a feedback circuit for acquiring a stable output. Because the frequency characteristics of the application change according to the inductance, output capacitor, and so on, the compensation constant should ideally be determined in such a way that the maximum band is acquired while the necessary phase for stable operation is maintained.

These compensation constants play an important role in the adjustment of the NJW4160 when mounted in an actual unit. Finally, select the constants while performing measurement, in consideration of the application specifications.

● Feedback and Stability

Basically, the feedback loop should be designed in such a way that the open loop phase shift at the point where the loop gain is 0 dB is less than -180°. It is also important that the loop characteristics have margin in consideration of ringing and immunity to oscillation during load fluctuations. With the NJW4160, the feedback circuit can be freely designed, enabling the arrangement of the poles and zeros which is important for loop compensation, to be optimized.

The characteristics of the poles and zeros are shown in Fig.11.
Poles: The gain has a slope of -20 dB/dec, and the phase shifts -90°.
Zeros: The gain has a slope of +20 dB/dec, and the phase shift +90°.

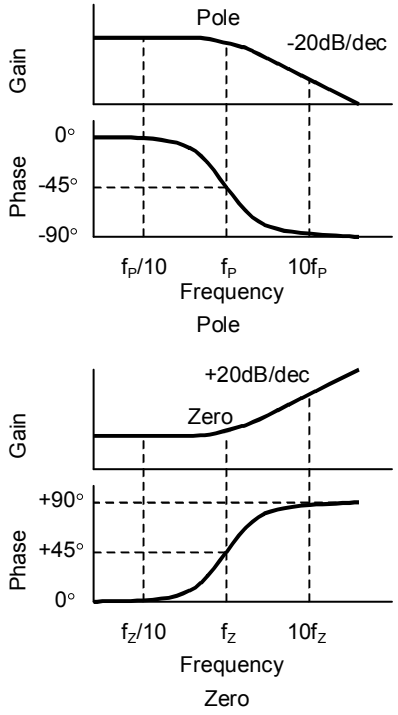


Fig. 11. Characteristics of Pole and Zero

If the number of factors constituting poles is defined as “n”, the change in the gain and phase will be “n”-fold. This also applies to zeros as well. The poles and zeros are in a reciprocal relationship, so if there is one factor for each pole and zero, they will cancel each other.

● Configuration of the compensation circuit

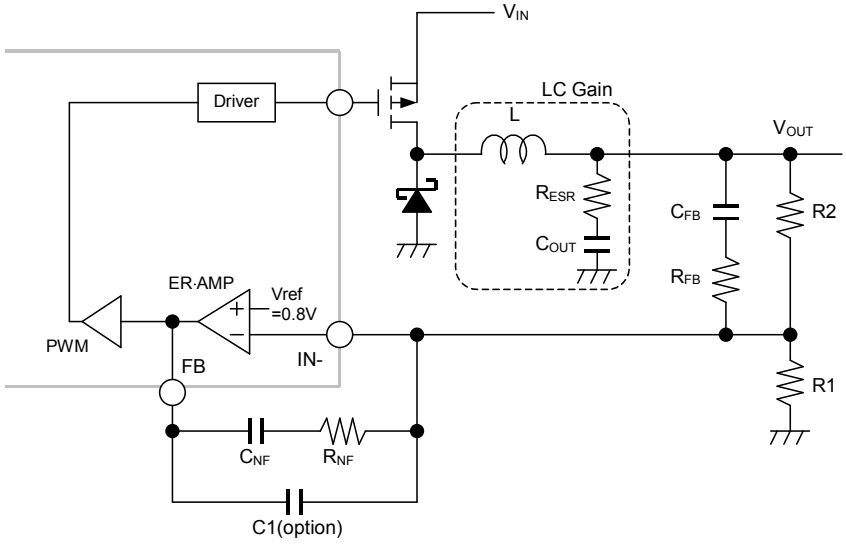


Fig. 12. Compensation Circuit Configuration

■ Compensation Design (Continued)

● Poles and zeros due to the inductance and output capacitor

Double poles $f_{P(LC)}$ are generated by the inductance and output capacitor. Simultaneously, single zeros $f_{Z(ESR)}$ are generated by the output capacitor and ESR. Each pole and zero is expressed by the following formula.

$$f_{Z(ESR)} = \frac{1}{2\pi C_{OUT} R_{ESR}} \qquad f_{P(LC)} = \frac{1}{2\pi\sqrt{LC_{OUT}}}$$

If the ESR of the output capacitor is high, $f_{Z(ESR)}$ will be located in the vicinity of $f_{P(LC)}$. In an application such as this, the zero $f_{Z(ESR)}$ compensates the double poles $f_{P(LC)}$, resulting in a tendency for stability to be readily maintained.

However, if the ESR of the output capacitor is low, $f_{Z(ESR)}$ shifts to the high region, and the phase is shifted -180° by $f_{P(LC)}$.The NJW4160 compensation circuit enables compensation to be realized by using zeros f_{Z1} and f_{Z2}.

● Poles and zeros due to error amplifier

The single poles and zeros generated by the error amplifier are obtained using the following formula.

Zero	Pole
$f_{Z1} = \frac{1}{2\pi C_{NF} R_{NF}}$	$f_{P1} = \frac{1}{2\pi C_{NF} A_V \left(\frac{R1 R2}{R1 + R2} \right)}$ (Av: Amplifier Open Loop Gain=80dB)
$f_{Z2} = \frac{1}{2\pi C_{FB} R2}$	$f_{P2} = \frac{1}{2\pi C_{FB} \left(R_{FB} + \frac{R1 R2}{R1 + R2} \right)}$
	$f_{P3} = \frac{1}{2\pi C1 R_{NF}}$ (Option)

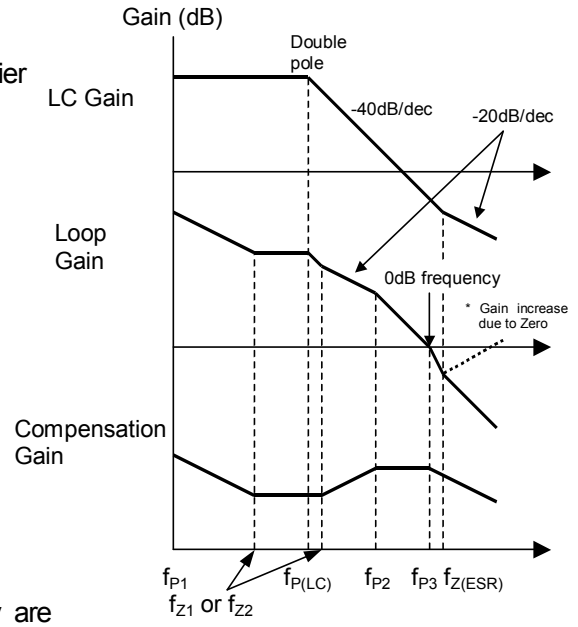


Fig. 13. Loop Gain examples

f_{Z1} and f_{Z2} are located on both sides of $f_{P(LC)}$.

Because the inductance and output capacitor vary, they are each set using the following as a rough guide.

$f_{P(LC)} \times$ 0.5-fold – 0.9-fold

$f_{P(LC)} \times$ 1.1-fold – 2.0-fold

There is also a method in which f_{Z1} and f_{Z2} are located at positions lower than even $f_{P(LC)}$. Because there is a tendency for the phase shift to increase and the gain to rise, it can be expected that the response will improve.

However, there is a tendency for the phase margin to become insufficient, so care is necessary.

f_{P1} creates poles in the low frequency region due to the Miller effect of the error amplifier. The stability becomes better as f_{P1} becomes lower. On the other hand, the frequency characteristics do not improve, so the response is adversely affected. f_{P1} is set using a frequency gain of 20 dB for $f_{P(LC)}$ as a rough guide.

If the open loop gain of the error amplifier is made 80 dB, design is carried out using $f_{P1} < f_{P(LC)} \div 10^3$ (= 60 dB) as a rough guide.

Above several 100 kHz, various poles are generated, so the upper limit of the frequency range where the loop gain is 0 dB is set to fifth (1/5) to tenth (1/10) of oscillation frequency. The $f_{Z(ESR)}$ in the high frequency region sometimes causes a loop gain to be generated (See Fig.13 Loop Gain “). Using f_{P2} and f_{P3}, perform adjustment with the NJW4160 mounted in an actual unit, so as to adequately reduce the loop gain in the high frequency region.

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