MOSFET Drive Switching Regulator IC for Boost / Fly-back Converter

■ FEATURES

- Current Mode Control
- Wide Operating Voltage Range 2.5 to 40V
- Nch MOFET Drive Voltage 10V typ.
- Oscillating Frequency 50kHz to 1MHz
- External Clock Synchronization
- PWM Control
- Soft Start Fixed 20ms typ.
- Adjustable Startup Voltage
- Over Voltage Protection
- Over Current Protection (Hiccup)
- UVLO (Undervoltage Lockout)
- Thermal Shutdown
- Standby Function
- Package MSOP10 (VSP10)*

*Meet JEDEC MO-187-DA

■ GENERAL DESCRIPTION

The NJW4142 is a MOSFET drive switching regulator IC for boost / fly-back converters that operates wide operating voltage range from 2.5V to 40V.

The internal Nch MOSFET driver circuit provides high efficiency driving, makes this device ideal for high output current applications.

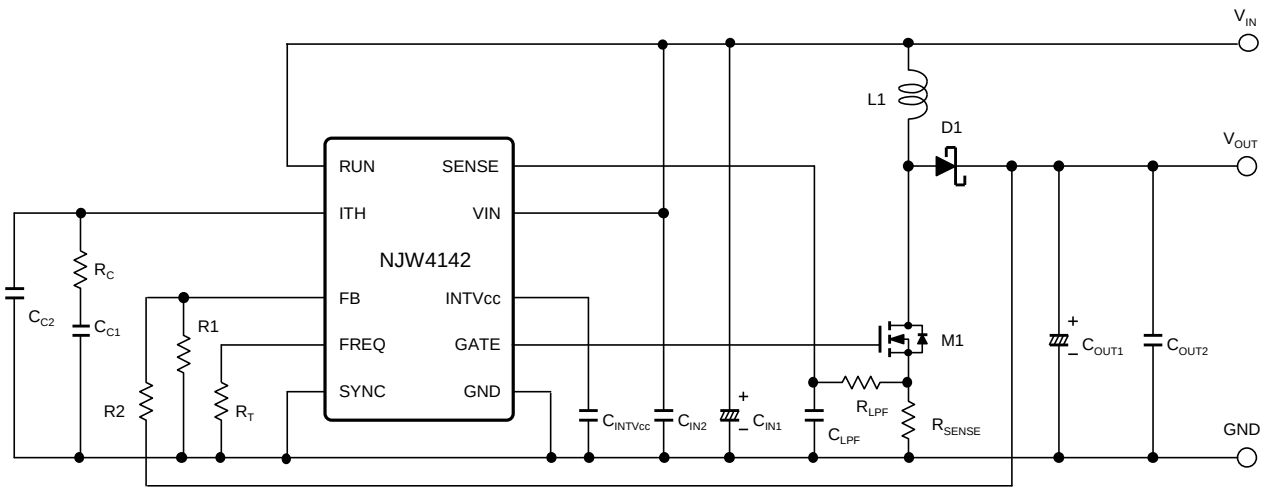
The protection function is equipped pulse-by-pulse overcurrent detection to limits the switching current at overload.

The NJW4142 is suitable for boost / fly-back applications such as industrial instruments and so on.

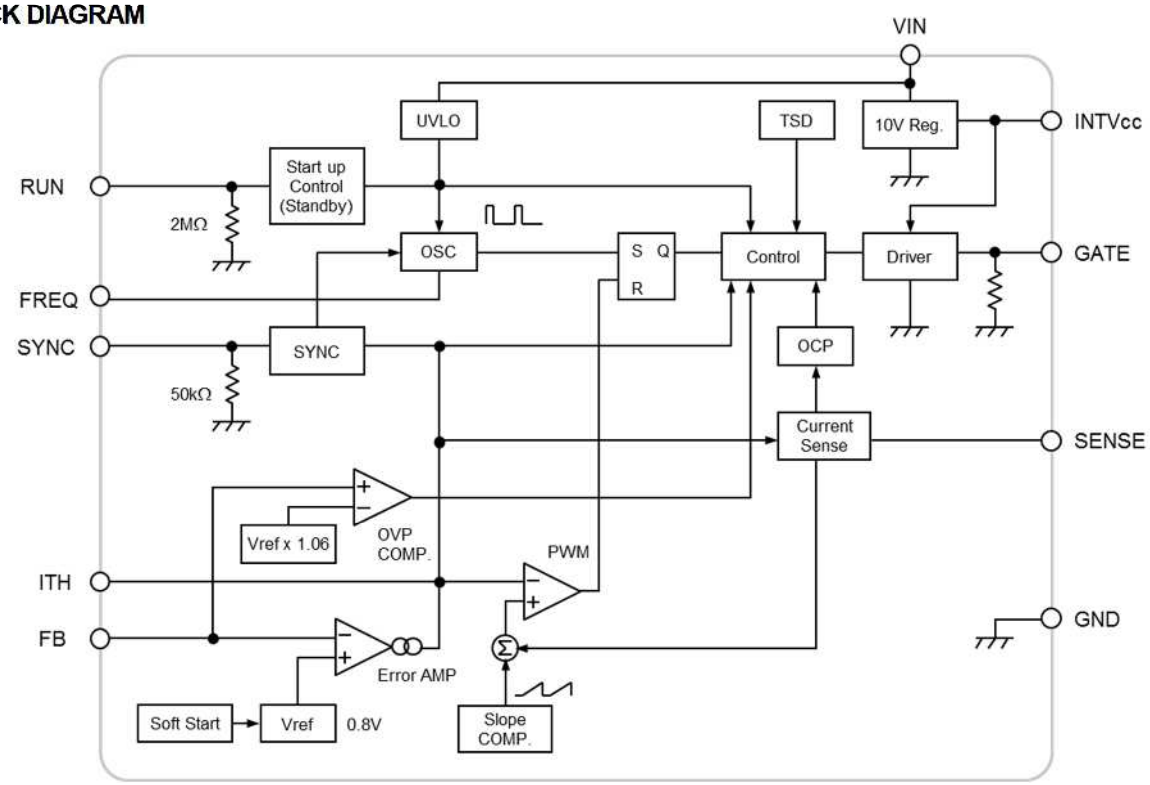
■ APPLICATION

- Consumer Electronics
- Industrial Instruments
- Boost Converter for Small to Middle Range Power Supplies

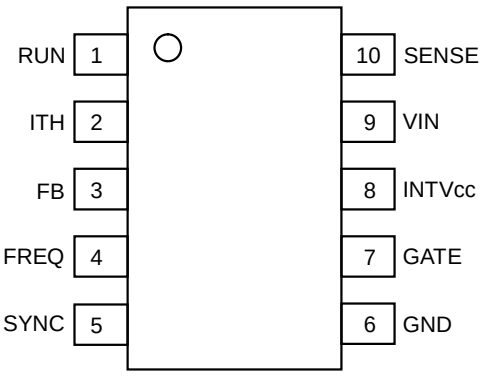
■ TYPICAL APPLICATION



■ BLOCK DIAGRAM



■ PIN CONFIGURATION



PIN No.	SYMBOL	DESCRIPTION
1	RUN	Start up control
2	ITH	Error amplifier output
3	FB	Voltage feedback input
4	FREQ	Oscillating frequency setting
5	SYNC	External CLK input
6	GND	Ground
7	GATE	Gate drive output
8	INTVcc	Capacitor connection pin for built-in regulator
9	VIN	Power supply input
10	SENSE	Current sense input

■ PRODUCT NAME INFORMATION

NJW4142 R (TE1)

- NJW4142: Part Number
- R: Package (R: MSOP)
- (TE1): Taping Form

■ ORDERING INFORMATION

PRODUCT NAME	PACKAGE OUTLINE	RoHS	HALOGEN-FREE	TERMINAL FINISH	MARKING	WEIGHT (mg)	MOQ (pcs)
NJW4142R (TE1)	MSOP10	yes	yes	Sn2Bi	4142	21	2000

■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{IN}	-0.3 to +45	V
INTVcc Pin Voltage	V_{INTVcc}	-0.3 to +11(1)	V
INTVcc Pin Output Current	I_{INTVcc}	50	mA
GATE Pin Voltage	V_{GATE}	-0.3 to V_{INTVcc}+0.3	V
GATE Pin Peak Current	I_{GATE_PEAK+} I_{GATE_PEAK-}	4400 (Source) 4200 (Sink)	mA
FB Pin Voltage	V_{FB}	-0.3 to +6	V
RUN Pin Voltage	V_{RUN}	-0.3 to +45	V
SYNC Pin Voltage	V_{SYNC}	-0.3 to +6	V
SENSE Pin Voltage	V_{SENSE}	-0.3 to +45	V
Power Dissipation (Ta=25°C) MSOP10	P_D	560(2) 780(3)	mW
Junction Temperature	T_j	-40 to +150	°C
Operating Temperature	T_{opr}	-40 to +125	°C
Storage Temperature	T_{stg}	-50 to +150	°C

(1): When supply voltage is less than +11V, the absolute maximum INTVcc pin voltage is same to the supply voltage.

(2): Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JEDEC standard, 2Layers)

(3): Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JEDEC standard, 4Layers, internal Cu Area:74.2×74.2mm)

■ RECOMMENDED OPERATING CONDITION

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{IN}	2.5 to 40	V
Timing Resistor	R_T	1.69 to 39	kΩ
Operating Frequency	f_{OSC}	50 to 1000	kHz
External Clock Input Range	f_{SYNC}	f_{OSC} × 0.9 to f_{OSC} × 1.7	kHz
INTVcc Capacitor	C_{INTVcc}	0.01 to 1 (0.1μF typ.)	μF

■ **ELECTRICAL CHARACTERISTICS** (V_{IN}=V_{INTVcc}=5V, V_{RUN}=1.5V, V_{SENSE}=0V, V_{SYNC}=0V, R_T=6.2kΩ, Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
General Characteristics						
Quiescent Current	I_Q	V_{IN}=12V, V_{FB}=0.9V	–	0.9	1.7	mA
Standby Current	I_{Q_STBY}	V_{RUN}=0V	–	10	20	μA
Under Voltage Lockout Block						
ON Threshold Voltage	V_{T_ON}	V_{IN}=L → H	2.3	2.4	2.5	V
OFF Threshold Voltage	V_{T_OFF}	V_{IN}=H → L	2.1	2.2	2.3	V
Hysteresis Voltage	V_{HYS}		150	200	–	mV
RUN Control Block						
ON Threshold Voltage	V_{RUN+}	V_{RUN}=L → H	1.298	1.348	1.398	V
OFF Threshold Voltage	V_{RUN-}	V_{RUN}=H → L	1.198	1.248	1.298	V
Hysteresis Voltage	V_{RUN_HYS}		50	100	150	mV
Input Bias Current	I_{RUN}		–	1	2	μA
Error Amplifier Block						
Reference Voltage	V_{FB}		-1.0%	0.8	+1.0%	V
Input Bias Current	I_{FB}		-0.1	–	0.1	μA
Over Voltage Lockout	ΔV_{FB_OV}	V_{FB_OV} –V_{FB} in percent	2.5	6	10	%
Transconductance	gm	I_{TH}=±5μA	–	650	–	μmho
Soft Start Block						
Soft Start Time	t_{SS}	V_{FB}=0.75V	10	20	30	ms
Current Sense Block						
Current Sense Threshold Voltage	V_{SENSE}		-8%	150	+8%	mV
Low Level Input Current	I_{SENSE_L}	V_{SENSE}=0V	–	2	4	μA
High Level Input Current	I_{SENSE_H}	V_{SENSE}=30V	–	0.1	5	μA
COOL DOWN Time	t_{COOL}		–	60	–	ms
Oscillator Block						
Oscillating Frequency	f_{OSC}	R_T=6.2kΩ	270	300	330	kHz
PWM Comparator Block						
Maximum Duty Cycle	D_{MAX}	V_{FB}=0.7V, V_{ITH}=OPEN	87	92	97	%
Minimum ON Time	t_{ON_min}		–	70	120	ns

■ **ELECTRICAL CHARACTERISTICS** (V_{IN}=V_{INTVcc}=5V, V_{RUN}=1.5V, V_{SENSE}=0V, V_{SYNC}=0V, R_T=6.2kΩ, Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
SYNC Control Block						
Minimum Input Pulse Width	t_{SYNC_MIN}	V_{SYNC}=0V→5V	–	25	–	ns
Maximum Input Pulse Width	t_{SYNC_MAX}	V_{SYNC}=0V→5V	–	0.8/f_{OSC}	–	ns
Low Level Input Voltage	V_{IL_SYNC}		0	–	0.5	V
High Level Input Voltage	V_{IH_SYNC}		1.2	–	5.5	V
Pull Down Resistance	R_{SYNC}		-30%	50	+30%	kΩ
LDO Block						
Output Voltage	V_{INTVcc}	V_{IN}=12V	9	10	11	V
Dropout Voltage	$V_{DROPOUT}$	V_{IN}=8.5V, I_{INTVcc}=20mA	200	300	400	mV
Bootstrap Mode INTVcc Quiescent Current	I_{INTVcc}	V_{RUN}=0V, V_{SENSE}=5V	–	10	20	μA
Gate Driver Block						
High Side ON Resistance	R_{GATEH}	I_{GATE}=50mA(Source)	–	1.5	3.0	Ω
Low Side ON Resistance	R_{GATEL}	I_{GATE}=50mA(Sink)	–	1.1	2.5	Ω
Pull Down Resistance	$R_{PD\text{-}GATE}$		–	500	–	kΩ

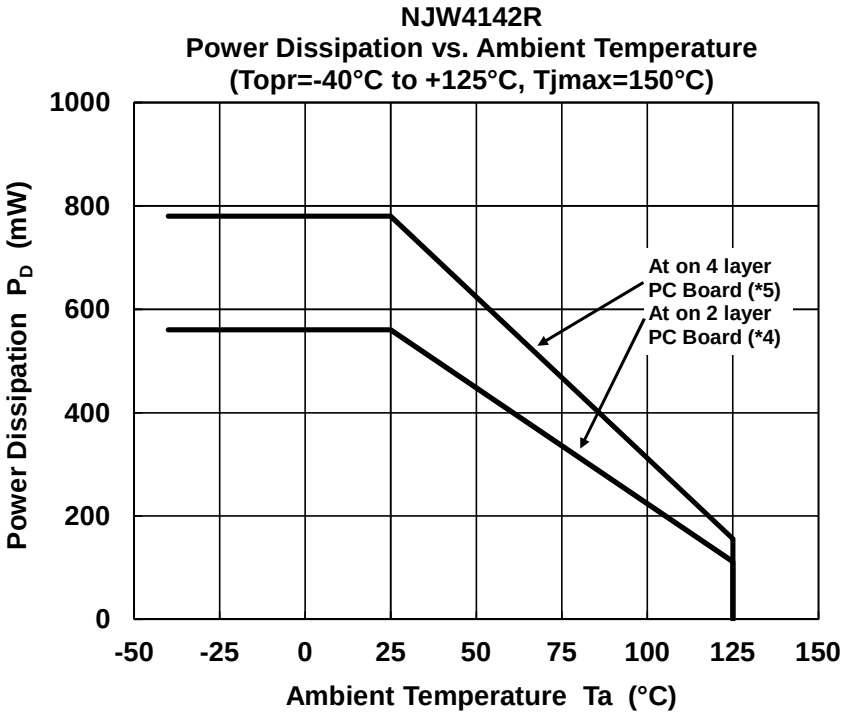
■ THERMAL CHARACTERISTICS

PARAMETER	SYMBOL	VALUE	UNIT
Junction to ambient thermal resistance	θja	224(4) 159(5)	°C/W
Junction to top of package characterization parameter	ψjt	40(4) 31(5)	°C/W

(4): Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JEDEC standard, 2Layers)

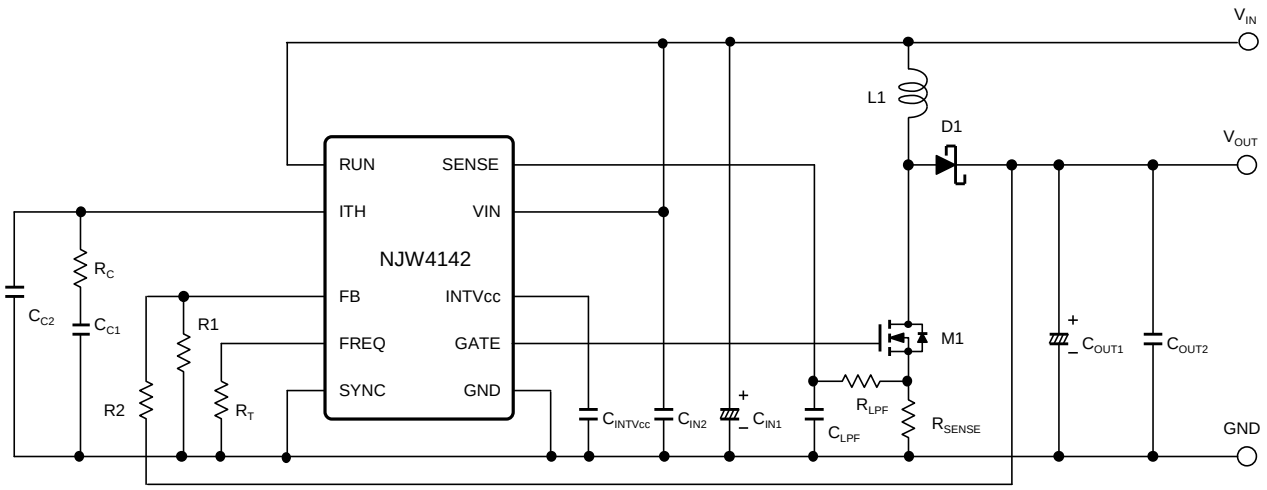
(5): Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JEDEC standard, 4Layers, internal Cu Area:74.2×74.2mm)

■ POWER DISSIPATION vs. AMBIENT TEMPERATURE

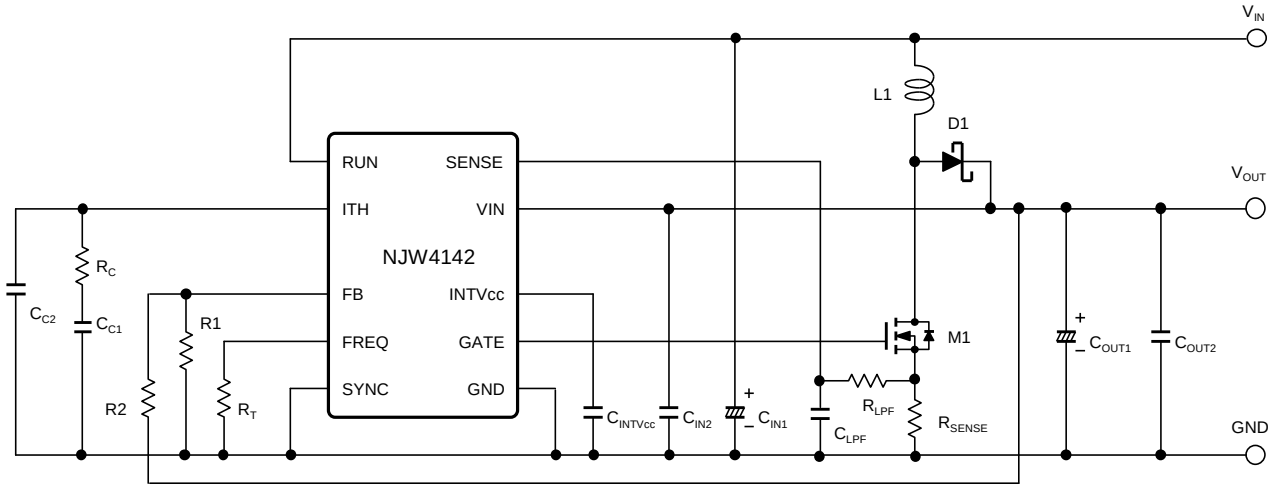


■ TYPICAL APPLICATION

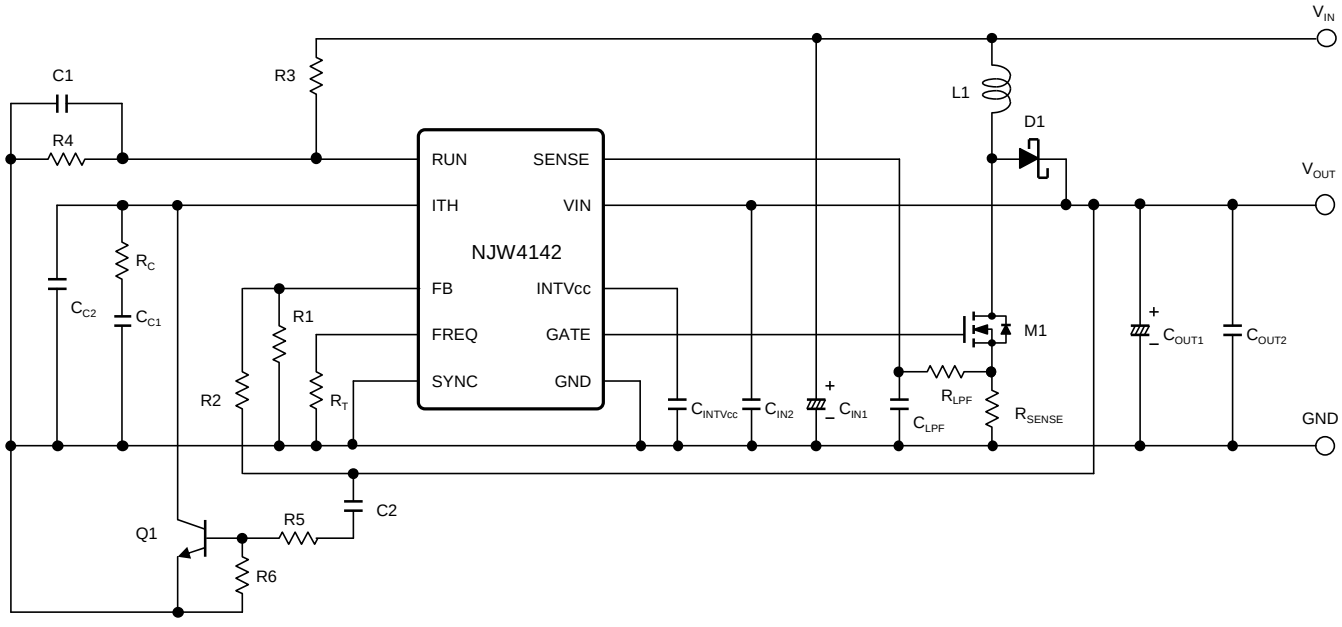
Typical Boost Converter



Power supply from the output voltage to the IC

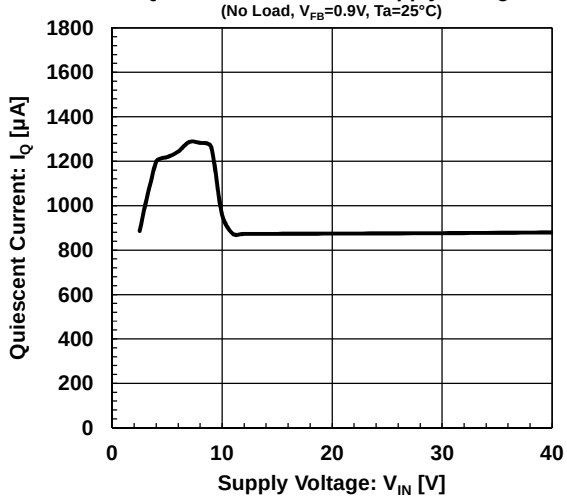


Adjustable start-up voltage and soft-start circuit

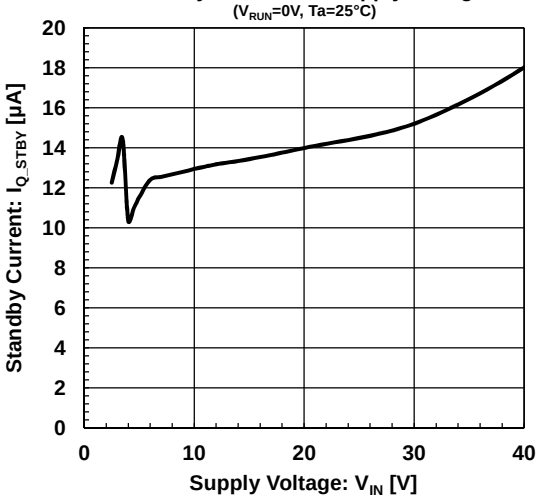


■ TYPICAL CHARACTERISTICS

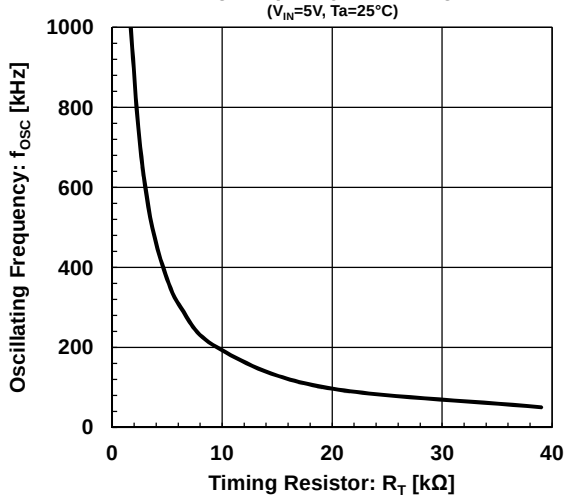
Quiescent Current vs. Supply Voltage
(No Load, V_{FB}=0.9V, Ta=25°C)



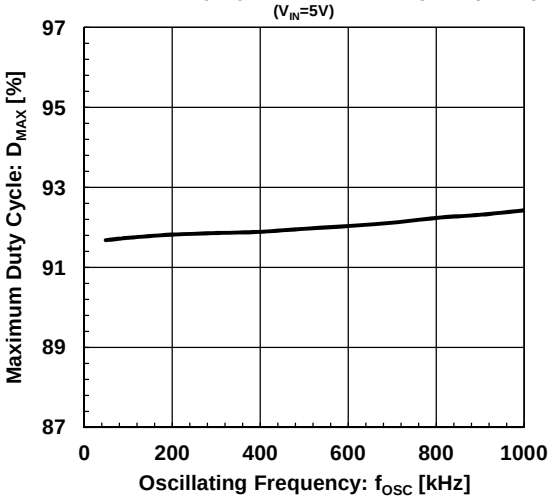
Standby Current vs. Supply Voltage
(V_{RUN}=0V, Ta=25°C)



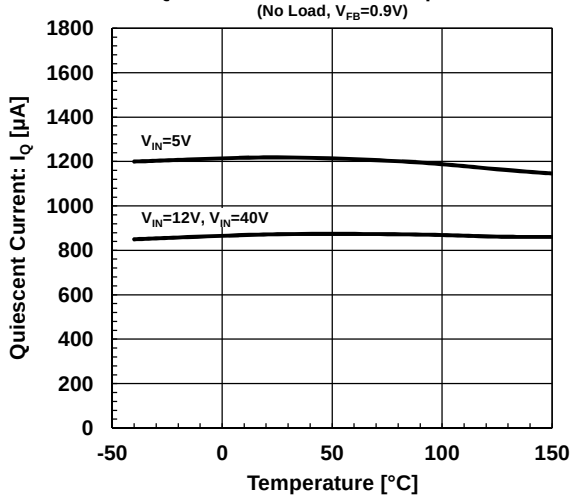
Oscillating Frequency vs. Timing Resistor
(V_{IN}=5V, Ta=25°C)



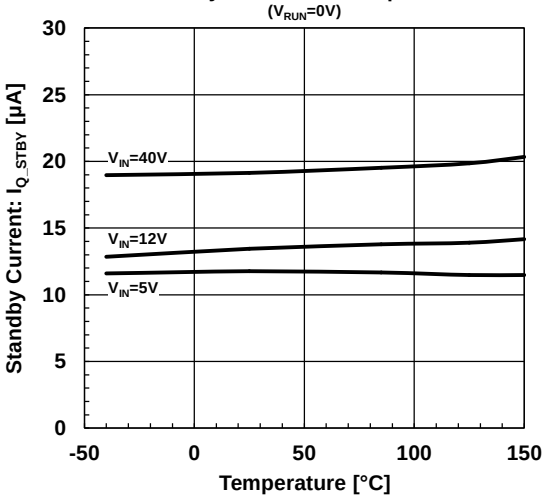
Maximum Duty Cycle vs. Oscillating Frequency
(V_{IN}=5V)



Quiescent Current vs. Temperature
(No Load, V_{FB}=0.9V)

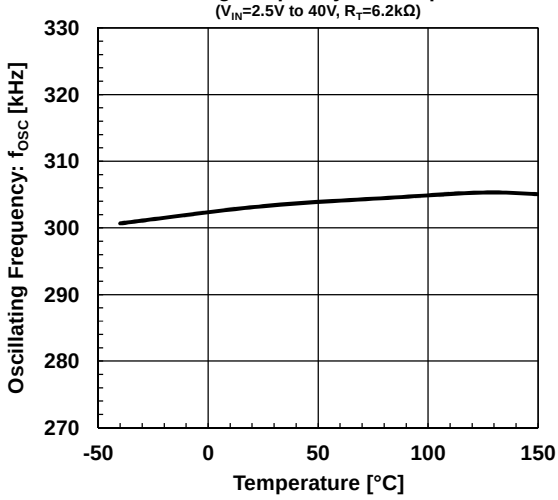


Standby Current vs. Temperature
(V_{RUN}=0V)

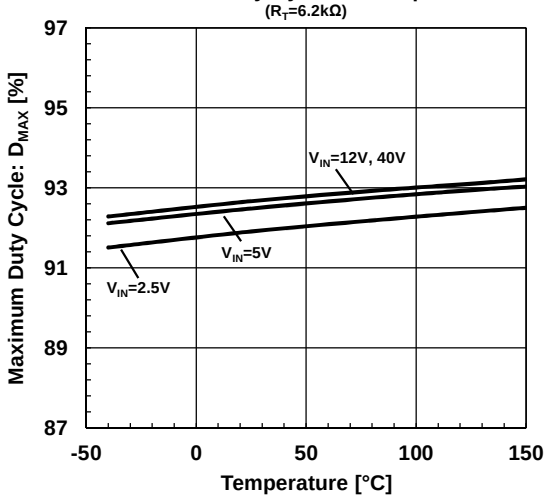


■ TYPICAL CHARACTERISTICS

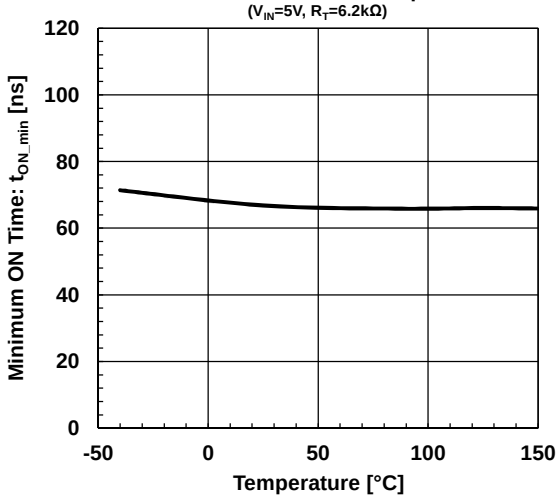
Oscillating Frequency vs. Temperature
(V_{IN}=2.5V to 40V, R_T=6.2kΩ)



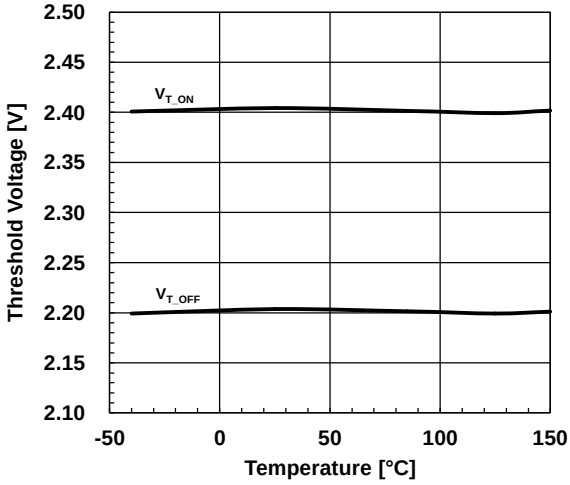
Maximum Duty Cycle vs. Temperature
(R_T=6.2kΩ)



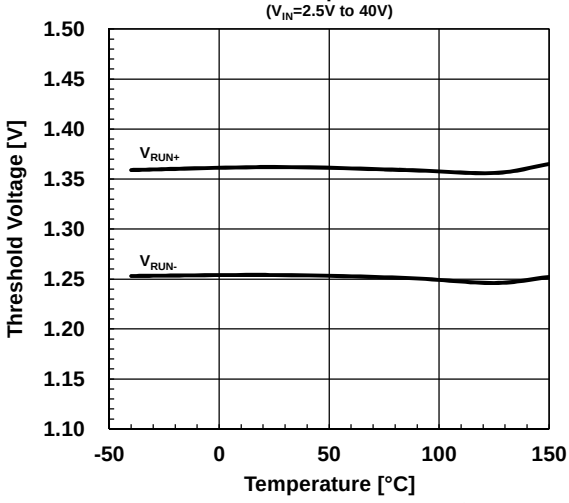
Minimum ON Time vs. Temperature
(V_{IN}=5V, R_T=6.2kΩ)



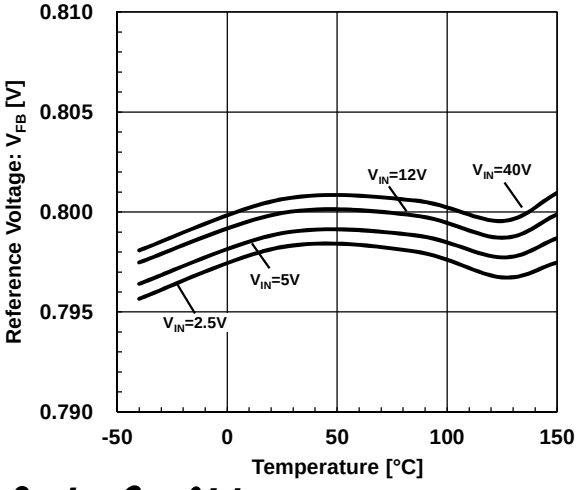
Under Voltage Lockout Voltage vs. Temperature



RUN pin ON/OFF Threshold Voltage vs. Temperature
(V_{IN}=2.5V to 40V)

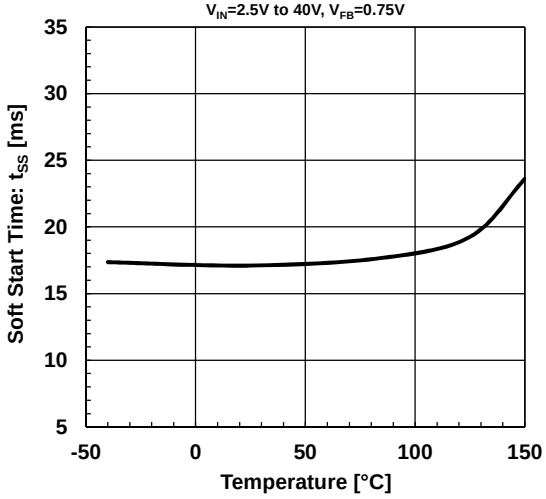


Reference Voltage vs. Temperature

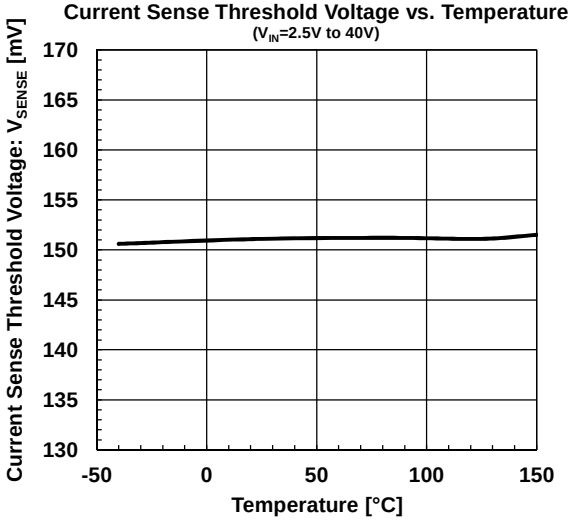


■ TYPICAL CHARACTERISTICS

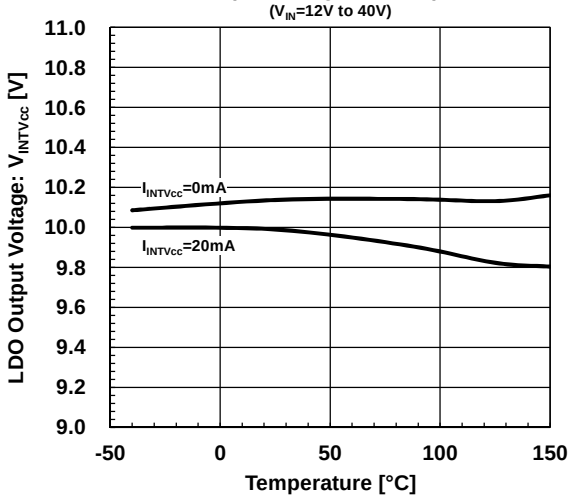
Soft Start Time vs. Temperature
(V_{IN}=2.5V to 40V, V_{FB}=0.75V)



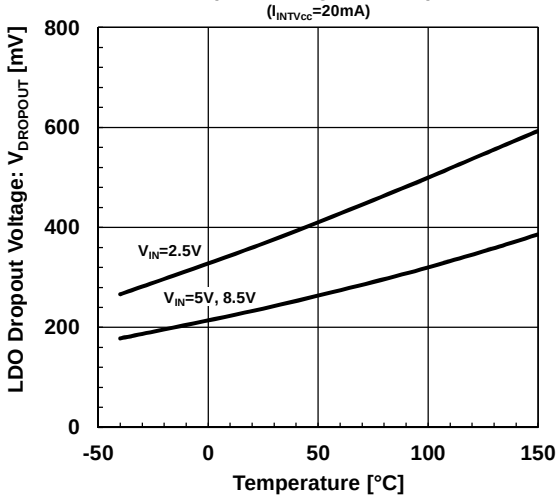
Current Sense Threshold Voltage vs. Temperature
(V_{IN}=2.5V to 40V)



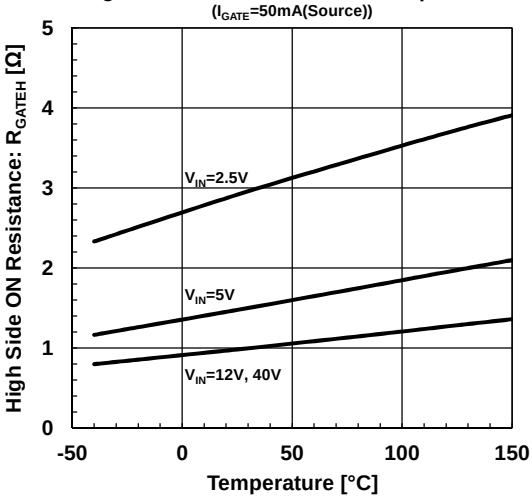
LDO Output Voltage vs. Temperature
(V_{IN}=12V to 40V)



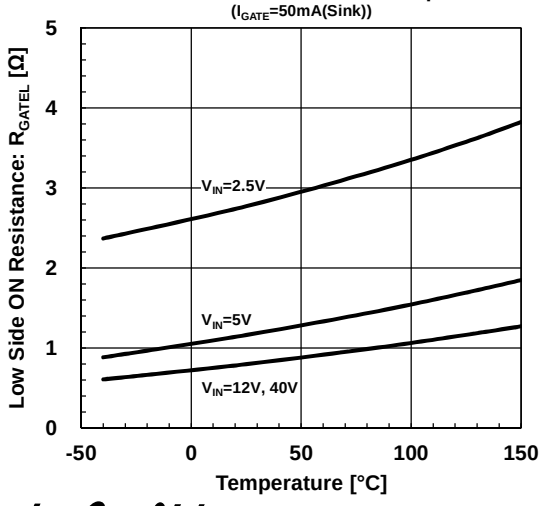
LDO Dropout Voltage vs. Temperature
(I_{INTVcc}=20mA)



High Side ON Resistance vs. Temperature
(I_{GATE}=50mA(Source))

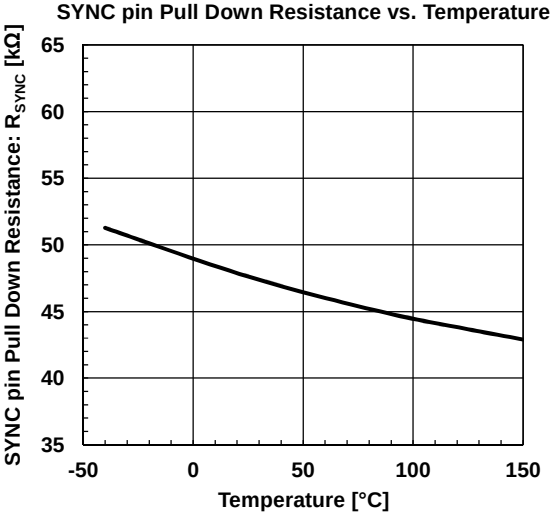


Low Side ON Resistance vs. Temperature
(I_{GATE}=50mA(Sink))

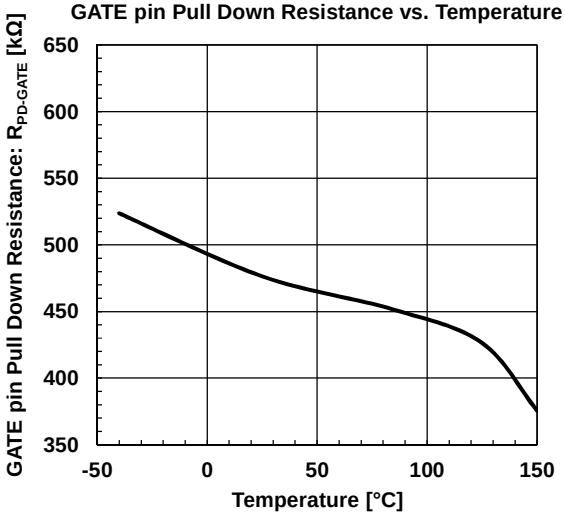


■ TYPICAL CHARACTERISTICS

SYNC pin Pull Down Resistance vs. Temperature



GATE pin Pull Down Resistance vs. Temperature



■ **PIN DISCRIPTION**

PIN NO.	PIN NAME	FUNCTION
1	RUN	ON/OFF control pin H level input : normal operation L level input or OPEN : standby In addition, it is possible to set the startup voltage by dividing and inputting from the power supply line.
2	ITH	Error amplifier output pin. The capacitor and resistor for phase compensation should be connected between ITH pin and GND pin.
3	FB	This pin detects the output voltage. The output voltage is divided and input so that the FB pin voltage becomes 0.8V typ.
4	FREQ	Oscillation frequency setting pin to connect the timing resistor. Set the oscillation frequency between 50kHz and 1MHz.
5	SYNC	When a clock signal is input from the outside, it operates at an oscillation frequency synchronized with this clock signal.
6	GND	Ground pin
7	GATE	Output pin for Power MOSFET driving
8	INTVcc	Internal 10V regulator output pin. The capacitor of 0.01µF to 1µF should be connected between INTVcc pin and GND pin.
9	VIN	Power supply input pin. Insert a bypass capacitor close to VIN pin - GND pin in order to lower the power supply line impedance.
10	SENSE	Current sensing pin. When difference voltage between SENSE pin and GND pin exceeds 150mV typ., the over current protection operates.

■ FUNCTION DESCRIPTION

1. Basic Function

- Error Amplifier Section (Error AMP)

0.8V±1% high precision reference voltage is connected to non-inverted input of this section.
The output voltage can be set by connection of converter's output to inverted input of this section (FB pin).

- Oscillating Circuit Section (OSC), PWM Comparator Section (PWM)

Oscillating frequency can be set by inserting resistor between the RT pin and GND.
Table1 shows example of oscillating frequency and timing resistor.
The resistor can be selected from E24 series or E96 series.
Also refer to the electrical characteristics in “Oscillating Frequency vs. Timing Resistor”, and set oscillation between 50kHz and 1MHz.

Table 1. NJW4142 oscillating frequency and timing resistor

Oscillating Frequency (kHz)	Timing Resistor (kΩ)	Oscillating Frequency (kHz)	Timing Resistor (kΩ)
50	39	600	3
100	19.1	700	2.55
200	9.53	800	2.21
300	6.2	900	1.96
400	4.7	1000	1.69
500	3.65		

When the switching regulator operates at high oscillating frequency, the application can use a small inductor and capacitor. If oscillating frequency is high, consider subject to efficiency reduction of the application and a restriction by minimum ON time. Since the minimum ON time of NJW4142 designed 70ns typ., it needs to select the oscillation frequency at which the ON time of the boost application become over 70ns.
The ON time of boost converter is calculated the following formula.

$$t_{ON}=\frac{V_{OUT}-V_{IN}}{V_{OUT}\times f_{OSC}}\,[s]$$

When the ON time of boost application becomes below in 70ns typ., it may be occurred duty fluctuation and pulse skipping in order to maintain output voltage at a stable state.

• Driver Circuit、10V Regulator (GATE pin, INTVcc pin)

The output driver circuit is configured a totem pole type, it can efficiently drive an Nch MOSFET switching device.

When the output is high level, the GATE pin voltage is clamped with 10V typ. by the internal regulator to protect gate of the Nch MOSFET.

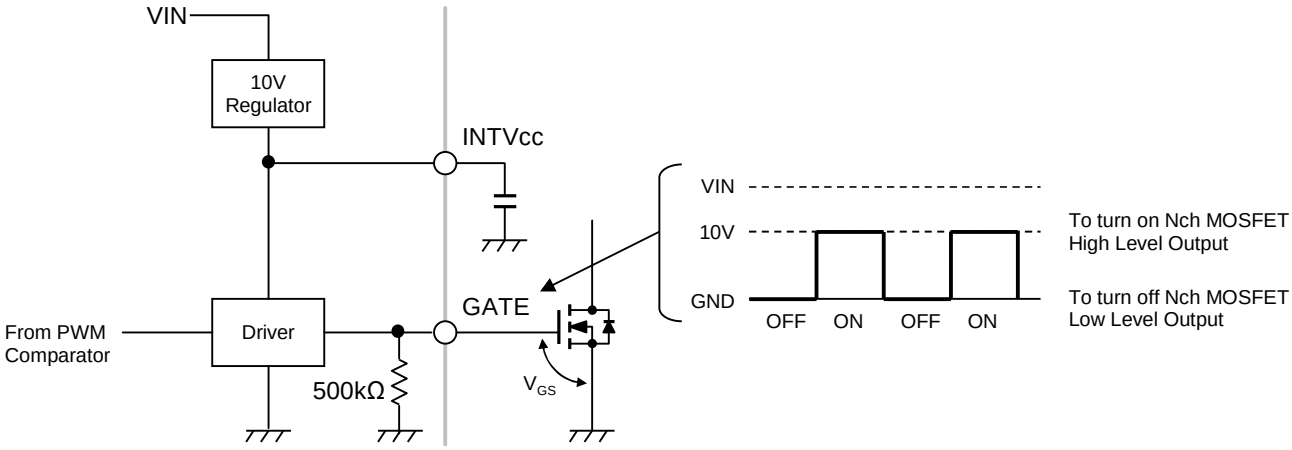


Figure 1. Driver Circuit and GATE Pin Voltage

Although gate drive voltage output from the gate pin decrease due to decrease supply voltage, the gate pin voltage is kept gate drive voltage by bypassing the internal regulator around supply voltage 10V.

Figure 2 shows the example of the gate pin voltage vs. supply voltage characteristics.

The optimum drive ability of MOSFET depends on the oscillation frequency and the gate capacitance of MOSFET.

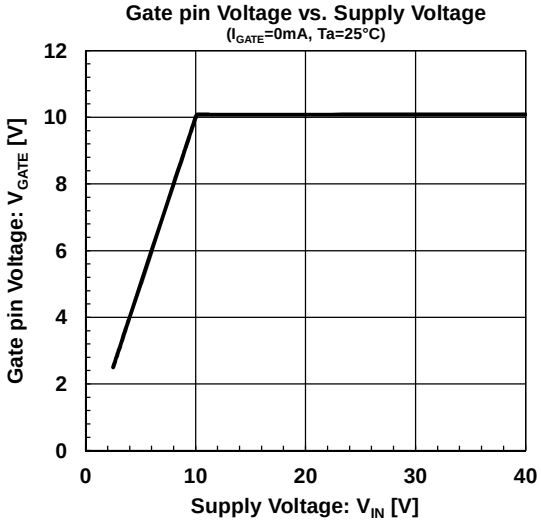


Figure 2. Gate Pin Voltage vs. Supply Voltage

2. Protection Function

• Over Voltage Protection (OVP)

Prevent the overvoltage when normal control of output voltage isn't performed due to any reasons.
While FB pin voltage exceeds 0.848V typ., driving of the power MOSFET is stopped.

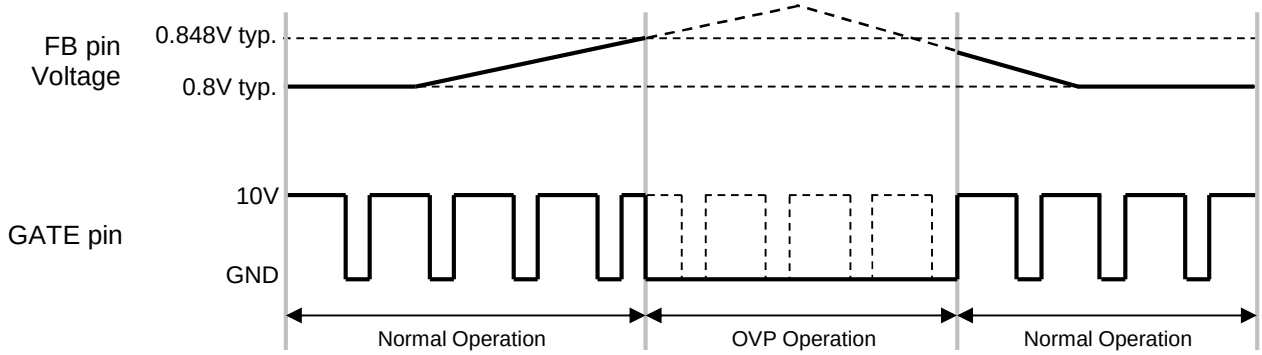


Figure 3. OVP Timing Chart (Assumes function stop of Error AMP)

• Undervoltage Lockout (UVLO)

In case of the supply voltage is low; the IC operation is stopped by the UVLO circuit.
The UVLO is released above 2.4V typ. and IC operation starts.
Then, power supply voltage decrease below 2.2V typ., IC is stopped operation by the UVLO.
There is 200mV typ. hysteresis voltage between detection and release to prevent the malfunction.

• Thermal Shutdown (TSD)

When Junction temperature exceeds the 160°C typ., switching operation is stopped by internal thermal shutdown circuit.
When junction temperature decreases to 145°C typ. or less, switching operation is returned with soft start function.
The thermal shutdown function is a preliminary circuit to prevent thermal runaway of the IC at high temperature and not to compensate for inappropriate thermal design.
Thermal design should be designed with a margin to operate within IC junction temperature (up to 150°C).

• Over Current Protection (OCP)

When the potential difference between the SENSE pin and the GND pin becomes 150mV typical or more, the over current protection circuit stops the switch output.

The switching current is detected by inserted current sensing resistor (R_{SENSE}) between the SENSE pin and the GND pin.

The NJW4142 contains hiccup overcurrent protection and decrease heat generation at the overload.

Then, output voltage of the switching regulator returns automatically when recovering from an abnormal state.

If the overcurrent is detected continuously for 8 pulses while the FB pin voltage is 0.6V typ. or less, the overcurrent protection function turns off the MOSFET.

After stopping, NJW4142 restarts with soft start after the cool down time of 60ms typ.

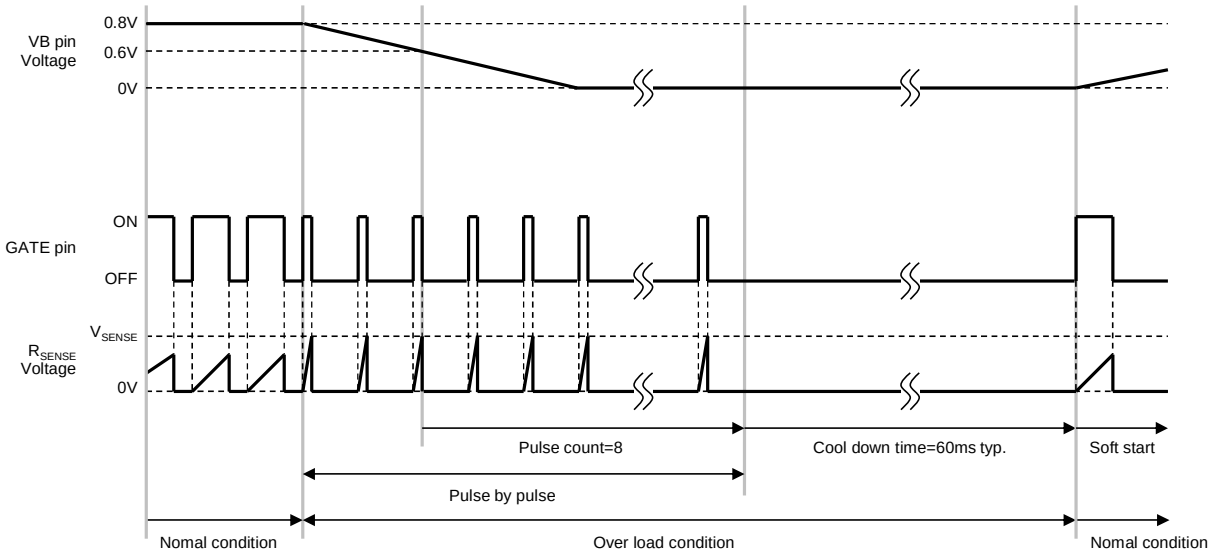


Figure 4. OCP Timing Chart

The current waveform contains high frequency superimposed noises due to the parasitic elements of MOSFET, the inductor and the others.

Depending on the application, inserting RC low-pass filter between current sensing resistor (R_{SENSE}) and the SENSE pin to prevent the malfunction due to such noise.

The time constant of RC low-pass filter should be equivalent to the spike width ($T \leq R \times C$) as a rough guide.

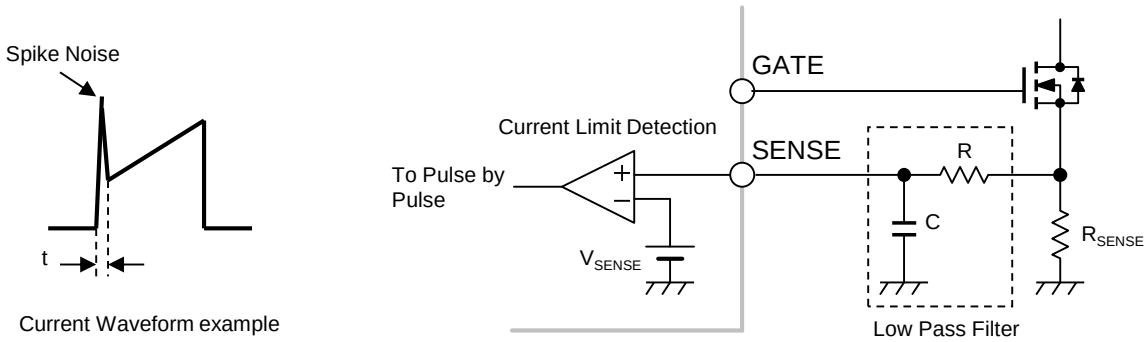


Figure 5. Current Waveform and Filter Circuit

3. Additional Function

- Soft Start

The output voltage rises gradually to the setting value by the soft start function.
The soft start time is 20ms typ. and it is defined as the time until error amplifier reference voltage reaches 0V to 0.75V.
The soft start circuit operates under the following conditions.

- After releasing UVLO
- After restoration from thermal shutdown
- After restoration from standby state
- After restoration from the cool down state

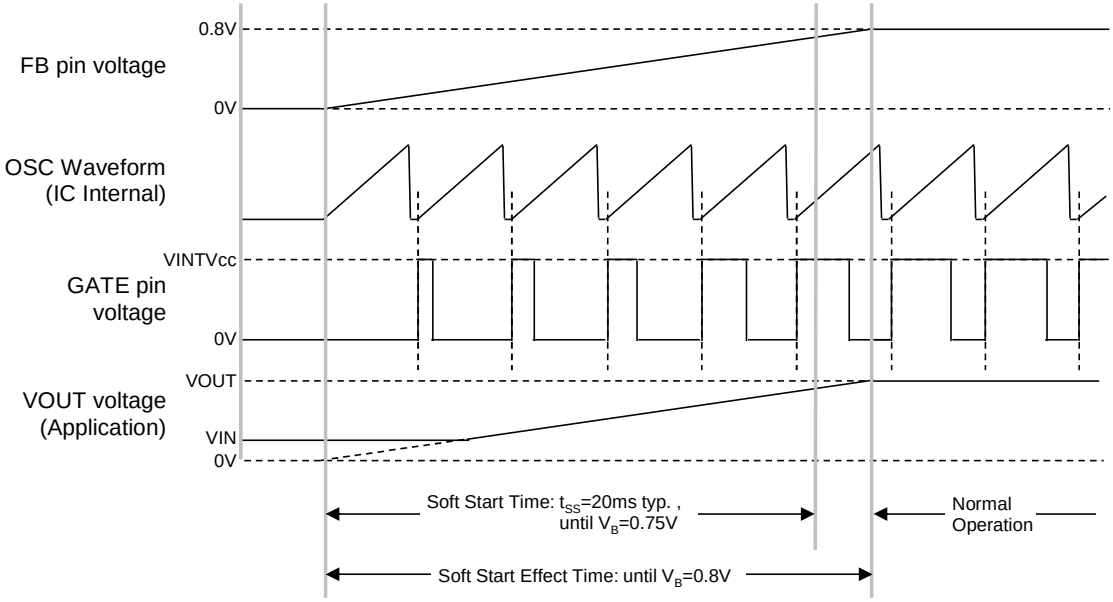


Figure 6. Soft Start Timing Chart

- Standby Function (RUN pin)

The standby function controls standby state by the RUN pin.
The device turns into standby mode when the input voltage at the RUN pin is below the threshold voltage (1.248V typ.). As shown in the application circuit example (startup voltage change circuit), startup voltage of input voltage can be adjusted by setting the voltage dividing resistors R3 and R4 from the power supply line.

$$V_{IN(OFF)}=1.248V\times\left(1+\frac{R_3}{R_4}\right)$$

$$V_{IN(ON)}=1.348V\times\left(1+\frac{R_3}{R_4}\right)$$

The internal of RUN pin is pulled down with 2MΩ, and it will be in standby mode when the pin is open.
Consider the fact that 2MΩ resistors are connected in parallel and set the optimum value, when setting the R4.
If standby function is not required, connect the RUN pin to the VIN pin.

• INTVcc pin

The internal power supply regulator outputs 10V and supplies power to the gate driver in the NJW4142.
The regulator supplies up to 50mA.
Insert a ceramic capacitor to GND nearby the INTVcc pin.
The INTVcc pin and VIN pin can be shorted directly if the input power does not exceed the absolute maximum ratings.
When the INTVcc pin and VIN pin are shorted, 10μA flows to the INTVcc pin even the device is in the standby mode,
Therefore, do not connect the INTVcc and the VIN pins in applications where standby current needs to be minimized.
In addition, it is also necessary to insert a ceramic capacitor nearby the INTVcc pin when shorting the INTVcc pin and the VIN pin.

• External Synchronous

By inputting a square-wave to the SYNC pin, the oscillator of the NJW4142 can be synchronized to the external frequency.
The square-wave needs to meet the specifications in Table 2.

	Conditions
Input Frequency	f_{OSC}×0.9 to f_{OSC}×1.7
Input Pulse Width	25ns to 0.8/f_{OSC}
Input Voltage Amplitude	Over than 1.2V(High Level) Less than 0.5V(Low Level)

Table 2. Square-Wave Inputs to the SYNC Pin

Switching operation during external synchronization is triggered on the rising edge of the SYNC input signal.
In order to prevent a malfunction, a delay time is provided for switching between the asynchronous operation and external synchronous operation.
Table 3 shows the delay time with respect to the oscillation frequency, and Figure 7 shows the timing chart.

Delay Time		
f_{OSC}=50kHz	f_{OSC}=300kHz	f_{OSC}=1000kHz
80μs to 230μs	10μs to 40μs	3μs to 12μs

Table 3. Oscillating Frequency and Delay Time

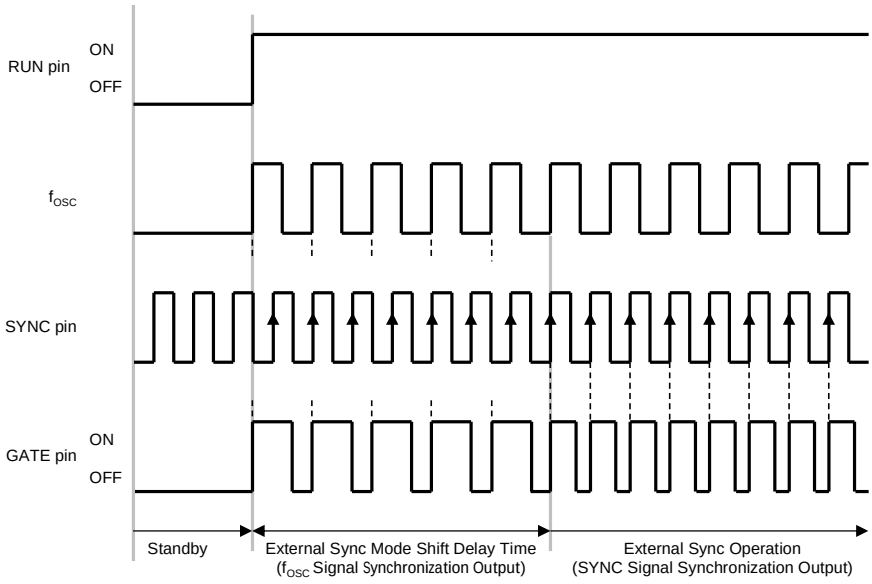


Figure 7. Switching Operation by External Synchronized Clock

■ APPLICATION INFORMATION

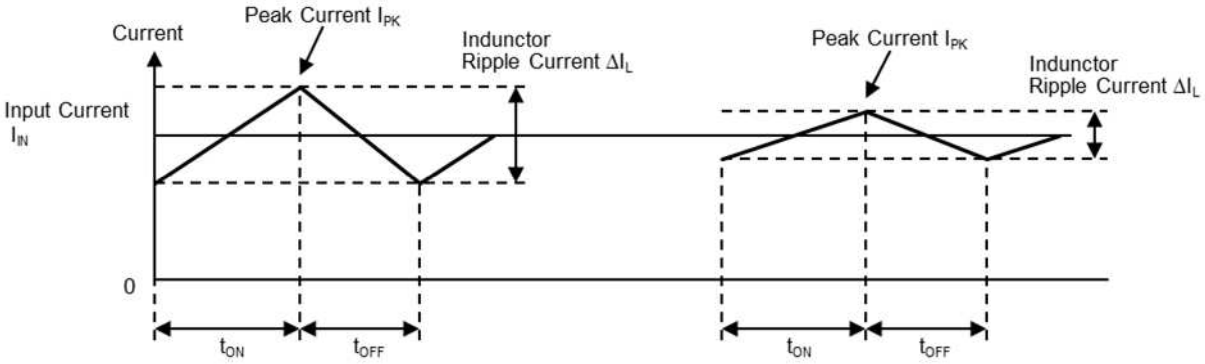
• Inductor

Since large current flows in the inductor, it is necessary to have current capability that does not saturate.
In the case of small inductor value, the peak current increases and conversion efficiency tends to decrease.
The peak current is calculated by the following formula.

$$I_{IN}=\frac{V_{OUT}\times I_{OUT}}{\eta\times V_{IN}}[A]$$

$$\Delta I_L=\frac{(V_{OUT}-V_{IN})\times V_{IN}}{L\times V_{OUT}\times f_{OSC}}[A]$$

$$I_{PK}=I_{IN}+\frac{\Delta I_L}{2}[A]$$



At Small L Value　　At Large L Value

Figure 8. Inductor Current State Transition (Continuous Conduction Mode)

In many cases, the value of the inductor is determined by input voltage, output voltage, oscillation voltage, and R_{SENSE}.
The inductor value is calculated by the following formula.

Lower Limit Value of Inductance : $(4.79\ V_{OUT}-7.27\ V_{IN})\times\frac{R_{SENSE}}{f_{OSC}}$

Higher Limit Value of Inductance : $(26.79\ V_{OUT}-7.27\ V_{IN})\times\frac{R_{SENSE}}{f_{OSC}}$

The Inductor value is the theoretical value.
This value varies depending on application specifications and applications, adjusting it on the actual device.

• Setting of Output voltage

The output voltage V_{OUT} is determined by the relative resistances of R1 and R2.The currents flowing through R1 and R2 need to be sufficiently larger than the bias current of the error amplifier.
The output voltage is calculated by the following formula.

$$V_{OUT}=\left[\frac{R2}{R1}+1\right]\times V_{FB}[V]$$

• Input Capacitor

Transient current depending on the frequency flows at the input section of the switching regulator.
If the power supply line impedance is high, it will lead to input voltage fluctuations and the performance of the NJW4142 cannot be fully drawn out.
Therefore, insert an input capacitor as close to the IC as possible.
A ceramic capacitor is the optimal for input capacitor.
The ripple input current is calculated by the following formula.

$$I_{RMS\_CIN}=0.3\times\Delta I_L[A]$$

• Output Capacitor

The output capacitor is responsible for storing power from the inductor and for stabilizing the supply voltage to the output.
To select the output capacitor, consider the characteristics of ESR (Equivalent Series Resistance), ripple current, and breakdown voltage.
The ripple voltage can be reduced by using a low ESR capacitor.
Since the capacitance of a ceramic capacitor decreases due to DC bias voltage and temperature drift, confirm the characteristics with spec sheets.
The capacitance of a ceramic capacitor is calculated by the following formula.

$$C_{OUT}=\frac{30}{V_{OUT}\times f_{OSC}}\times 10^6[\mu F]$$

The output ripple voltage is calculated by the following formula.

$$V_{ripple(p\text{-}p)}=ESR\times I_{PK}+\frac{I_{OUT}}{C_{OUT}}\times t_{ON}\ [V]$$

The effective value of ripple current is calculated by the following formula.

$$I_{RMS\_COUT}=I_{OUT}\times\sqrt{\frac{V_{OUT}-V_{IN}}{V_{IN}}}\ [A]$$

• Power Supply, GND pin (VIN pin, GND pin)

With the switching operation, switching current flows into the IC depends on oscillation frequency.
If the impedance of power supply line is high, IC performance will not be drawn out due to input voltage fluctuation.
Therefore insert an input capacitor close to the VIN pin - the GND pin connection in order to lower high frequency impedance.

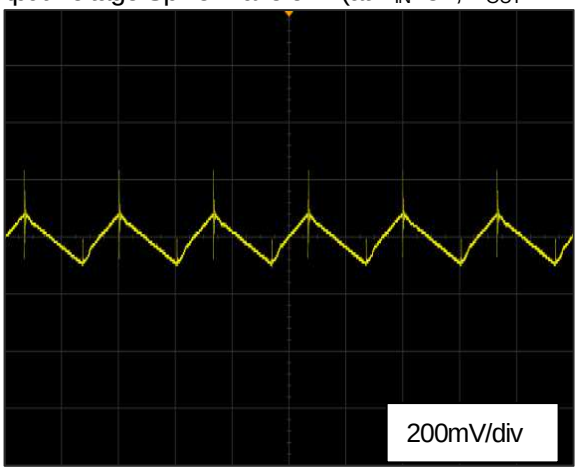
• Catch Diode

During the OFF cycle of the power MOSFET, the power stored in the inductor flows through the catch diode into the output capacitor.
Therefore, electric current depending on the load current flows into the diode every OFF cycle.
Since a diode's forward saturation voltage and the current accumulation cause power loss, a SBD (Schottky Barrier Diode) which has a low forward saturation voltage is the most suitable.
During the ON cycle of the MOSFET, reverse voltage is applied to the diode.
Considering the margin for the withstand voltage of the diode with respect to the output voltage.
The SBD has a large increase in reverse current characteristics at high temperatures compared to general diodes.
Depending on the operating conditions of the application, efficiency may be improved by emphasizing reverse current characteristics rather than forward saturation voltage.

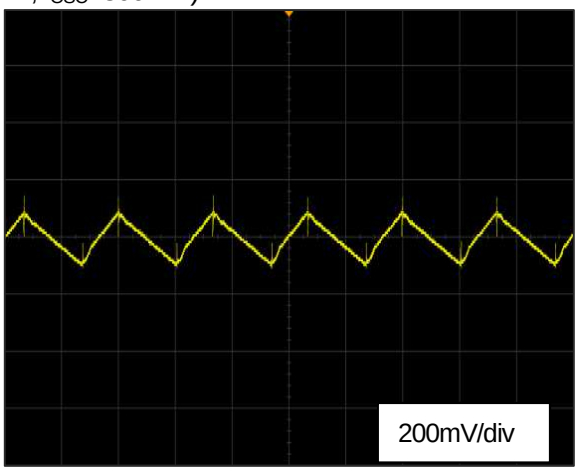
- Switching Element

The switching element is used an Nch MOSFET specified for switching applications.
The GATE pin voltage of NJW4142 is limited to 10V typ., thus select a MOSFET with a gate-source voltage less than 10V and a sufficiently low drain-source ON resistance.
The gate drive voltage output from the GATE pin decreases as the power supply voltage of the NJW4142 becomes lower; therefore, determine MOSFET usage according to the input voltage range.
A large gate capacity leads to reduction in efficiency.
Switching loss will occur due to delay of the time rising/falling by discharging current to gate capacity.
Additionally, a parasitic inductance component may cause spike noise when the gate capacitance charge/discharge is accompanied by a rapid current change.
If the gate capacitance is small, insert a resistor between a GATE pin and a gate to limit the current moderately.
When inserting a gate resistor, 10Ω is recommended; provided that the waveform is blunted due to a resistance and the efficiency is reduced, determine the optimum value by actual machine evaluation.

<Output Voltage Spike Waveform (at V_{IN}=5V, V_{OUT}=12V, I_{OUT}=2A, f_{OSC}=300kHz)>

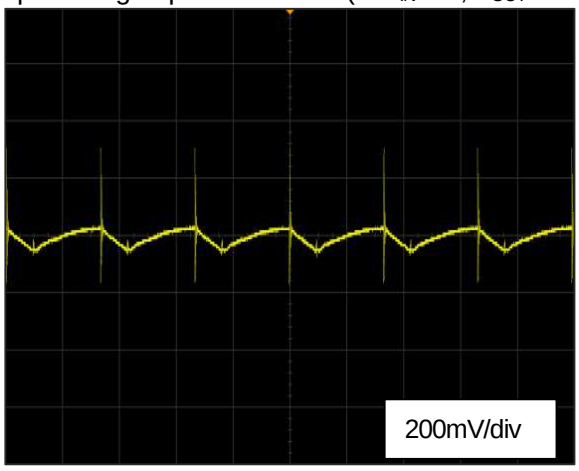


No gate resistor

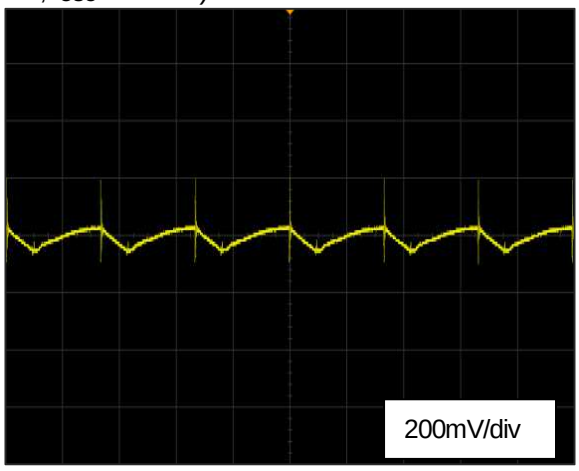


With gate resistor 10Ω

<Output Voltage Spike Waveform (at V_{IN}=9V, V_{OUT}=12V, I_{OUT}=2A, f_{OSC}=300kHz)>

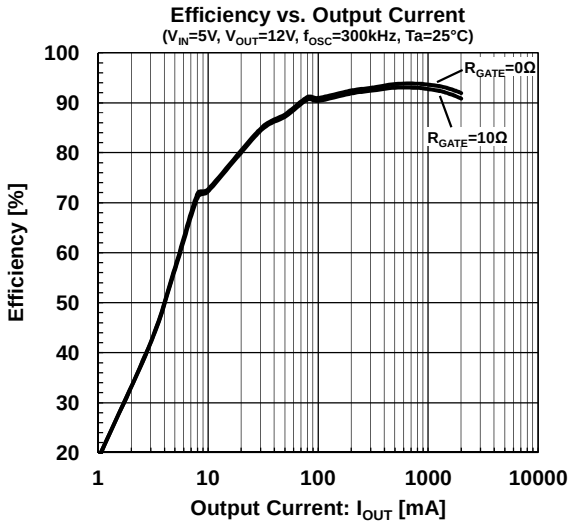


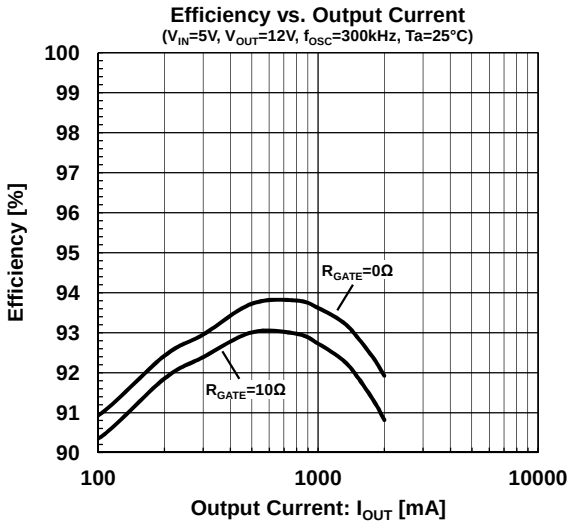
No gate resistor

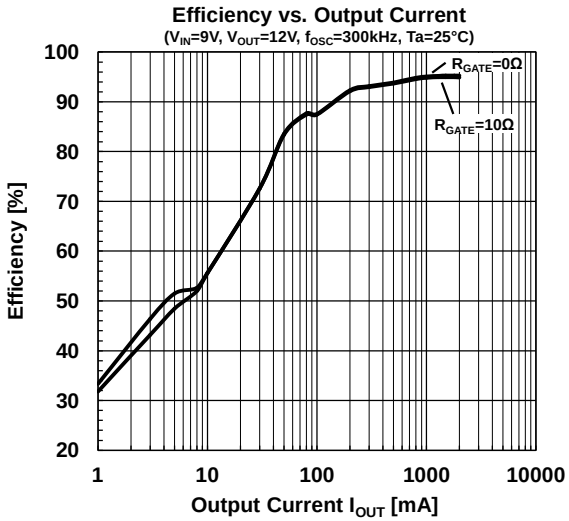


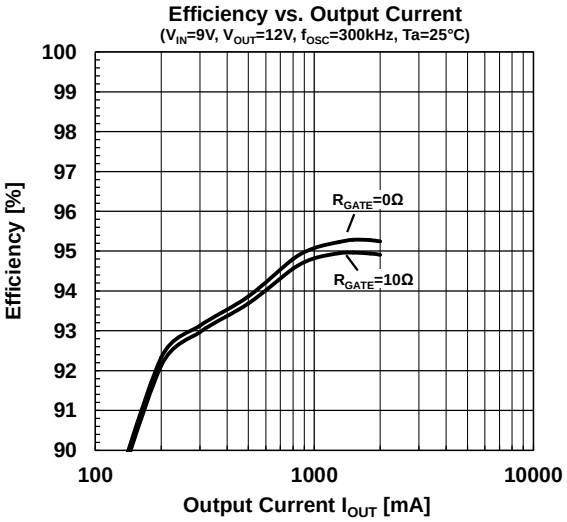
With gate resistor 10Ω

<Efficiency Characteristics>









- Phase Compensation design example

A switching regulator needs a feedback circuit to stabilize the output voltage.
Frequency characteristics of the application change due to inductance and output capacitor.
It is ideal phase compensation design that can obtain the maximum bandwidth while ensuring the phase margin necessary for stable operation.
For the phase compensation designs, actual machine adjustment is also important. Ultimately please select a constant while considering the application specification.

- Feedback and Stability

The feedback loop should be designed the open loop phase shift less than -180 ° at frequency where the loop gain is 0dB.
Also, the loop characteristics should have margin in consideration of ringing and immunity to oscillation during load fluctuations.
The NJW4142 can arbitrarily design the feedback circuit; it is possible to optimize the placement of Pole and Zero that are important for loop compensation.

The characteristics of the Pole and Zero are shown in Figure 9.
Pole: The gain has a slope of -20 dB/dec, and the phase shifts -90°.
Zero: The gain has a slope of +20 dB/dec, and the phase shifts +90°.

If the number of factors constituting Pole is “n”, the gain phase change will also be “n”-fold.
It is the same for Zero.
The Pole and Zero are in a reciprocal relationship, if there is one factor for each Pole and Zero, they will cancel each other.

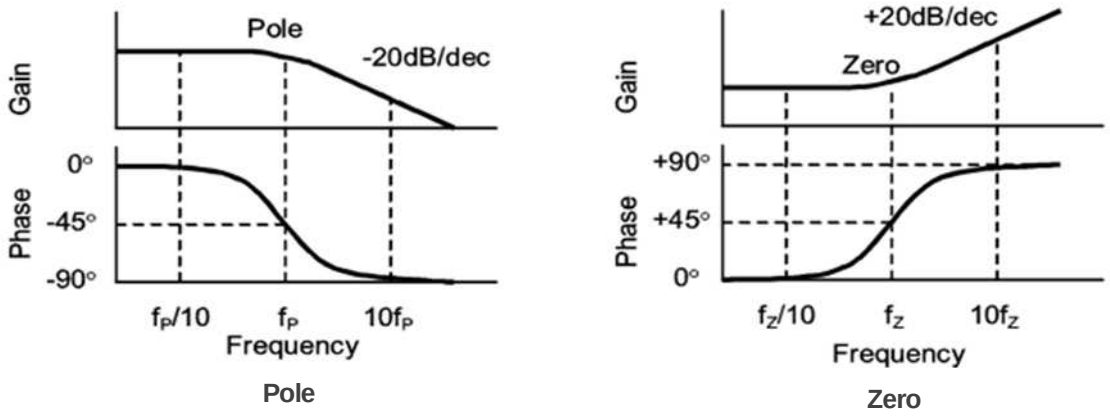


Figure 9. Pole and Zero Characteristics

- Setting of Pole and Zero

The position of the Pole and Zero are determined by the application condition and error amplifier setting.
Figure 10 shows phase compensation circuit and Table 4 shows setting of Pole and Zero.

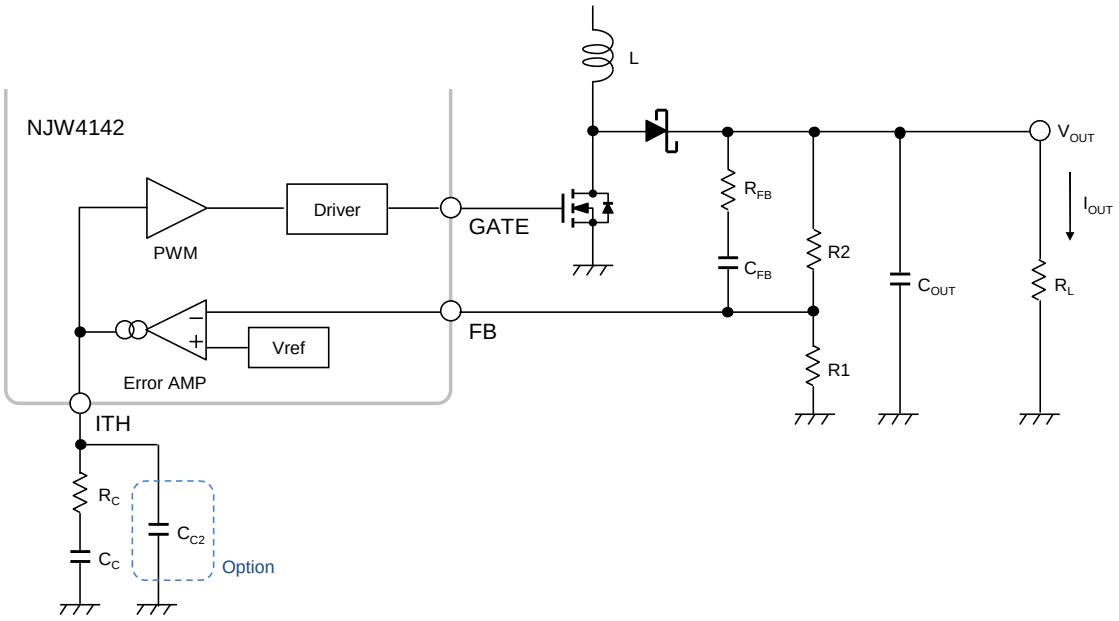


Figure 10. Phase Compensation Circuit Configuration

Table 4. Setting of Pole and Zero

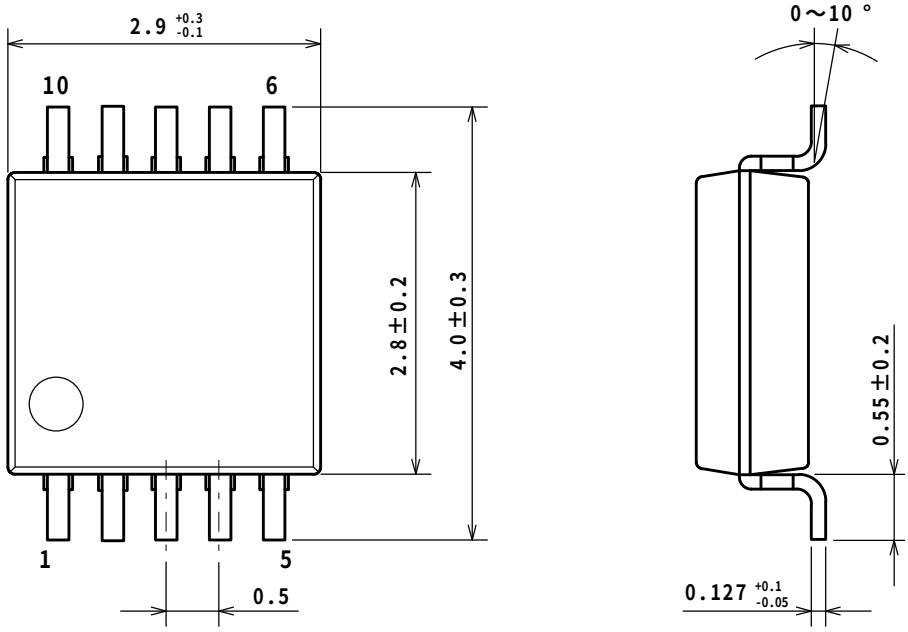
Symbol	Calculating formula	Setting example	Description
f_{P1}	$f_{P1}=\frac{1}{2\times\pi\times\frac{Av}{gm}\times C_C}$	$f_{P1}<\frac{f_{ZRPH}}{10000}$ to $\frac{f_{ZRPH}}{5000}$	A position of 1st pole f_{P1} is fixed by C_C connected to the output of the error amplifire. Av=55dB typ.
f_{ZRPH}	$f_{ZRPH}=\frac{(1-D)^2\times\frac{V_{OUT}}{I_{OUT}}}{2\times\pi\times L}$		The position of f_{ZRPH} is determined by input / output condition, L value and load current. It is recommended to limit the f_{0dB} frequency of the loop gain to the upper limit of 1/5 to 1/10 of f_{ZRPH}.
f_{POUT}	$f_{POUT}=\frac{1}{2\times\pi\times\frac{V_{OUT}}{I_{OUT}}\times C_{OUT}}$	$1<\frac{f_{Z1}}{f_{POUT}}<15$	The pole f_{POUT} is caused by capacitor and load resistance connected to the output. In the case, the load resistance asumes a maximum load current and calculates. When it uses a ceramic capacitor for C_{OUT}, it is realistic to calculate at effective capacitance in consideration of DC bias.
f_{Z1}	$f_{Z1}=\frac{1}{2\times\pi\times R_C\times C_C}$		A position of zero f_{Z1} is fixed by R_C and C_C connected to the output of the error amplifire.
f_{Z2}	$f_{Z2}=\frac{1}{2\times\pi\times R2\times C_{FB}}$	20kHz to 60kHz	The Zero f_{Z2} is caused by R2 and C_{FB}. The f_{Z2} compensates it for a phase shift of f_{P2}.

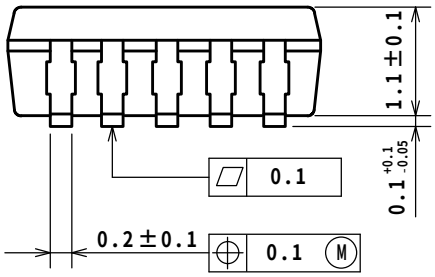
Various Poles are occurred at hundreds of kHz or more, the 0dB frequency of the loop gain is set to 1/5 to 1/10 of the oscillation frequency as the upper limit.
If the oscillation frequency is high, the loop gain 0dB frequency should be set around 100 kHz in order to ensure sufficient phase margin.
When the loop gain is affected by the stability in the high frequency region, adjust the actual equipment using R_{FB}, C_{C2}.

MSOP10 (VSP10) MEET JEDEC MO-187-DA

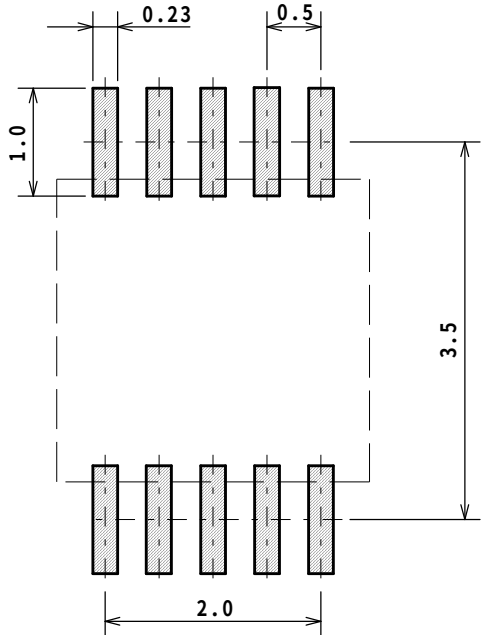
Unit: mm

■ PACKAGE DIMENSIONS





■ EXAMPLE OF SOLDER PADS DIMENSIONS

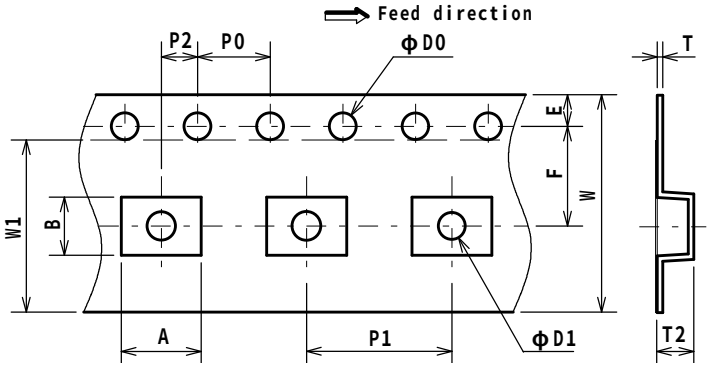


MSOP10 (VSP10) MEET JEDEC MO-187-DA

Unit: mm

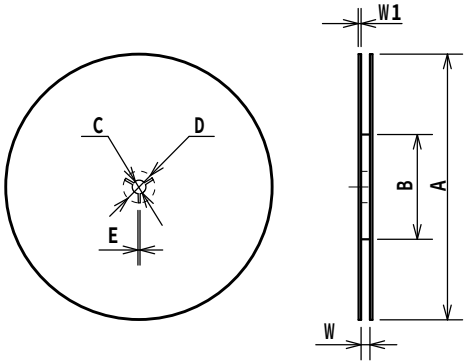
■ PACKING SPEC

TAPING DIMENSIONS



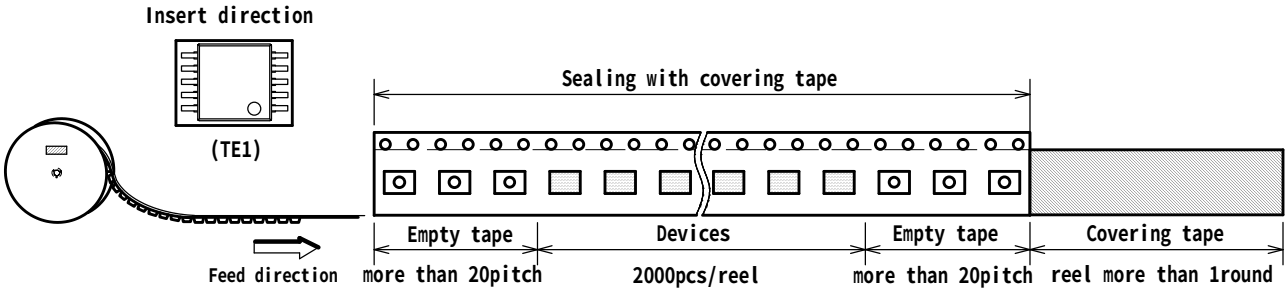
SYMBOL	DIMENSION	REMARKS
A	4.4	BOTTOM DIMENSION
B	3.2	BOTTOM DIMENSION
D0	$1.5^{+0.1}_{0}$	
D1	$1.5^{+0.1}_{0}$	
E	1.75±0.1	
F	5.5±0.05	
P0	4.0±0.1	
P1	8.0±0.1	
P2	2.0±0.05	
T	0.30±0.05	
T2	2.0 (MAX.)	
W	12.0±0.3	
W1	9.5	THICKNESS 0.1max

REEL DIMENSIONS

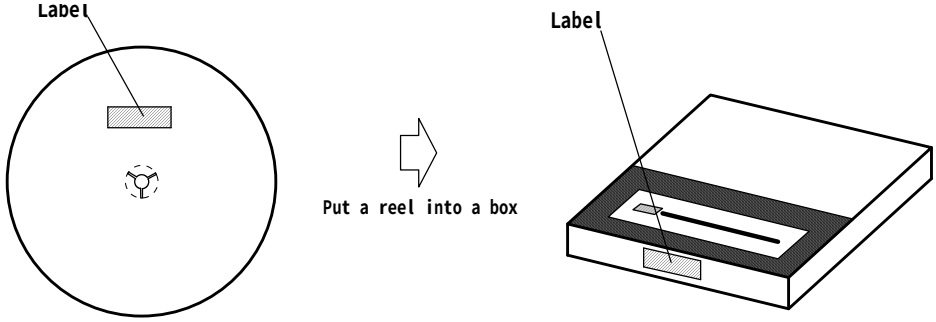


SYMBOL	DIMENSION
A	φ254±2
B	φ100±1
C	φ 13±0.2
D	φ 21±0.8
E	2±0.5
W	13.5±0.5
W1	2.0±0.2

TAPING STATE



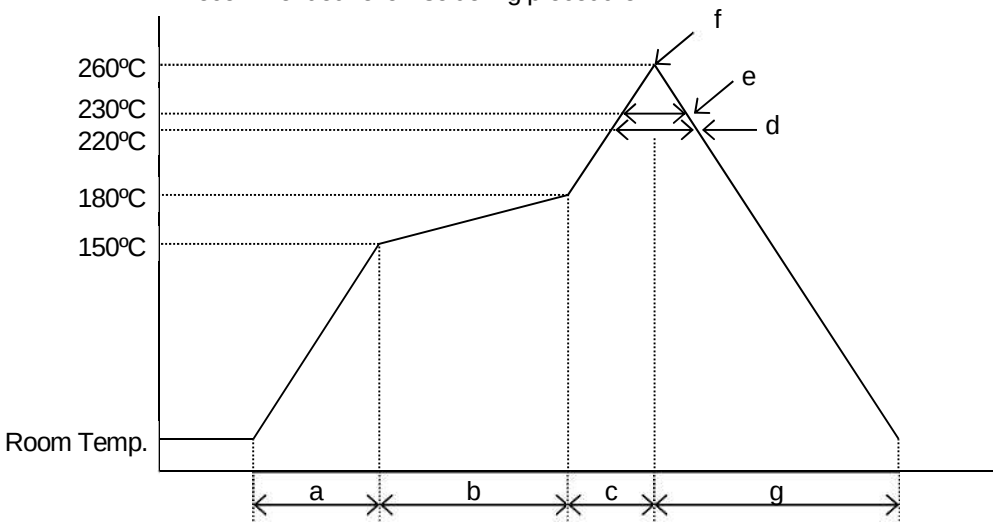
PACKING STATE



■ RCOMMENDED MOUNTING METHOD

INFRARED REFLOW SOLDERING METHOD

*Recommended reflow soldering procedure



a:Temperature ramping rate	: 1 to 4ºC/s
b:Pre-heating temperature time	: 150 to 180ºC : 60 to 120s
c:Temperature ramp rate	: 1 to 4ºC /s
d:220ºC or higher time	: Shorter than 60s
e:230ºC or higher time	: Shorter than 40s
f:Peak temperature	: Lower than 260ºC
g:Temperature ramping rate	: 1 to 6ºC/s

The temperature indicates at the surface of mold package.

■ REVISION HISTORY

Date	Revision	Changes
14 June, 2019	Ver.1.0	New Release
28 July, 2021	Ver.1.1	Corrected the Typical Characteristics. (Standby Current vs. Temperature, Under Voltage Lockout Voltage vs. Temperature) Updated the Application Information. (Corrected the Output Voltage Spike Waveform, added Output Voltage Spike Waveform with other condition and Efficiency Characteristics. Added Av=55dB typ. in description of Setting of Pole and Zero.)

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   - Equipment Used in the Deep Sea
   - Power Generator Control Equipment (Nuclear, steam, hydraulic, etc.)
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   - Various Safety Devices

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