2.4MHz, 45V, 5A MOSFET Switching Regulator IC for Boost Converter

■ FEATURES

- Switch Current Limit 5A min.
- Oscillating Frequency 100kHz to 2.4MHz
- Current Mode Control
- Phase compensation can be adjusted with an external circuit.
- Correspond to Ceramic Capacitor (MLCC)
- External Clock Synchronization
- Soft Start Function 20ms typ.
- Wide Operating Input Voltage Range 3V to 40V
- PWM control
- Internal Protection Function
  - Over Voltage Protection Function
  - Under Voltage Lockout Function(UVLO)
  - Over Current Protection Function(Hiccup)
  - Thermal Shutdown Function
- Standby Function
- Package HSOP8-M1

■ GENERAL DESCRIPTION

The NJW4133 is a high speed oscillating frequency boost converter with 45V/5A MOSFET.

Operating voltage range is wide input range from 3.0V to 40V, it can correspond to supply voltage drop such as cold crank.

The NJW4133 has wide oscillating frequency range from 100kHz to 2.4MHz and external clock synchronization function.

Therefore the NJW4133 can avoid interference with the AM radio frequency.

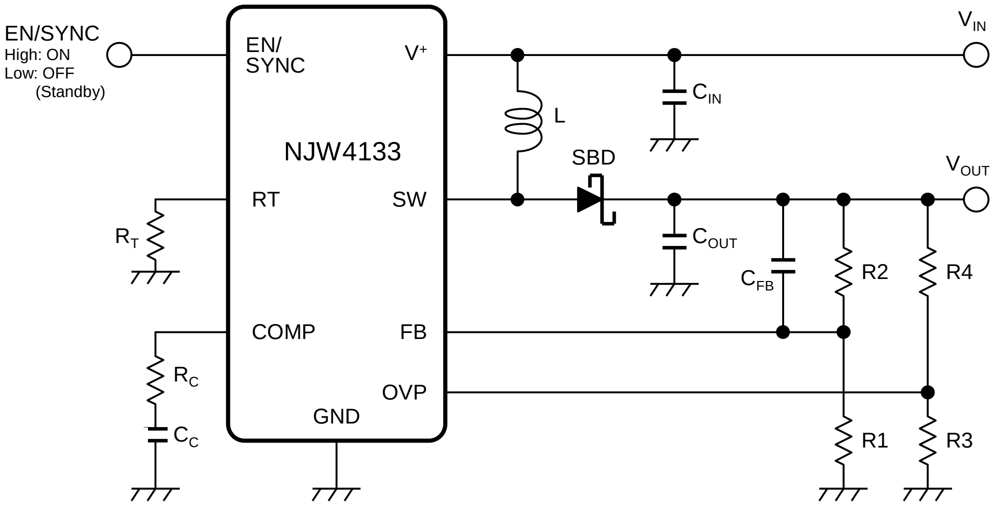
Internal protection functions: UVLO, over voltage protection, over current protection and thermal shutdown circuit can protect IC when abnormal condition.

The NJW4133 has wide coverage in consumer electronics and industrial application, because of features that are wide input operating voltage range and wide oscillating frequency range.

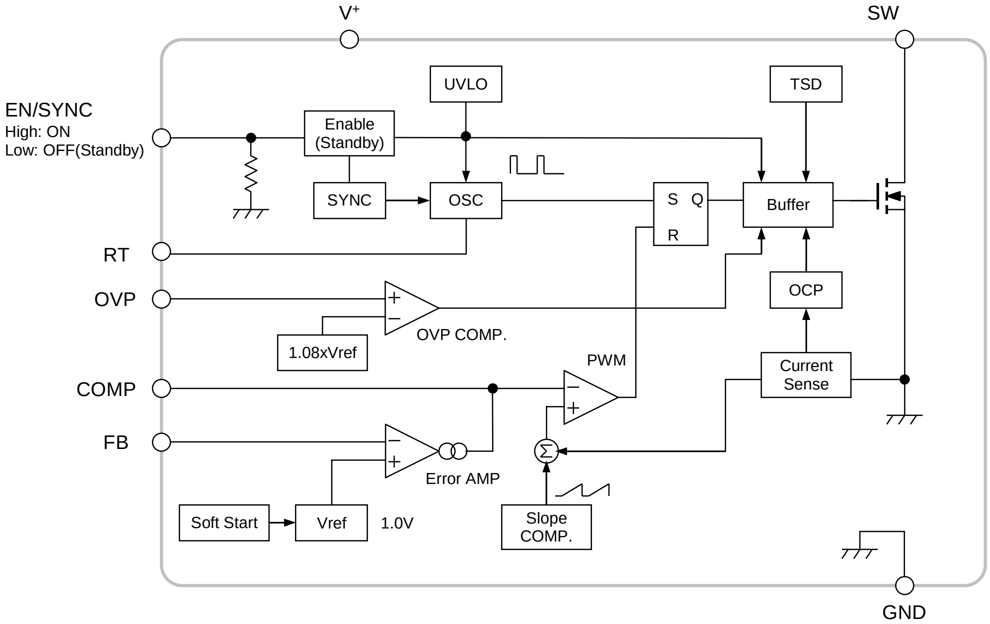
■ TARGET APPLICATION

- Power supply for LCD and OLED
- Piezo Element drive
- And other low/ middle range boost application

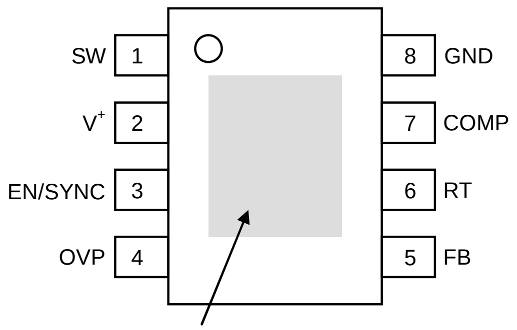
■ APPLICATION



■ BLOCK DIAGRAM



■ PIN CONFIGRATION



Note) Exposed Pad on backside should be connected to ground and soldered to PCB.

PIN NO.	SYMBOL	DESCRIPTION
1	SW	Output
2	V+	Power supply input
3	EN/SYNC	Enable input/External CLK input
4	OVP	Over voltage protection input
5	FB	Voltage feedback input
6	RT	Oscillating frequency setting
7	COMP	Error amplifier output
8	GND	Ground

■ PRODUCT NAME INFORMATION

NJW4133 GM1 - (TE1)

Part Number

Package
GM1:HSOP8-M1

Taping Form

■ ORDERING INFORMATION

PRODUCT NAME	PACKAGE	AUTO MOTIVE	RoHS	HALOGEN-FREE	TERMINAL FINISH	MARKING	WEIGHT (mg)	MOQ (pcs)
NJW4133GM1(TE1)	HSOP8-M1	-	Yes	Yes	Sn100%	4133	81	3000
NJW4133GM1-T1(TE1)	HSOP8-M1	Yes	Yes	Yes	Sn100%	4133T1	81	3000

This data sheet is applied to "NJW4133GM1".
Please refer to each data sheet for other versions.

■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	-0.3 to +45	V
SW pin Voltage	V_{SW}	-0.3 to +45	V
EN/SYNC pin Voltage	$V_{EN/SYNC}$	-0.3 to +45	V
FB pin Voltage	V_{FB}	-0.3 to +7	V
OVP pin Voltage	V_{OVP}	-0.3 to +7	V
Power Dissipation (Ta=25°C) HSOP8-M1	P_D	(2-layer/ 4-layer) 860(1)/ 2900(2)	mW
Junction Temperature	Tj	-40 to +150	°C
Operating Temperature	Topr	-40 to +125	°C
Storage Temperature	Tstg	-50 to +150	°C

(1): Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JEDEC standard, 2Layers)

(2): Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JEDEC standard, 4Layers)

(For 4Layers: Applying 74.2×74.2mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5)

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V^+	3.0 to 40	V
Timing Resistor	R_T	2.32 to 82	kΩ
Oscillating Frequency	f_{OSC}	100 to 2400	kHz
External Clock Input	f_{SYNC}	f_{OSC}×0.9 to f_{OSC}×1.7 Maximum 2800kHz	kHz

■ ELECTRICAL CHARACTERISTICS

(Unless otherwise noted, $V^{+}=V_{EN/SYNC}$=12V, R_T=27kΩ, Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Under Voltage Lockout Block						
ON Threshold Voltage	V_{T_ON}	V^{+}= L → H	2.70	2.85	3.00	V
OFF Threshold Voltage	V_{T_OFF}	V^{+}= H → L	2.60	2.75	2.90	V
Hysteresis Voltage	V_{HYS}		70	100	–	mV
Soft Start Block						
Soft Start time	t_{SS}	V_B=0.95V	10	20	30	ms
Oscillator Block						
Oscillating Frequency1	f_{OSC1}	R_T=27kΩ	270	300	330	kHz
Oscillating Frequency2	f_{OSC2}	R_T=7.32kΩ	820	1000	1180	kHz
Oscillating Frequency3	f_{OSC3}	R_T=2.32kΩ	2100	2400	2700	kHz
Error Amp Block						
Reference Voltage	V_B		-1.0%	1.0	+1.0%	V
Input Bias Current	I_B		-0.1	–	0.1	μA
Error Amplifire Transconductance	gm		–	1200	–	μA/V
Error Amplifire Gain	A_V		–	1000	–	–
Output Source Current	I_{OM+}		90	130	170	μA
Output Sink Current	I_{OM-}		90	130	170	μA
PWM Comparator Block						
Minimum OFF Time	$t_{OFF-min}$	V_{FB}=0.9V, R_T=7.32kΩ	–	65	110	ns
Minimum ON Time	t_{ON-min}		–	110	160	ns
Maximum Duty Cycle	$M_{AX}D_{UTY}$	V_{FB}=0.9V	92	95	98	%
Over Current Protection Block						
COOL DOWN Time	t_{COOL}		–	500	–	ms
Output Block						
Output ON Resistance	R_{ON}	I_{SW}=3A	–	0.085	0.105	Ω
Switching Current Limit	I_{LIM}		5.0	8.0	10.0	A
Switching Leak Current	I_{LEAK}	$V_{EN/SYNC}$=0V, V_{SW}=40V	–	–	4	μA
Over Voltage Protection Block						
Detection Reference Voltage	V_{REF_OVP}		-1.0%	1.08	+1.0%	V
Release Reference Voltage	V_{REF_OVPR}		-2.0%	1.04	+2.0%	V
Input Bias Current	I_{B_OVP}		–	–	1	μA

■ ELECTRICAL CHARACTERISTICS

(Unless otherwise noted, $V^+=V_{EN/SYNC}$=12V, R_T=27kΩ, Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Enable Control / Sync Block (EN/SYNC)						
High Threshold Voltage	$V_{THH\_EN/SYNC}$	$V_{EN/SYNC}$= L → H	1.6	–	V^+	V
Low Threshold Voltage	$V_{THL\_EN/SYNC}$	$V_{EN/SYNC}$= H → L	0	–	0.5	V
Input Bias Current	$I_{EN/SYNC}$	$V_{EN/SYNC}$=12V	–	0.9	1.7	µA
General characteristic						
Quiescent Current	I_{DD}	R_L=No load, V_{FB}=1.1V	–	2.2	2.8	mA
Standby Current	I_{DD_STB}	$V_{EN/SYNC}$=0V	–	–	3	µA

■ THERMAL CHARACTERISTICS

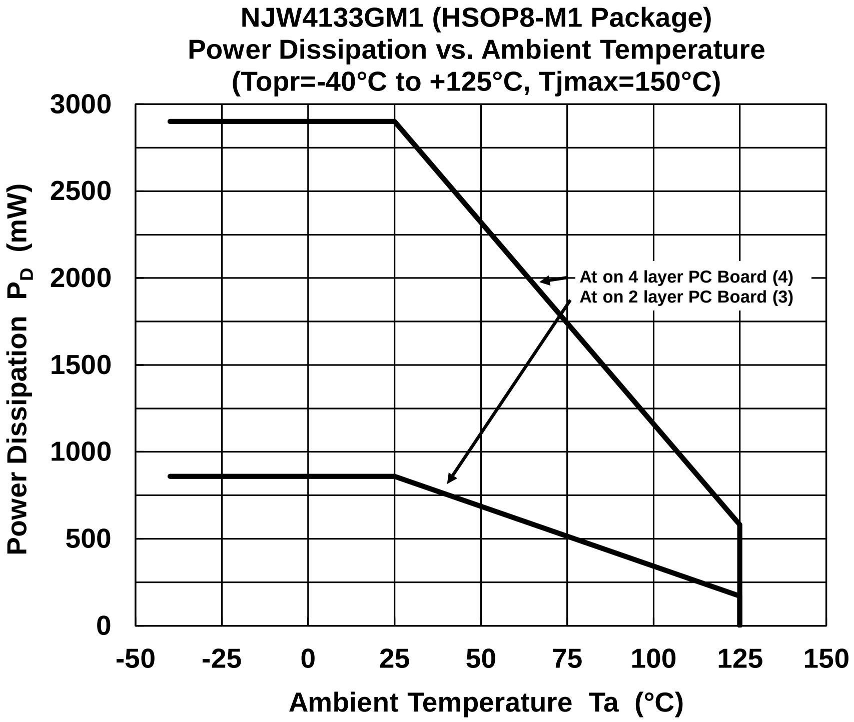
Parameter	Symbol	Value		Unit
Junction-to-ambient thermal resistance	θja	HSOP8-M1	145(3) 43(4)	°C /W
Junction-to-Top of package characterization parameter	ψjt	HSOP8-M1	22(3) 6.3(4)	°C /W

(3): Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JEDEC standard, 2Layers)

(4): Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JEDEC standard, 4Layers)

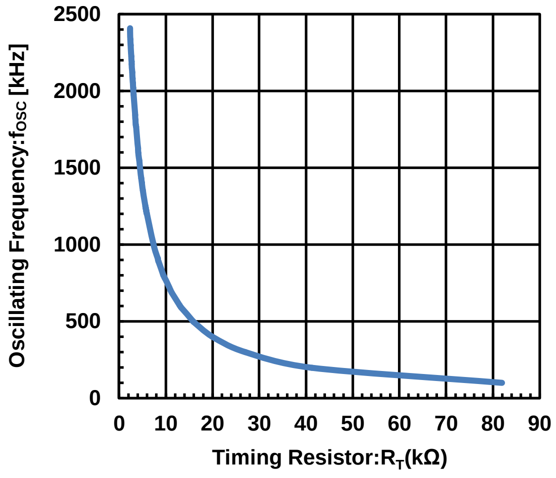
(For 4Layers: Applying 74.2×74.2mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5)

■ POWER DISSIPATION vs. AMBIENT TEMPERATURE

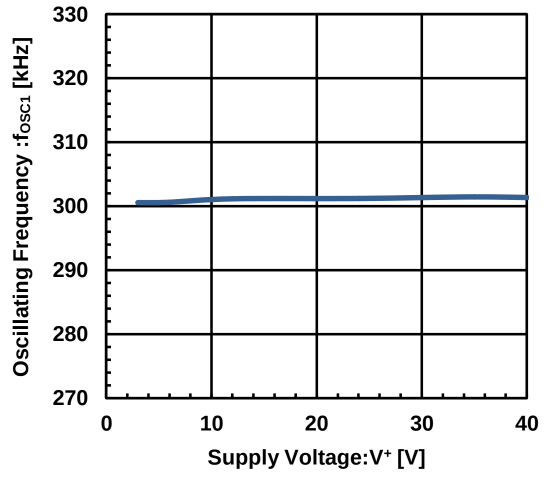


■ TYPICAL CHARACTERISTICS

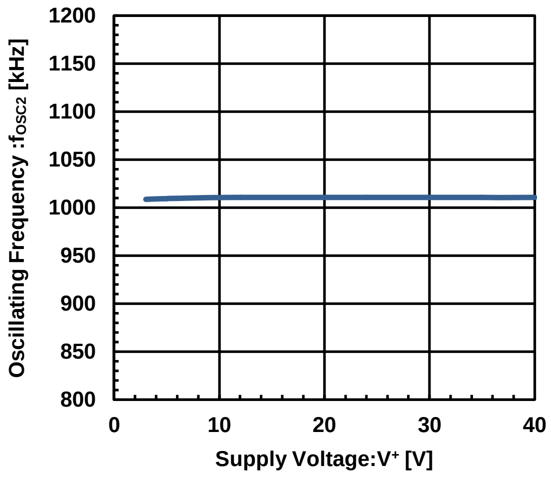
Oscillating Frequency vs.Timing resistor
(V^{+}=12V, Ta=25ºC)



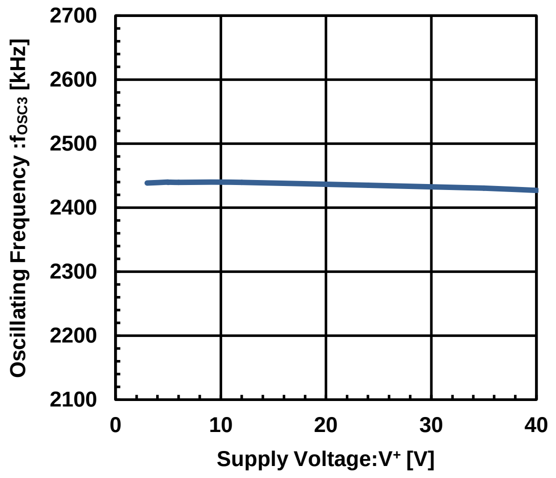
Oscillating Frequency 1 vs. Supply Voltage
(R_T=27kΩ,Ta=25ºC)



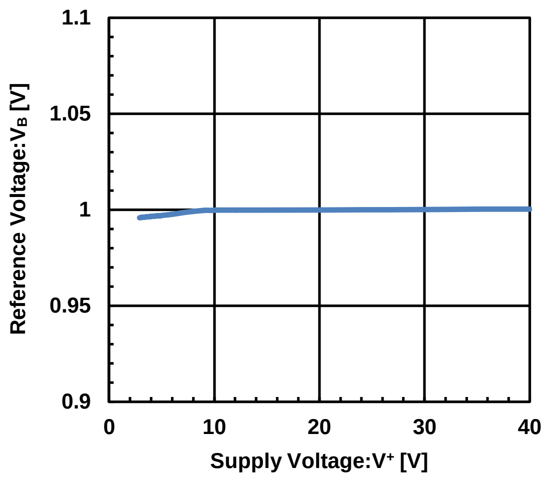
Oscillating Frequency 2 vs. Supply Voltage
(R_T=7.32kΩ,Ta=25ºC)



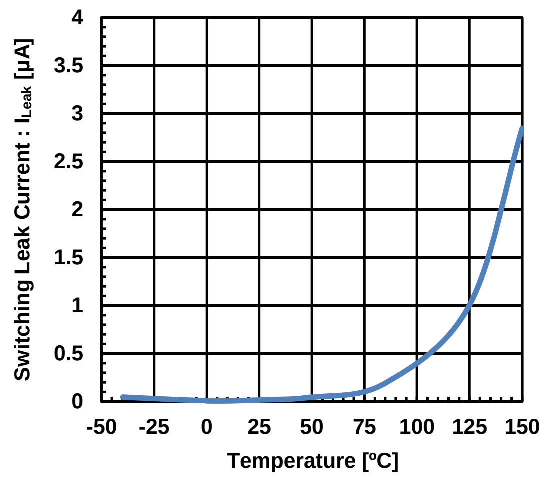
Oscillating Frequency 3 vs. Supply Voltage
(R_T=2.32kΩ,Ta=25ºC)



Reference Voltage vs. Supply Voltage
(Ta=25ºC)

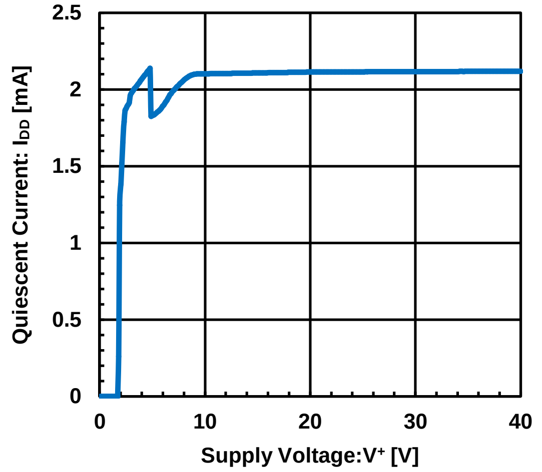


Switching Leak Current vs. Temperature
(V^{+}=12V, $V_{EN/SYNC}$=0V, V_{SW}=40V)

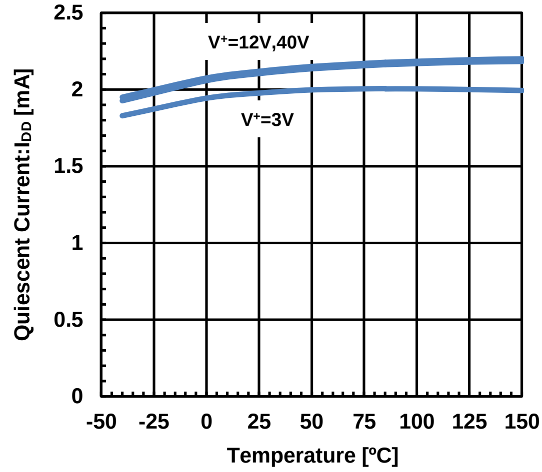


■ TYPICAL CHARACTERISTICS

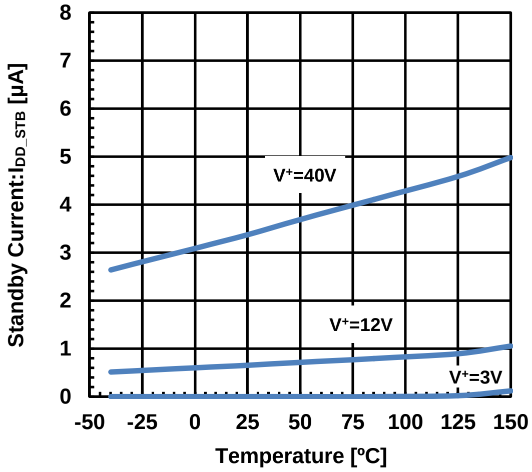
Quiescent Current vs. Supply Voltage
(No Load, Not Switching, Ta=25ºC)



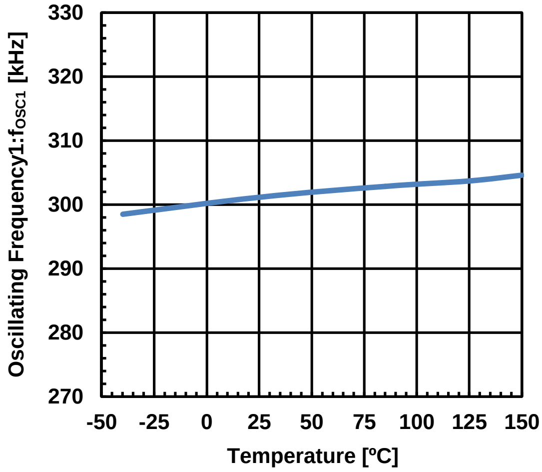
Quiescent Current vs. Temperature
(No Load, Not Switching)



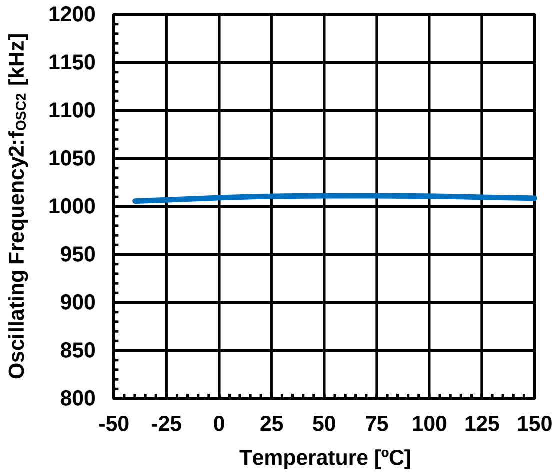
Standby Current vs. Temperature
($V_{EN/SYNC}$=0V)



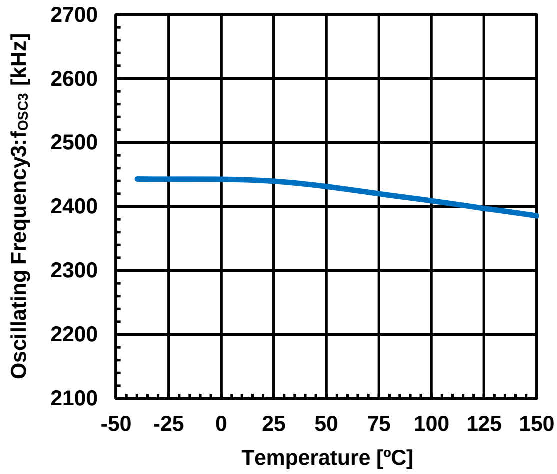
Oscillating Frequency vs. Temperature
(V+=12V, R_T=27kΩ)



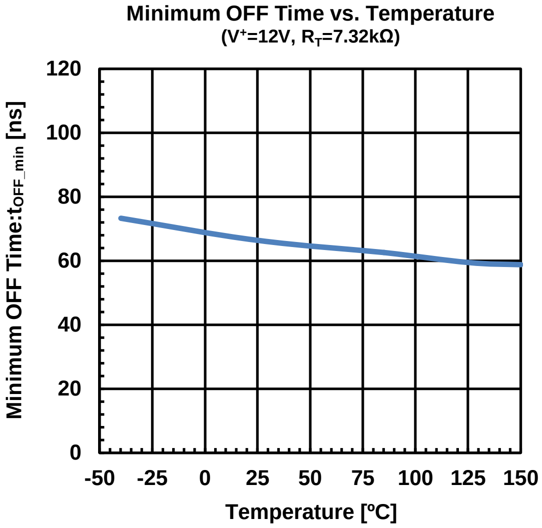
Oscillating Frequency vs. Temperature
(V+=12V, R_T=7.32kΩ)

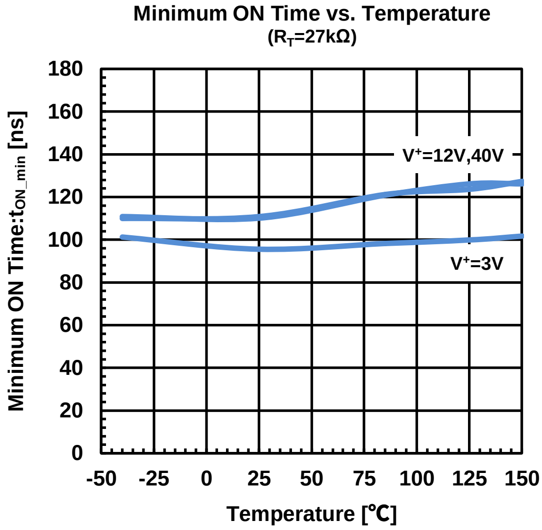


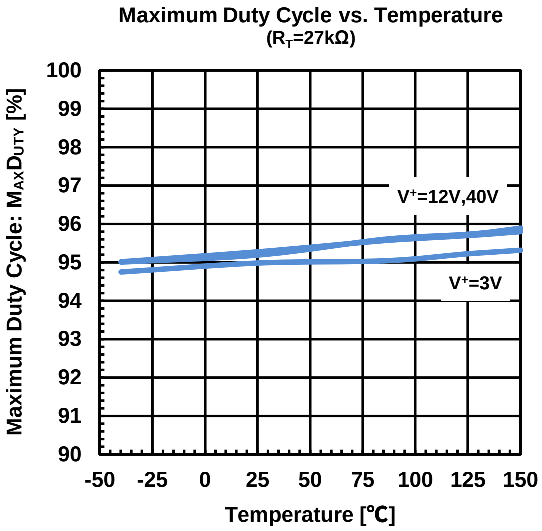
Oscillating Frequency vs. Temperature
(V+=12V, R_T=2.32kΩ)

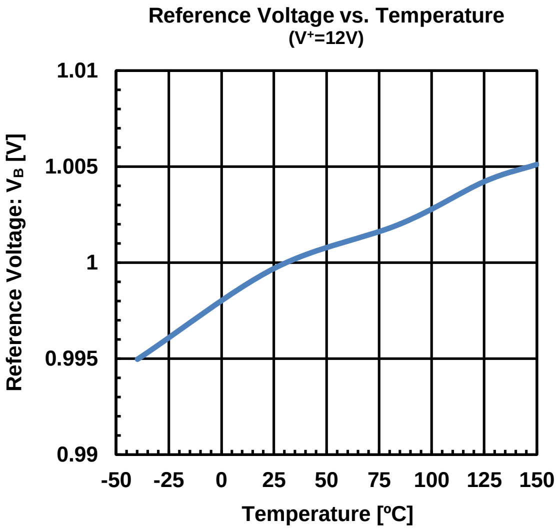


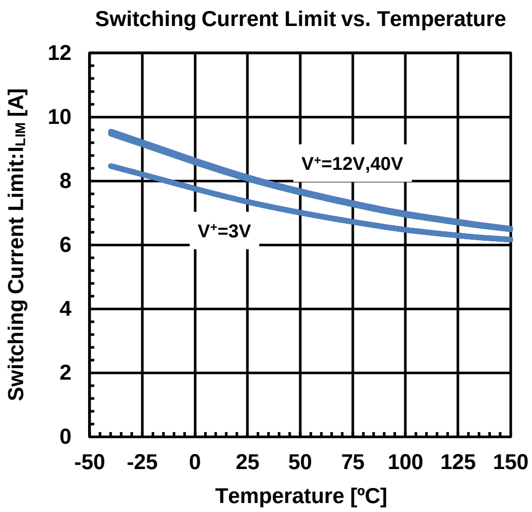
■ TYPICAL CHARACTERISTICS

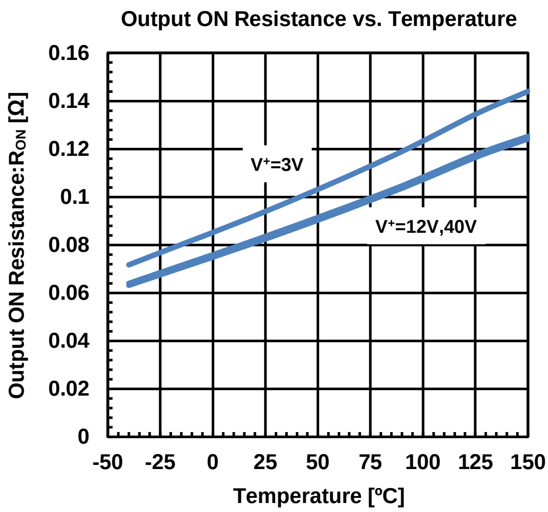




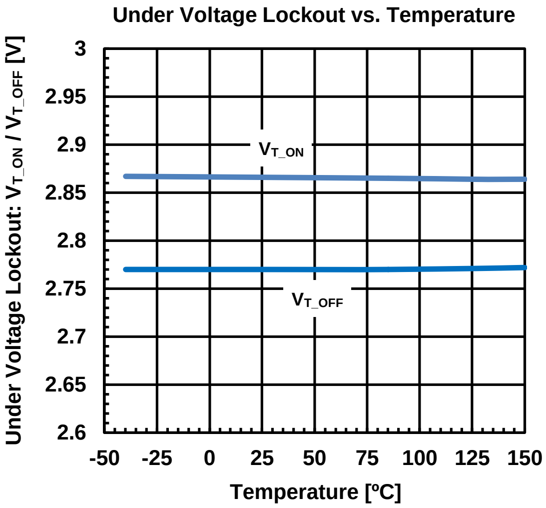


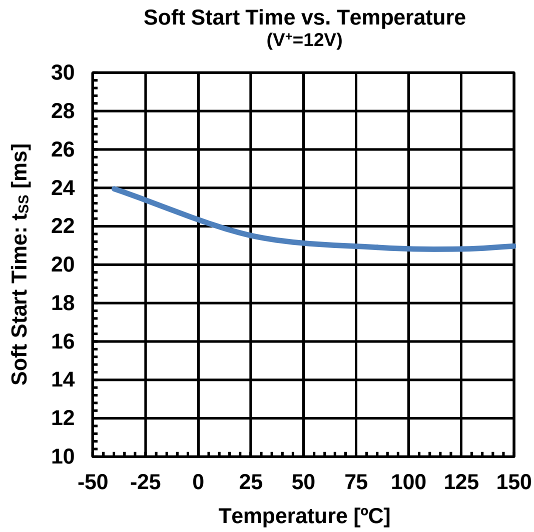






■ TYPICAL CHARACTERISTICS





■ PIN DISCRIPTION

PIN NO.	SYMBOL	Function
1	SW	Switch output pin of internal MOSFET.
2	V^+	Power supply input pin. Insert a bypass capacitor close to the V^+ pin – GND pin in order to lower high frequency impedance.
3	EN/SYNC	Standby control pin. The EN/SYNC pin is internally pulled down resistor. Normal Operation at the time of High Level. Standby Mode at the time of Low Level or OPEN. Also, it operates in synchronization with the clock frequency by inputting a external clock signal.
4	OVP	This pin detects output overvoltage. When the output voltage becomes the overvoltage detection value, divide the output voltage so that the OVP terminal voltage becomes 1.08 V typ.
5	FB	This pin detects the output voltage. The output voltage is divided and input so that the FB pin voltage becomes 1.0 V typ.
6	RT	Oscillation frequency setting pin to connect the timing resistor. Set the oscillation frequency between 100 kHz and 2.4 MHz.
7	COMP	Error amplifier output pin. The capacitor and resistor for phase compensation should be connected between COMP pin and GND pin.
8	GND	Ground pin
-	Exposed PAD	Exposed PAD on backside should be connected to ground and soldered to PCB.

Technical Information

■ **DESCRIPTION BLOCK FEATURES**

1. Basic Function

• **Error Amplifier Section (Error AMP)**

1.0V±1% precise reference voltage is connected to non-inverted input of this section.
Output voltage can be set by connection of converter's output to inverted input of this section (FB pin).
If the output voltage over 1.0V is required, a resistor divider must be inserted.

• **PWM Comparator Section (PWM), Oscillating Circuit Section (OSC)**

Oscillating frequency can be set by inserting resistor between the RT pin and GND. Refer to the sample characteristics in “Oscillating Frequency vs. Timing Resistor”, and set oscillation between 100kHz and 2.4MHz.,
Table 1. shows example of oscillating frequency and timing resistor. The resistance supports a series of E24 and a series of E96

Table 1. NJW4133 oscillating frequency and timing resistor.

Oscillating Frequency (MHz)	Timing Resistor (kΩ)	Oscillating Frequency (MHz)	Timing Resistor (kΩ)
0.1	82	1.2	5.9
0.2	41.2	1.4	4.87
0.3	27	1.6	4.12
0.4	20	1.8	3.48
0.5	15.8	2.0	3
0.6	13	2.1	2.8
0.7	11	2.2	2.67
0.8	9.53	2.3	2.49
0.9	8.25	2.4	2.32
1.0	7.32		

When the switching regulator operates at high oscillating frequency, the application can use a small inductor and capacitor.
If oscillating frequency is high, consider subject to efficiency reduction of the application and a restriction by minimum ON time.
Since the minimum ON time of NJW4133 designed 110ns(typ.), It needs to select the oscillation frequency at which the ON time of the boost application become over 110ns.
The ON time of boost converter is calculated the following formula.

$$t_{ON} = \frac{V_{OUT} - V_{IN}}{V_{OUT} \times f_{OSC}} \ [s]$$

When the ON time of boost application becomes below in 110ns(typ.), it may be occurred duty fluctuation and pulse skipping in order to maintain output voltage at a stable state.

■ **DESCRIPTION BLOCK FEATURES(Continuous)**

• **Maximum Duty Cycle and Oscillation Frequency**

The maximum duty cycle of NJW4133 operates at 95% typ. (f_{OSC}=300kHz)
Since the minimum OFF time is set to 65 ns typ., the faster the oscillation frequency, the lower the maximum duty cycle.

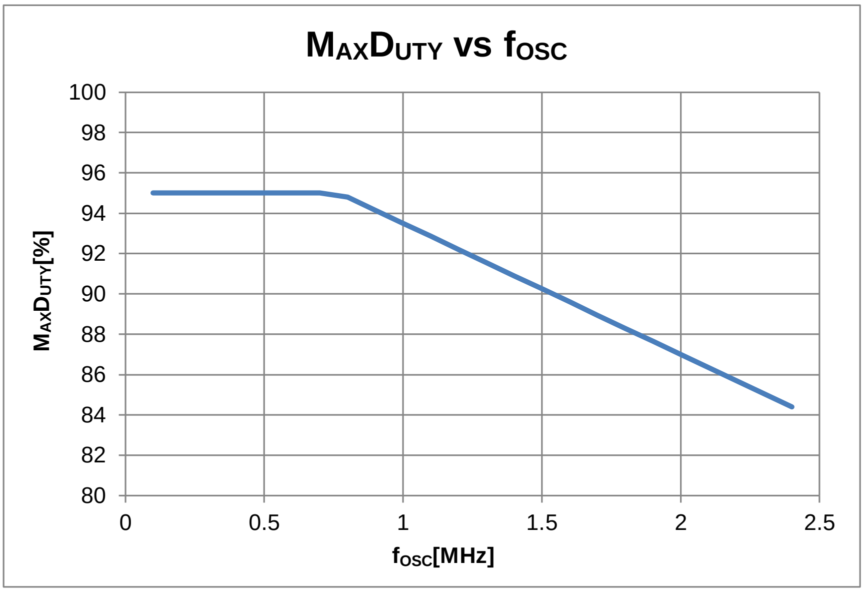


Fig.1 Maximum duty cycle vs. oscillation frequency.

• **POWER MOSFET**

Supply the power to the inductor by the switching operation of built-in power MOSFET.
Switching current is limited to 5.0A (min.) by overcurrent protection function.

• **Power Supply, GND pin (V^+, GND)**

In line with switching element drive, current flows into the IC according to frequency. If the power supply impedance provided to the power supply circuit is high, it will not be possible to take advantage of IC performance due to input voltage fluctuation. Therefore insert a bypass capacitor close to the V+ pin – the GND pin connection in order to lower high frequency impedance.

■ DESCRIPTION BLOCK FEATURES(Continuous)

2.Additional and Protection Function

• Over Voltage Protection(OVP)

Prevent the overvoltage when normal control of output voltage isn't performed due to any reasons.
Switching is stopped when the OVP pin voltage reaches 1.08 V(typ.) and overvoltage protection is released when it decreases to 1.04 V typ.

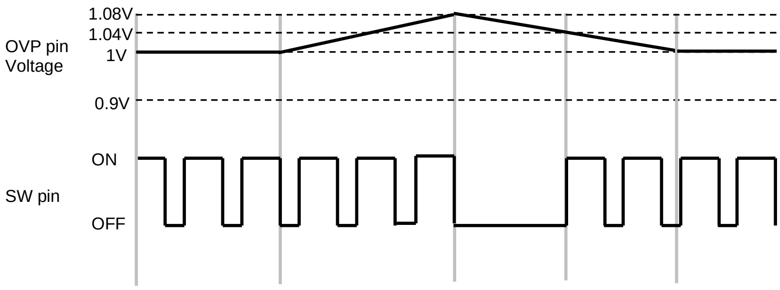


Fig.2 Timing chart of overvoltage protection function (Assumes function stop of Error AMP.)

• Under Voltage Lockout (UVLO)

In case of the supply voltage is low, the IC operation is stopped by the UVLO circuit.
The UVLO is released above V^+=2.85V(typ.) and IC operation starts. Then, power supply voltage decrease below 2.85V(typ.), IC is stopped operation by the UVLO. There is 100mV(typ.) hysteresis voltage between detection and release to prevent the malfunction.

• Soft Start Function (Soft Start)

The output voltage rises gradually to the setting value by the soft start function. The soft start time is 20ms (typ.) and It is defined as the time until error amplifier reference voltage reaches 0V to 0.95V.
The soft start circuit operates after the release UVLO and/or recovery from thermal shutdown.

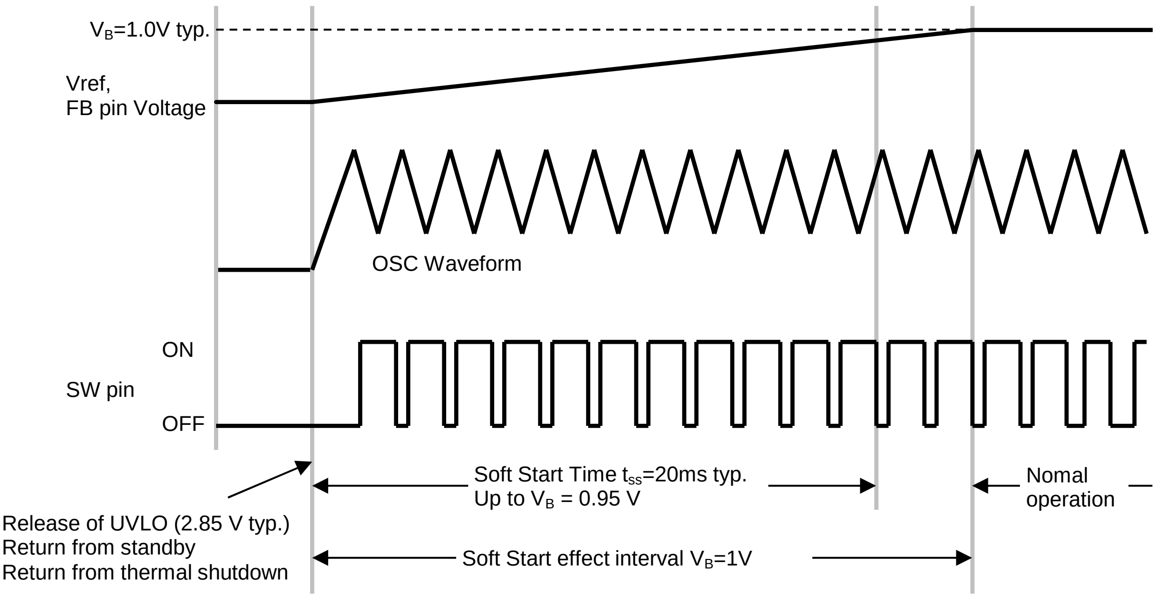


Fig.3 Soft start timing chart

■ **DESCRIPTION BLOCK FEATURES(Continuous)**

• Over Current Protection Function (OCP)

The NJW4133 contains Hiccup overcurrent protection and decrease heat generation at the overload.
Then, output voltage of the switching regulator returns automatically when recovering from an abnormal state.
If the overcurrent is detected continuously for 128 pulses while the FB pin voltage is 0.75 V or less, the overcurrent protection function turns off the MOSFET.
After stopping, NJW4133 restarts by soft start after the cool down time of 500ms(typ.).

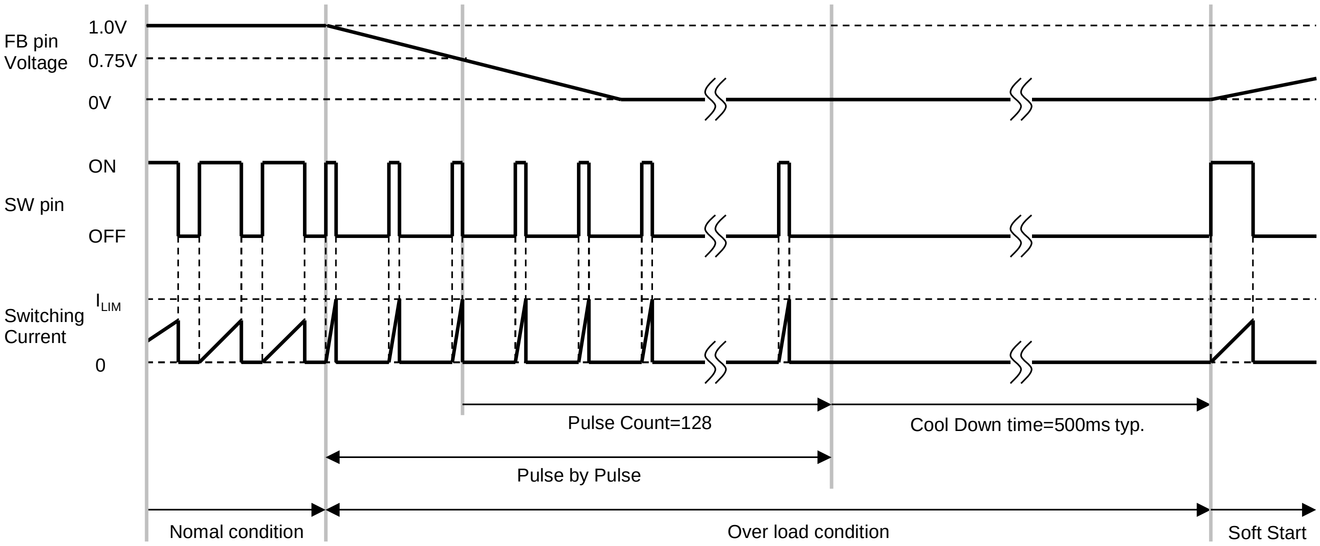


Fig.4 OCP Timing chart

• Thermal Shutdown Function (TSD)

When Junction temperature of the NJW4133 exceeds the 170°C*, switching operation is stopped by internal thermal shutdown circuit. When junction temperature decreases to 150°C* or less, switching operation is returned with soft start function.
The thermal shutdown function is a preliminary circuit to prevent thermal runaway of the IC at high temperature and not to compensate for inappropriate thermal design. Thermal design should be designed with a margin to operate within IC junction temperature (~ + 150°C).
(* Design value)

• Standby Function

The NJW4133 is stopped the operating and becomes standby status by setting EN/SYNC pin to 0.5V(max.)or less.
The EN/SYNC pin is pulled down by resistor internally, therefore the NJW4133 becomes standby mode when the EN/SYNC pin is OPEN. When not using the standby function, connect the EN / SYNC pin to V^+.

■ **DESCRIPTION BLOCK FEATURES(Continuous)** Technical Information

• External Clock Synchronization

The NJW4133 can synchrnize to the external frequency by inputting a square wave to the EN / SYNC pin. The square wave must meet the specifications in Table 2.

Table 2 The input square wave to an EN/SYNC pin.

	Condition
Input Frequency	$f_{OSC}\times0.9$ to $f_{OSC}\times1.7$ 2,800kHz maximum
Duty Cycle	40% to 60%
Voltage magnitude	High level 1.6V or more Low level 0.5Vor less

The switching operation during external clock synchronization triggers on the rising edge of the input signal. Also, it has the delay time to prevent malfunction when switching from standby state or asynchronous operation to external clock synchronous operation. Table 3 shows the delay time with respect to the oscillation frequency, and Figure 5 shows the timing chart.

Table 3 Oscillating frequency and delay time.

Delay time(µs)		
f_{OSC}=300kHz	f_{OSC}=1MHz	f_{OSC}=2.4MHz
10 to 60	3 to 20	1.5 to 10

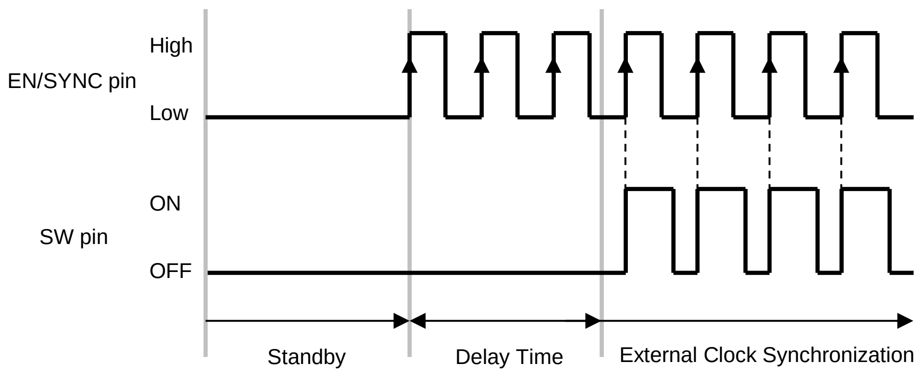


Fig.5 Switching Operation by External Synchronized Clock

■ **APPLICATION INFORMATION**

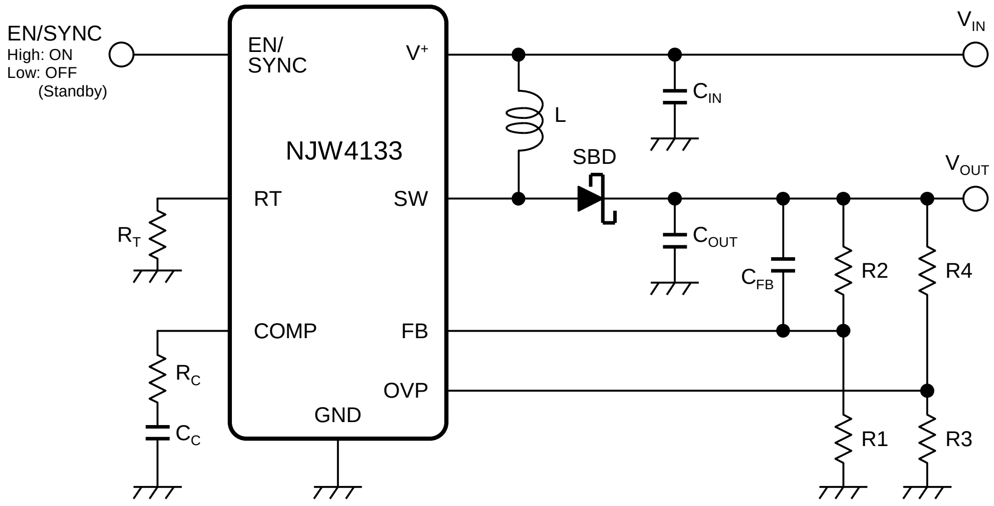


Fig.6 NJW4133 Boost converter configuration example

• **Inductor**

Since large current flows in the inductor, it is necessary to have current capability that does not saturate.
In the case of small inductor value, the peak current increases and conversion efficiency tends to decrease. (refer to Fig.7)

Peak current is calculated by the following formula

$$I_{IN}=\frac{V_{OUT}\times I_{OUT}}{\eta\times V_{IN}}[A]$$

$$\Delta I_L=\frac{(V_{OUT}-V_{IN})\times V_{IN}}{L\times V_{OUT}\times f_{OSC}}[A]$$

$$I_{PK}=I_{IN}+\frac{\Delta I_L}{2}[A]$$

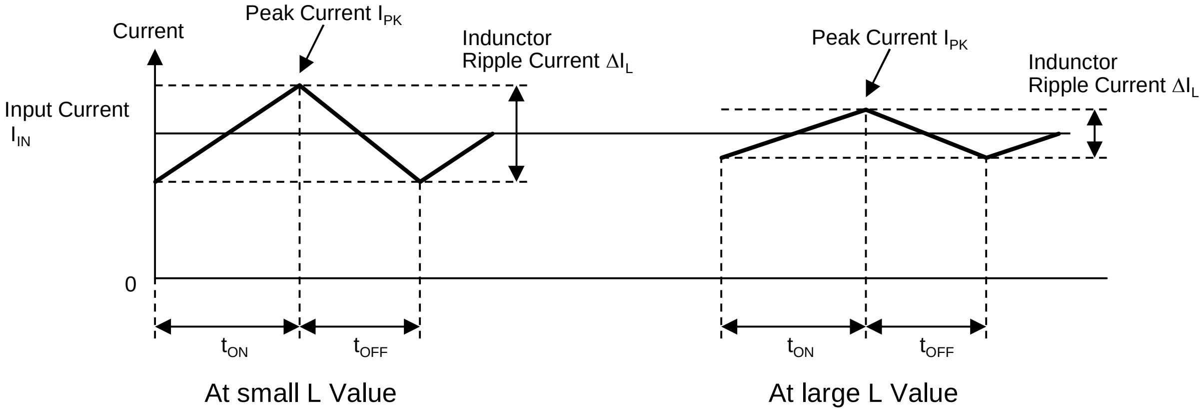


Fig.7 Inductor Current State Transition (Continuous Conduction Mode)

In many cases, the value of the inductor is determined by the oscillation frequency.(Table.4)

■ APPLICATION INFORMATION(Continuous)

Table. 4 Oscillating frequency and Inductor value

Oscillating frequency [MHz]	Inductor value [µH]
0.1	22
0.3	10
0.5	4.7
1	3.3
1.5	2.2
2	1.5
2.4	1

The Inductor value is the theoretical value.
This value varies depending on application specifications, used parts etc.
Please make fine adjustment with user's application.

- **Input Capacitor**

Transient current depending on the frequency flows at the input section of the switching regulator
If the power supply line impedance is high, it will lead to input voltage fluctuations and the performance of the NJW4133 cannot be fully drawn out. Therefore insert an input capacitor as close to the IC as possible.
A ceramic capacitor is the optimal for input capacitor.

The RMS ripple input current is calculated by the following formula.

$$I_{RMS}=0.3\times\Delta I_L[A]$$

- **Output Capacitor**

An output capacitor stores power from the inductor, and stabilizes voltage provided to the output.
A ceramic capacitor is the optimal for output capacitor.
Since the capacitance of a ceramic capacitor decreases due to DC bias voltage and temperature drift, check the characteristics with a spec sheet etc.
The capacitance of a ceramic capacitor is calculated by the following formula.

$$C_{OUT}>\frac{30}{V_{OUT}\times f_{OSC}}\times 10^6[\mu F]$$

To select the output capacitor, it is necessary to consider characteristics of ESR (Equivalent Series Resistance), ripple current and breakdown voltage.

The ripple voltage can be reduced by using a low ESR capacitor.
The ripple voltage is calculated by the following formula.

$$V_{ripple(p\text{-}p)}=ESR\times\Delta I_L[V]$$

The ripple current through capacitor is calculated by the following formula.

$$I_{RMS}=\sqrt{I_{PK}^2-I_{OUT}^2}[A]$$

■ APPLICATION INFORMATION(Continuous)

• **Catch Diode**

During the OFF cycle of the power MOSFET, the power stored in the inductor flows through the catch diode into the output capacitor.
Therefore, electric current depending on the load current flows into the diode every OFF cycle.
Since a diode's forward saturation voltage and the current accumulation cause power loss, a Schottky Barrier Diode(SBD) which has a low forward saturation voltage is the most suitable.
During the ON cycle of the MOSFET, reverse voltage is applied to the diode.
Consider the margin for the withstand voltage of the diode with respect to the output voltage.
Also, it is important to consider reverse current at high temperature when selecting SBD.
SBD has larger reverse current characteristics than a general diode. If the reverse current is large, it leads to diode loss, so check the SBD specifications.

• **Setting of Output voltage**

The output voltage V_{OUT} is determined by the relative resistances of R1, R2.
The currents flowing through R1 and R2 need to be sufficiently larger than the bias current of the error amplifier.
The output voltage is calculated the following formula.

$$V_{OUT}=\left[\frac{R2}{R1}+1\right]\times V_{FB}[V]$$

• **Setting of Over Voltage Protection**

The over voltage protection value is determined by the relative resistances of R3, R4.
The current flowing to R3 and R4 need to be sufficiently larger than the bias current into the OVP pin.
The over voltage protection value is calculated the following formula.

$$V_{OVP}=\left[\frac{R4}{R3}+1\right]\times V_{REF\_OVP}[V]$$

■ APPLICATION INFORMATION(Continuous)

• Phase Compensation design example

A switching regulator needs a feedback circuit to stabilize the output voltage.
Frequency characteristics of the application change due to inductance, output capacitor, etc.
So it is ideal phase compensation design that can obtain the maximum bandwidth while ensuring the phase margin necessary for stable operation.
For the phase compensation designs, actual machine adjustment is also important. Ultimately please select a constant while considering the application specification.

Feedback and Stability

Basically, the feedback loop should be designed the open loop phase shift less than -180 ° at frequency where the loop gain is 0 dB.
It is also important that the loop characteristics have margin in consideration of ringing and immunity to oscillation during load fluctuations. The NJW4133 can arbitrarily design the feedback circuit, so it is possible to optimize the placement of Pole and Zero, which are important for loop compensation.

The characteristics of the Pole and Zero are shown in Fig. 8

Pole: The gain has a slope of -20 dB/dec, and the phase shifts -90.
Zero: The gain has a slope of +20 dB/dec, and the phase shifts +90.

If the number of factors constituting Pole is “n”, the gain phase change will also be “n”-fold. It is the same for Zero. The Pole and Zero are in a reciprocal relationship, so if there is one factor for each Pole and Zero, they will cancel each other.

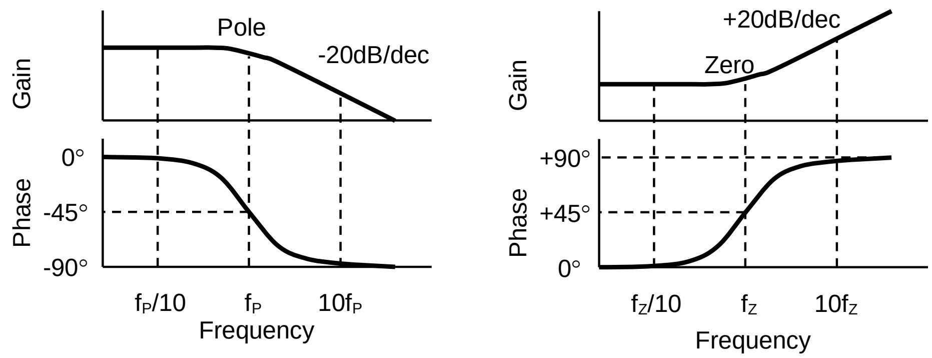


Fig.8 Characteristics of Pole and Zero

■ APPLICATION INFORMATION

Technical Information

• Setting of Pole and Zero

The position of the Pole and Zero are determined by the application condition and error amplifier setting.
Fig. 9 shows phase compensation circuit and Table 5. shows setting of Pole and Zero.

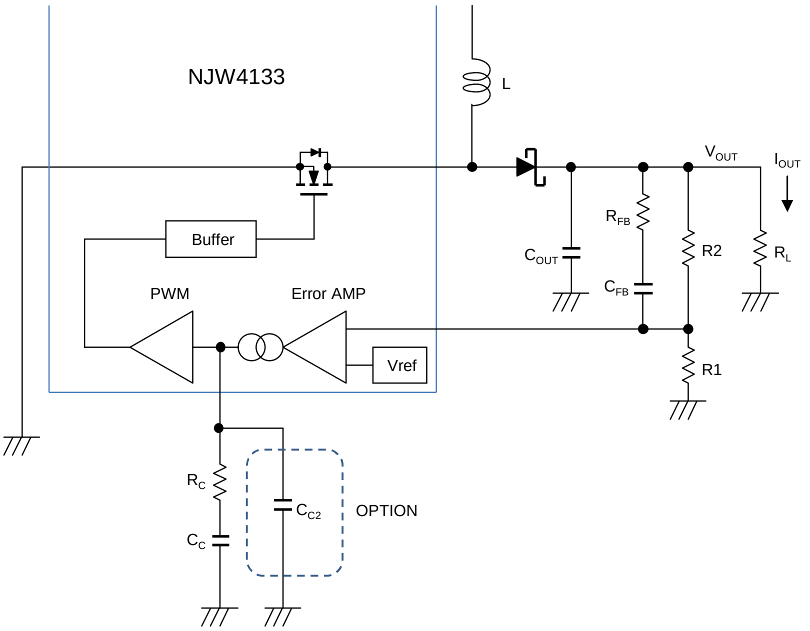


Fig. 9 Phase compensation Circuit Configuration

Table.5 Setting of Pole and Zero

Symbol	Calculating formula	Setting example	description
f_{P1}	$f_{P1}=\frac{1}{2\times\pi\times\frac{A_V}{gm}\times C_C}$	$f_{P1}<\frac{f_{ZRPH}}{10000}\sim\frac{f_{ZRPH}}{5000}$	A position of 1st pole f_{P1} is fixed by C_C connected to the output of the error amplifire
f_{ZRPH}	$f_{ZRPH}=\frac{(1-D)^2\times\frac{V_{OUT}}{I_{OUT}}}{2\times\pi\times L}$		The position of f_{ZRPH} is determined by input / output condition, L value and load current. It is recommended to limit the f_{0dB} frequency of the loop gain to the upper limit of 1/5 to 1/10 of f_{ZRPH}.
f_{POUT}	$f_{POUT}=\frac{1}{2\times\pi\times\frac{V_{OUT}}{I_{OUT}}\times C_{OUT}}$	$1<\frac{f_{Z1}}{f_{POUT}}<15$	The pole f_{POUT} is caused by capacitor and load resistance connected to the output. In the case, the load resistance asumes a maximum load current and calculates. When it uses a ceramic capacitor for C_{OUT}, it us realistic to calculate at effective capacitance in consideration of DC bias.
f_{Z1}	$f_{Z1}=\frac{1}{2\times\pi\times R_C\times C_C}$		A position of zero f_{Z1} is fixed by R_C and C_C connected to the output of the error amplifire
f_{Z2}	$f_{Z2}=\frac{1}{2\times\pi\times R2\times C_{FB}}$	20kHz to 60kHz	It should be set when it is difficult to secure phase margin.

Various Pole are occurred at hundreds of kHz and above, so it should be set the loop gain 0 dB frequency to 1/5 to 1/10 of the oscillation frequency as the upper limit

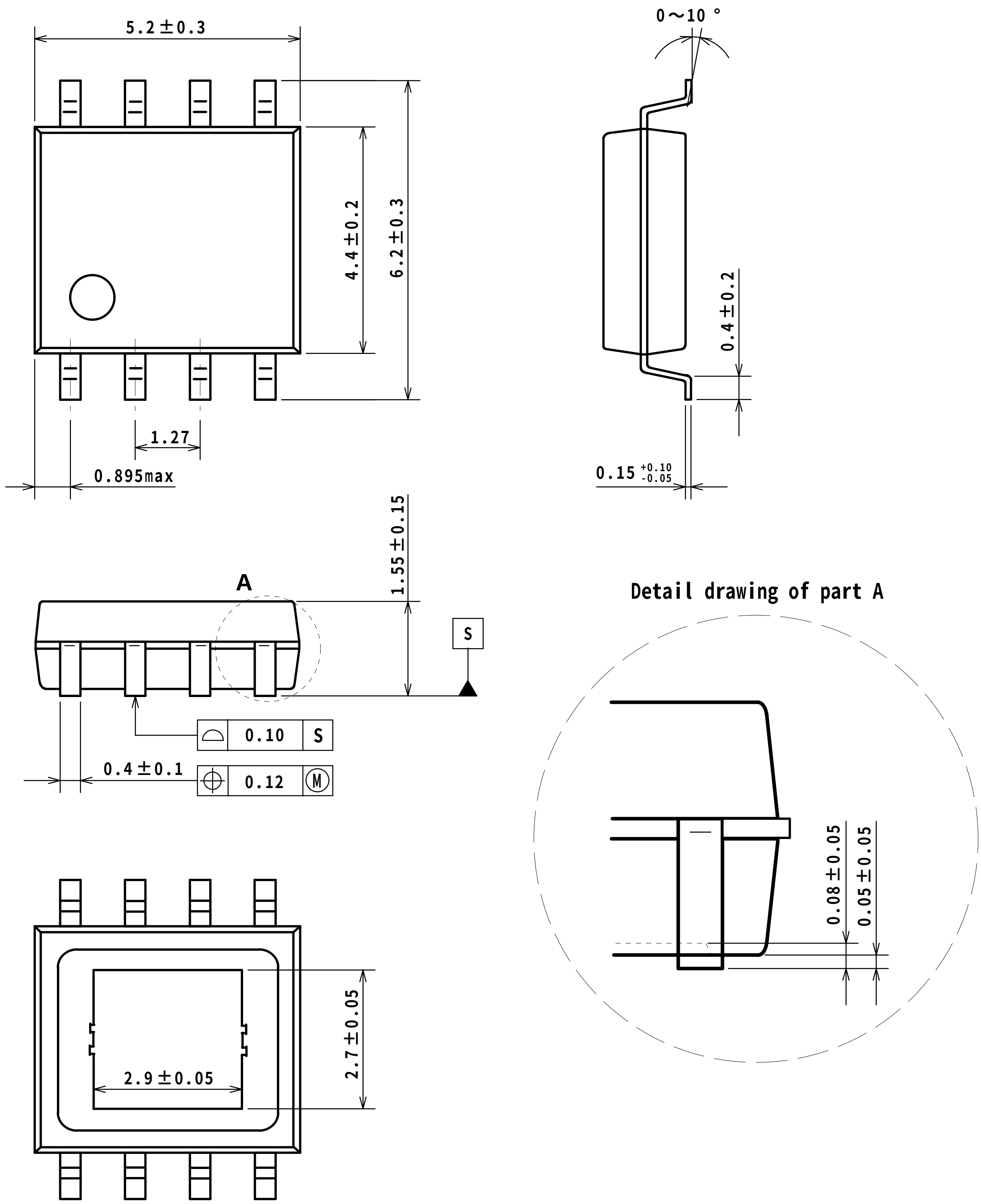
In case of high oscillating frequency, in order to ensure sufficient phase margin, keep the loop gain 0 dB frequency to around 100 kHz.

Also, Also, when the loop gain becomes unstable in the high frequency region, please adjust the actual equipment using R_{FB}, C_{C2}.

■ PACKAGE DIMENSIONS

HSOP8

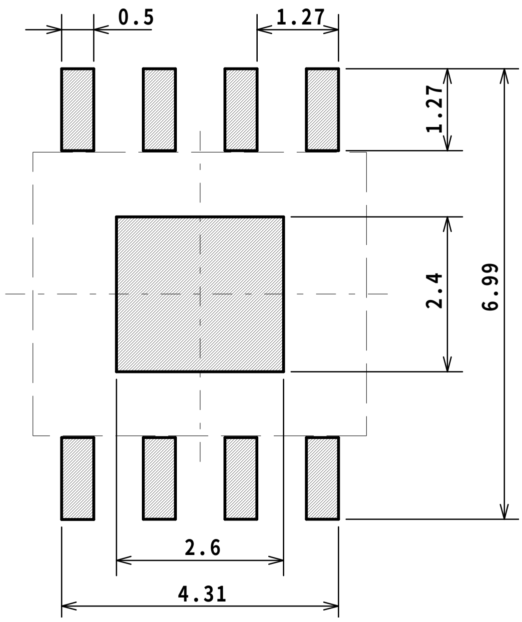
Unit: mm



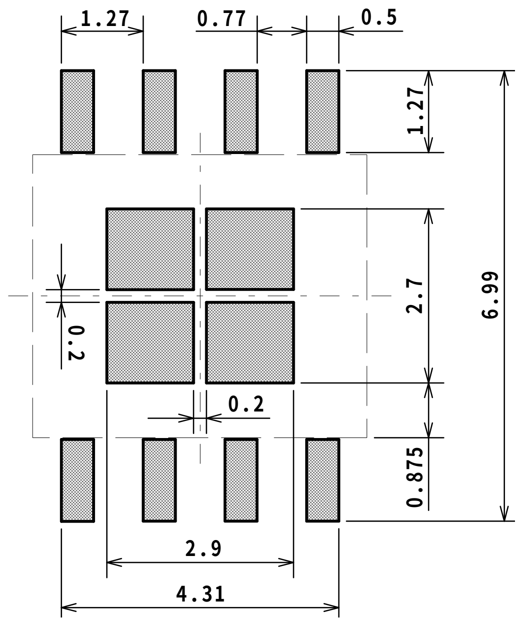
■ EXAMPLE OF SOLDER PADS DIMENSION

HSOP8

Unit: mm



<Solder pattern>



<Metal mask>

<Instructions for mounting>

Please note the following points when you mount HSOP-8 package IC because there is a standoff on the backside electrode.

(1) Temperature profile of lead and backside electrode.

It is necessary that both re-flow temperature profile of lead and backside electrode are higher than preset temperature.

When solder wet temperature is lower than lead/backside electrode temperature, there is possibility of defect mounting.

(2) Design of foot pattern / metal mask

Metal mask thickness of solder pattern print is more than 0.13mm.

(3) Solder paste

The mounting was evaluated with following solder paste, foot pattern and metal mask.

Because mounting might be greatly different according to the manufacturer and the product number even if the solder composition is the same.

We will strongly recommend to evaluate mounting previously with using foot pattern, metal mask and solder paste.

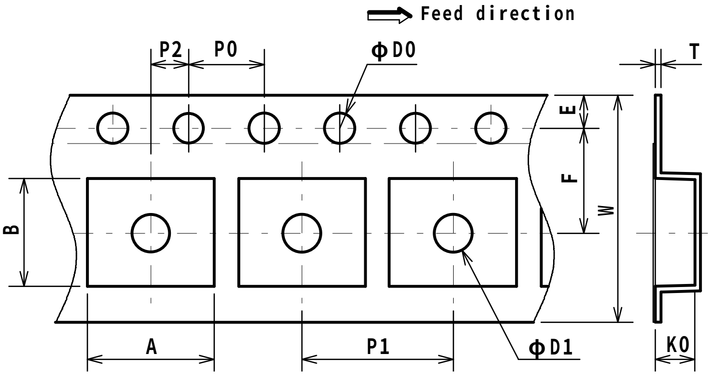
Solder paste composition	Sn37Pb (Senju Metal Industry Co., Ltd: OZ7053-340F-C)
	Sn3Ag0.5Cu (Senju Metal Industry Co., Ltd: M705-GRN350-32-11)

HSOP8

■ PACKAGING SPEC

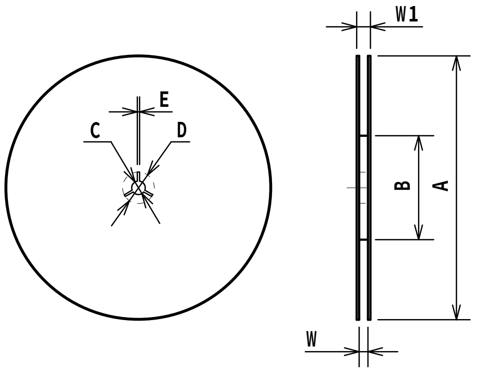
Unit: mm

TAPING DIMENSIONS



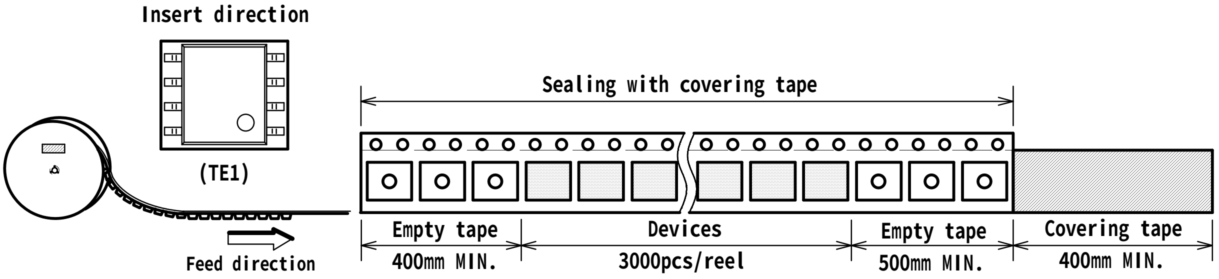
SYMBOL	DIMENSION	REMARKS
A	6.7±0.1	
B	5.55±0.1	
D0	1.55±0.05	
D1	2.05±0.05	
E	1.75±0.1	
F	5.5±0.05	
P0	4.0±0.1	
P1	8.0±0.1	
P2	2.0±0.05	
T	0.3±0.05	
T2	2.47	
K0	2.1±0.1	
W	12.0±0.2	

REEL DIMENSIONS

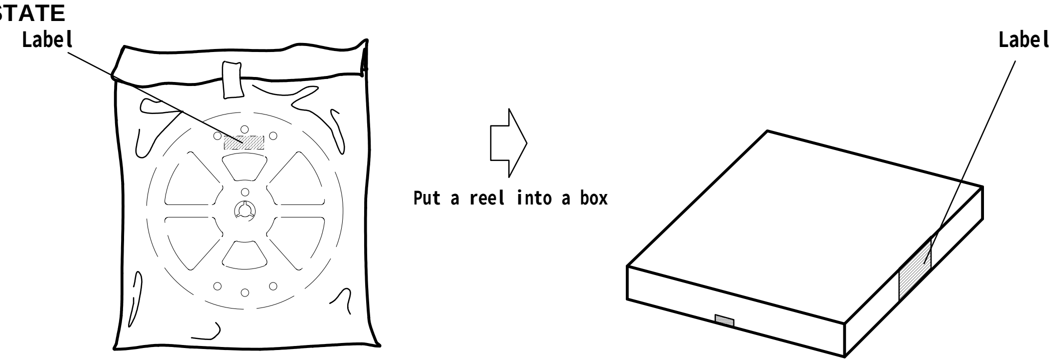


SYMBOL	DIMENSION
A	φ330±2
B	φ 80±1
C	φ 13±0.2
D	φ 21±0.8
E	2±0.5
W	13.5±0.5
W1	17.5±1

TAPING STATE



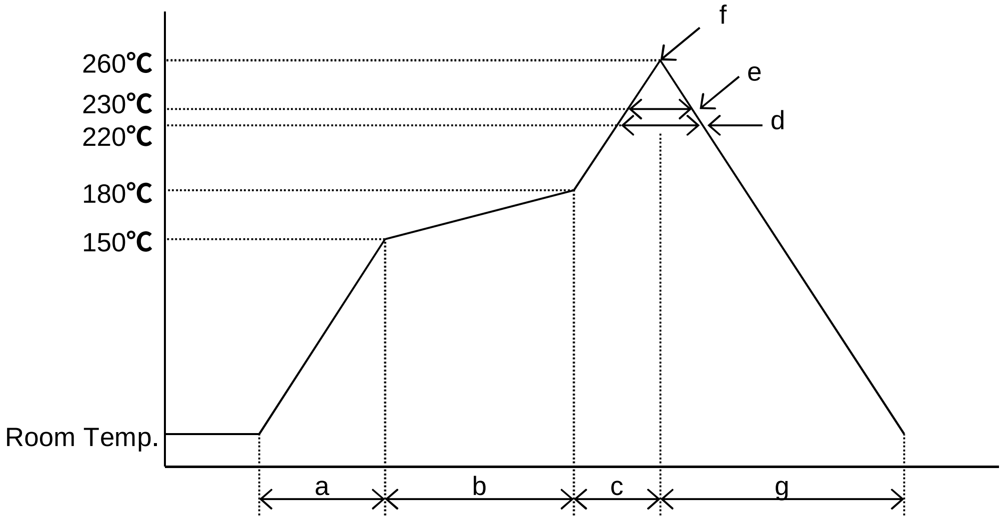
PACKING STATE



■ RECOMMENDED MOUNTING METHOD

・INFRARED REFLOW SOLDERING METHOD

＊Recommended reflow soldering procedure



a：Temperature ramping rate	: 1 to 4℃/s
b：Pre-heating temperature	: 150 to 180℃
time	: 60 to 120s
c：Temperature ramp rate	: 1 to 4℃/s
d：220℃ or higher time	: Shorter than 60s
e：230℃ or higher time	: Shorter than 40s
f：Peak temperature	: Lower than 260℃
g：Temperature ramping rate	: 1 to 6℃/s

The temperature indicates at the surface of mold package.

■ REVISION HISTORY

DATE	REVISON	CHANGES
22.Mar.2018	Ver. 1.0	New Release
18.Mar.2019	Ver. 1.1	Correct the error : OCP Timing chart
01.Sep.2021	Ver. 2.0	SW leak current test condition of Electrical Characteristics Typical Characteristics(format) Technical Information Corrected of Application

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