

HIGH VOLTAGE $I_o = 500 \text{ mA}$ ADJUSTABLE LDO REGULATOR

■ FEATURES*

- AEC-Q100 grade 1 qualified
- Fast transient response
- Wide operating voltage $4.0 \text{ V to } 40 \text{ V}$
- Wide operating temperature $T_a = -40^\circ\text{C} \text{ to } 125^\circ\text{C}$
- High-accuracy ADJ voltage
 $V_{ADJ} = 1.24 \text{ V} \pm 1.0\% \text{ } (T_a = 25^\circ\text{C})$
 $V_{ADJ} = 1.24 \text{ V} \pm 2.0\% \text{ } (T_a = -40^\circ\text{C} \text{ to } 125^\circ\text{C})$
- Adjustable output voltage range $2.5 \text{ V to } 16 \text{ V}$
- Output current $500 \text{ mA } (\text{min})$
- ON/OFF control
- Ceramic capacitor compatible
- Undervoltage lockout
- Thermal shutdown
- Overcurrent protection
- Package TO-252-5-L5

■ APPLICATIONS*

- Car infotainment
- Automotive ECUs
- Industrial equipment

*T1 grade is not recommended for powertrain, vehicle electrification and autonomous driving related applications.

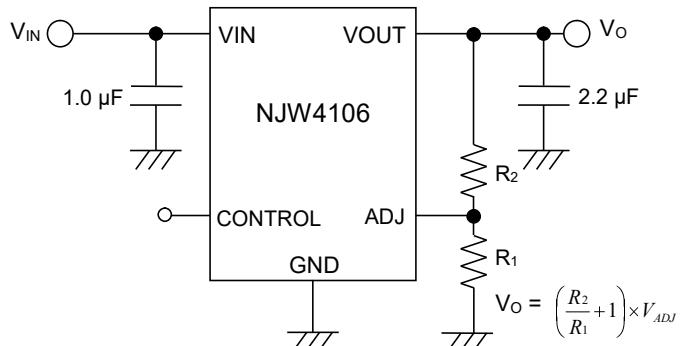
■ DESCRIPTION

The NJW4106-T1 is a 45 V, $I_o = 500 \text{ mA}$ fast transient response low dropout regulator. This device achieves fast transient response and offers stable output voltage at line or load fluctuations.

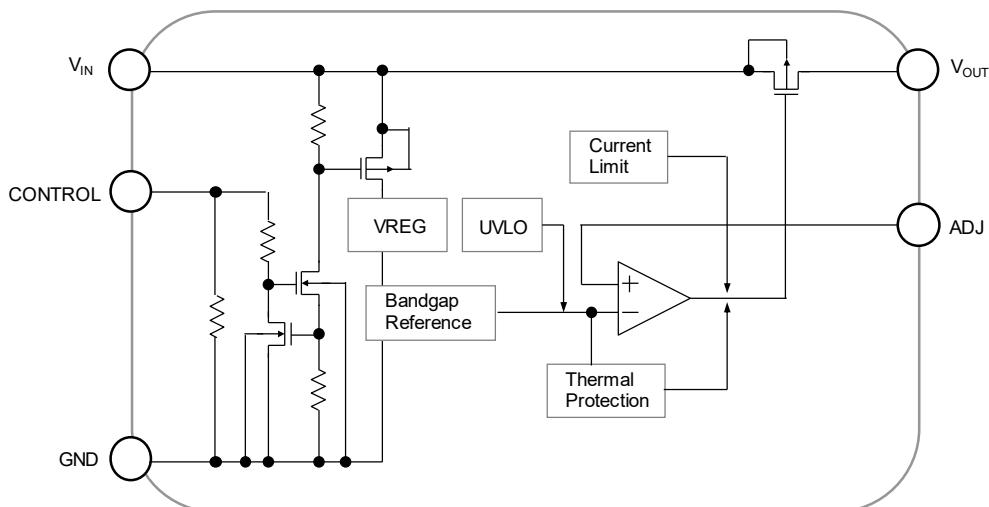
The NJW4106-T1 provides outstanding high ADJ voltage accuracy that guaranteed $1.24 \text{ V} \pm 2.0\%$ under the conditions of $V_{IN} = V_o + 1 \text{ V}$ to 40 V , $I_o = 0 \text{ mA}$ to 500 mA , and $T_a = -40^\circ\text{C}$ to 125°C .

Moreover, wide operating voltage and wide operating temperature makes the NJW4106-T1 ideal for automotive equipment or applications that require high reliability.

■ TYPICAL APPLICATION

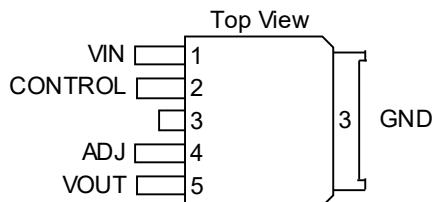


■ BLOCK DIAGRAM



■ PIN CONFIGURATION

TO-252-5-L5



PIN NO.	NAME	FUNCTION
1	VIN	Input pin
2	CONTROL	ON/OFF control pin
3	GND	Ground pin
4	ADJ	Output voltage adjustment pin
5	VOUT	Output pin

■ PRODUCT NAME INFORMATION

NJW4106 DL5 - T1 - (TE1)
 Part Number Package Grade Taping Form
 DL5: TO-252-5-L5 T1: Automotive*

* The detail information of automotive grades and recommended applications are described in NJR website.
https://www.njr.com/electronic_device/semiconductor/application/automotive.html.

■ ORDERING INFORMATION

PRODUCT NAME	PACKAGE	RoHS	HALOGEN-FREE	TERMINAL FINISH	MARKING	WEIGHT (mg)	MOQ (pcs)
NJW4106DL5-T1 (TE1)	TO-252-5-L5	Yes	Yes	Sn-2Bi	4106T1	301	3000

■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Input Voltage	V _{IN}	-0.3 to 45	V
Control Pin Voltage	V _{CONT}	-0.3 to 45	V
ADJ Pin Voltage	V _{ADJ}	-0.3 to 6	V
Output Voltage	V _O	-0.3 to V _{IN} ≤ +17 ⁽¹⁾	V
Power Dissipation (T _a = 25°C) TO-252-5-L5	P _D	2-Layer / 4-Layer / High Power 4-Layer 870 ⁽²⁾ / 3000 ⁽³⁾ / 4700 ⁽⁴⁾	mW
Junction Temperature	T _j	-40 to 150	°C
Storage Temperature	T _{stg}	-50 to 150	°C

(1) When the input voltage is less than 17 V, the absolute maximum output voltage is equal to the input voltage. If the input voltage is below 17 V, the maximum output voltage is 17 V.

(2) 2-Layer: Mounted on glass epoxy board (76.2 mm × 114.3 mm × 1.6 mm: based on EIA/JEDEC standard, 2-layer FR-4).

(3) 4-Layer: Mounted on glass epoxy board (76.2 mm × 114.3 mm × 1.6 mm: based on EIA/JEDEC standard, 4-layer FR-4).

(For 4-layer: Applying 74.2 mm × 74.2 mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5.)

(4) High Power 4-Layer: Mounted on glass epoxy board (76.2 mm × 114.3 mm × 1.6 mm, 4-layer FR-4).

(For 4-layer: Applying 74.2 mm × 74.2 mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5.)

*For the specifications of each board, see the Board Specifications of THERMAL CHARACTERISTICS.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Operating Voltage	V _{IN}	4.0 to 40	V
Control Voltage	V _{CONT}	0 to 40	V
Output Voltage Setting	V _O	2.5 to 16	V
Output Voltage Setting Resistor	R ₁	5 to 500	kΩ
Output Current	I _O	0 to 500	mA
Operating Temperature	T _{opr}	-40 to 125	°C

■ ELECTRICAL CHARACTERISTICS

$V_o \geq 3 \text{ V}$: $V_{IN} = V_o + 1 \text{ V}$, $C_{IN} = 1.0 \mu\text{F}$, $C_O = 2.2 \mu\text{F}$, $R1 = 250 \text{ k}\Omega$, $T_a = 25^\circ\text{C}$
 $V_o < 3 \text{ V}$: $V_{IN} = 4.0 \text{ V}$, $C_{IN} = 1.0 \mu\text{F}$, $C_O = 4.7 \mu\text{F}$, $R1 = 250 \text{ k}\Omega$, $T_a = 25^\circ\text{C}$, unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADJ Voltage	V_{ADJ}	$V_{IN} = 4 \text{ V to } 40 \text{ V} (V_o < 3 \text{ V})$, $V_{IN} = V_o + 1 \text{ V to } 40 \text{ V} (V_o \geq 3 \text{ V})$, $I_o = 0 \text{ mA to } 500 \text{ mA}$	-1.0%	1.24	+1.0%	V
		$V_{IN} = 4 \text{ V to } 40 \text{ V} (V_o < 3 \text{ V})$, $V_{IN} = V_o + 1 \text{ V to } 40 \text{ V} (V_o \geq 3 \text{ V})$, $I_o = 0 \text{ mA to } 500 \text{ mA}, T_a = -40^\circ\text{C to } 125^\circ\text{C}$	-2.0%	-	+2.0%	
Quiescent Current	I_Q	$I_o = 0 \text{ mA, except } I_{CONT}$	-	65	105	μA
		$I_o = 0 \text{ mA, except } I_{CONT}, T_a = -40^\circ\text{C to } 125^\circ\text{C}$	-	-	115	
Quiescent Current at Control OFF	$I_{Q(OFF)}$	$V_{CONT} = 0 \text{ V}$	-	-	1	μA
		$V_{CONT} = 0 \text{ V}, T_a = -40^\circ\text{C to } 125^\circ\text{C}$	-	-	1	
Output Current	I_o	$V_o \times 0.9$	500	-	-	mA
		$V_o \times 0.9, T_a = -40^\circ\text{C to } 125^\circ\text{C}$	500	-	-	
Line Regulation	$\Delta V_o / \Delta V_{IN}$	$V_{IN} = V_o + 1 \text{ V to } 40 \text{ V}, I_o = 30 \text{ mA}, V_o = 5.0 \text{ V}$	-	-	34.0	mV
		$V_{IN} = V_o + 1 \text{ V to } 40 \text{ V}, I_o = 30 \text{ mA}, V_o = 5.0 \text{ V}, T_a = -40^\circ\text{C to } 125^\circ\text{C}$	-	-	51.0	
Load Regulation	$\Delta V_o / \Delta I_o$	$I_o = 0 \text{ mA to } 500 \text{ mA}, V_o = 5.0 \text{ V}$	-	-	22.5	mV
		$I_o = 0 \text{ mA to } 500 \text{ mA}, V_o = 5.0 \text{ V}, T_a = -40^\circ\text{C to } 125^\circ\text{C}$	-	-	45.0	
Ripple Rejection	RR	$V_{IN} = V_o + 1 \text{ V}, e_{IN} = 200 \text{ mVrms}, f = 1 \text{ kHz}, I_o = 30 \text{ mA}, V_o = 5.0 \text{ V}$	-	53	-	dB
Dropout Voltage 1	ΔV_{IO1}	$I_o = 300 \text{ mA}$	-	0.24	0.42	V
		$I_o = 300 \text{ mA}, T_a = -40^\circ\text{C to } 125^\circ\text{C}$	-	-	0.60	
Dropout Voltage 2	ΔV_{IO2}	$I_o = 500 \text{ mA}$	-	0.40	0.70	V
		$I_o = 500 \text{ mA}, T_a = -40^\circ\text{C to } 125^\circ\text{C}$	-	-	1.00	
Control Current	I_{CONT}	$V_{CONT} = 1.6 \text{ V}$	-	0.5	2.0	μA
		$V_{CONT} = 1.8 \text{ V}, T_a = -40^\circ\text{C to } 125^\circ\text{C}$	-	-	3.0	
Control Voltage for ON-State	$V_{CONT(ON)}$		1.6	-	-	V
		$T_a = -40^\circ\text{C to } 125^\circ\text{C}$	1.8	-	-	
Control Voltage for OFF-State	$V_{CONT(OFF)}$		-	-	0.6	V
		$T_a = -40^\circ\text{C to } 125^\circ\text{C}$	-	-	0.6	
UVLO Release Voltage	V_{UVLO}	$V_{IN} = \text{low to high}$	2.3	2.7	3.1	V
		$V_{IN} = \text{low to high}, T_a = -40^\circ\text{C to } 125^\circ\text{C}$	2.2	-	3.2	
UVLO Hysteresis Voltage	V_{HYS}	$V_{IN} = \text{high to low}$	200	500	-	mV
		$V_{IN} = \text{high to low}, T_a = -40^\circ\text{C to } 125^\circ\text{C}$	200	-	-	
Average Temperature Coefficient of Output Voltage	$\Delta V_o / \Delta T_a$	$T_a = -40^\circ\text{C to } 125^\circ\text{C}, I_o = 30 \text{ mA}$	-	± 50	-	$\text{ppm}/^\circ\text{C}$

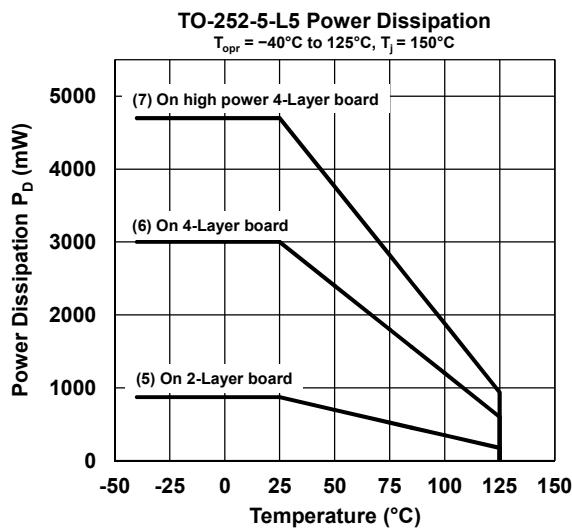
■ THERMAL CHARACTERISTICS

PARAMETER	SYMBOL	VALUE	UNIT
Junction-To-Ambient Thermal Resistance TO-252-5-L5	θ_{ja}	2-Layer / 4-Layer / High Power 4-Layer 143 ⁽⁵⁾ / 41 ⁽⁶⁾ / 26 ⁽⁷⁾	°C/W
Junction-To-Top of Package Characterization Parameter TO-252-5-L5	Ψ_t	2-Layer / 4-Layer / High Power 4-Layer 30 ⁽⁵⁾ / 15 ⁽⁶⁾ / 11 ⁽⁷⁾	°C/W

■ BOARD SPECIFICATIONS

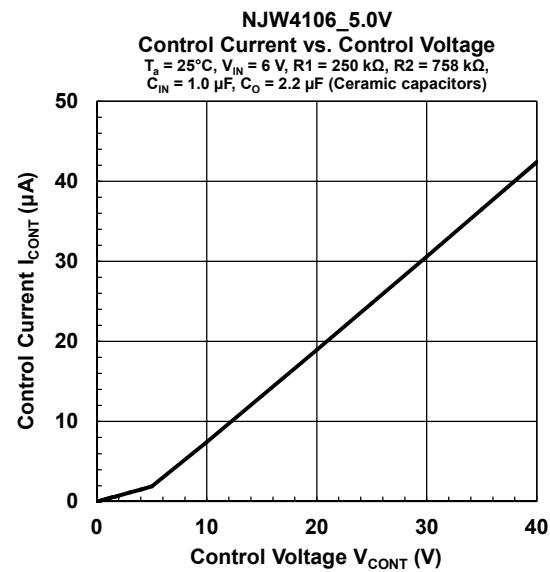
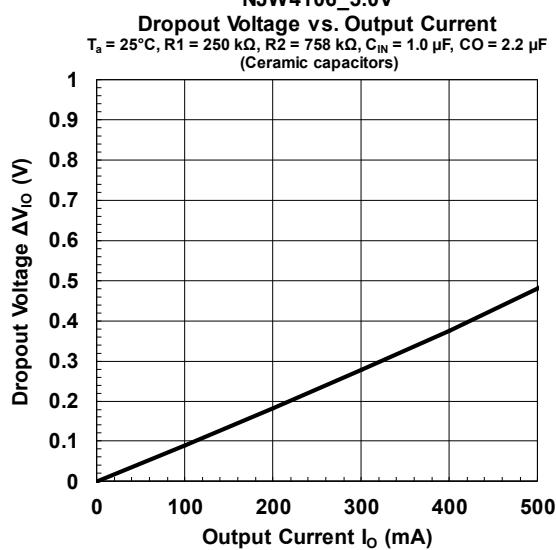
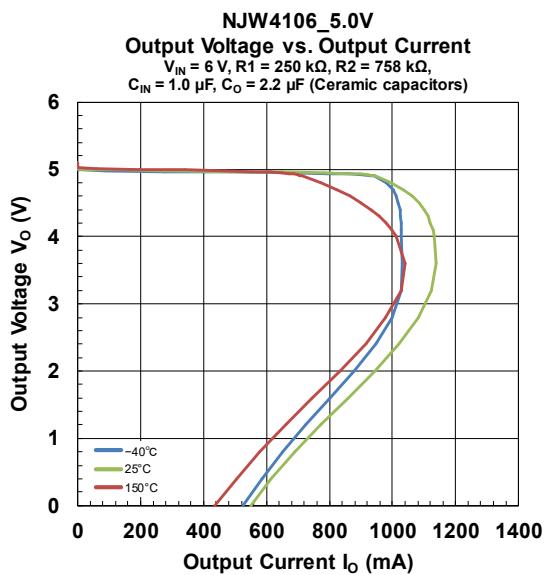
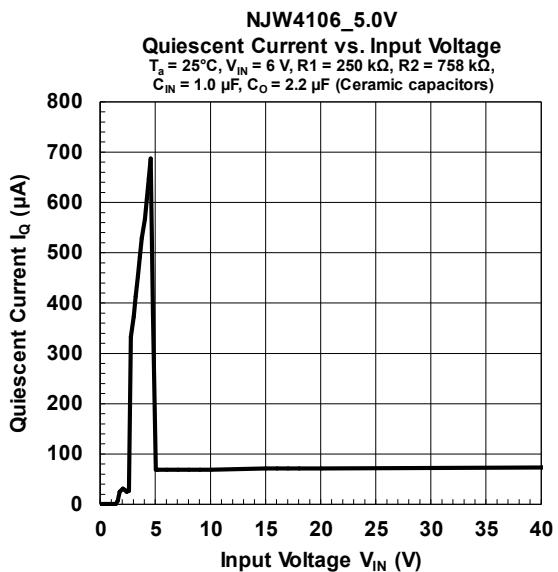
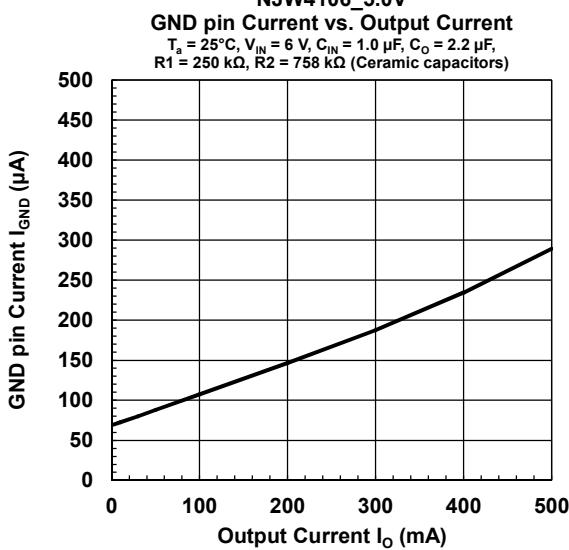
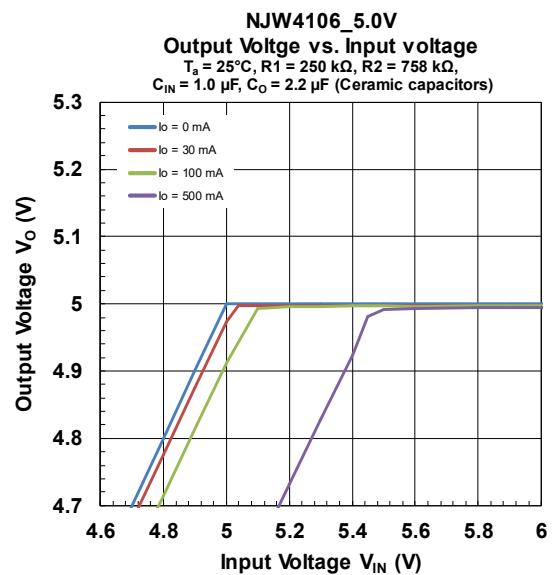
BOARD	JEDEC 2-LAYER BOARD	JEDEC 4-LAYER BOARD	HIGH POWER 4-LAYER BOARD
Dimension	76.2 mm × 114.3 mm, t = 1.6 mm		
Material	FR-4		
Cu Area	Surface Layer (Thickness: 70 µm)	NJR recommended land pattern + Measurement wiring	NJR recommended land pattern + Measurement wiring
	2 nd Layer (Thickness: 35 µm)	-	74.2 mm × 74.2 mm
	3 rd Layer (Thickness: 35 µm)	-	74.2 mm × 74.2 mm
	Back Layer (Thickness: 70 µm)	-	74.2 mm × 74.2 mm
	Thermal Vias	-	Connected from surface layer to 2 nd layer
			All layers are connected

■ POWER DISSIPATION vs. AMBIENT TEMPERATURE



- (5) 2-Layer: Mounted on glass epoxy board (76.2 mm × 114.3 mm × 1.6 mm: based on EIA/JEDEC standard, 2-layer FR-4).
- (6) 4-Layer: Mounted on glass epoxy board (76.2 mm × 114.3 mm × 1.6 mm: based on EIA/JEDEC standard, 4-layer FR-4).
 (For 4-layer: Applying 74.2 mm × 74.2 mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5.)
- (7) High Power 4-Layer: Mounted on glass epoxy board (76.2 mm × 114.3 mm × 1.6 mm, 4-layer FR-4).
 (For 4-layer: Applying 74.2 mm × 74.2 mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5.)

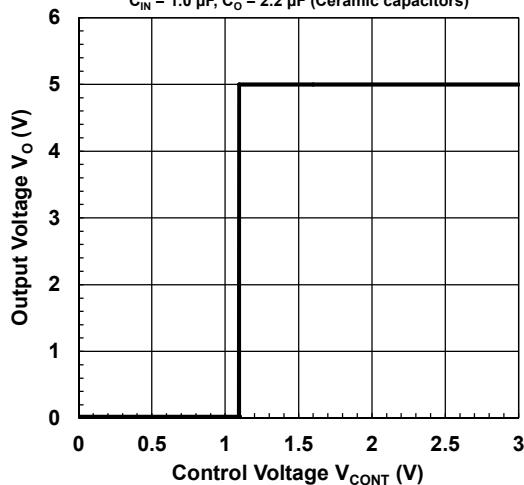
■ TYPICAL CHARACTERISTICS



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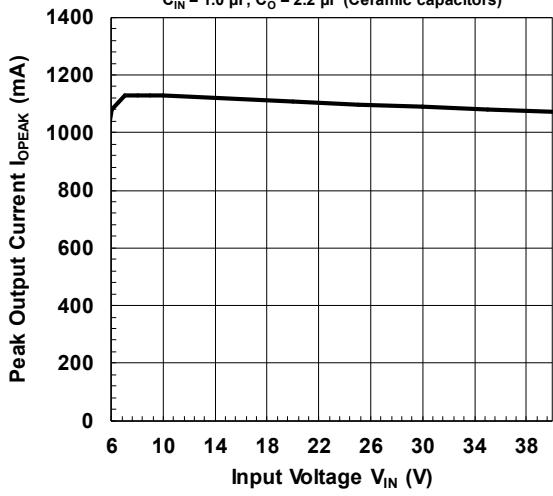
NJW4106_5.0V

Output Voltage vs. Control Voltage
 $T_a = 25^\circ\text{C}$, $V_{IN} = 6 \text{ V}$, $R1 = 250 \text{ k}\Omega$, $R2 = 758 \text{ k}\Omega$,
 $C_{IN} = 1.0 \mu\text{F}$, $C_O = 2.2 \mu\text{F}$ (Ceramic capacitors)



NJW4106_5.0V

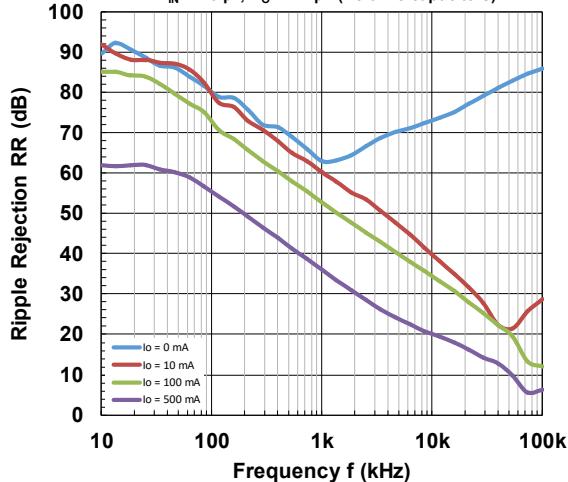
Peak Output Current vs. Input Voltage
 $T_a = 25^\circ\text{C}$, $V_{IN} = 4.5 \text{ V}$, $R1 = 250 \text{ k}\Omega$, $R2 = 758 \text{ k}\Omega$,
 $C_{IN} = 1.0 \mu\text{F}$, $C_O = 2.2 \mu\text{F}$ (Ceramic capacitors)



NJW4106_5.0V

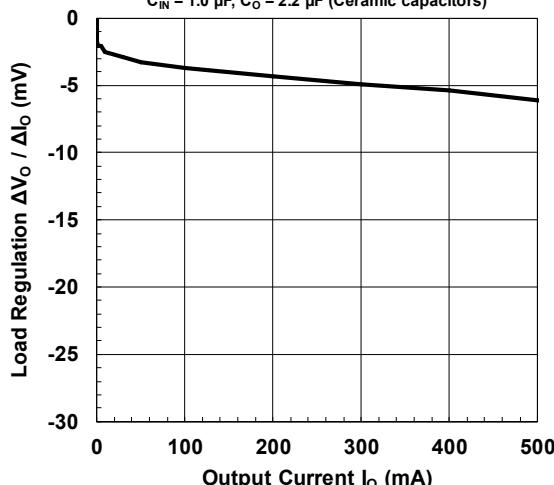
Ripple Rejection vs. Frequency

$T_a = 25^\circ\text{C}$, $V_{IN} = 6 \text{ V}$, $e_{IN} = 200 \text{ mVrms}$, $R1 = 250 \text{ k}\Omega$, $R2 = 758 \text{ k}\Omega$,
 $C_{IN} = 1.0 \mu\text{F}$, $C_O = 2.2 \mu\text{F}$ (Ceramic capacitors)



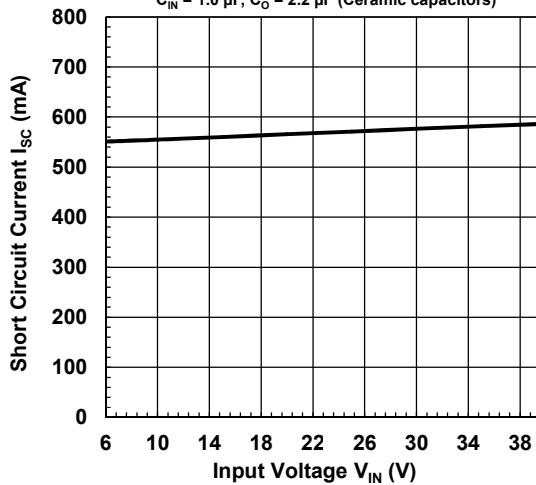
NJW4106_5.0V

Load Regulation vs. Output Current
 $T_a = 25^\circ\text{C}$, $V_{IN} = 6 \text{ V}$, $R1 = 250 \text{ k}\Omega$, $R2 = 758 \text{ k}\Omega$,
 $C_{IN} = 1.0 \mu\text{F}$, $C_O = 2.2 \mu\text{F}$ (Ceramic capacitors)



NJW4106_5.0V

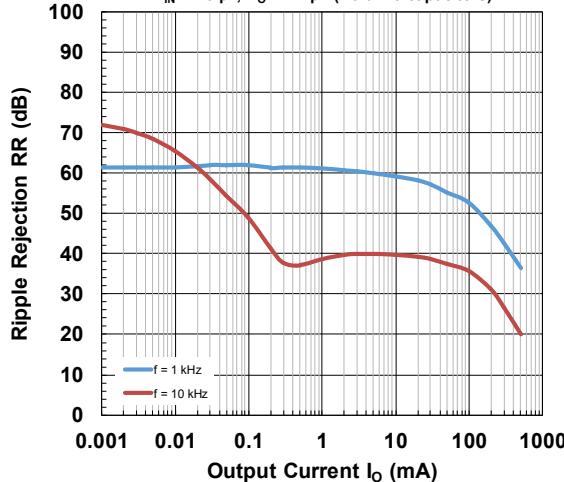
Short Circuit Current vs. Input Voltage
 $T_a = 25^\circ\text{C}$, $V_o = 0 \text{ V}$, $R1 = 250 \text{ k}\Omega$, $R2 = 758 \text{ k}\Omega$,
 $C_{IN} = 1.0 \mu\text{F}$, $C_O = 2.2 \mu\text{F}$ (Ceramic capacitors)



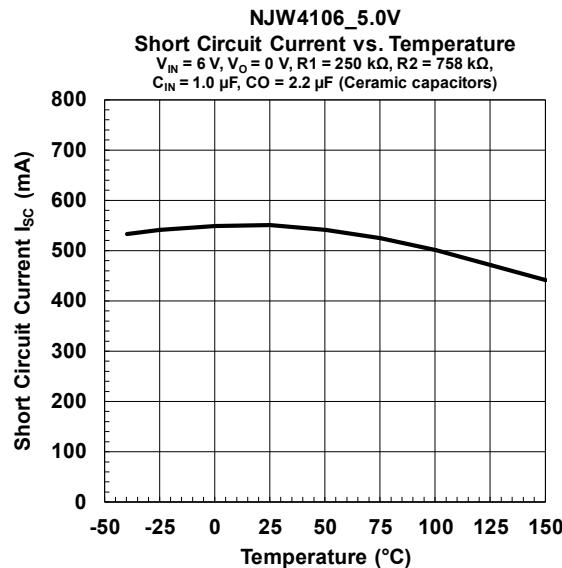
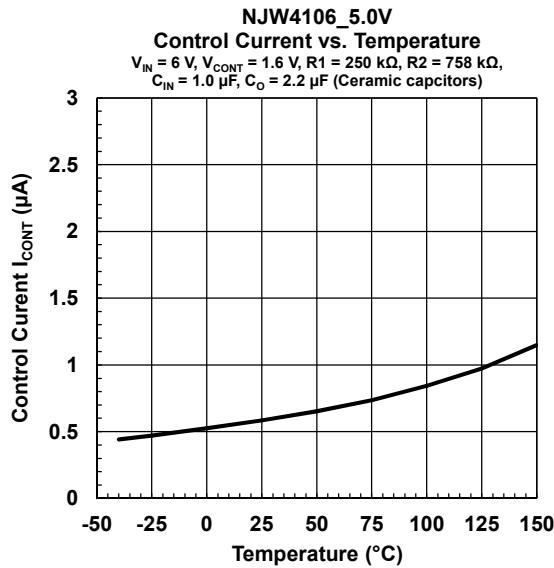
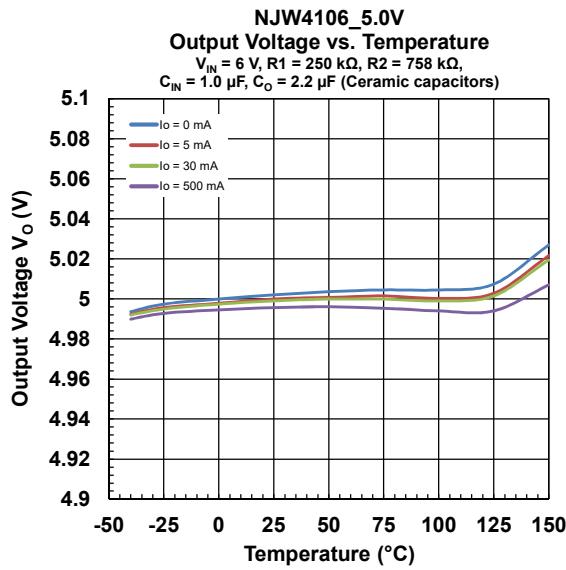
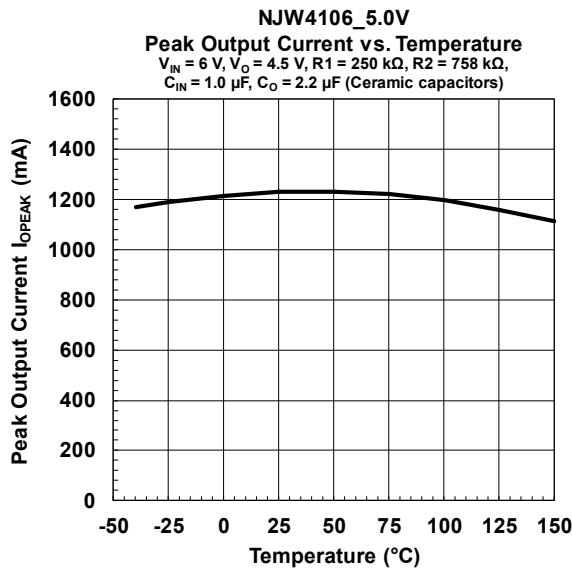
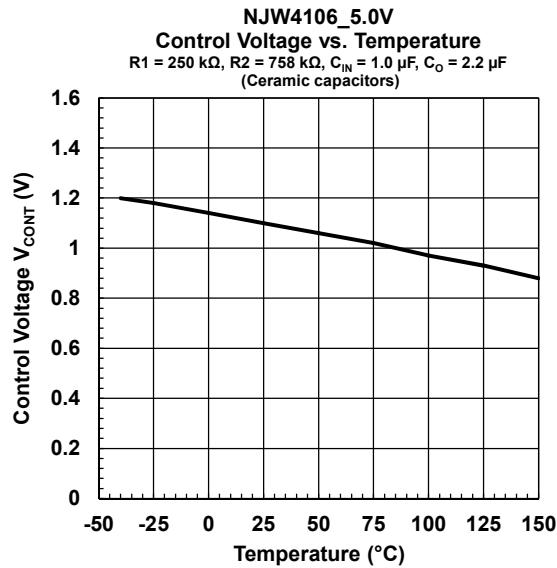
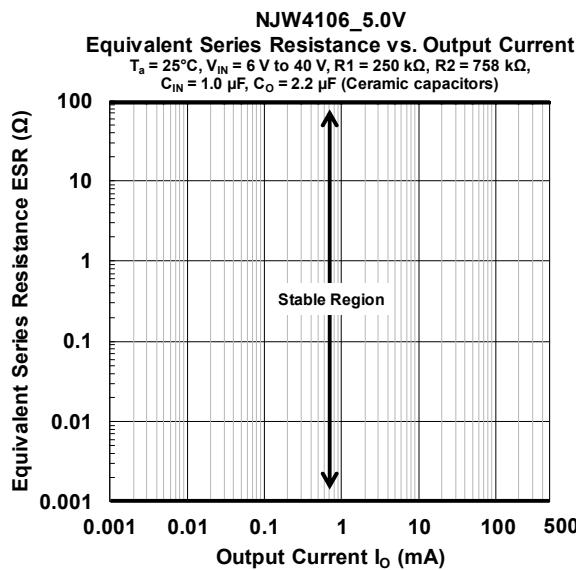
NJW4106_5.0V

Ripple Rejection vs. Output Current

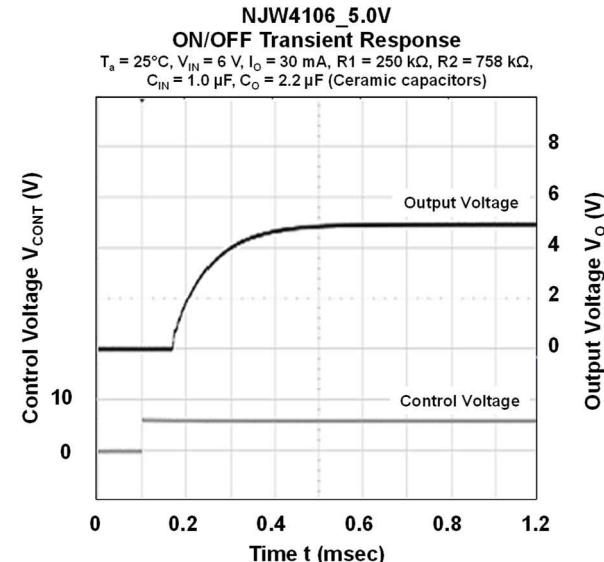
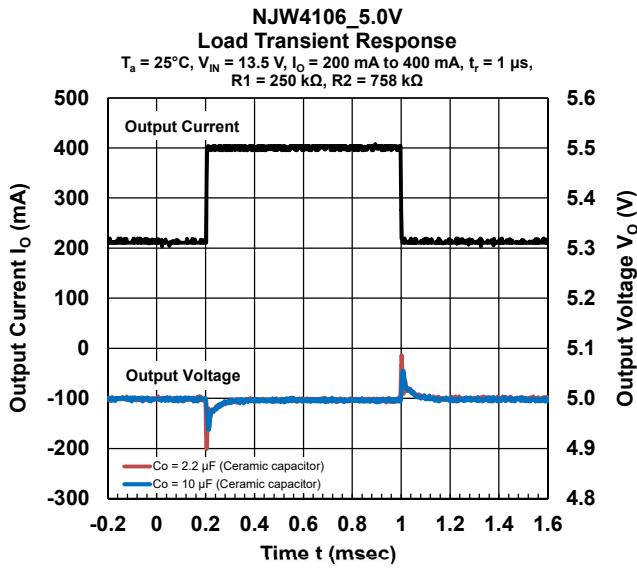
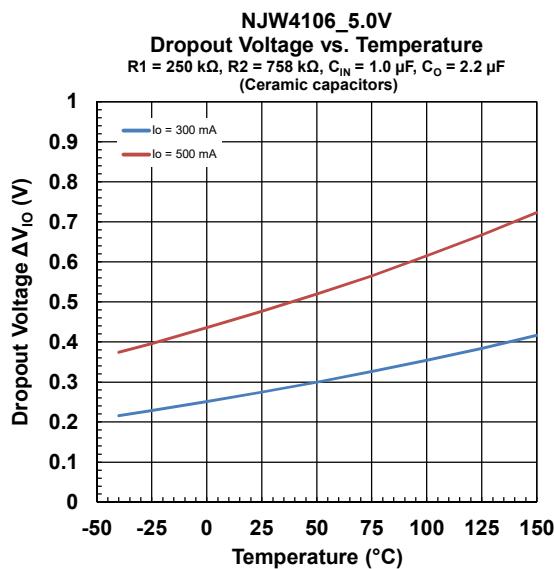
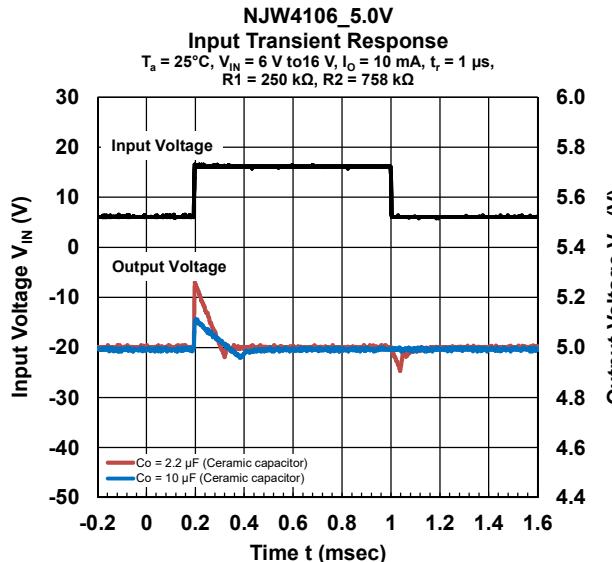
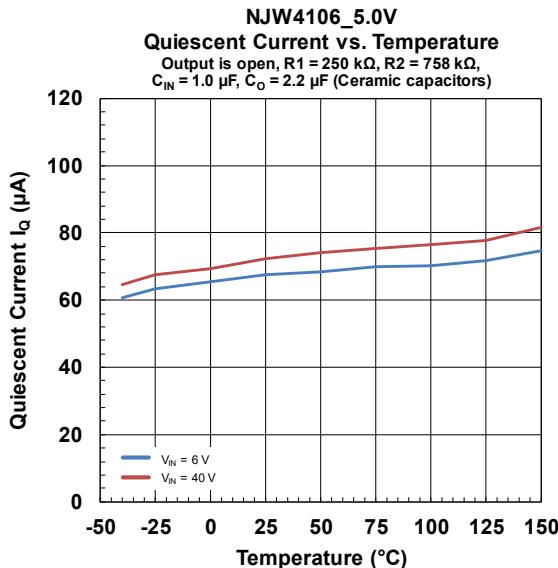
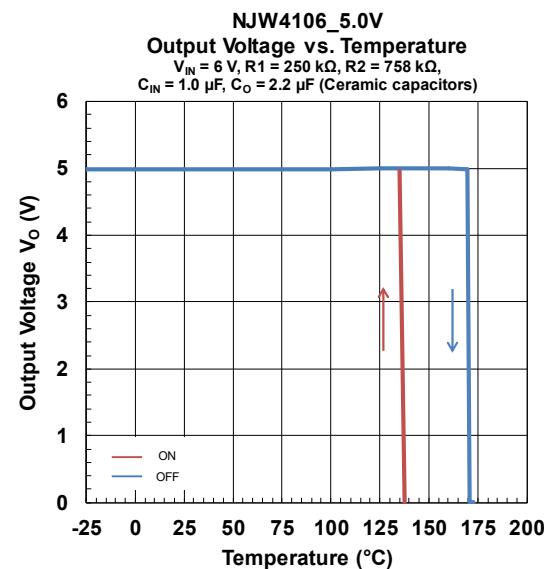
$T_a = 25^\circ\text{C}$, $V_{IN} = 6 \text{ V}$, $e_{IN} = 200 \text{ mVrms}$, $R1 = 250 \text{ k}\Omega$, $R2 = 758 \text{ k}\Omega$,
 $C_{IN} = 1.0 \mu\text{F}$, $C_O = 2.2 \mu\text{F}$ (Ceramic capacitors)



■ TYPICAL CHARACTERISTICS

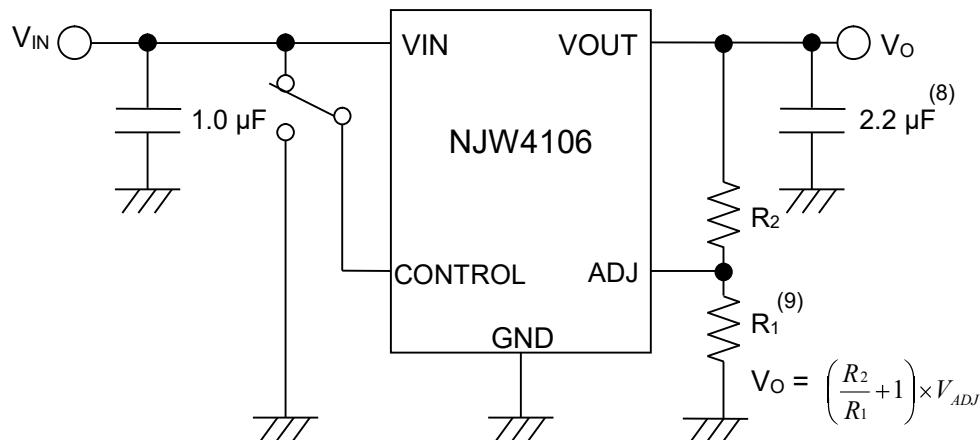


■ TYPICAL CHARACTERISTICS



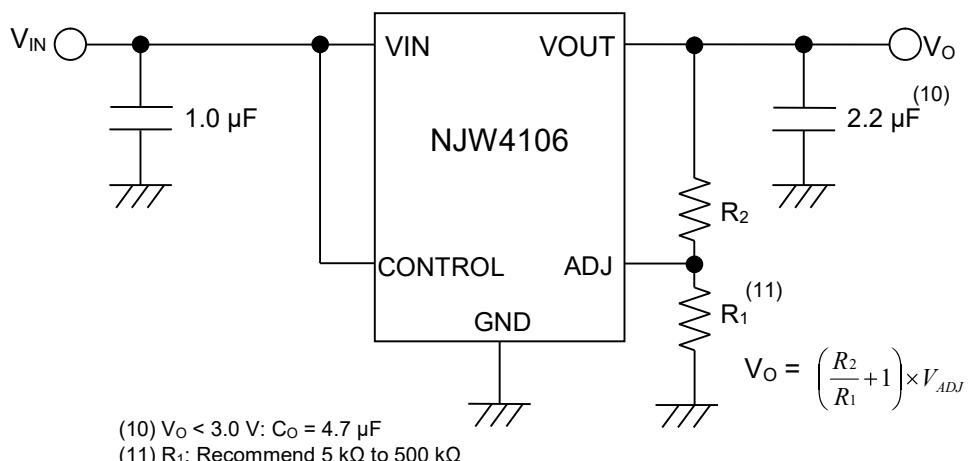
■TYPICAL APPLICATION

- When ON/OFF control is used.



The CONTROL pin is turned on at high level and turned off at open or low level.

- When ON/OFF control is not used.



Connect the CONTROL pin to the V_{IN} .

■ APPLICATION NOTE**Input Capacitor (C_{IN})**

The C_{IN} prevents oscillations and reduce power supply ripple of applications when the power supply impedance is high or power supply line is long. Connecting a 1.0 μF or larger C_{IN} between V_{IN} and GND pins as short path as possible.

Output Capacitor (C_O)

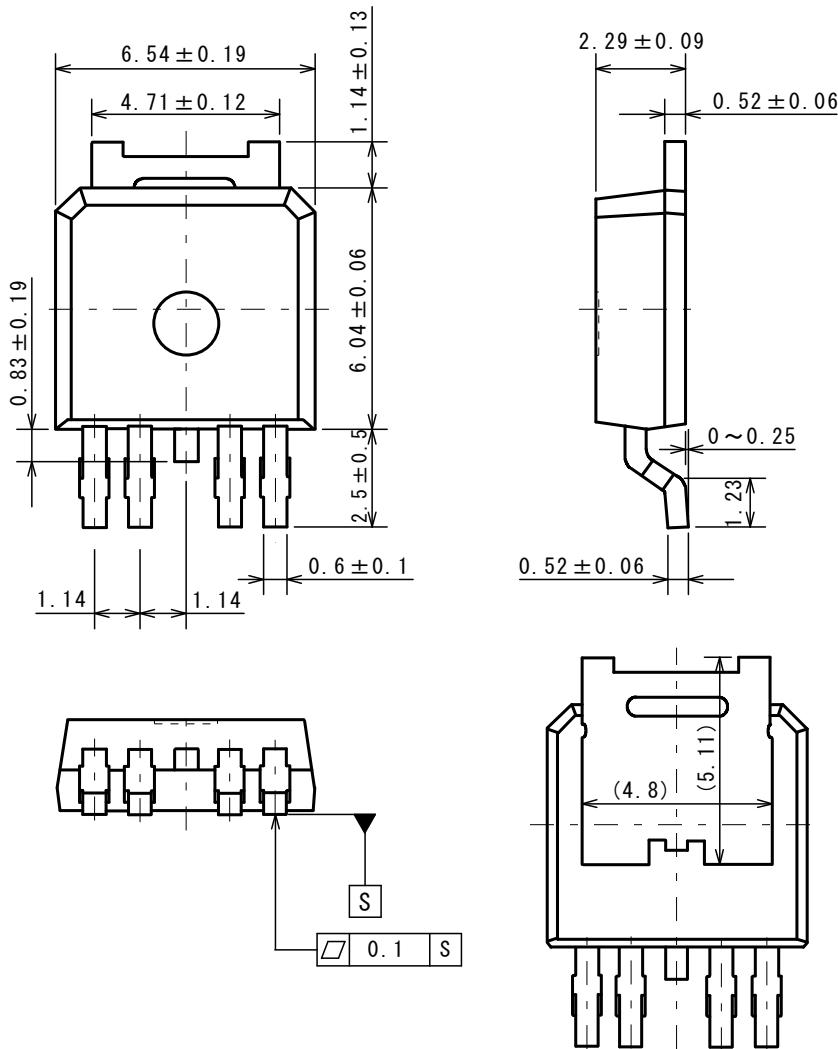
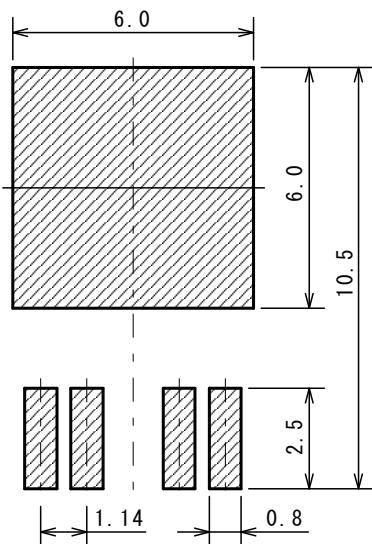
C_O is necessary for phase compensation of the internal error amplifier in the regulator, and the capacitance value and ESR affect the stability of the circuit. If a capacitor less than 2.2 μF (at $V_O \geq 3\text{ V}$) is used, output noise and/or regulator oscillation may occur due to lack of the phase compensation. For stable operation, connect a 2.2 μF or larger C_O within the stable operation region ($0.001\text{ }\Omega \leq \text{ESR} \leq 100\text{ }\Omega$) between the V_{OUT} and GND pins as short path as possible. The recommended capacitance value varies depending on the output voltage, and a low output voltage may require a large capacitance value; therefore, confirm the recommended capacitance of the required output voltage. As the capacitance value of C_O increases, output noise and ripple decrease, and the response to output load fluctuations also improves.

Select the output capacitor considering various characteristics such as frequency characteristics, temperature characteristics, and DC bias characteristics. For the C_O , a capacitor with excellent temperature characteristics and sufficient margin for output voltage is recommended.

Undervoltage Lockout (UVLO)

This circuit prevents malfunction by locking out the output when V_{IN} is below the UVLO detection voltage. The output voltage rises when the input voltage rises and exceeds the UVLO release voltage (2.7 V, typ). When the input voltage drops below the UVLO detection voltage (2.2 V, typ)*, the output voltage falls.

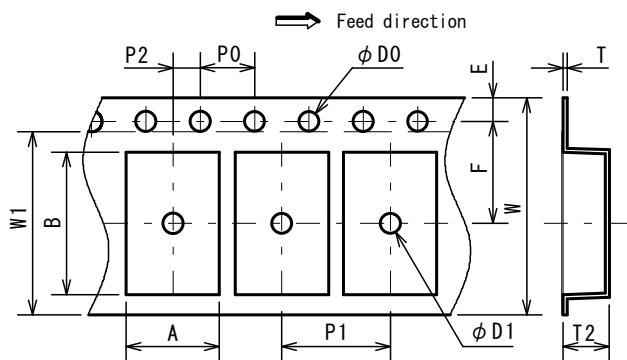
*UVLO detection voltage (2.2 V, typ) = UVLO release voltage (2.7 V, typ) - UVLO hysteresis voltage (500 mV, typ)

■ PACKAGE DIMENSIONS**■ EXAMPLE OF SOLDER PADS DIMENSIONS**

■ PACKING SPEC

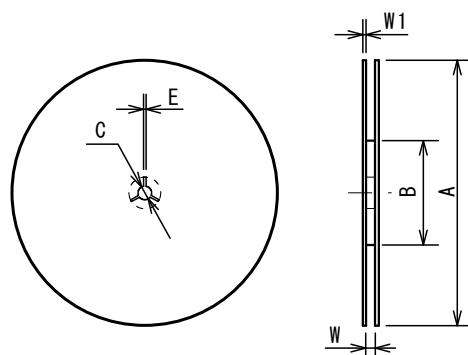
Unit: mm

TAPING DIMENSIONS



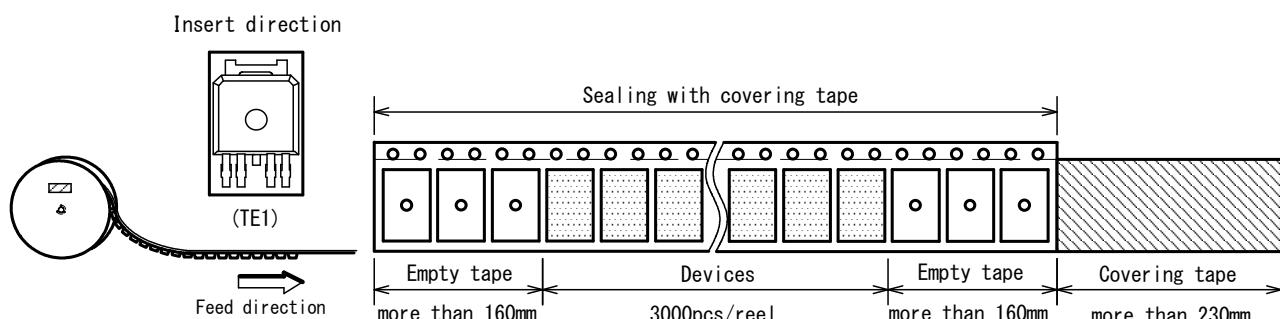
SYMBOL	DIMENSION	REMARKS
A	6.9 ± 0.1	BOTTOM DIMENSION
B	10.5 ± 0.1	BOTTOM DIMENSION
D0	$1.5^{+0.1}_0$	
D1	$1.5^{+0.1}_0$	
E	1.75 ± 0.1	
F	7.5 ± 0.1	
P0	4.0 ± 0.1	
P1	8.0 ± 0.1	
P2	2.0 ± 0.1	
T	0.3 ± 0.1	
T2	3.4 max	
W	16.0 ± 0.3	
W1	13.5	THICKNESS 0.1max

REEL DIMENSIONS

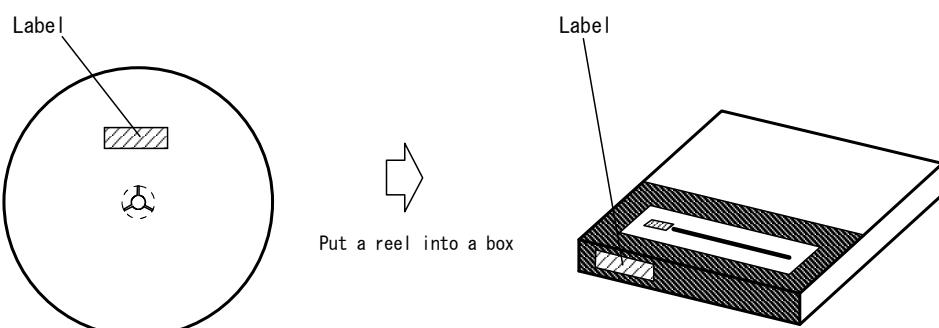


SYMBOL	DIMENSION
A	$\phi 330 \pm 2$
B	$\phi 80 \pm 1$
C	$\phi 13 \pm 0.5$
E	2
W	17.5 ± 0.5
W1	2 ± 0.5

TAPING STATE

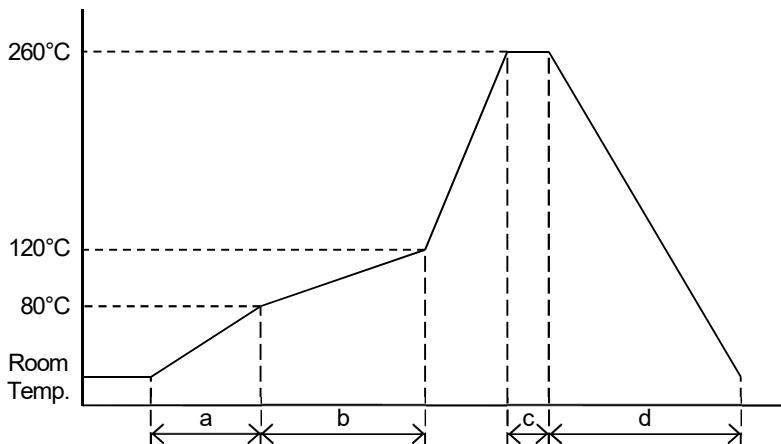


PACKING STATE



■ RECOMMENDED MOUNTING METHOD

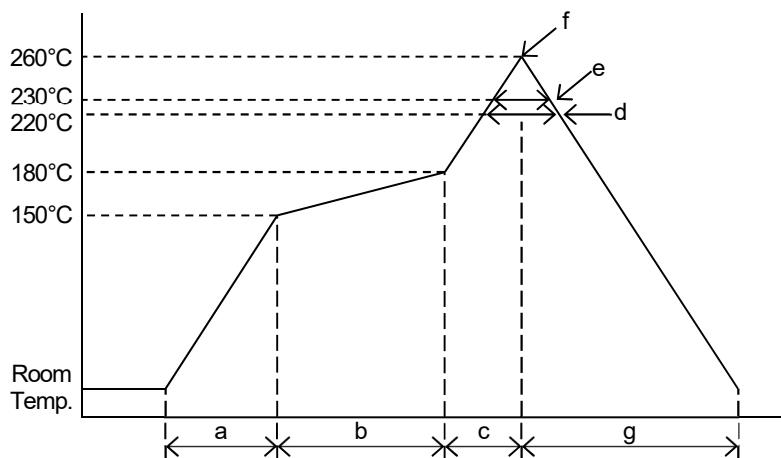
FLOW SOLDERING PROFILE



The temperature indicates at the surface of mold package.

a	Temperature ramping rate	1 to 7°C/s
b	Pre-heating temperature Pre-heating time	80 to 120°C 60 to 120s
c	Peak temperature Peak time	lower than 260°C shorter than 10s
d	Temperature ramping rate	1 to 7°C/s

INFRARED REFLOW SOLDERING PROFILE



The temperature indicates at the surface of mold package.

a	Temperature ramping rate	1 to 4°C/s
b	Pre-heating temperature Pre-heating time	150 to 180°C 60 to 120s
c	Temperature ramp rate	1 to 4°C/s
d	220°C or higher time	shorter than 60s
e	230°C or higher time	shorter than 40s
f	Peak temperature	lower than 260°C
g	Temperature ramping rate	1 to 6°C/s

■ REVISION HISTORY

DATE	REVISION	CHANGES
June 9, 2021	Ver.1.0	New Release

[CAUTION]

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9. The product specifications and descriptions listed in this datasheet are subject to change at any time, without notice.

