MPQ3367A

Low-EMI, 6-Channel, Max 150mA/Ch Boost WLED Driver with 15000:1 Dimming Ratio and I²C, AEC-Q100

DESCRIPTION

The MPQ3367A is a step-up converter with 6 channel current sources. The device is designed to drive the white LED arrays as backlighting for small- or medium-sized LCD panels.

The device uses peak current mode as its PWM control architecture to regulate the boost converter. Six channel current sources are applied to the LED cathode to adjust the LED brightness. The MPQ3367A regulates the current in each LED string to the value set by an external current-setting resistor, with 2.5% current matching between strings.

A low on resistance MOSFET and headroom voltage are provided to improve efficiency. The MPQ3367A has a standard I²C digital interface for easy use. The switching frequency can be configured via a resistor, I²C interface, or external clock.

The MPQ3367A provides analog, PWM, and mix dimming mode with a PWM input. The dimming mode can be selected with the I²C interface or the MIX/AD pin. The device also has a phase shift function to improve or eliminate noise during PWM dimming.

Robust protections are included to guarantee safe operation of the device. Protection modes include over-current protection (OCP), over-voltage protection (OVP), over-temperature protection (OTP), LED short and open protection. The MPQ3367A can automatically decrease the LED current at high temperatures.

The MPQ3367A is available in a QFN-24 (4mmx4mm) package.

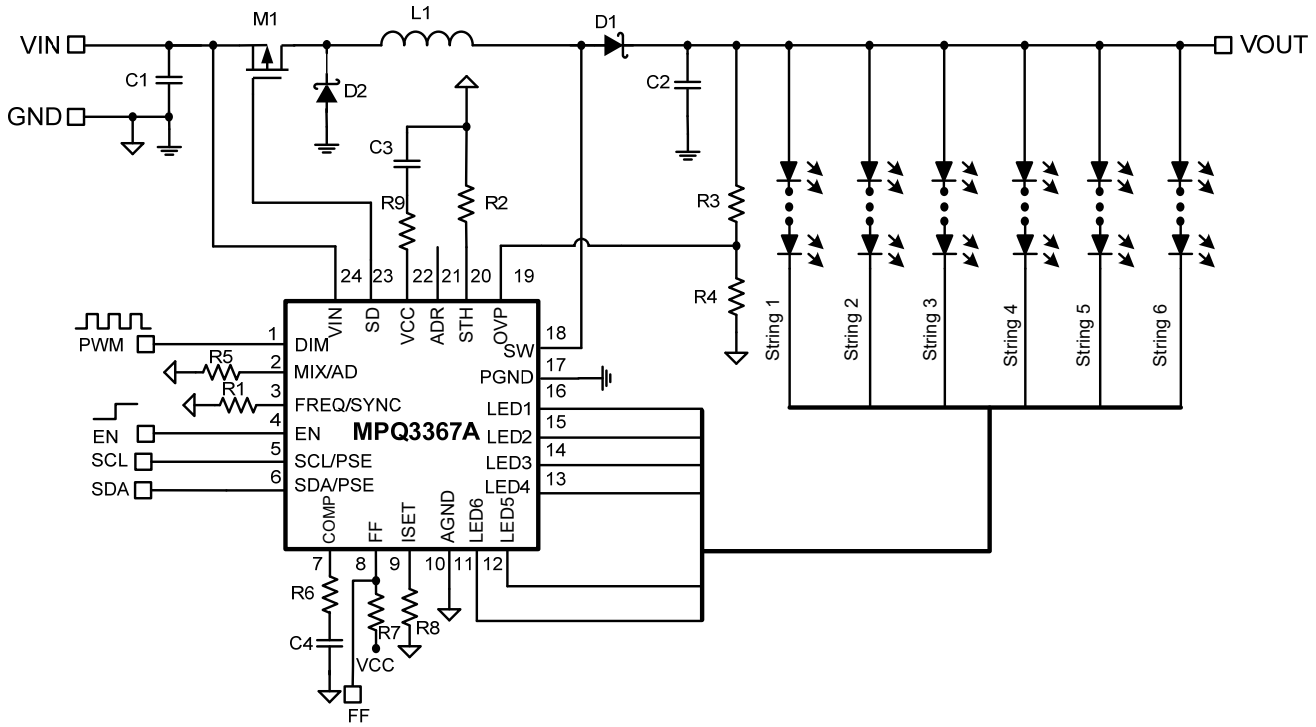
FEATURES

- 3.5V to 36V Input Voltage Range
- 6 Channels with Maximum 150mA per Channel
- Internal 100mΩ, 50V MOSFET
- Configurable f_{SW} up to 2.2MHz
- External Sync Switching Frequency Function
- Multi-Dimming Operation Mode through PWM Input, Including:
  - Direct PWM Dimming
  - Analog Dimming
  - Mix Dimming with 25% or 12.5% Transfer Point
- 15000:1 Dimming Ratio in PWM Dimming Mode when $f_{PWM} \leq 200Hz$
- 200:1 Dimming Ratio at Analog Dimming through PWM Dimming Signal Input
- Excellent EMI Performance, Frequency Spread Spectrum
- I²C Interface with 3 Selectable IC Addresses
- Phase Shift Function for PWM Dimming
- 2.5% Current Matching
- Cycle-by-Cycle Current Limit
- Disconnect VOUT from VIN
- Optional LED Current Auto-Decrease at High Temperatures
- LED Short/Open, OTP, OCP, and Inductor Short Protection
- Configurable LED Short Threshold
- Configurable OVP Threshold
- Fault Indicator Signal Output
- Available in a QFN-24 (4mmx4mm) Package
- Available in AEC-Q100 Grade 1

APPLICATIONS

- Tablets and Notebooks
- Automotive Displays

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number	Package	Top Marking	MSL Rating
MPQ3367AGR-AEC1*	QFN-24 (4mmx4mm)	*See Below*	1
MPQ3367AGRE-AEC1**	QFN-24 (4mmx4mm) WF	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MPQ3367AGR–AEC1-Z).

* * For Tape & Reel, add suffix -Z (e.g. MPQ3367AGRE–AEC1-Z).

TOP MARKING (MPQ3367AGR-AEC1)

MPSYWW
M3367A
LLLLLL

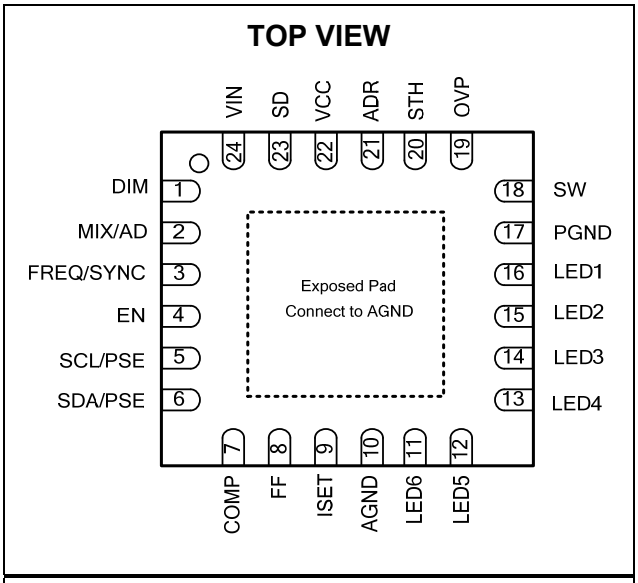
MPS: MPS prefix
Y: Year code
WW: Week code
M3367A: Part number
LLLLLL: Lot number

TOP MARKING (MPQ3367AGRE-AEC1)

MPSYWW
M3367A
LLLLLL
E

MPS: MPS prefix
Y: Year code
WW: Week code
M3367A: Part number
LLLLLL: Lot number
E: Wettable lead flank

PACKAGE REFERENCE



QFN-24 (4mmx4mm)

PIN FUNCTIONS

Pin #	Name	Description
1	DIM	**PWM signal input pin.** Apply a PWM signal on the DIM pin for brightness control. DIM is pulled low internally, and a 100Hz to 20kHz PWM signal is recommended.
2	MIX/AD	**Dimming mode setting pin.** MIX/AD is a current-source output (18μA). Connect a resistor to this pin to configure its voltage. When MIX/AD is low (<0.3V), the device uses mix dimming. When MIX/AD is middle level (0.5V to 0.8V), the device uses PWM dimming. When MIX/AD is high (1.0V to 1.3V), the device uses analog dimming. When MIX/AD is floating, the dimming mode is set by the internal MODE register.
3	FREQ/ SYNC	**Switching frequency setting and SYNC pin.** Connect a resistor between FREQ/SYNC and GND to set the converter's switching frequency, or connect an external clock to synchronize the boost switching frequency. Float FREQ/SYNC if the internal switching frequency is set by FSW1:0.
4	EN	**IC enable pin.** Pull EN high to enable the IC. Pull EN low to shut down the IC.
5	SCL/PSE	**I²C interface clock pin.** Connect SDA/PSE to SCL/PSE, and pull them up between 0.75V and 1V to enable the phase shift PWM dimming function. If this pin is not used, please connect it to a high level or to GND, do not float this pin.
6	SDA/PSE	**I²C interface data pin.** Connect SDA/PSE to SCL/PSE, and pull them up between 0.75V and 1V to enable the phase shift PWM dimming function. If this pin is not used, please connect it to a high level or to GND, do not float this pin.
7	COMP	**Compensation pin.**
8	FF	**Fault flag pin.** Open drain during normal operation. FF is pulled low if a fault occurs.
9	ISET	**LED current setting pin.** Tie a current-setting resistor from ISET to GND to configure the current in each LED string.
10	AGND	**Analog ground pin.**
11	LED6	**LED string 6 current input pin.** Connect the LED string 6 cathode to this pin. If LED6 is unused, tie it to GND.
12	LED5	**LED string 5 current input pin.** Connect the LED string 5 cathode to this pin. If LED5 is unused, tie it to GND.
13	LED4	**LED string 4 current input pin.** Connect the LED string 4 cathode to this pin. If LED4 is unused, tie it to GND.
14	LED3	**LED string 3 current input pin.** Connect the LED string 3 cathode to this pin. If LED3 is unused, tie it to GND.
15	LED2	**LED string 2 current input pin.** Connect the LED string 2 cathode to this pin. If LED2 is unused, tie it to GND.
16	LED1	**LED string 1 current input pin.** Connect the LED string 1 cathode to this pin. If LED1 is unused, tie it to GND.
17	PGND	**Step-up converter power ground pin.**
18	SW	**Drain pin of the internal low-side MOSFET.** Connect the power inductor to SW.
19	OVP	**Over-voltage protection setting pin.** Connect a resistor divider from the VOUT pin to OVP pin and OVP pin to GND to configure the over-voltage protection threshold.
20	STH	**Short LED protection threshold pin.** STH is a current-source output (18μA). Connect a resistor to this pin to configure its voltage. Float STH if the internal short LED protection threshold is set by TH_S1:0.
21	ADR	**IC address setting pin.** Connect a resistor to this pin to set the IC address. When ADR is floating, the IC address is 0x38. When ADR < 0.4V, the IC address is 0x3A. When ADR is between 0.4V and 1.4V, the IC address is 0x39. The ADR pin's pull-up current is 18μA.
22	VCC	**5V LDO output pin.** VCC provides power to the internal logic and gate driver. Place a ceramic capacitor as close to this pin as possible to reduce noise.

PIN FUNCTIONS *(continued)*

Pin #	Name	Description
23	SD	**External disconnect PMOS gate drive pin.** Turn off the external PMOS if a fault occurs. Float the SD pin if it is not used.
24	VIN	**Power supply input.** VIN supplies power to the IC.
Pad	Exposed pad	**Chip ground.** Connect the exposed pad to AGND.

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} .....-0.3V to +42V
V_{SW}, V_{LED1} to V_{LED6}.....-0.5V to +50V
V_{SW}..... -1.0V for <100ns
V_{SD} .....V_{IN} - 6V to V_{IN}
All other pins .....-0.3V to +6V
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to +150°C
Continuous power dissipation (T_A = 25°C) (2)
QFN-24 (4mmx4mm)..... 2.97W

ESD Ratings

Human body model (HBM)
LED1~6 ESD..... ±7kV
All other pins ..... ±4kV
Charged device model (CDM) ..... ±2kV

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) .....3.5V to 36V
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-24 (4mmx4mm)…….…42…….9....°C/W		

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +125°C, typical value is at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Operating input voltage	V_{IN}		3.5		36	V
Supply current (quiescent)	I_Q	No switching		5		mA
Supply current (shutdown)	I_{ST}	V_{EN} = 0V, V_{IN} = 12V			1	μA
Input UVLO threshold	V_{IN_UVLO}	Rising edge		3.1		V
Input UVLO hysteresis				100		mV
LDO output voltage	V_{CC}	V_{EN} = 2V, 6V < V_{IN} < 24V, 0 < I_{VCC} < 10mA		5		V
EN on threshold	V_{EN_ON}	V_{EN} rising	1.2			V
EN off threshold	V_{EN_OFF}	V_{EN} falling			0.4	V
EN pull-down resistance	R_{EN}			1		MΩ
Step-Up Converter						
Low-side MOSFET on resistance	R_{DS_LS}	V_{IN} = 12V		100		mΩ
SW leakage current	I_{SW_LK}	V_{SW} = 45V			1	μA
Switching frequency	f_{SW}	R_{FREQ} = 10kΩ	1.98	2.2	2.42	MHz
		R_{FREQ} = 40kΩ	495	550	605	kHz
		FSW1:0 = 01, FREQ floating	340	400	460	kHz
FREQ voltage	V_{FREQ}		0.57	0.6	0.63	V
ADR pull-up current	I_{ADR}			18		μA
Maximum duty cycle	D_{MAX}	f_{SW} = 1MHz	90			%
Cycle-by-cycle current limit	I_{SW_LIMIT}	T_J = 25°C, Duty = 90%	2.6			A
		Duty = 90%	2.3			A
Latch off Current limit protection	I_{CL}	To trigger current limit protection		7.5		A
SYNC input low threshold	V_{SYNC_LO}	V_{SYNC} falling			0.4	V
SYNC input high threshold	V_{SYNC_HI}	V_{SYNC} rising	1.2			V
PSE active threshold	V_{PSE}	Phase shift enabled	0.75	0.9	1.0	V
COMP trans-conductance	G_{COMP}	ΔI_{COMP} ≤ 10μA		100		μA/V
COMP source current limit	I_{COMP_SO}			90		μA
COMP sink current limit	I_{COMP_SI}			30		μA
Current Dimming						
DIM input low threshold	V_{DIM_LO}	V_{DIM} falling			0.4	V
DIM input high threshold	V_{DIM_HI}	V_{DIM} rising	1.2			V
MIX/AD input low threshold	V_{MIX_LO}	Mix dimming threshold			0.3	V
MIX/AD input middle threshold	V_{MIX_MID}	PWM dimming threshold	0.5		0.8	V
MIX/AD input high threshold	V_{MIX_HI}	Analog dimming threshold	1.0		1.3	V

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +125°C, typical value is at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
MIX/AD pull-up current	I_{MIX}	MIX/AD pull-up current		18		µA
Mix dimming transfer point		MIXTP = 0		25		%
Transfer point hysteresis				0.5		%
Mix dimming output dimming frequency	f_{MIX}	MIXFR = 0		200		Hz
LED Current Regulator						
LEDx regulation voltage	V_{HD}	I_{LED} = 20mA		350		mV
		I_{LED} = 100mA		850	1000	mV
Current matching (5)		I_{LED} = 20mA	-2.5		+2.5	%
		I_{LED} = 100mA	-2.5		+2.5	%
ISET voltage	V_{ISET}			1.2		V
LED current	I_{LED}	R_{ISET} = 24.9kΩ, T_J = 25°C	48.75	50	51.25	mA
		I_{LED} = 1/50 x 50mA = 1mA	0.9	1.05	1.2	mA
Phase shift degree		LED1 to LED6 enabled		60		deg
		LED1 to LED4 enabled		90		deg
Protection						
Over-voltage protection threshold	V_{OVP}		1.9	2	2.1	V
OVP hysteresis				200		mV
OVP UVLO threshold	V_{OVP_UV}	Step-up converter fails		100		mV
LEDx over-voltage threshold	V_{LEDX_OV}	TH_S bits= 01		5		V
LEDx over-voltage fault timer				7.7		ms
LEDx UVLO threshold	V_{LEDX_UV}			100		mV
Thermal shutdown threshold (6)	T_{ST}	Rising edge		170		°C
		Hysteresis		20		°C
SD pull-down current	I_{SD}			60		µA
SD voltage (respective to V_{IN})	V_{SD-IN}	V_{IN} = 12V, V_{IN} - V_{SD}		6		V
STH pull-up current	I_{STH}	STH pull-up current		18		µA
I²C Interface						
Input logic low	V_{IL}				0.4	V
Input logic high	V_{IH}		1.2			V
Output logic low	V_{OL}	I_{LOAD} = 3mA			0.4	V
SCL clock frequency (6)	f_{SCL}				400	kHz
SCL high time (6)	t_{HIGH}		0.6			µs
SCL low time (6)	t_{LOW}		1.3			µs
Data set-up time (6)	t_{SU_DAT}		100			ns
Data hold time (6)	t_{HD_DAT}		0		0.9	µs
Set-up time for repeated start (6)	t_{SU_STA}		0.6			µs

ELECTRICAL CHARACTERISTICS *(continued)*

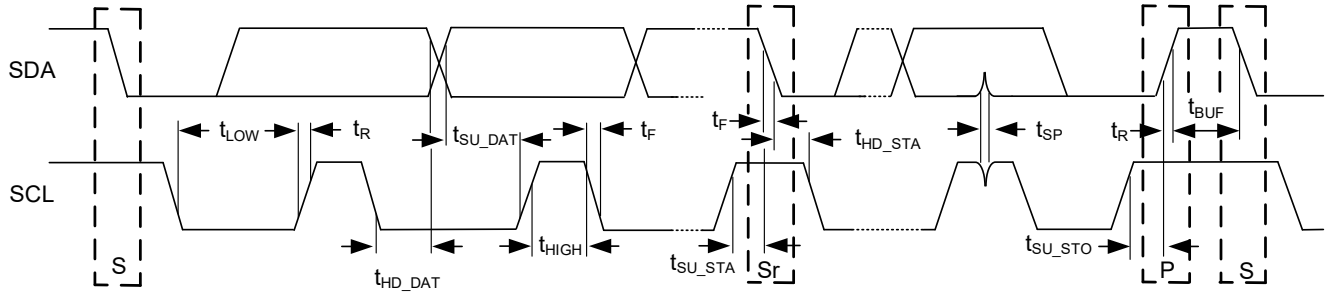
V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +125°C, typical value is at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Hold time for start (6)	t_{HD_STA}		0.6			µs
Bus free time between start and stop condition (6)	t_{BUF}		1.3			ms
Set-up time for stop condition (6)	t_{SU_STO}		0.6			µs
Rising time of SCL and SDA (6)	t_R		20 + 0.1 x C_B		300	ns
Falling time of SCL and SDA (6)	t_F		20 + 0.1 x C_B		300	ns
Pulse-width of suppressed spike (6)	t_{SP}		0		50	ns
Capacitance bus for each bus line (6)	C_B				400	pF

Notes:

5) Matching is defined as the difference of the maximum to minimum current divided by 2 times the average current.
6) Not tested in production. Guaranteed by characterization.

I²C-COMPATIBLE INTERFACE TIMING DIAGRAM



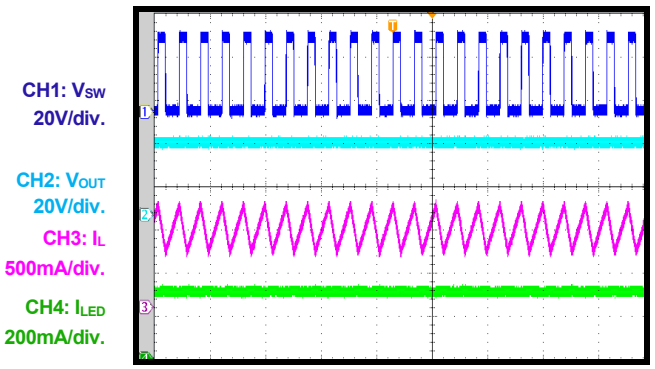
S = Start Condition
Sr = Repeated Start Condition
P = Stop Condition

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, L = 22µH, LED = 6P12S, f_{SW} = 650kHz, I_{SET} = 50mA, T_A = 25°C, unless otherwise noted.

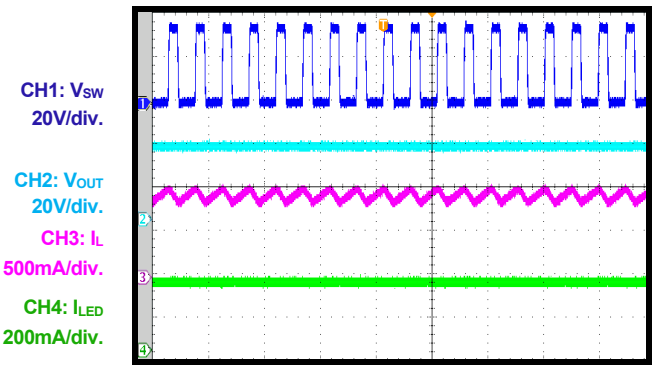
Steady State

f_{SW} = 650kHz

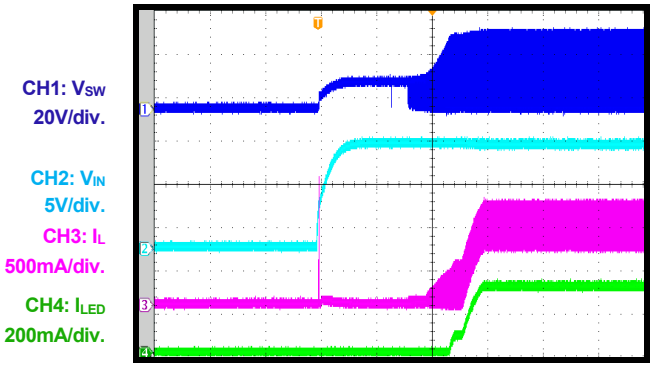


Steady State

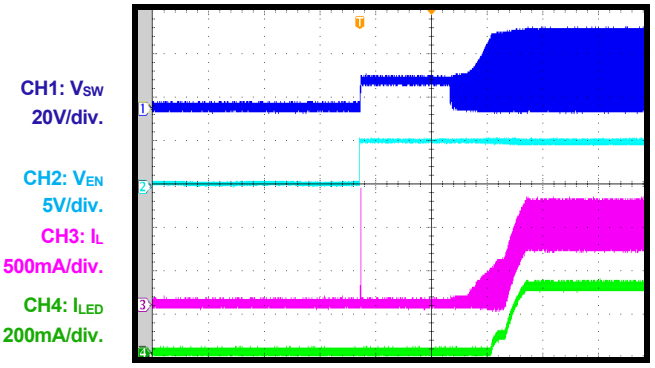
f_{SW} = 2.2MHz



Start-Up through VIN

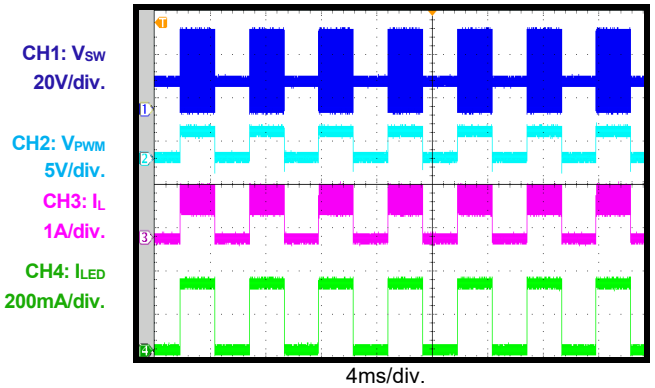


Start-Up through EN



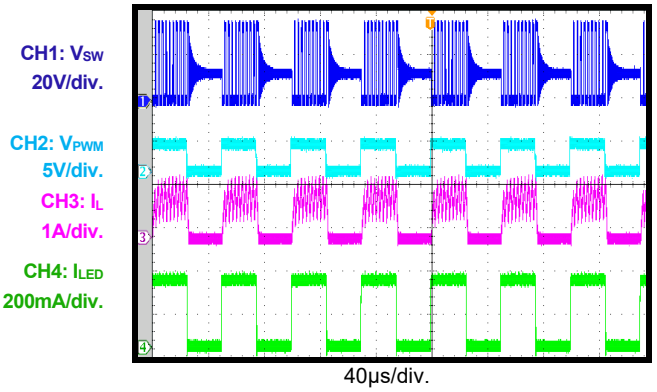
PWM Dimming

f_{PWM} = 200Hz, D_{PWM} = 50%



PWM Dimming

f_{PWM} = 20kHz, D_{PWM} = 50%

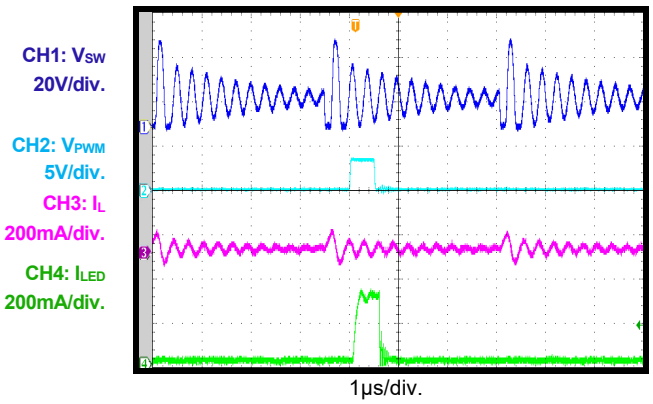


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, L = 22µH, LED = 6P12S, f_{SW} = 650kHz, I_{SET} = 50mA, T_A = 25°C, unless otherwise noted.

PWM Dimming

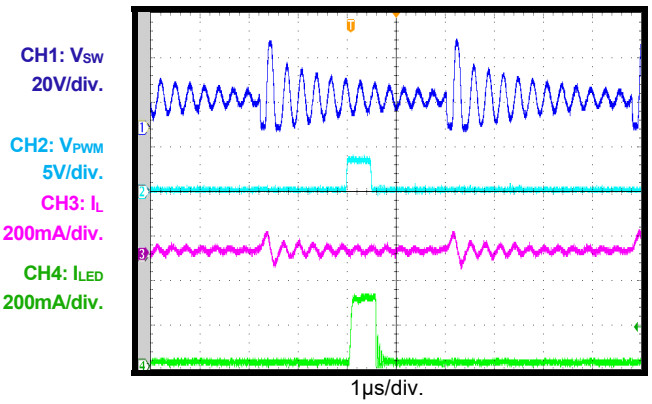
f_{PWM} = 200Hz, D_{PWM} = 0.01%



1µs/div.

PWM Dimming

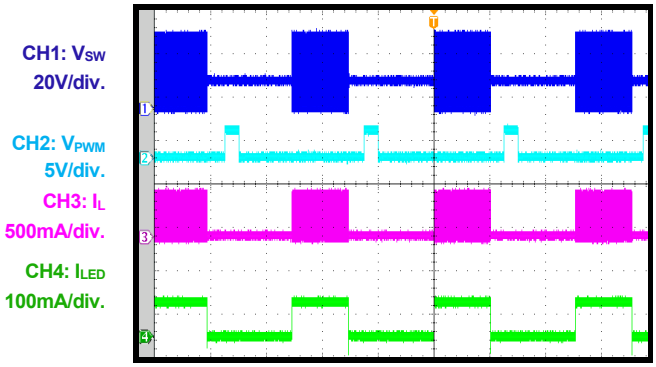
f_{PWM} = 100Hz, D_{PWM} = 0.005%



1µs/div.

Mix Dimming

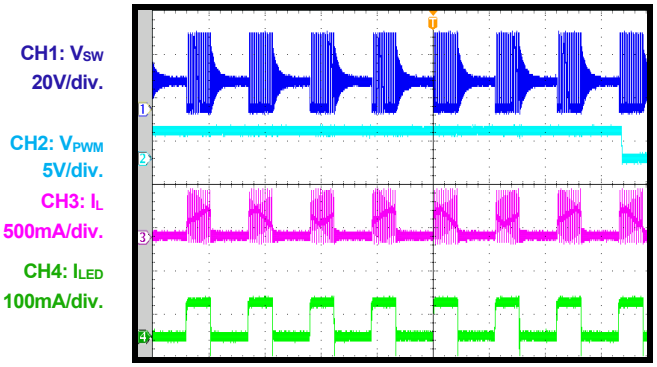
f_{PWM} = $f_{(ILED)}$ = 200Hz, D_{PWM} = 10%, TP=25%



2ms/div.

Mix Dimming

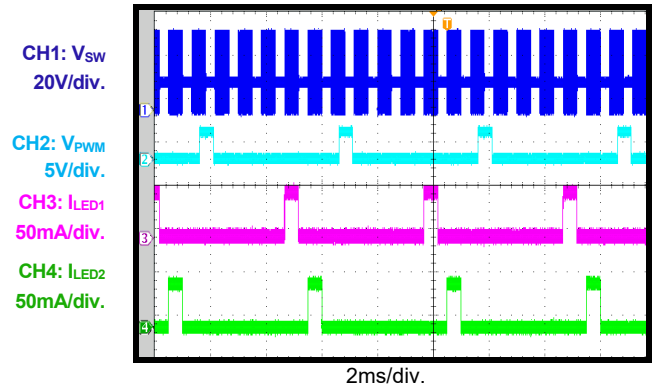
f_{PWM} = 200Hz, $f_{(ILED)}$ = 23kHz, D_{PWM} = 10%, TP=25%



40µs/div.

Phase Shift Function

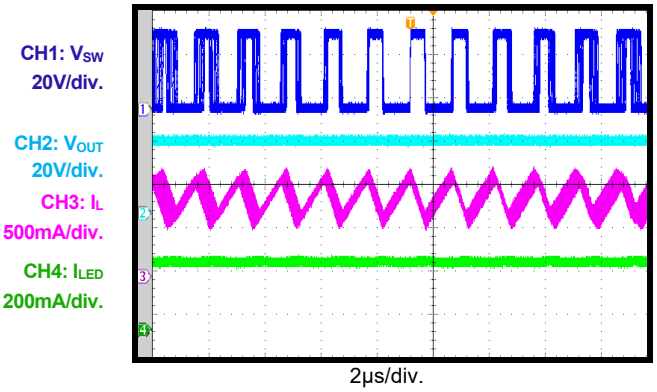
f_{PWM} = 200Hz, PWM dimming, 6-channel enable



2ms/div.

Frequency Spread Spectrum

1/100 of switching frequency



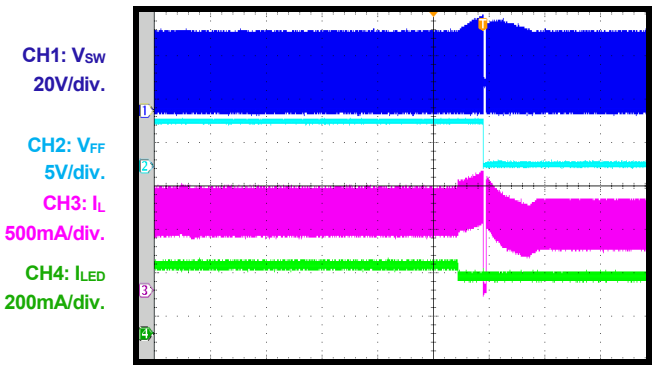
2µs/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, L = 22µH, LED = 6P12S, f_{SW} = 650kHz, I_{SET} = 50mA, T_A = 25°C, unless otherwise noted.

Open LED Protection

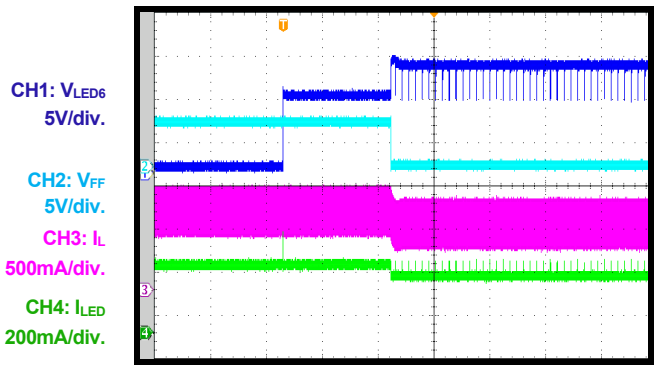
Open 1 string when working



2ms/div.

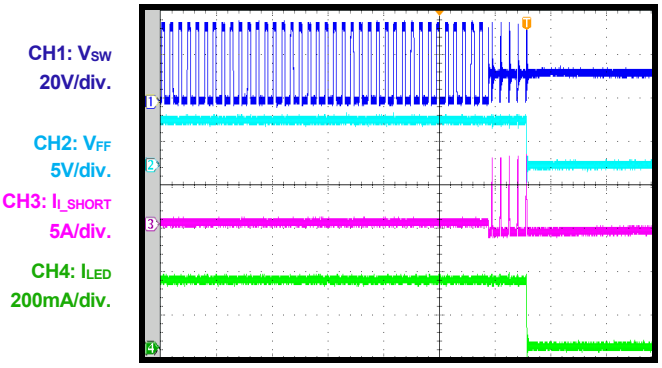
Short LED Protection

Short 1 string when working



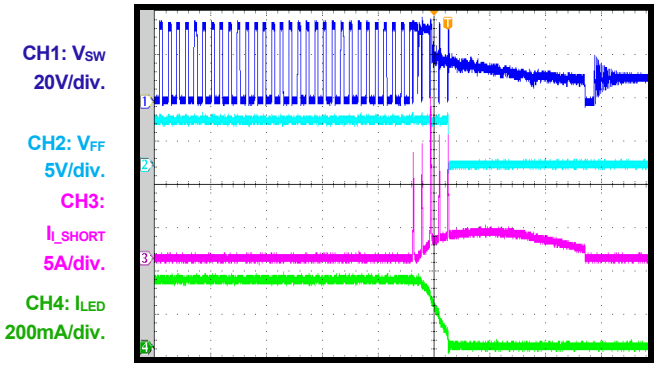
4ms/div.

Short Inductor Protection



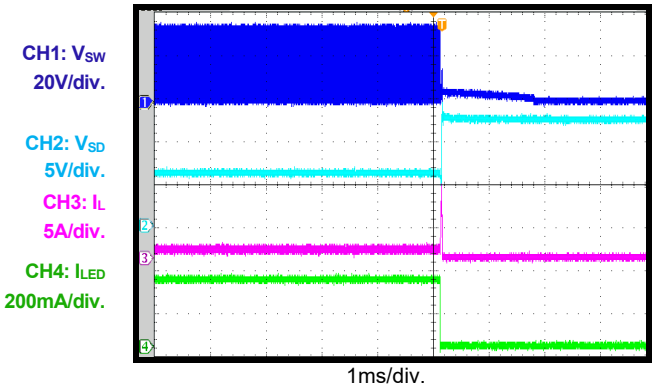
10µs/div.

Short Diode Protection



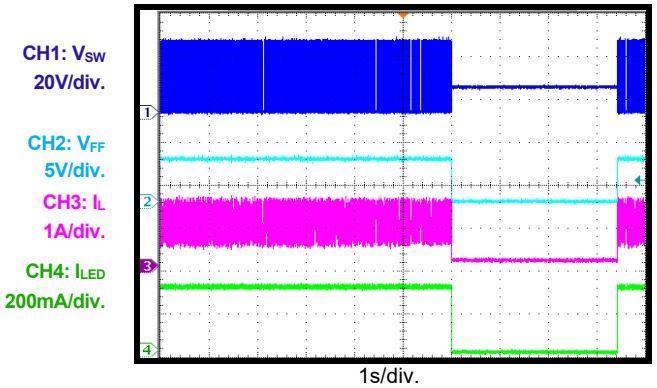
10µs/div.

Short VOUT to GND Protection



1ms/div.

Thermal Protection



1s/div.

FUNCTIONAL BLOCK DIAGRAM

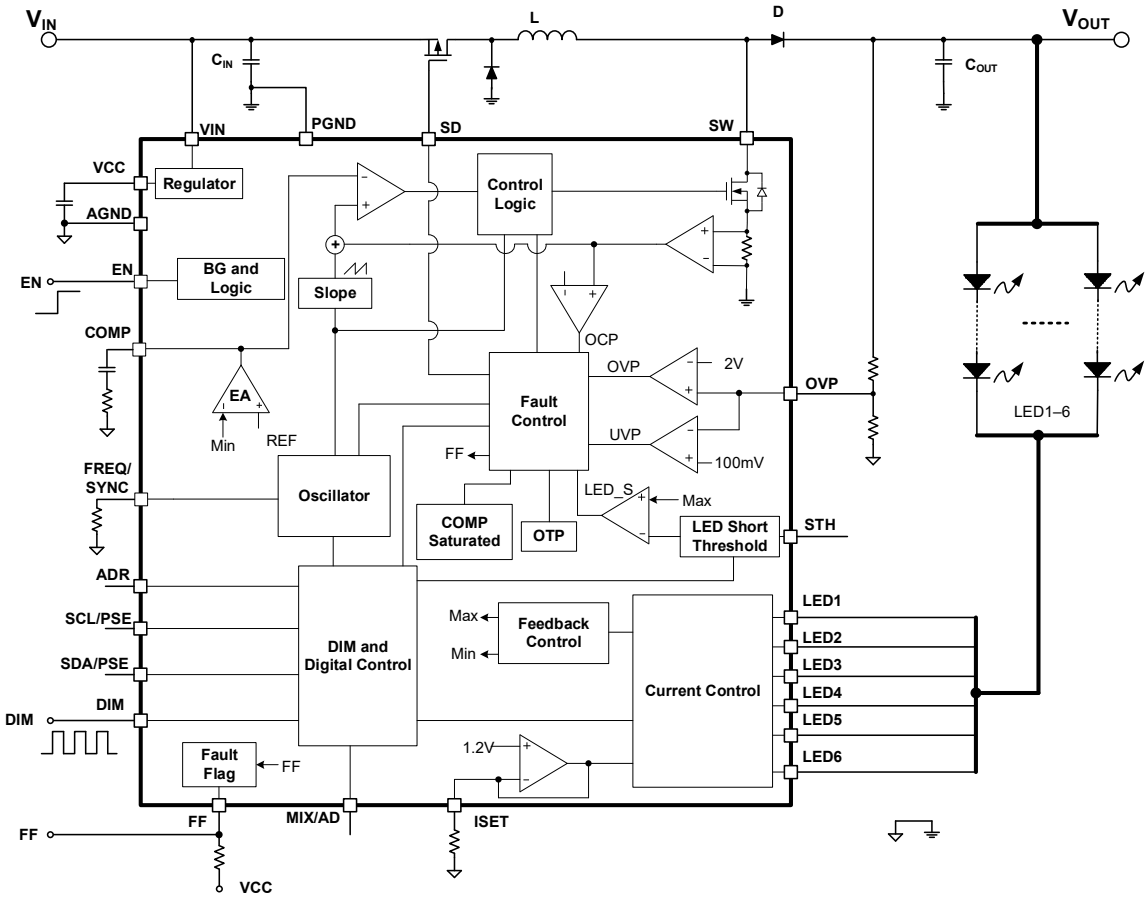


Figure 1: Functional Block Diagram

OPERATION

The MPQ3367A is a configurable, constant-frequency, peak current mode step-up converter with up to 6 channels of regulated current sources to drive an array of white LEDs.

Internal 5V Regulator

The MPQ3367A includes an internal linear regulator (VCC). When V_{IN} exceeds 6V, this regulator outputs a 5V power supply to the internal MOSFET switch gate driver and the internal control circuitry. The VCC voltage (V_{CC}) drops to 0V when the chip shuts down. The chip remains disabled until V_{CC} exceeds the under-voltage lockout (UVLO) threshold.

System Start-Up

When enabled, the MPQ3367A checks the topology connection. The IC draws current from SD to turn on the input disconnect PMOS (if this PMOS is used). After a 500µs delay, the IC monitors the OVP pin to see if the output is shorted to GND. If the OVP voltage is below 100mV, the IC is disabled, and it latches off. The MPQ3367A then continues to check other safety limits (e.g. LED open, over-voltage protection). If all protection tests pass, the IC starts boosting the step-up converter.

The recommended start-up sequence is listed below:

1. V_{IN}
2. EN
3. I²C (optional)
4. PWM dimming signal

Step-Up Converter

The MPQ3367A employs peak current mode control to regulate the output power. At the beginning of each switching cycle, the internal clock turns on the internal N-channel MOSFET. In normal operation, the minimum turn-on time is about 100ns. A stabilizing ramp is added to the output of the current-sense amplifier to prevent sub-harmonic oscillations for duty cycles exceeding 50%. This result is fed into the PWM comparator. When the summed voltage reaches the output voltage of the error amplifier, the internal MOSFET turns off.

The output voltage of the internal error amplifier is an amplified signal of the difference between the reference voltage (V_{REF}) and the feedback voltage (V_{FB}). The converter automatically chooses the lowest active LEDx pin voltage to provide a sufficient output voltage to power all the LED arrays.

If V_{FB} drops below V_{REF}, the output of the error amplifier increases. Then more current flows through the MOSFET, which increases the power delivered to the output. This forms a closed loop that regulates the output voltage.

During light-load operation (e.g. when V_{OUT} is almost equal to V_{IN}), the switching frequency will be stretched down.

Dimming Control

The MPQ3367A provides analog, PWM, and mix dimming methods. The dimming mode can be set with the I²C, or by connecting a different resistor at MIX/AD. The MIX/AD voltage can be calculated with Equation (1):

$$V_{\_MIX/AD}\ (mV) = 18\ (\mu A) \times R_{\_MIX/AD}\ (k\Omega) \quad (1)$$

Where $V_{\_MIX/AD}$ is the MIX/AD voltage and $R_{\_MIX/AD}$ is the MIX/AD resistor.

Mix Dimming Mode

The MPQ3367A works in mix dimming mode with a 25% or 12.5% transfer point (selected through the internal register).

The first method is to connect a resistor and set MIX/AD to a low level (<0.3V).

The second method is to float MIX/AD, and set the internal mode selection register (MODE1:0) to 00 through the I²C.

A PWM dimming signal is applied to DIM. When the dimming duty exceeds 25%, the device uses analog dimming, and the LED current amplitude follows the PWM duty.

When the dimming duty is below 25%, the device uses PWM dimming (see Figure 2 on page 16). The LED current amplitude remains at 1/4 of the full-scale current, and the output dimming duty is 4 times the duty of the input PWM signal.

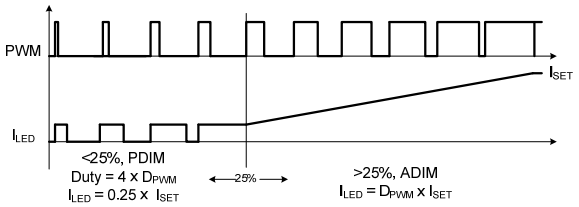


Figure 2: Mix Dimming with 25% Transfer Point

There are two options for the output dimming frequency when the device uses mix dimming: 200Hz (default), or 23kHz (no audible noise, but larger minimum dimming duty). The output dimming frequency is not related to the input PWM dimming frequency. The output dimming frequency is selected with the mix dimming output frequency selection bit through the I²C. This function eliminates audible noise and improves the dimming performance when there is a small dimming ratio.

Direct PWM Dimming Mode

Connect a resistor to set MIX/AD to a middle level (0.5V to 0.8V), or float MIX/AD and set the internal mode selection register (MODE1:0) to 01 through the I²C.

When a PWM signal is applied to DIM, the amplitude of the LED current remains at the LED full-scale current, and the LED current is chopped by the input PWM signal. The LED current duty follows the PWM input duty, and the LED current frequency is the same as the PWM input.

Analog Dimming Mode

Connect a resistor to set MIX/AD to a high level (1V to 1.3V), or float MIX/AD and set the internal mode selection register (MODE1:0) to 10 through the I²C.

The PWM input signal is calculated by an internal counter. The amplitude of the LED current is equal to I_{SET} x D_{DIM}, where I_{SET} is the full-scale LED current, and D_{DIM} is the duty of the input PWM signal.

Analog dimming supports a 200:1 dimming ratio.

Deep Dimming Ratio for PWM Dimming

When the output dimming on time is shorter than 7μs, V_{OUT} is regulated to be 93% of the OVP voltage (see Figure 3).

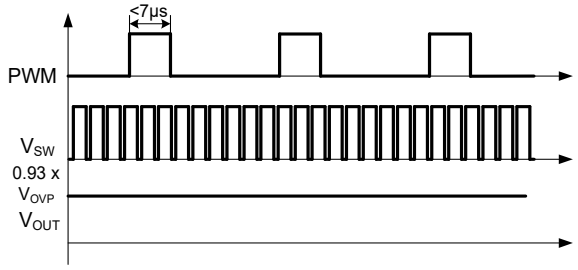


Figure 3: Deep Dimming Ratio for PWM Dimming

Unused LED Channel Setting

If an unused LEDx pin is connected to GND, the MPQ3367A can automatically detect it and remove it from the control loop during start-up. For example, if five strings are used, connect the LED6 pin to GND. If four strings are used, connect the LED5 and LED6 pins to GND.

The MPQ3367A can also disable the unused string via internal register (CH2:0), described in greater detail below:

- CH2:0 = 000: All 6 channels are in use
- CH2:0 = 001: LED1~5 are in use
- CH2:0 = 010: LED1~4 are in use
- CH2:0 = 011: LED1~3 are in use
- CH2:0 = 100: LED1~2 are in use
- CH2:0 = 101: LED1 is in use

Phase Shift Function

To reduce inrush current and eliminate audible noise during PWM dimming, the MPQ3367A employs a phase shift function.

Two methods can be used to enable the phase shift function. The first method is to connect SCL/PSE and SDA/PSE together, and set them between 0.75V and 1V. The second method is to set the internal register PSE bit to 1 through the I²C.

The LED channels' current source are phase shifted when the IC employs PWM dimming. The shifted phase depends on how many LED channels are in use.

The phase shift can be calculated with Equation (2):

$$Phase(°) = \frac{360}{n}(°) \quad (2)$$

Where n is the number of LED channels being used. For example, if all six channels are in use, the shifted phase is 60°. LED1 directly follows the internal calculated PWM signal PWMI, and LED2 lags 60° behind (see Figure 4).

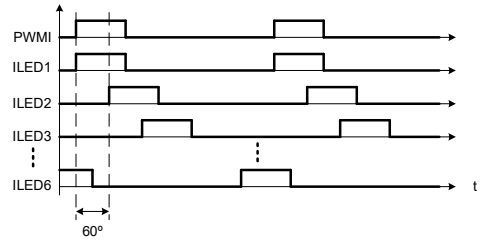


Figure 4: Phase Shift with 6 Channels

Figure 5 shows the phase shift function when four channels are enabled. In this case, the phase shift is 90°.

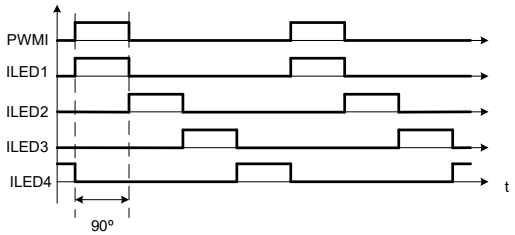


Figure 5: Phase Shift with 4 Channels

In phase shift operation, the channels must be disabled in descending order of channel number. For example, if three strings are employed in an application, then channels 6, 5, and 4 are disabled.

It is not recommended to tie two channels to 1 LED string when the phase shift function is enabled.

Frequency Spread Spectrum

The MPQ3367A uses switching frequency jitter to spread the switching frequency spectrum. This reduces the spectrum spike around the switching frequency and its harmonic frequencies.

The frequency jitter range is selected by the FSPR bit.

- When FSPR = 0 (default), the frequency jitter range is 1/10 of the switching frequency.
- When FSPR = 1, the frequency jitter range is 1/16 of the switching frequency.

The modulation frequency is selected by the FSPMF1:0 bits.

- When FSPMF1:0 = 00, the modulation frequency is 1/100 of the switching frequency.
- When FSPMF1:0 = 01, the modulation frequency is 1/150 of the switching frequency.
- When FSPMF1:0 = 10, the modulation frequency is 1/200 of the switching frequency.
- When FSPMF1:0 = 11 (default), this function is disabled.

Protections

The MPQ3367A provides open LED protection, short LED protection, short LEDx to GND protection, over-current protection, short VOUT to GND protection, and thermal protection. Once the protection is triggered, FF is pulled to GND, and the corresponding fault bit is set to 1. After the IC recovers from a protection, FF is pulled high with a 750μs delay.

Open LED Protection

Open string protection is achieved by detecting the voltage on the OVP pin and LEDx pins. If one string is open during normal operation, the respective LEDx voltage is low to ground, and the IC keeps charging the output voltage until it reaches the over-voltage protection threshold.

If over-voltage protection (OVP) has been triggered, the chip stops switching and marks off the fault string which has a LEDx pin voltage below 100mV. The remaining LED strings force the output voltage back into normal regulation. The string with the largest voltage drop determines the output regulation value. Every 500μs, the string that was marked off sends a 10μs pulse current to check whether the open fault is removed. This means that open string protection is recoverable.

Short String Protection

The MPQ3367A monitors the LEDx voltages to determine whether a short string fault has occurred. If one or more strings are shorted, the shorted LEDx pins tolerate the high voltage stress. If an LEDx voltage exceeds the short protection threshold, an internal counter starts.

If the fault condition lasts for 7.7ms (D_{PWM} = 100%), the fault string is marked off. Once a string is marked off, it disconnects from the output voltage loop until the short condition is removed.

Two methods can set the short protection threshold. The first method is to connect a resistor on the STH pin. STH outputs an 18μA current source. The short protection threshold is 10 times the voltage on STH. The threshold can be calculated with Equation (3):

$$V_{\_STH\_TH}(V) = 0.18 \times R_{\_STH}(k\Omega) \quad (3)$$

The second method is to set the internal register (TH_S1:0) when STH is floating.

If all LEDx voltages exceed the threshold for 480ms (D_{PWM} = 100%), all strings are marked off. The IC remains on standby mode until the strings are released from the short condition. Enable or disable this function through SEN.

Every 500μs, the string that was marked off sends a 10μs pulse current to check if the short fault is removed. This means that short string protection is recoverable.

Short LEDx to GND Protection

If LEDx is shorted to GND, the COMP voltage increases and saturates. If COMP is saturated for 40ms, a protection is triggered. FF pulls low, and SD pulls high to turn off the external P-channel MOSFET. Then the IC latches off.

Short VOUT to GND Protection

When VOUT is shorted to GND, the output voltage decreases. If the voltage on the OVP pin reaches the under-voltage lockout (UVLO) threshold for 10μs, the protection is triggered. SD pulls high to turn off the external P-channel MOSFET. VOUT disconnects from VIN, and the IC latches off.

Cycle-by-Cycle Current Limit

To prevent the external components from exceeding the current stress rating, the IC has cycle-by-cycle current limit protection. When the current exceeds the current limit value, the internal low side MOSFET turns off until the next clock cycle.

Latch-Off Current Limit Protection

The device can be damaged by extreme conditions, such as an inductor or diode short to GND. To avoid this, the MPQ3367A provides latch-off current limit protection. If the current flowing through the internal MOSFET reaches 7.5A, and lasts for 5 switching cycles, current limit protection is triggered.

Thermal Protection

To prevent the IC from operating at exceedingly high temperatures, the MPQ3367A implements thermal protection by detecting the silicon die temperature.

Over-Temperature LED Current Decrement

If the die temperature exceeds 140°C, the MPQ3367A automatically decreases the LED current amplitude (see Figure 6).

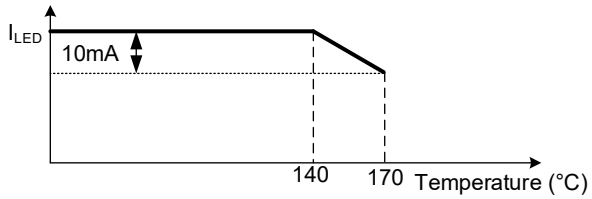


Figure 6: I_{LED} Decreases with Temperature

This function is enabled by the over-temperature current decrement bit (OTID).

- When OTID = 0, the over-temperature current decrement is disabled.
- When OTID = 1 (default), the over-temperature current decrement is enabled.

Thermal Shutdown

If the die temperature exceeds the upper threshold (T_{ST}), the IC shuts down. When the temperature drops below the lower threshold, the IC recovers. The typical hysteresis value is 20°C.

I²C Interface

I²C Chip Address

The 7-bit MSB device address is 0x38~0x3A. This address can be selected through the ADR pin. When the ADR pin is floating, the IC address is 0x38. When ADR < 0.4V, the IC address is 0x3A. When ADR is between 0.4V and 1.4V, the IC address is 0x39. The ADR pin's pull-up current is 18μA.After the start condition, the I²C-compatible master sends a 7-bit address followed by an eighth read (1) or write (0) bit.

Figure 7 shows an I²C-compatible device address.

0	1	1	1	0	X	X	R/W

Figure 7: I²C-Compatible Device Address

REGISTER MAP

If using the internal registers, float the corresponding pins.

Add	D7	D6	D5	D4	D3	D2	D1	D0
00h	OTID	MODE1	MODE0	MIXTP	MIXFR	FSPMF1	FSPMF0	FSPR
01h	PSE	TH_S1	TH_S0	FSW1	FSW0	CH2	CH1	CH0
02h	SEN	DISABLE_IC	FT_LEDG	FT_OTP	FT_UVP	FT_OCP	FT_LEDS	FT_LEDO
03h	RESERVED	RESERVED	ID5	ID4	ID3	ID2	ID1	ID0

Function Set Register 1

Addr: 0x00				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7	OTID	R/W	1	Over-temperature LED current decrement function enable bit. 0: Disabled 1: Enabled
6:5	MODE	R/W	00	Dimming mode selection bits. Float the MIX/AD pin if this register is used. 00: Mix dimming 01: PWM dimming 10: Analog dimming 11: Reserved
4	MIXTP	R/W	0	Mix dimming transfer point selection bit. 0: 25% transfer point 1:12.5% transfer point
3	MIXFR	R/W	0	Mix dimming output frequency selection bit. 0: 200Hz 1: 23kHz
2:1	FSPMF1:0	R/W	11	Frequency spread spectrum modulation frequency selection bits. 00: 1/100 of the switching frequency 01: 1/150 of the switching frequency 10: 1/200 of the switching frequency 11: Disable the frequency spread spectrum function
0	FSPR	R/W	0	Frequency spread spectrum jitter range selection bit. 0: 1/10 of the central frequency 1: 1/16 of the central frequency

Function Set Register 2

Addr: 0x01				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7	PSE	R/W	0	Phase shift enable bit. 0: Phase shift disabled 1: Phase shift enabled

6:5	TH_S1:0	R/W	01	LED short protection threshold setting bits. 00: 2.5V 01: 5V 10: 7.5V 11: 10V
4:3	FSW1:0	R/W	01	Switching frequency setting bits. Float the FREQ/SYNC pin if this register is used. 00: 200kHz 01: 400kHz 10: 1MHz 11: 2.2MHz
2:0	CH2:0	R/W	000	Channel selection bits. 000: All 6 channels are in use 001: LED1~5 are in use 010: LED1~4 are in use 011: LED1~3 are in use 100: LED1~2 are in use 101: LED1 is in use 110, 111: Reserved

Fault Register

Addr: 0x02				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7	SEN	R/W	0	Short all LED protection enable bit. 0: Disabled 1: Enabled
6	DISABLE_IC	R/W	0	This bit disables the IC. 0: The IC is enabled 1: The IC is disabled
5	FT_LEDG	R	0	LEDx short to GND protection fault indication bit. If a LEDx short fault occurs, the fault bit is set to 1 until a power reset occurs. 0: No LEDx short fault has occurred 1: An LEDx short fault has occurred
4	FT_OTP	R	0	Over-temperature protection (OTP) fault indication bit. If an OT fault occurs, the fault bit is set to 1 until a readback or power reset occurs. The fault status latches off. If the fault is removed, it is reset to 0 after this bit is read. 0: No OT fault has occurred 1: An OT fault has occurred
3	FT_UVP	R	0	Output under-voltage protection (UVP) fault indication bit. If a UV fault occurs, the fault bit is set to 1 until a power reset occurs. 0: No UV fault has occurred 1: A UV fault has occurred
2	FT_OCP	R	0	Over-current protection (OCP) fault indication bit. If an OC fault occurs, the fault bit is set to 1 until a power reset occurs. 0: No OC fault has occurred 1: An OC fault has occurred

1	FT_LEDS	R	0	LED short fault indication bit. If a current source short fault occurs, the fault bit is set to 1 until a readback or power reset occurs. The fault status latches off. If the fault is removed, it is reset to 0 after this bit is read. 0: No LED current source short fault has occurred 1: An LED current source short fault has occurred
0	FT_LEDO	R	0	LED open fault indication bit. If an open fault occurs, the fault bit is set to 1 until a readback or power reset occurs. The fault status latches off. If the fault is removed, it is reset to 0 after this bit is read. 0: No LED current source open fault has occurred 1: An LED current source open fault has occurred

ID Register

Addr: 0x03				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:6	RESERVED	-	-	Reserved.
5:0	ID7:0	R	01100111	Device ID bits.

APPLICATION INFORMATION

LED Current Setting

The LED current amplitude is set by an external resistor connected from ISET to GND. The LED current amplitude can be calculated with Equation (4):

$$I_{LED}(mA) = \frac{1245}{R_{ISET}(k\Omega)} \quad (4)$$

For example, if R_{ISET} = 24.9kΩ, the LED current is 50mA.

Switching Frequency

The switching frequency can be configured by a resistor, I²C interface, or external clock.

To configure the frequency with an external resistor on FREQ/SYNC, the switching frequency can be estimated with Equation (5):

$$f_{SW}(kHz) = \frac{22000}{R_{FREQ}(k\Omega)} \quad (5)$$

For example, if R_{FREQ} = 44.2kΩ, the switching frequency is set to 500kHz.

If setting the switching frequency via the I²C interface, float the FREQ/SYNC pin. The FSW1:0 bits have the following options:

- 00: 200kHz
- 01: 400kHz
- 10: 1MHz
- 11: 2.2MHz

Selecting the Input Capacitor

The input capacitor reduces the surge current drawn from the input supply, as well as the switching noise from the device. Use ceramic capacitors with X5R or X7R dielectrics due to their low ESR and small temperature coefficients. For most applications, a 10µF ceramic capacitor is sufficient.

Selecting the Inductor

The MPQ3367A requires an inductor to supply a higher output voltage while being driven by the input voltage. A larger-value inductor results in less ripple current, lower peak inductor current, and less stress on the internal N-channel MOSFET. However, a larger-value inductor has a larger physical size, higher series resistance, and lower saturation current.

Choose an inductor that does not saturate under the worst-case load conditions. Select the minimum inductor value to ensure that the boost converter works in continuous conduction mode (CCM) with high efficiency and good EMI performance.

Calculate the required inductance value using Equation (6):

$$L \geq \frac{\eta \times V_{OUT} \times D \times (1-D)^2}{2 \times f_{SW} \times I_{LOAD}} \quad (6)$$

Where V_{OUT} is the output voltage, I_{LOAD} is the LED load current, η is the efficiency, f_{SW} is the switching frequency, and D can be estimated with Equation (7):

$$D = 1 - \frac{V_{IN}}{V_{OUT}} \quad (7)$$

Where V_{IN} is the input voltage.

With the given inductor value, the inductor DC current rating should be at least 40% greater than the maximum input peak inductor current for most applications. The inductor's DC resistance should be as small as possible for higher efficiency.

Selecting the Output Capacitor

The output capacitor keeps the output voltage ripple small and ensures feedback loop stability. Ceramic capacitors with X7R dielectrics are recommended for their low-ESR characteristics. For most applications, a 10µF ceramic capacitor is sufficient.

Selecting the Over-Voltage Protection (OVP) Threshold

Open string protection is achieved by monitoring the voltage on the OVP pin. An LED string failure can result in the feedback voltage dropping to 0. If this occurs, the MPQ3367A continues boosting the output voltage until it reaches the configured OVP threshold. Then OVP is triggered.

Select appropriate values for the OVP pin's resistor divider to set the OVP threshold. The recommended OVP threshold is about 1.1 to 1.2 times the output voltage under normal operation.

The OVP threshold can be estimated with Equation (8):

$$V_{OVP} = 2 \times (1 + \frac{R_{OVP\_HIGH}}{R_{OVP\_LOW}}) \quad (8)$$

Where R_{OVP_HIGH} is the OVP pin's high-side resistor, and R_{OVP_LOW} is the OVP pin's low-side resistor.

PCB Layout Guidelines

Careful attention must be given to the PCB layout and component placement. Efficient placement of the high-frequency switching path is critical to prevent noise and electromagnetic interference. For the best results, refer to Figure 8 and follow the guidelines below:

1. Connect the IC's exposed pad to the AGND pin, and ensure that all logic signals are referred to AGND.
2. Externally connect PGND to AGND. Route PGND away from the logic signals.
3. Keep the loop between the SW and PGND pin, output diode (D1), and capacitors (C1 and C2) as short as possible due to the high-frequency pulse current.

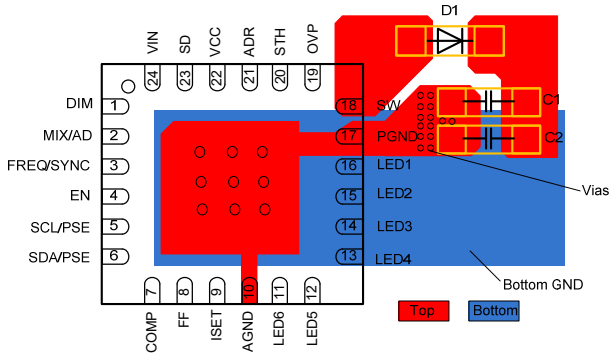


Figure 8: Recommended PCB Layout

TYPICAL APPLICATION CIRCUIT

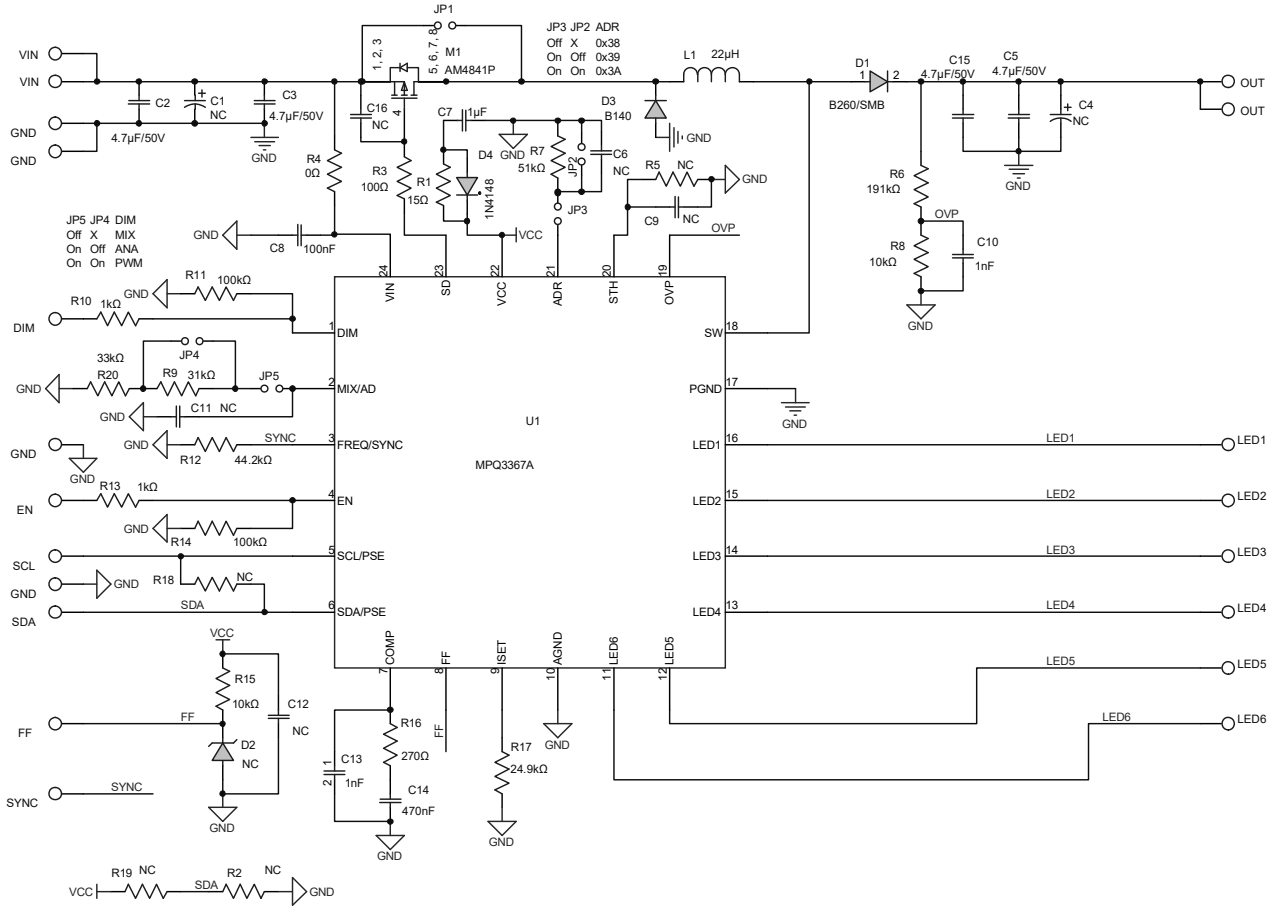
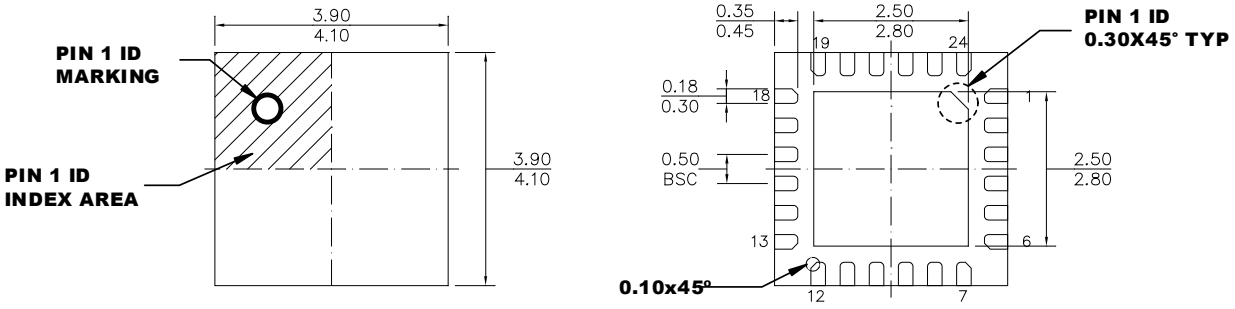


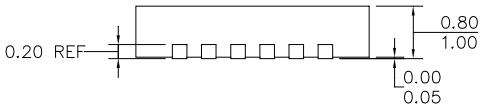
Figure 9: Typical Application Circuit

PACKAGE INFORMATION

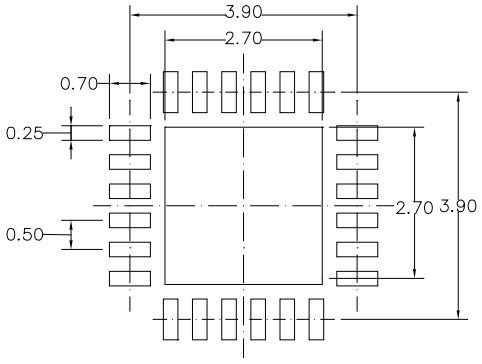
QFN-24
(4mmx4mm)



TOP VIEW **BOTTOM VIEW**



SIDE VIEW



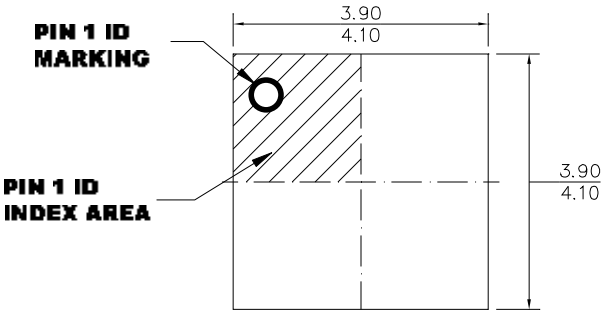
RECOMMENDED LAND PATTERN

NOTE:

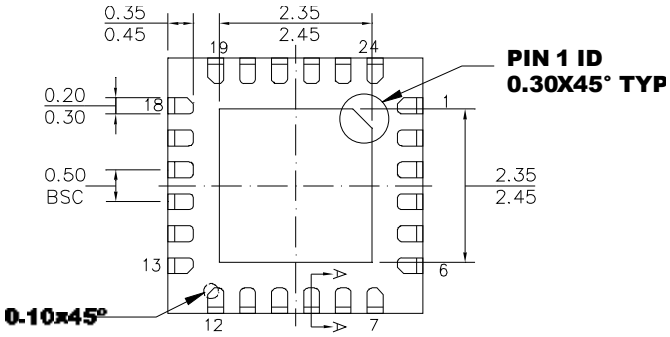
1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220
5) DRAWING IS NOT TO SCALE.

PACKAGE INFORMATION

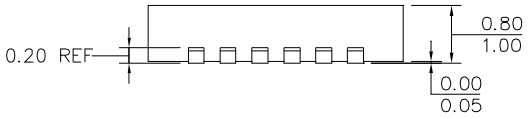
QFN-24 (4mmx4mm) WF



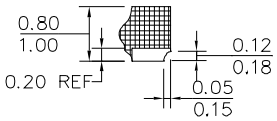
TOP VIEW



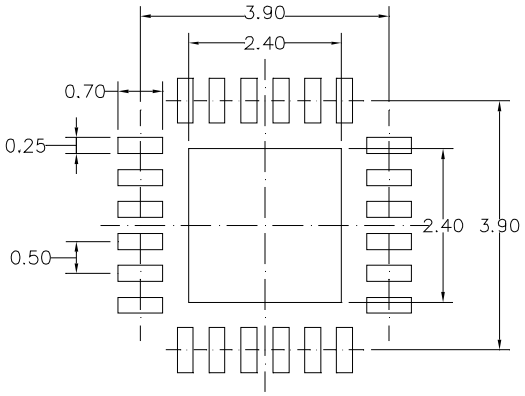
BOTTOM VIEW



SIDE VIEW



SECTION A-A

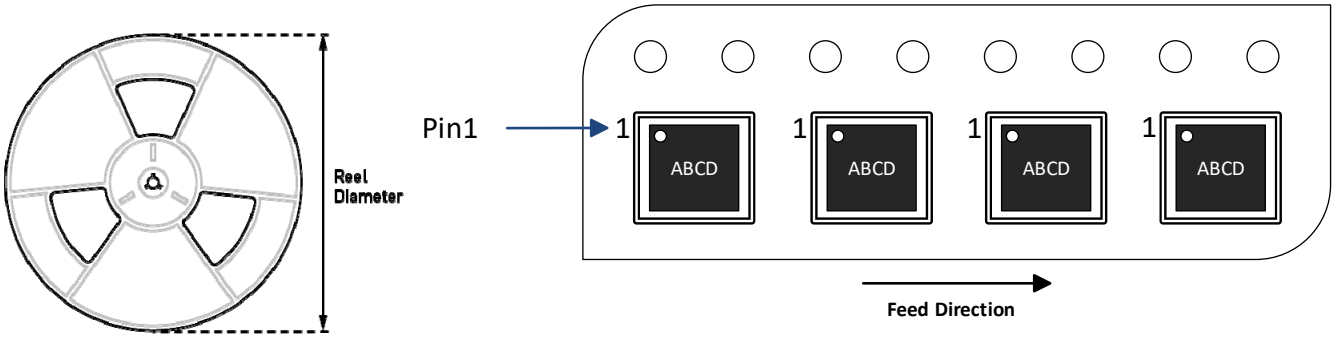


RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tray	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ3367AGR-AEC1-Z	QFN-24 (4mmx4mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	09/17/2021	Initial Release	-