



6V Input, 1.2A Module Synchronous Step-Down Converter with Integrated Inductor AEC-Q100 Qualified

DESCRIPTION

The MPM3810 is an automotive-grade, step-down module converter with built-in power MOSFETs and inductor. The module's integrated inductor simplifies the power system design and provides easy, efficient use. The DC/DC module comes in a small surface-mount QFN-12 (2.5mmx3.0mmx0.9mm) package and achieves 1.2A peak output current from a 2.5V-6V input voltage with excellent load and line regulation. The output voltage is regulated as low as 0.6V. Only FB resistors and input/output capacitors are needed to complete the design.

The constant-on-time control (COT) scheme provides fast, transient response and eases loop stabilization. Fault condition protection includes cycle-by-cycle current limiting and thermal shutdown (TSD).

The MPM3810 is ideal for a wide range of automotive applications, including small ECUs, camera modules, telematics, and infotainment systems.

FEATURES

- Guaranteed Industrial/Automotive Temp
- Wide 2.5V to 6V Operating Input Range
- Adjustable Output from 0.6V
- QFN-12 (2.5mmx3.0mmx0.9mm) Package
- Total Solution Size 6mmx3.8mm
- Up to 1.2A Peak Output Current
- 100% Duty Cycle in Dropout
- Ultra Low I_O: 17µA
- EN and Power Good for Power Sequencing
- Cycle-by-Cycle Over-Current Protection
- Short-Circuit Protection with Hiccup Mode
- Only Needs 4 External Components: 2 Ceramic Capacitors and FB Divider Resistors
- Available in AEC-Q100

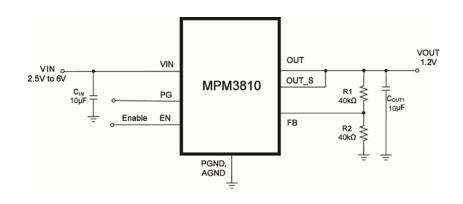
APPLICATIONS

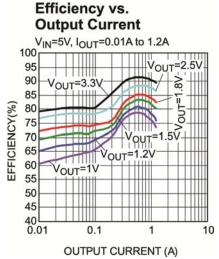
- Automotive ECU
- Rear Camera
- Ecall
- Telematics
- Infotainment System

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance.

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TYPICAL APPLICATION







ORDERING INFORMATION

Part Number*	Package	Top Marking
MPM3810GQB-AEC1	QFN-12 (2.5mmx3.0mmx0.9mm)	See Below

^{*} For Tape & Reel, add suffix –Z (e.g. MPM3810GQB-AEC1–Z)

TOP MARKING

AEZ

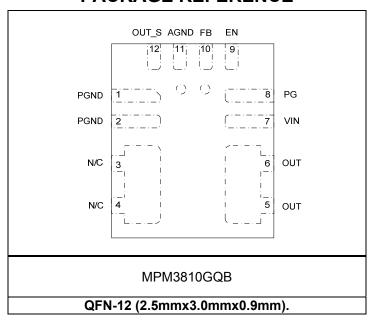
YWW

LLL

AEZ: Product code of MPM3810GQB-AEC1

Y: Year code WW: Week code LLL: Lot number

PACKAGE REFERENCE



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ABSOLUTE MAXIMUM RATINGS (1)
Supply voltage (V _{IN}) 6.5V
V _{SW}
-0.3V (-5V for <10ns) to 6.5V (7V for <10ns)
All other pins0.3V to 6.5 V
Junction temperature
Lead temperature
Continuous power dissipation $(T_A = +25^{\circ}C)^{(2)}$
1.9W
Storage temperature65°C to +150°C
Recommended Operating Conditions
Supply voltage (V _{IN})2.5V to 6V
Output voltage (V _{OUT})12% x V _{IN} to V _{IN}
Operating junction temp. (T _J)40°C to +125°C

Thermal Resistance (3)	$oldsymbol{ heta}_{JA}$	$\boldsymbol{ heta}_{JC}$	
QFN-12 (2.5mmx3.0mm)	65	13	°C/W

Notes:

- 1) Exceeding these ratings may damage the device.
- 2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA} , and the ambient temperature T_A . The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = $(T_J$ (MAX)- T_A)/ θ_{JA} . Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- 3) Measured on JESD51-7, 4-layer PCB.

3/24/2016



ELECTRICAL CHARACTERISTICS

 V_{IN} = 5V, T_J = -40°C to +125°C, unless otherwise noted. Typical value are at T_J = +25°C.

Parameter	Symbol	Condition	Min	Тур	Max	Units	
Foodback voltage	V	$2.5V \le V_{IN} \le 6V,$ $T_{J} = +25^{\circ}C$	588	600	612	m\/	
Feedback voltage	V_{FB}	$2.5V \le V_{IN} \le 6V$, $T_{J} = -40^{\circ}C$ to $+125^{\circ}C$	573		627	– mV	
Feedback current	I _{FB}	V _{FB} = 0.63V		10	1000	nA	
PFET switch-on resistance	R _{DSON P}			100	230	mΩ	
NFET switch-on resistance	R _{DSON N}			60	130	mΩ	
Inductor L value	L	Inductance value at 1MHz		0.47		μH	
Inductor DC resistance	R _{DCR}			120		mΩ	
Dropout resistance	R_{DR}	100% on duty		220		mΩ	
Switch leakage		$V_{EN} = 0V, V_{IN} = 6V$ $V_{SW} = 0V \text{ and } 6V, ,$ $T_{J} = +25^{\circ}C$		0	1	μA	
PFET current limit		$T_J = +25^{\circ}C$	1.6	2.1	2.6	A	
PFET Current iimit		$T_J = -40^{\circ}\text{C to } +125^{\circ}\text{C}$	1.5		2.7		
On time	т	$V_{IN} = 5V, V_{OUT} = 1.2V$		70		no	
On time	T _{ON}	$V_{IN} = 3.6V, V_{OUT} = 1.2V$		100		- ns	
Switching frequency	F _s	$V_{IN} = 3.6V, V_{OUT} = 1.2V$	2800	3500	4200	kHz	
Minimum off time	$T_{MIN\text{-}OFF}$			60		ns	
Soft-start time	T _{SS-ON}			1.5		ms	
Power good upper trip threshold	PG _H	FB voltage in respect to the regulation		+10		%	
Power good lower trip threshold	PG_L			-10		%	
Power good delay	PG_D			50		μs	
Power good sink current capability	V_{PG-L}	Sink 1mA			0.4	V	
Power Good Logic High Voltage	V_{PG-H}	V _{IN} =5V, V _{FB} =0.6V	4.9			V	
Power Good Internal Pull-Up Resistor	R _{PG}			550		kΩ	



ELECTRICAL CHARACTERISTICS (continued)

 V_{IN} = 5V, T_J = -40°C to +125°C, unless otherwise noted. Typical value are at T_J = +25°C.

Parameter	Symbol	Condition	Min	Тур	Max	Units
Under-voltage lockout threshold rising			2.15	2.3	2.48	V
Under-voltage lockout threshold hysteresis				300		mV
EN input logic low voltage					0.4	V
EN input logic high voltage			1.2			V
EN input ourrent		V _{EN} = 2V		1.5		μA
EN input current		V _{EN} = 0V		0.1	1	μΑ
		$V_{EN} = 0V, T_J = +25^{\circ}C$			1	
Supply current (shutdown)		$V_{EN} = 0V$, $T_J = -40^{\circ}C$ to $+125^{\circ}C$			10	μA
		$V_{EN} = 2V, V_{FB} = 0.63V,$ $V_{IN} = 5V, T_J = +25^{\circ}C$		17	21	
Supply current (quiescent)		$V_{EN} = 2V, V_{FB} = 0.63V,$ $V_{IN} = 5,$ $T_{J} = -40^{\circ}C$ to +125°C			30	μA
Thermal shutdown ⁽⁴⁾				150		°C
Thermal hysteresis ⁽⁴⁾				30		°C

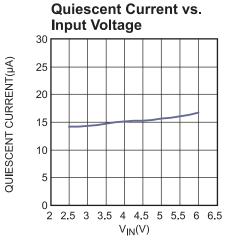
Notes:

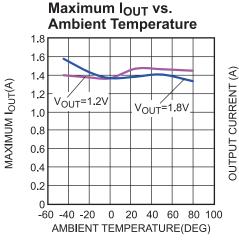
⁴⁾ Not production tested, guaranteed by design.

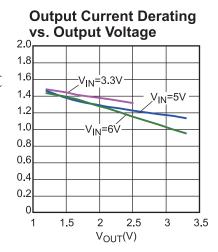


TYPICAL PERFORMANCE CHARACTERISTICS

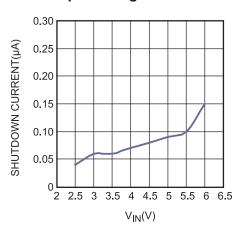
 V_{IN} = 5V, V_{OUT} = 1.2V, C_{IN} = 10 μ F, C_{OUT} = 20 μ F, T_A = +25°C, unless otherwise noted.



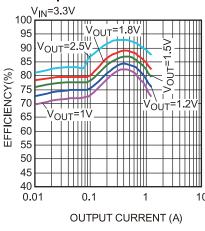




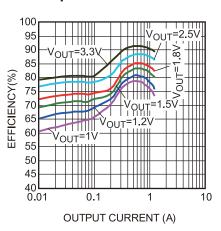
Shutdown Current vs. **Input Voltage**



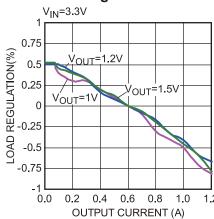
Efficiency vs. **Output Current**



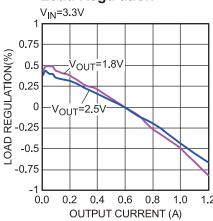
Efficiency vs. **Output Current**



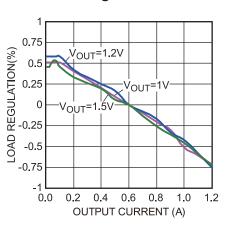
Load Regulation



Load Regulation



Load Regulation

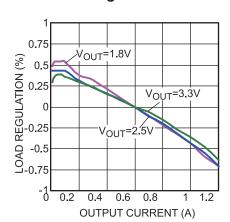


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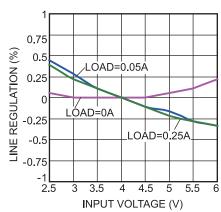


 V_{IN} = 5V, V_{OUT} = 1.2V, C_{IN} = 10 μ F, C_{OUT} = 20 μ F, T_A = +25 $^{\circ}$ C, unless otherwise noted.

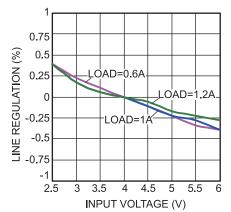
Load Regulation



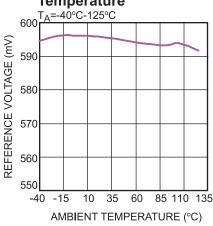
Line Regulation



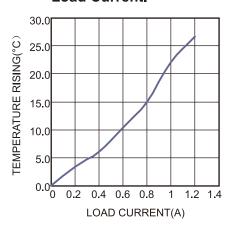
Line Regulation



Reference Voltage vs. Temperature

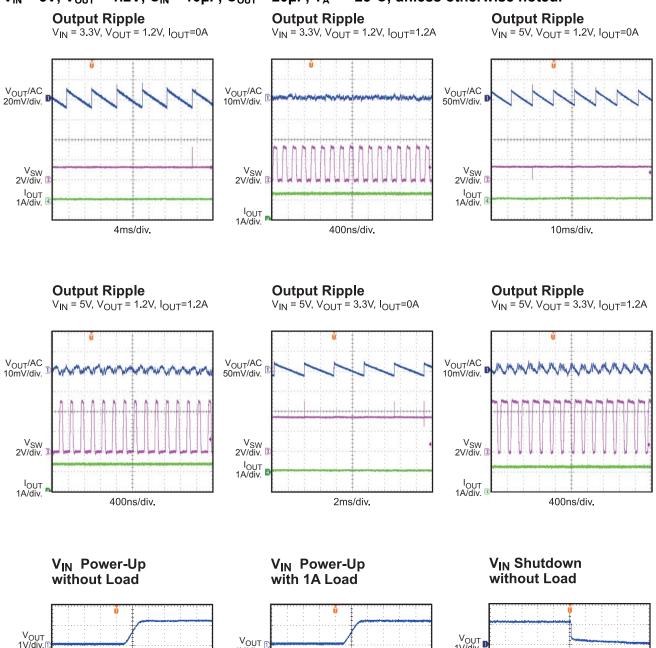


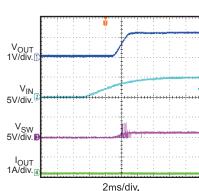
Thermal Rising vs. Load Current.

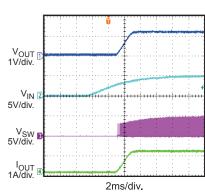


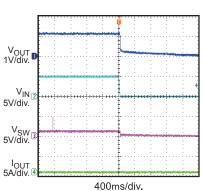


 V_{IN} = 5V, V_{OUT} = 1.2V, C_{IN} = 10 μ F, C_{OUT} = 20 μ F, T_A = +25 $^{\circ}$ C, unless otherwise noted.



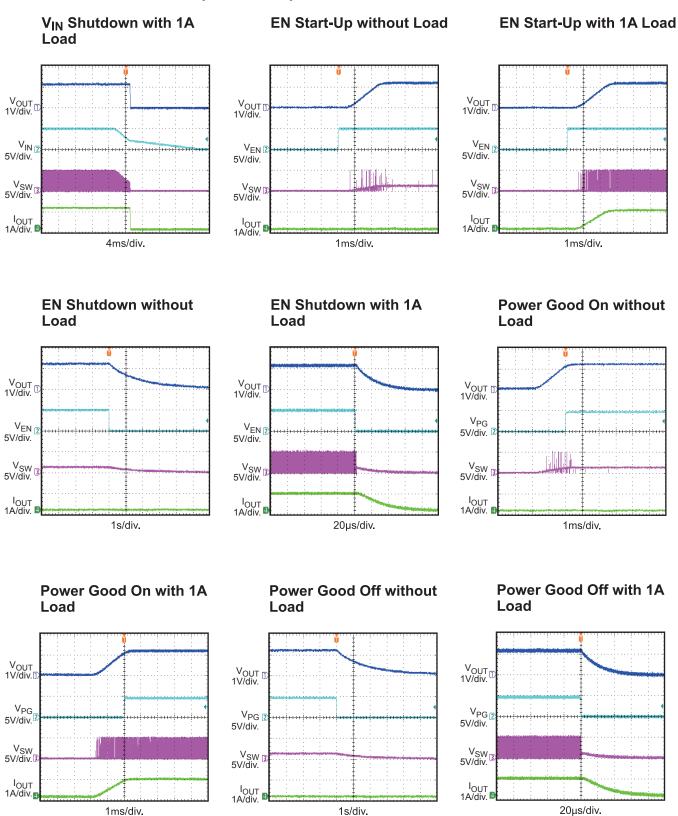








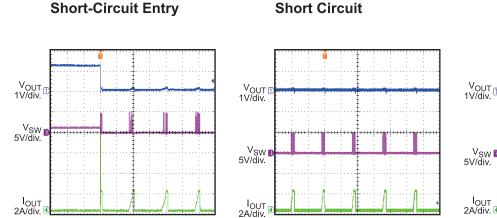
 V_{IN} = 5V, V_{OUT} = 1.2V, C_{IN} = 10 μ F, C_{OUT} = 20 μ F, T_A = +25 $^{\circ}$ C, unless otherwise noted.



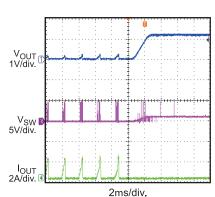
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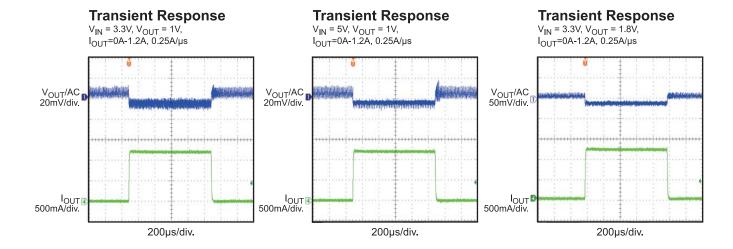
 V_{IN} = 5V, V_{OUT} = 1.2V, C_{IN} = 10 μ F, C_{OUT} = 20 μ F, T_A = +25°C, unless otherwise noted.



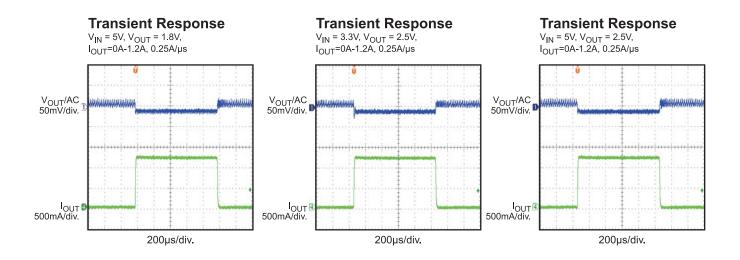
1ms/div.



Short-Circuit Recovery



1ms/div.

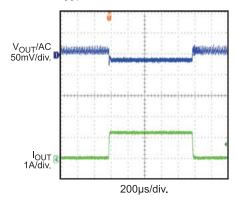




 V_{IN} = 5V, V_{OUT} = 1.2V, C_{IN} = 10 μ F, C_{OUT} = 20 μ F, T_A = +25 $^{\circ}$ C, unless otherwise noted.

Transient Response

 V_{IN} = 5V, V_{OUT} = 3.3V, I_{OUT} =0A-0.6A, 0.25A/µs





PIN FUNCTIONS

Pin#	Name	Description
1, 2	PGND	Power ground.
3, 4	N/C	Internal SW pad.
5, 6	OUT	Output voltage power rail. Connect the load to OUT. An output capacitor is required.
7	VIN	Supply voltage . The MPM3810 operates from a +2.5V to +6V unregulated input. A decoupling capacitor is needed to prevent large voltage spikes from appearing at the input. Place the decoupling capacitor as close to VIN as possible.
8	PG	Power good indicator . The output of PG is an open drain with an internal pull-up resistor to VIN. PG is pulled up to VIN when the FB voltage is within 10% of the regulation level. If the FB voltage is out of that regulation range, PG is low.
9	EN	On/off control.
10	FB	Feedback. An external resistor divider from the output to GND (tapped to the FB) sets the output voltage.
11	AGND	Analog ground for internal control circuit.
12	OUT_S	Output voltage sense.



OPERATION

The MPM3810 is available in a small surface-mount QFN-12 (2.5mmx3.0mmx0.9mm) package. The DC/DC module's integrated inductor simplifies the schematic and layout design. Only FB resistors and input/output capacitors are needed to complete the design. The MPM3810 uses constant-on-time control (COT) with input voltage feed forward to stabilize the switching frequency over a full input range. At light load, the MPM3810 employs a proprietary control of the low-side switch and inductor current to improve efficiency.

Constant-On-Time Control (COT)

Compared to a fixed-frequency PWM control, constant-on-time control (COT) offers the advantage of a simpler control loop and faster transient response. Using input voltage feed forward, the MPM3810 maintains a nearly constant switching frequency across the input and output voltage range. The on time of the switching pulse can be estimated with Equation (1):

$$T_{ON} = \frac{V_{OUT}}{V_{IN}} \cdot 0.28us \tag{1}$$

To prevent inductor current run away during the load transition, the MPM3810 fixes the minimum off time to 60ns. However, this minimum off-time limit does not affect operation in a steady state.

Light-Load Operation

In a light-load condition, the MPM3810 uses a proprietary control scheme to save power and improve efficiency. The MP3810 turns off the low-side switch when the inductor current begins to reverse. Then the MP3810 works in discontinuous conduction mode (DCM) operation.

A zero-current cross circuit detects if the inductor current begins to reverse. Considering the internal circuit propagation time, the typical delay time is 30ns. This means the inductor current continues to fall after the ZCD is triggered. If the inductor current falling slew rate is fast (Vo voltage is high or close to Vin), the low-side MOSFET turns off (this means the inductor current may be negative). This does not allow the MPM3810 to enter DCM. If DCM is required, the off time of the low-side MOSFET in continuous conduction mode (CCM) should be longer than

60ns. For example, if Vin is 3.6V and Vo is 3.3V, the off time in CCM is 24ns. It is difficult to enter DCM at light load.

Enable (EN)

If the input voltage is greater than the undervoltage lockout threshold (UVLO), typically 2.3V, the MPM3810 is enabled by pulling EN above 1.2V. Leaving EN floating or pulling it down to ground disables the MPM3810. There is an internal $1M\Omega$ resistor from EN to ground.

Soft Start (SS)

The MPM3810 has a built-in soft start that ramps up the output voltage in a controlled slew rate. This avoids overshoot at start-up. The soft-start time is about 1.5ms typically.

Power GOOD Indictor (PGOOD)

The MPM3810 has an open drain with a $550k\Omega$ pull-up resistor pin for the power good indicator (PGOOD). When FB is within +/-10% of the regulation voltage (i.e. 0.6V), PGOOD is pulled up to IN by the internal resistor. If FB voltage is out of the +/-10% window, PGOOD is pulled down to ground by an internal MOSFET. The MOSFET has a maximum R_{dson} of less than 400Ω .

Current Limit

The MPM3810 has a typical 2.1A current limit for the high-side switch. When the high-side switch reaches the current limit, the MPM3810 hits the hiccup threshold until the current decreases. This prevents the inductor current from continuing to build, which results in damage to the components.

Short Circuit and Recovery

The MPM3810 enters short-circuit protection (SCP) mode when the current limit is reached; then it tries to recover from the short circuit with hiccup mode. In SCP, the MPM3810 disables the output power stage, discharges the soft-start cap, and then automatically tries to soft start again. If the short circuit remains after the soft start ends, The MPM3810 repeats the cycle until the short circuit disappears, and the output rises back to the regulation level.



FUNCTIONAL BLOCK DIAGRAM

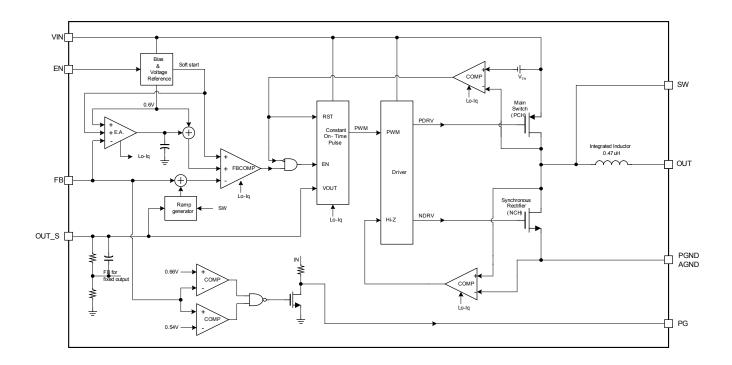


Figure 1: Functional Block Diagram



APPLICATION INFORMATION

COMPONENT SELECTION

Setting the Output Voltage

The external resistor divider is used to set the output voltage (see the Typical Application on page 16). The feedback resistor R1 cannot be too large or too small considering the trade-off for stability and dynamics. Choose a value for R1 between $40k\Omega$ to $80k\Omega$. R2 is can then be calculated with Equation (2):

$$R2 = \frac{R1}{\frac{V_{\text{out}}}{0.6} - 1}$$
 (2)

The feedback circuit is shown in Figure 2.

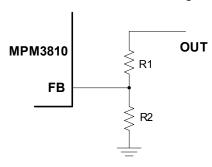


Figure 2: Feedback Network

Table 1 lists the recommended resistor values for common output voltages.

Table 1: Resistor Values for Common Output Voltages

V _{OUT} (V)	R1 (kΩ)	R2 (kΩ)
1.0	40(1%)	60(1%)
1.2	40(1%)	40(1%)
1.8	60(1%)	30(1%)
2.5	80(1%)	25(1%)
3.3	80(1%)	17.7(1%)

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current while maintaining the DC input voltage. For optimal performance, use low ESR capacitors. Ceramic capacitors with X5R or X7R dielectrics are highly recommended due to their low ESR and small temperature coefficients. For most applications, a 10µF capacitor is sufficient.

For a higher output voltage, a 22µF may be needed to enhance system stability.

Since the input capacitor absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (3):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}}} \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$
 (3)

The worst case condition occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (4):

$$I_{C1} = \frac{I_{LOAD}}{2} \tag{4}$$

For simplification, choose an input capacitor that has a RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum capacitors, a small, high-guality capacitor (i.e. 0.1µF) should be placed as close to the IC as possible. When using ceramic ensure they have capacitors. capacitance to provide sufficient charge to prevent an excessive voltage ripple at the input. The input voltage ripple caused by capacitance is estimated with Equation (5):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$
 (5)

Selecting the Output Capacitor

The output capacitor (C_{OUT}) is required to maintain the DC output voltage. Ceramic are recommended. capacitors Low capacitors are preferred to keep the output voltage ripple low. The output voltage ripple is estimated with Equation (6):

$$\Delta V_{\text{OUT}} = \frac{V_{\text{OUT}}}{f_s \times L_1} \times \left(1 - \frac{V_{\text{OUT}}}{V_{\text{IN}}}\right) \times \left(R_{\text{ESR}} + \frac{1}{8 \times f_s \times C2}\right)$$
 (6)

Where L₁ is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor (L_1 is 0.47 μ H).

When using ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly



caused by the capacitance. For simplification, the output voltage ripple is estimated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$
 (7)

When using tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR}$$
 (8)

The characteristics of the output capacitor affect the stability of the regulation system.

PCB Layout

Efficient PCB layout is critical for stable operation. The module's integrated inductor simplifies the schematic and layout design. Only FB resistors and input/output capacitors are needed to complete the design. For best results, refer to Figure 3 and Figure 4 and follow the guidelines below:

- Place the high-current paths (PGND, IN and OUT) very close to the device with short, direct, and wide traces.
- 2. Place the input capacitor as close to IN and PGND as possible.
- 3. Place the external feedback resistors next to FB.
- 4. Keep the switching node away from the feedback network.

For additional device applications, please refer to related evaluation board datasheets (EVB).

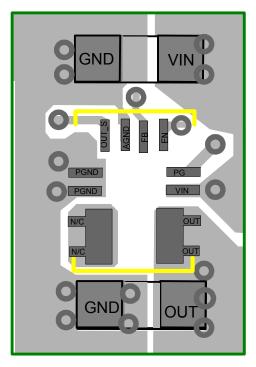


Figure 3: Top View of Layout Guide

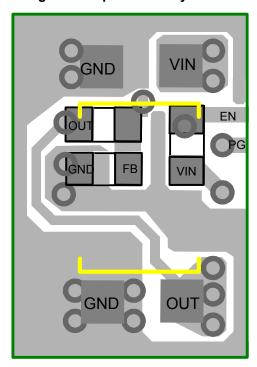


Figure 4: Bottom View of Layout Guide



TYPICAL APPLICATION CIRCUITS

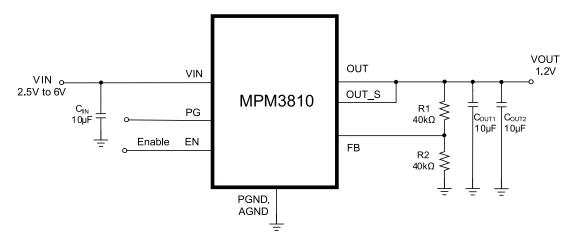
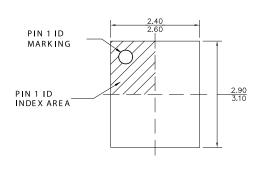


Figure 5: Typical Application Circuits

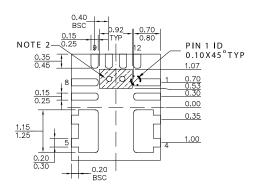


PACKAGE INFORMATION

QFN-12 (2.5mmx3.0mm)



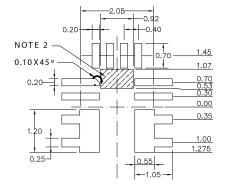




BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS
 2) SHADED AREA IS THE KEEPOUT ZONE. THE EXPOSED BOTTOM METAL PADS ENCLOSED BY THIS ZONE IS NOT TO BE CONNECTED TO ANY PCB METAL TRACE& VIA ELECTRICALLY OR MECHANICALLY.
- 3) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
- 4) LEAD COPLANARITY SHALL BE0.10 MILLIMETERS MAX.
- 5) JEDEC REFERENCE IS MO220.
- 6) DRAWING IS NOT TO SCALE

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