MPM3630

18V/3A DC/DC Module
Synchronous Step-Down Regulator
with Integrated Inductor

The Future of Analog IC Technology

DESCRIPTION

The MPM3630 is a synchronous rectified, step-down module regulator with built-in power MOSFETs, inductor, and two capacitors. It offers a very compact solution to achieve a 3A continuous output current with excellent load and line regulation over a wide input supply range. The MPM3630 has a 1.4MHz switching frequency, which provides fast load transient response.

Full protection features include over-current protection (OCP) and thermal shutdown (TSD).

The MPM3630 eliminates design and manufacturing risks while dramatically improving time-to-market.

The MPM3630 is available in a space-saving QFN20 (3mmx5mmx1.6mm) package.

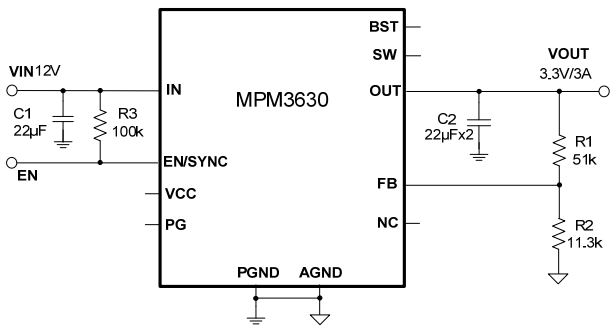
FEATURES

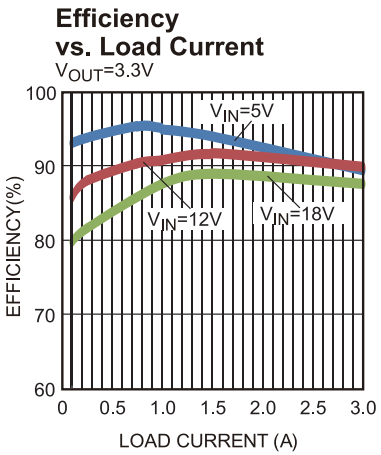
- Complete Switch Mode Power Supply
- 4.5V to 18V Wide Operating Input Range
- 3A Continuous Load Current
- 50mΩ/22mΩ Low RDS(ON) Internal Power MOSFETs
- Integrated Inductor
- Fixed 1.4MHz Switching Frequency
- 1MHz-2MHz Frequency Sync
- Internal Power Save Mode for Light Load
- Power Good Indicator
- OCP Protection and Hiccup
- Thermal Shutdown
- Output Adjustable from 0.6V
- Available in QFN20 (3x5x1.6mm) Package

APPLICATIONS

- Industrial Controls
- Medical and Imaging Equipment
- Telecom Applications
- LDO Replacement
- Space and Resource-Limited Applications
- Distributed Power Systems

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking
MPM3630GQV	QFN-20 (3mmx5mmx1.6mm)	*See Below*

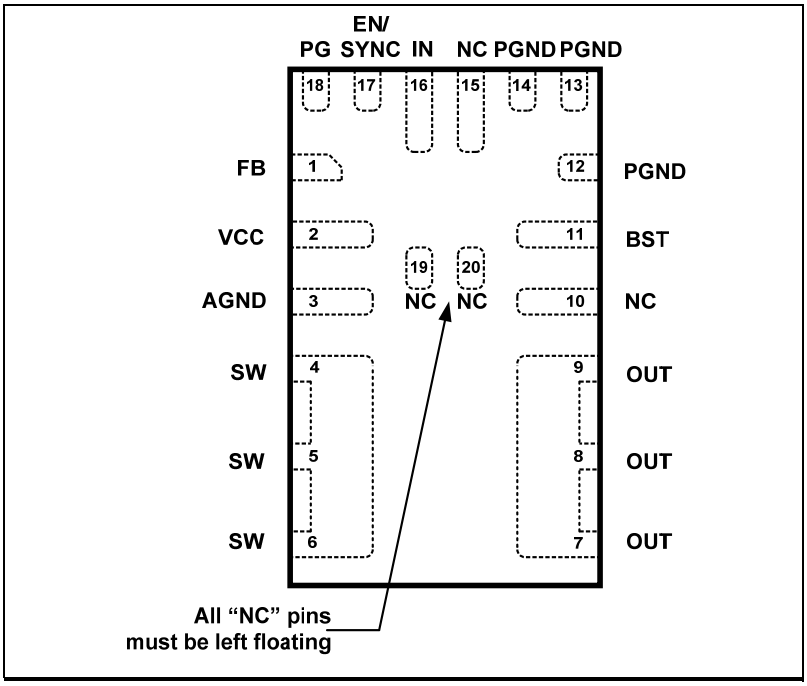
* For Tape & Reel, add suffix –Z (e.g. MPM3630GQV–Z)

TOP MARKING

MPYW
3630
LLL
M

MP: MPS prefix
Y: Year code
W: Week code
3630: First four digits of the part number
LLL: Lot number
M: Module

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} ..... -0.3V to 20V
V_{OUT} ..... -0.3V to 20V
V_{SW} .....
-0.3V (-5V for <10ns) to 20V (22V for <10ns)
V_{BST}.....V_{SW}+5.5V
All other pins ..... -0.3V to 5.5V (2)
Continuous power dissipation (T_A = +25°C) (3)
.....2.7W
Junction temperature ..... 150°C
Lead temperature..... 260°C
Storage temperature .....-65°C to 150°C

Recommended Operating Conditions (4)

Supply voltage (V_{IN}) ..... 4.5V to 18V
Output voltage (V_{OUT}) ……..
……..……...0.6V to V_{IN} *D_{MAX} (5)
Operating junction temp. (T_J)....-40°C to +125°C

Thermal Resistance (6) θ_{JA} θ_{JC}

QFN-20 (3mmx5mmx1.6mm)	46	10 ... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) For additional details on EN pin's ABS MAX rating, please refer to the "Enable/SYNC Control" section.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) In practical design, the minimum V_{OUT} is limited by the minimum on-time. To allow a margin, a 50ns on-time is recommended for calculating. To set the output voltage above 5.5V, please refer to the application information.
6) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C(7), typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply current (shutdown)	I_{IN}	VEN = 0V		5.5	8	μA
Supply current (quiescent)	I_q	V_{FB} = 0.7V		320	420	μA
HS switch on resistance	HS_{RDS-ON}	V_{BST-SW} = 5V		50		mΩ
LS switch on resistance	LS_{RDS-ON}	V_{CC} = 5V		22		mΩ
Inductor DC resistance	L_{DCR}			40		mΩ
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 0V			1	μA
Current limit (8)	I_{LIMIT}	30% Duty cycle	5	6.5		A
Oscillator frequency	f_{SW}	V_{FB} = 0.5V	1100	1400	1600	kHz
Foldback frequency	f_{FB}	V_{FB} = 200mV		0.4		f_{SW}
Maximum duty cycle	D_{MAX}	V_{FB} = 500mV	85	90		%
Minimum on time(8)	T_{ON_MIN}			50		ns
Feedback voltage	V_{FB}	T_A = 25°C	594	600	606	mV
Feedback voltage	V_{FB}		591	600	609	mV
Feedback current	I_{FB}	V_{FB} = 620mV		10	50	nA
EN Rising threshold	V_{EN_RISING}		1.2	1.4	1.6	V
EN Falling threshold	$V_{EN\_FALLING}$		1.1	1.25	1.4	V
EN input current	I_{EN}	V_{EN} = 2V		1.8		μA
EN turn off delay(8)	EN_{Td-off}			2.5		μs
SYNC frequency range			1000		2000	kHz
VIN under-voltage lockout threshold—rising	$INUV_{Vth}$		3.9	4.1	4.3	V
VIN under-voltage lockout threshold—hysteresis	$INUV_{HYS}$			740		mV
PG rising threshold	PG_{Vth-Hi}		0.87	0.92	0.97	V_{FB}
PG falling threshold	PG_{Vth-Lo}		0.76	0.81	0.86	V_{FB}
PG rising delay	PG_{Td}	Rising edge		110		μs
PG falling delay	PG_{Td}	Falling edge		26		
PG sink current capability	V_{PG}	Sink 2mA			0.4	V
PG leakage current	$I_{PG-LEAK}$	4.5V		2		μA
VCC regulator	V_{CC}			5		V
VCC load regulation		I_{CC} = 5mA			3	%
Soft-start time	t_{SS}	V_{OUT} from 10% to 90%		2.2		ms
Thermal shutdown (8)				150		°C
Thermal hysteresis (8)				20		°C

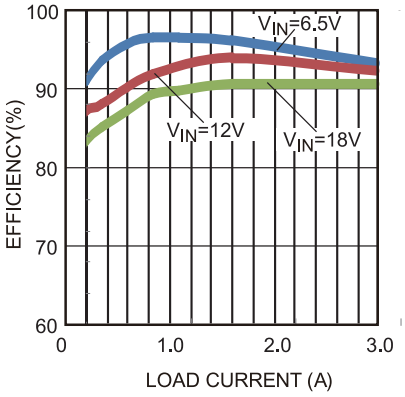
Notes:

7) Not tested in production. Guaranteed by over-temperature correlation.
8) Guaranteed by engineering sample characterization test.

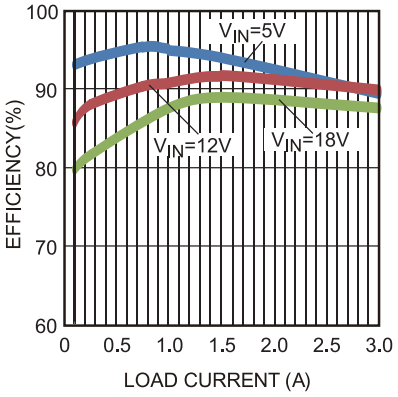
TYPICAL CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 3.3V, T_A = 25°C, unless otherwise noted.

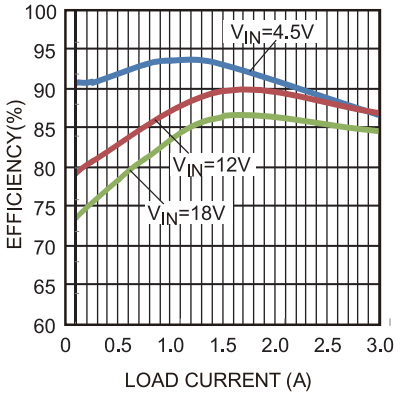
Efficiency vs. Load Current
V_{OUT}=5V



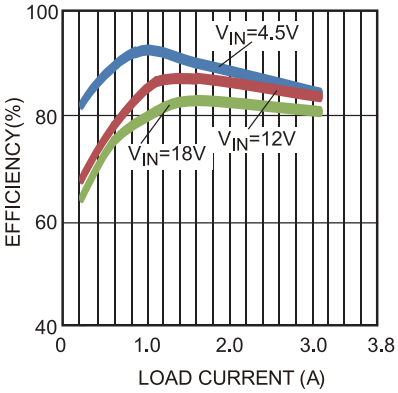
Efficiency vs. Load Current
V_{OUT}=3.3V



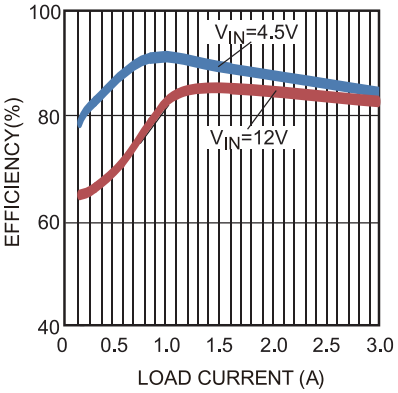
Efficiency vs. Load Current
V_{OUT}=2.5V



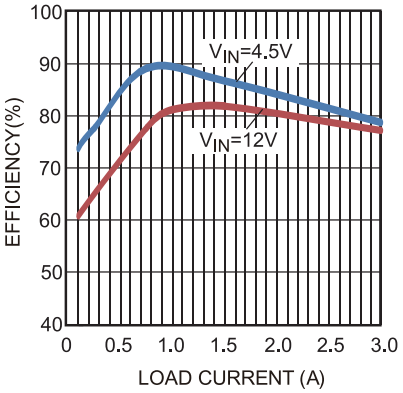
Efficiency vs. Load Current
V_{OUT}=1.8V



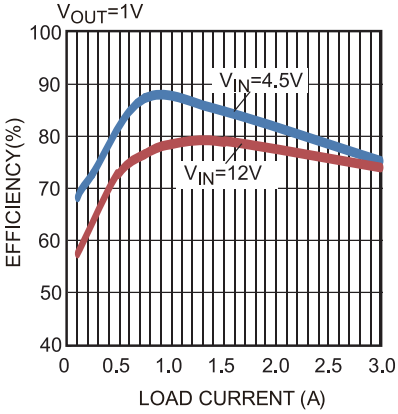
Efficiency vs. Load Current
V_{OUT}=1.5V



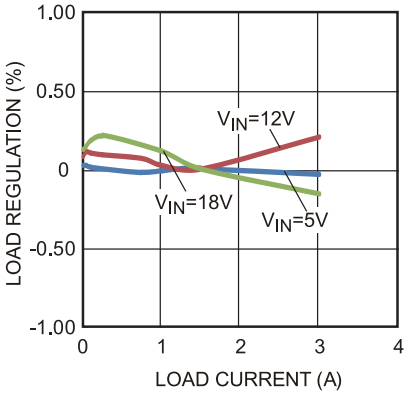
Efficiency vs. Load Current
V_{OUT}=1.2V



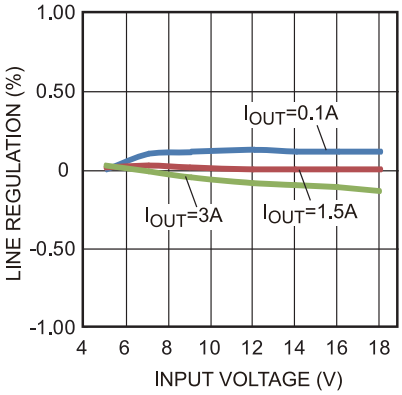
Efficiency vs. Load Current
V_{OUT}=1V



Load Regulation
V_{OUT}=3.3V



Line Regulation
V_{OUT}=3.3V



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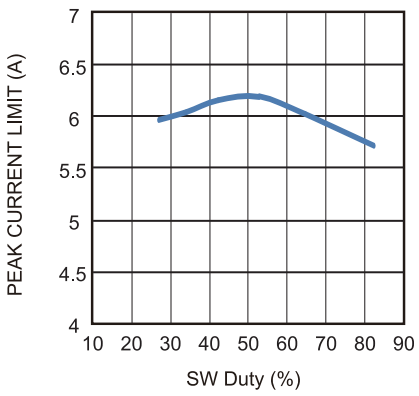
TYPICAL CHARACTERISTICS *(continued)*

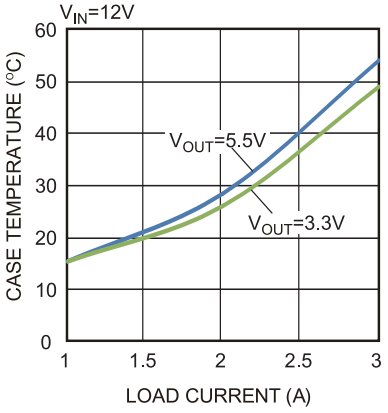
V_{IN} = 12V, V_{OUT} = 3.3V, T_A = 25°C, unless otherwise noted.

Inductor Peak-Current Limit vs. Duty Cycle



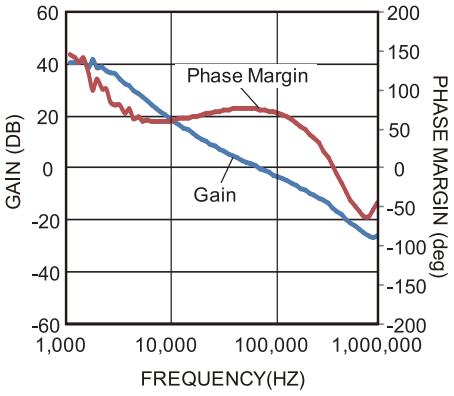
Case Temperature Rise vs. I_{OUT}

V_{IN}=12V

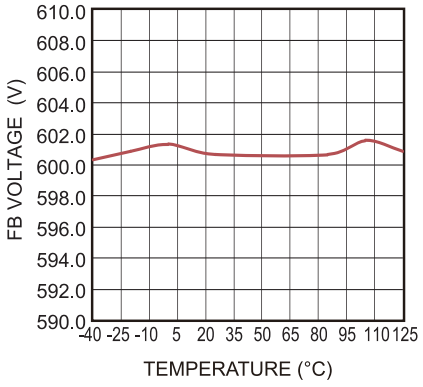


Bode Plot

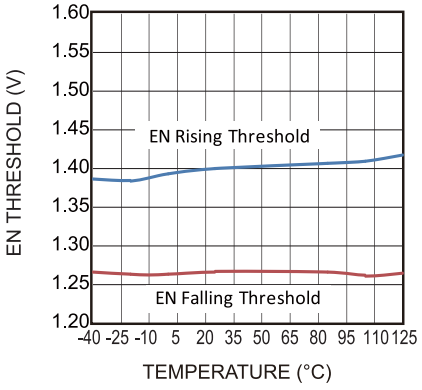
I_{OUT}=1.5A



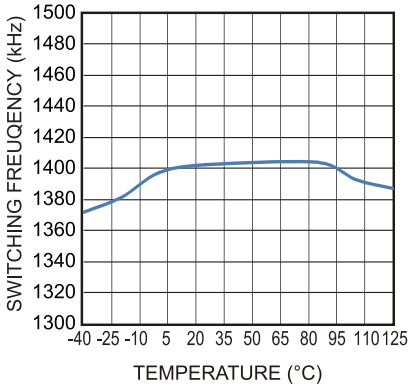
FB Voltage vs. Temperature



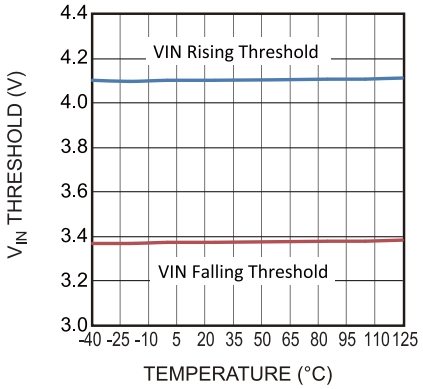
EN Threshold vs. Temperature



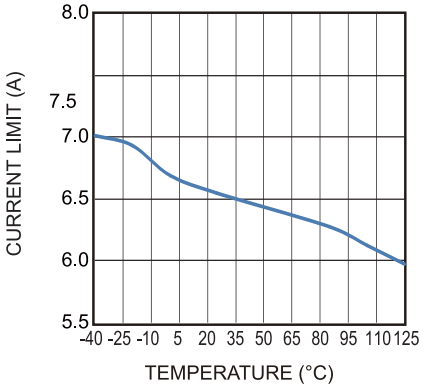
Switching Frequency vs. Temperature



FB Voltage vs. Temperature



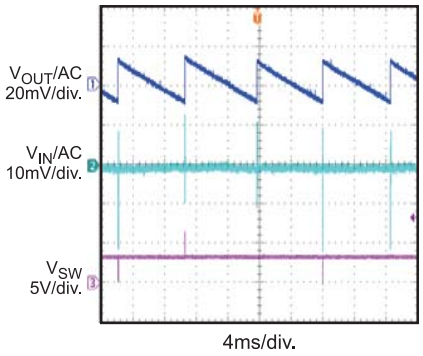
Inductor Peak-Current Limit vs. Temperature



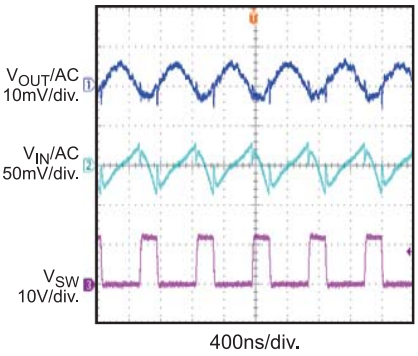
TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are captured from the evaluation board discussed in the Design Example section.V_{IN} = 12V, V_{OUT} = 3.3V, C_{OUT} = 22µFx2, T_A = 25°C, unless otherwise noted.

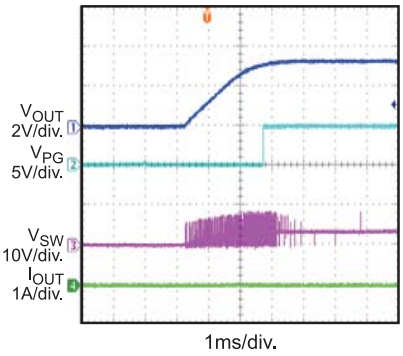
Output Ripple
I_{OUT}=0A



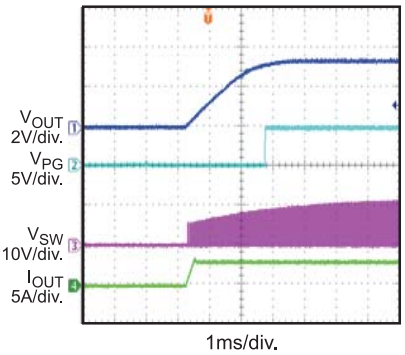
Output Ripple
I_{OUT}=3A



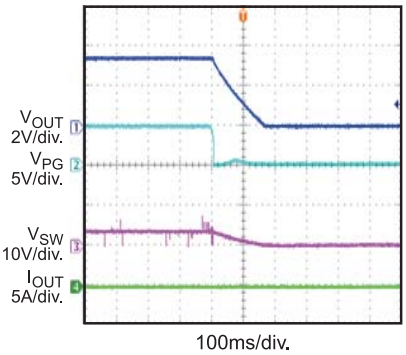
Start-Up through Input Voltage
I_{OUT}=0A



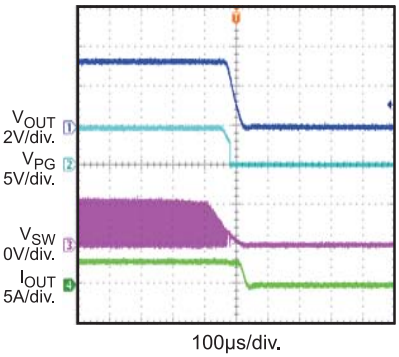
Start-Up through Input Voltage
I_{OUT}=3A



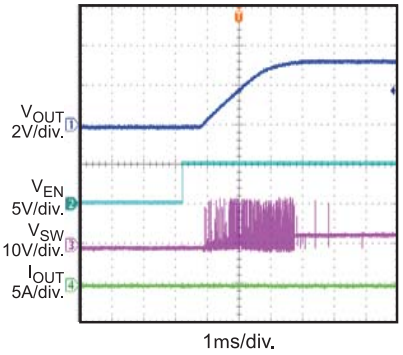
Shutdown through Input Voltage
I_{OUT}=0A



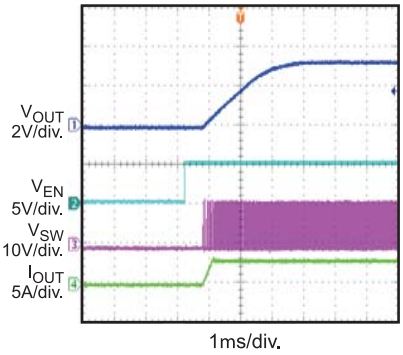
Shutdown through Input Voltage
I_{OUT}=3A



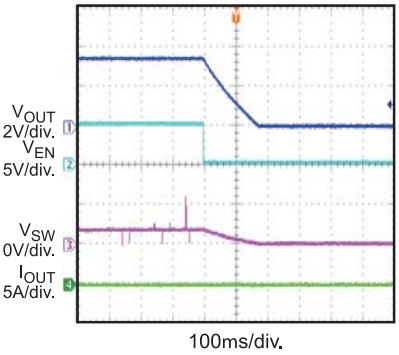
Start-Up through Enable
I_{OUT}=0A



Start-Up through Enable
I_{OUT}=3A



Shutdown through Enable
I_{OUT}=0A

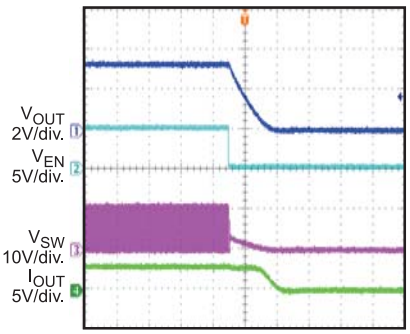


TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are captured from the evaluation board discussed in the Design Example section.V_{IN} = 12V, V_{OUT} = 3.3V, C_{OUT} = 22µFx2, T_A = 25°C, unless otherwise noted.

Shutdown through Enable

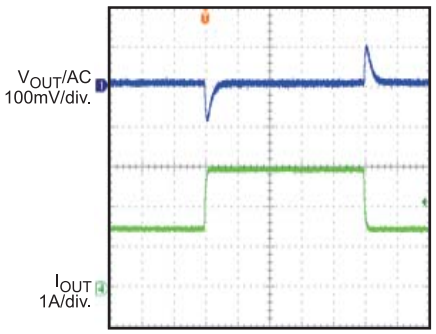
I_{OUT}=3A



40µs/div.

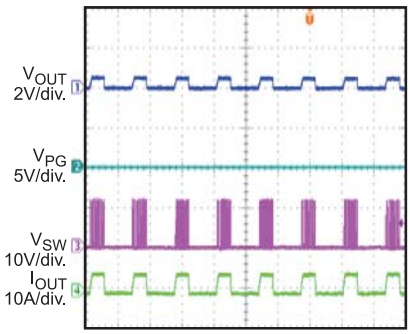
Load Transient Response

I_{OUT} transient from 1.5A to 3A



100µs/div.

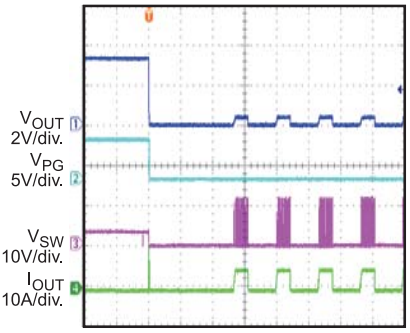
Short-Circuit Steady State



4ms/div.

Short-Circuit Entry

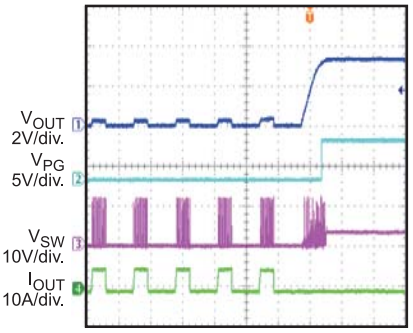
I_{OUT}=0A



4ms/div.

Short-Circuit Recovery

I_{OUT}=0A



4ms/div.

PIN FUNCTIONS

Package Pin #	Name	Description
1	FB	**Feedback.** Connect FB to the tap of an external resistor divider from the output to AGND to set the output voltage. To prevent current-limit runaway during a short-circuit fault, the frequency foldback comparator lowers the oscillator frequency when the FB voltage is below 240mV. Place the resistor divider as close as possible to FB. Avoid placing vias on the FB traces.
2	VCC	**Internal 5V LDO output.** The internal circuit integrates an LDO output capacitor, so there is no need to add an external capacitor.
3	AGND	**Analog ground.** Reference ground of the logic circuit. It needs to be connected to PGND on PCB layout.
4, 5, 6	SW	**Switch Output.** There is no needed connection for the SW pins, but a large copper plane is recommended on pins 4, 5, and 6 for improved heat sink.
7, 8, 9	OUT	**Power output.** Connect the load to OUT. An output capacitor is needed.
10, 15, 19, 20	NC	**DO NOT CONNECT**. NC must be left floating.
11	BST	**Bootstrap.** The bootstrap capacitor is integrated internally. There is no need for external connections.
12, 13, 14	PGND	**Power ground.** Reference ground of the power device. PCB layout requires extra care (see Page 15). For best results, connect to PGND with copper and vias.
16	IN	**Supply voltage.** IN supplies power for the internal MOSFET and regulator. The MPM3630 operates from a +4.5V to +18V input rail. It requires a low ESR and low-inductance capacitor to decouple the input rail. Place the input capacitor very close to IN and connect it with wide PCB traces and multiple vias.
17	EN/SYNC	**Enable/Sync.** EN = high to enable the module. Floating EN or connecting it to ground will disable the converter. Apply an external clock to EN to change the switching frequency.
18	PG	**Power good indicator.** Open drain structure.

FUNCTIONAL BLOCK DIAGRAM

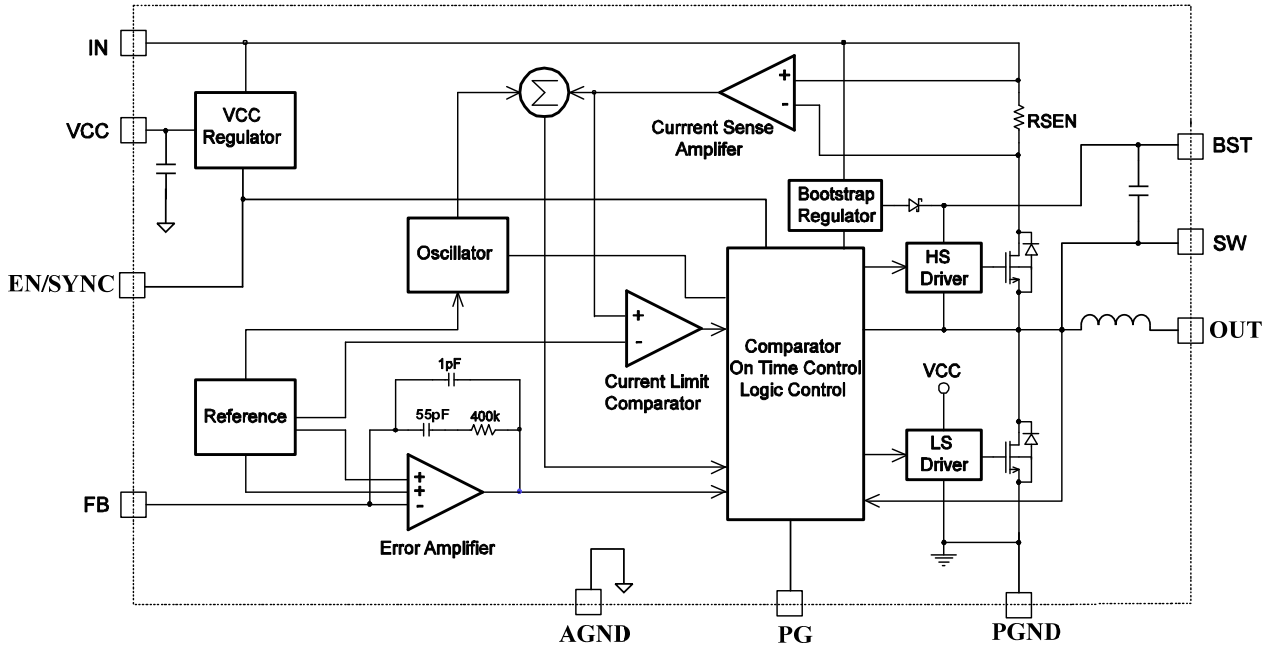


Figure 1: Functional Block Diagram

OPERATION

The MPM3630 is a high frequency, synchronous, rectified, step-down, switch-mode converter with built-in power MOSFETs, integrated inductor, and two capacitors. It offers a very compact solution that achieves a 3A continuous output current with excellent load and line regulation over a 4.5V to 18V input supply range.

The MPM3630 has three working modes: advanced asynchronous modulation (AAM), similar to PFM mode, discontinuous conduction mode (DCM), and continuous conduction mode (CCM). The load current increases as the device transitions from AAM mode to DCM to CCM.

AAM Operation

In a light-load condition, the MPM3630 operates in AAM mode (see Figure 2). V_{COMP} is the error-amplifier output, which represents the peak inductor current information. When V_{COMP} is lower than V_{AAM}, the internal clock is blocked. This causes the MPM3630 to skip pulses, achieving the light-load power save. Refer to AN032 for additional details.

The internal clock re-sets every time V_{COMP} exceeds V_{AAM}. Simultaneously, the high-side MOSFET (HS-FET) turns on and remains on until $V_{ILsense}$ reaches the value set by V_{COMP}.

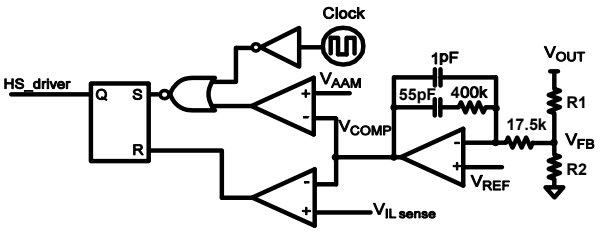


Figure 2: Simplified AAM Control Logic

DCM Control Operation

The V_{COMP} ramps up as the output current increases. When its minimum value exceeds V_{AAM}, the device enters DCM. In this mode the internal 1.4MHz clock initiates the PWM cycle, the HS-FET turns on and remains on until $V_{ILsense}$ reaches the value set by V_{COMP} (after a period of dead time), and then the low-side MOSFET (LS-FET) turns on and remains on until the inductor-current value decreases to zero. The device repeats the same operation in every clock cycle to regulate the output voltage (see Figure 3).

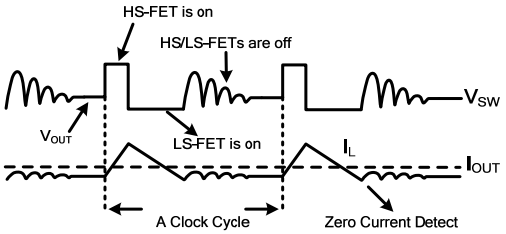


Figure 3: DCM Control Operation

CCM Control Operation

The device enters CCM from DCM once the inductor current no longer drops to zero in a clock cycle. In CCM, the internal 1.4MHz clock initiates the PWM cycle, the HS-FET turns on and remains on until $V_{ILsense}$ reaches the value set by V_{COMP} (after a period of dead time), and then the LS-FET turns on and remains on until the next clock cycle starts. The device repeats the same operation in every clock cycle to regulate the output voltage.

If $V_{ILsense}$ does not reach the value set by V_{COMP} within 90% of one PWM period, the HS-FET will be forced off.

Internal V_{CC} Regulator

A 5V internal regulator powers most of the internal circuitries. This regulator takes V_{IN} and operates in the full V_{IN} range. After EN pulls high, when V_{IN} exceeds 5V, the output of the regulator is in full regulation. When V_{IN} is less than 5V, the output decreases, and the part integrates an internal decoupling capacitor. There is no need to add an external VCC output capacitor.

Error Amplifier (EA)

The error amplifier compares the FB pin voltage to the internal 0.6V reference (V_{REF}) and outputs a current proportional to the difference between the two. This output current then charges or discharges the internal

compensation network to form the COMP voltage, which controls the power MOSFETcurrent. The optimized internal compensation network minimizes the external component counts and simplifies the control loop design.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The MPM3630 UVLO comparator monitors the output voltage of the internal regulator (VCC). The UVLO rising threshold is about 4.1V while its falling threshold is 3.36V.

ENABLE/SYNC Control (EN)

EN turns the converter on and off. Drive EN high to turn on the converter; drive EN low to turn off the converter. An internal 1.1MΩ resistor from EN to GND allows EN to be floated to shut down the chip.

EN is clamped internally using a 5.6V series-Zener-diode (see Figure 4).

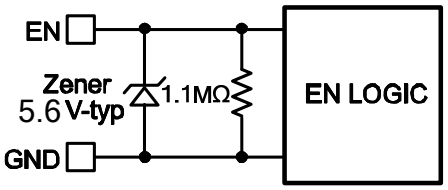


Figure 4: 5.6V Zener Diode Connection

Connecting EN to a voltage source directly without a pull-up resistor requires limiting the amplitude of the voltage source to ≤ 5V to prevent damage to the Zener diode.

Connecting the EN input through a pull-up resistor to the voltage on VIN limits the EN input current to less than 100μA.

For example, with 12V connected to V_{IN}, $R_{PULLUP} \geq (12V – 5.6V) \div 100\mu A = 64k\Omega$.

For external clock synchronization, connect a clock with a frequency range between 1MHz and 2MHz. 2.2ms after the output voltage is set, the internal clock rising edge will synchronize with the external clock rising edge. Meanwhile the width of the high level should be longer than 250ns, and the width of the low level should be longer than 100ns.

Internal Soft Start (SS)

The soft start prevents the converter output voltage from overshooting during startup. When the chip starts, the internal circuitry generates a soft-start voltage (SS) that ramps up from 0V to 5V. When SS is lower than REF, the error amplifier uses SS as the reference. When SS is higher than REF, the error amplifier uses REF as the reference. The SS time is set to 2.2ms internally.

Power Good Indicator (PG)

The MPM3630 has power good (PG) output to indicate whether the output voltage of the module is ready. PG is an open-drain output. Connect PG to VCC (or another voltage source) through a pull-up resistor (e.g. 10 kΩ). When the input voltage is applied, PG is pulled down to GND before the internal V_{SS} > 1V. Once V_{SS} > 1V (when V_{FB} is above 92% of V_{REF}), PG is pulled high (after a 110 μs delay). During normal operation, PG is pulled low when the V_{FB} drops below 81% of V_{REF} (after a 26μs delay).

Since the MPM3630 doesn't implement dedicated output over-voltage protection, PG will not respond to an output over-voltage condition.

Over-Current Protection (OCP) and Hiccup

The MPM3630 has a cycle-by-cycle over-current limiting control. When the inductor current peak value exceeds the internal peak current limit threshold, the HS-FET turns off and the LS-FET turns on, remaining on until the inductor current falls below the internal valley current limit threshold. The valley current limit circuit is employed to decrease the operation frequency (after the peak current limit threshold is triggered). Meanwhile, the output voltage drops until V_{FB} is below the under-voltage (UV) threshold (240mV, typically). Once UV is triggered, the MPM3630 enters hiccup mode to re-start the part periodically. This protection mode is useful when the output is dead-shorted to ground and greatly reduces the average short-circuit current to alleviate thermal issues and protect the converter. The MPM3630 exits hiccup mode once the over-current condition is removed.

Thermal Shutdown (TSD)

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die reaches temperatures that exceed 150°C, it shuts down the whole chip. When the temperature drops below its lower threshold, typically 130°C, the chip is enabled again.

Floating Driver and Bootstrap Charging

An internal bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection. This UVLO's rising threshold is 2.2V with a hysteresis of 150mV. The bootstrap capacitor voltage is regulated internally by V_{IN} through D1, M1, C4, L1, and C2 (see Figure 5). If (V_{IN}-V_{SW}) exceeds 5V, U1 will regulate M1 to maintain a 5V BST voltage across C4.

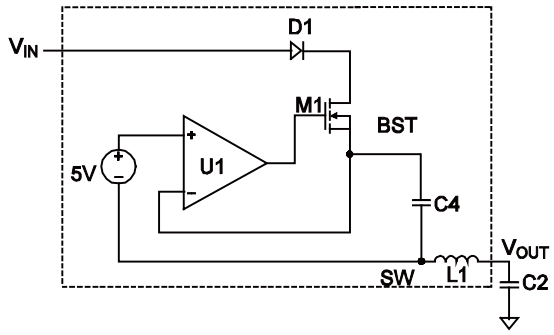


Figure 5: Internal Bootstrap Charging Circuit

Startup and Shutdown

If both V_{IN} and V_{EN} exceed their respective thresholds, the chip starts up. The reference block starts first, generating stable reference voltage, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

Three events shut down the chip: V_{IN} low, V_{EN} low, and thermal shutdown. During the shutdown procedure, the signaling path is blocked first to avoid any fault triggering. The COMP voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

Additional RC Snubber Circuit

An additional RC snubber circuit can be chosen to clamp the voltage spike and damp the ringing voltage for better EMI performance.

The power dissipation of the RC snubber circuit is estimated using Equation (1):

$$P_{Loss} = f_S \times C_S \times V_{IN}^2 \quad (1)$$

Where f_S is the switching frequency, C_s is the snubber capacitor, and V_{IN} is the input voltage.

For improved efficiency, the value of C_S should not be set too high. Generally, a 4.99Ω R_S and a 470pF C_S are recommended to generate the RC snubber circuit (see Figure 6).

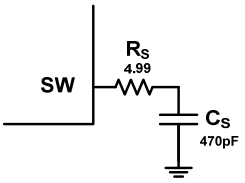


Figure 6: Additional RC Snubber Circuit

APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider sets the output voltage (see Typical Application on page 1). The feedback resistor R1 also sets the feedback loop bandwidth with the internal compensation capacitor (see Figure 7). R2 is then given using Equation (2):

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.6V} - 1} \quad (2)$$

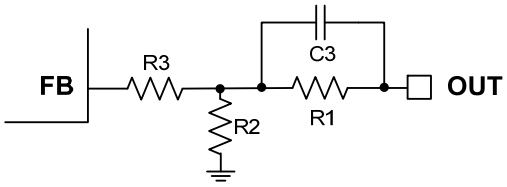


Figure 7: Feedback Network

Table 1 lists the recommended resistor values for common output voltages.

Table 1: Resistor Selection for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	R3 (kΩ)	C3 (pF)	C_{OUT} (µF)
1.0	51	76.8	51	22	3x22
1.2	51	51	51		3x22
1.5	51	34	51		3x22
1.8	51	25.5	0		2x22
2.5	51	16	0		2x22
3.3	51	11.3	0		2x22
5	51	6.98	0		2x22

Normally, it is recommended to set the output voltage from 0.6V to 5.5V. However, it can be set higher than 5.5V. In this case, the output-voltage ripple is larger due to a larger inductor ripple current. An additional output capacitor is needed to reduce the output ripple voltage.

If the output voltage is high, heat dissipation becomes more important. Please refer to the "PCB Layout Guidelines" section to achieve better thermal performance. Also, the output will downgrade when the output voltage is higher than 5.5V due to thermal concerns.

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous, therefore it requires a capacitor to supply the AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Use ceramic capacitors with X5R or X7R dielectrics for best results because of their low ESR and small temperature coefficients. For most applications, use a 22µF capacitor.

Since the capacitor absorbs the input switching current, it requires an adequate ripple current rating. The

RMS current in the input capacitor can be estimated using Equation (3) and Equation (4):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (3)$$

The worst case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (4)$$

To simplifiy, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g. 0.1µF) placed as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple caused by capacitance can be estimated with Equation (5):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (5)$$

Selecting the Output Capacitor

The output capacitor (C2) maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated using Equation (6):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right) \quad (6)$$

Where L_1 is the inductor value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor, and L_1=1μH.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency, and the capacitance causes the majority of the output voltage ripple. For simplification, the output voltage ripple can be estimated using Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (7)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. To simlpify, the output ripple can be approximated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (8)$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MPM3630 can be optimized for a wide range of capacitance and ESR values.

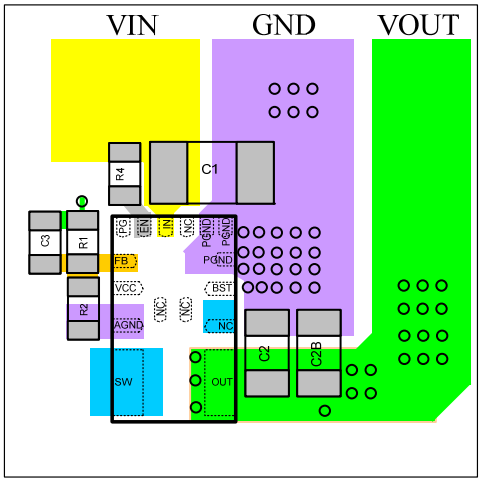
PCB Layout [9]

Efficient PCB layout is critical to achieve stable operation, especially for input capacitor placement. For best results, see Figure 8 and follow the guidelines below:

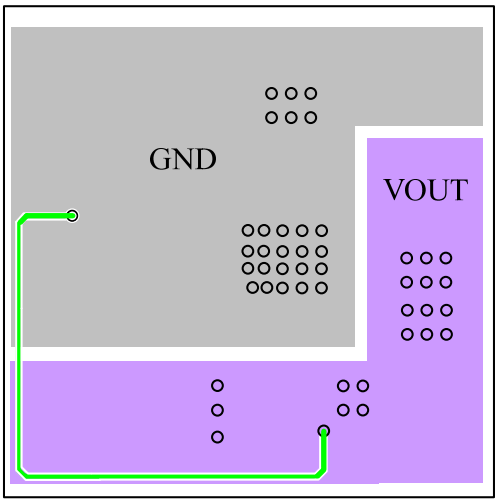
1. Place the high current paths GND and IN very close to the device with short, direct, and wide traces.
2. Use a large ground plane to connect directly to PGND. Add vias near PGND if the bottom layer is ground plane.
3. Place the ceramic input capacitor close to IN and the PGND pins. Keep the connection of the input capacitor and IN as short and wide as possible.
4. Place the external feedback resistors next to FB.
5. Keep the feedback network away from the switching node.

Notes:

9) The recommended layout is based on the Figure 14 Typical Application circuit.



Top Layer



Bottom Layer

Figure 8: Recommended PCB Layout

Design Example

Below is a design example following the application guidelines for the specifications below:

Table 2: Design Example

V_{IN}	12V
V_{OUT}	3.3V
Io	3A

The detailed application schematic is shown in Figure 14. The typical performance and circuit waveforms have been shown in the Typical Performance Characteristics section. For more device applications, please refer to the related Evaluation Board Datasheets.

TYPICAL APPLICATION CIRCUITS

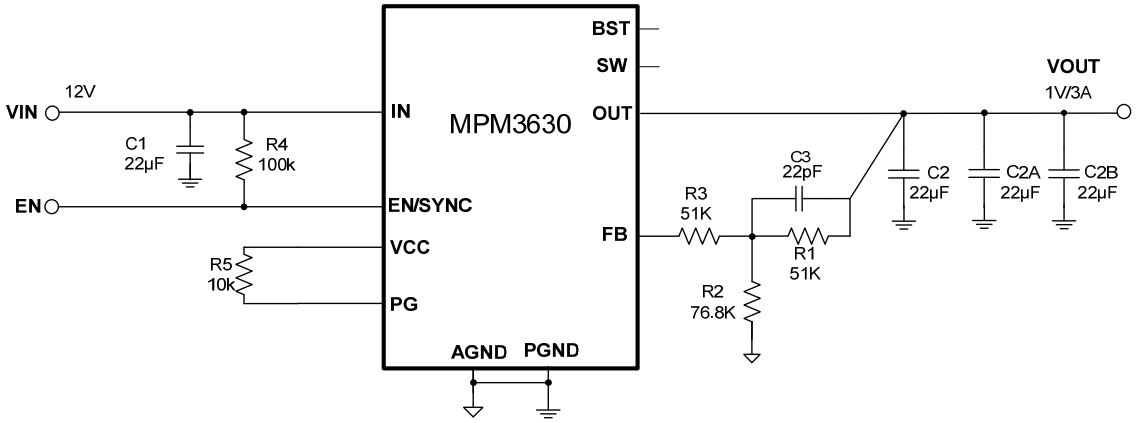


Figure 9: Vo = 1V, Io = 3A

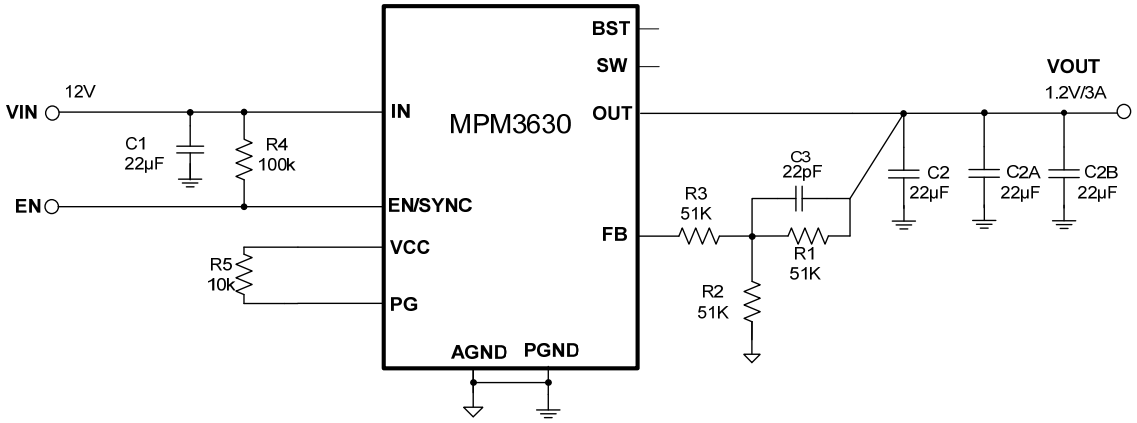


Figure 10: Vo = 1.2V, Io = 3A

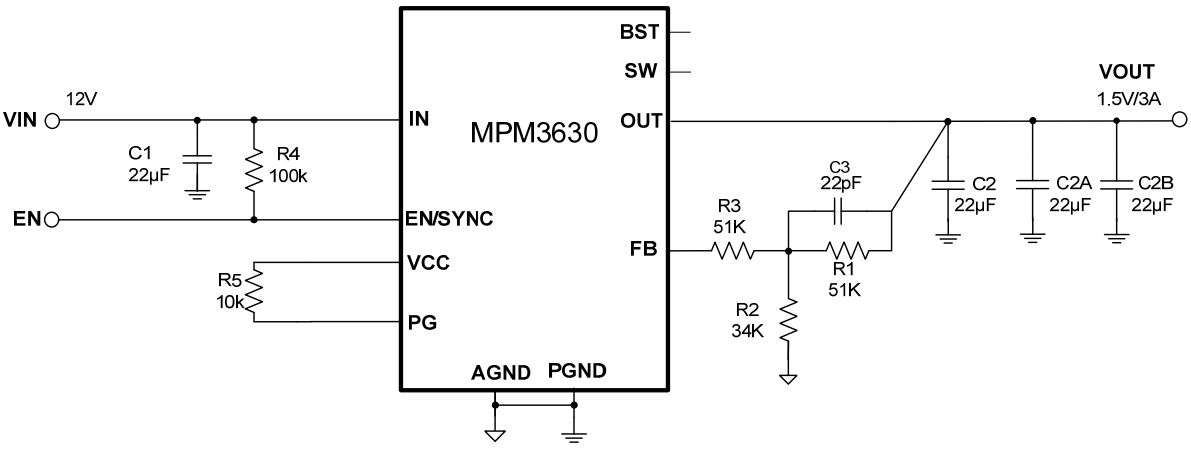


Figure 11: Vo = 1.5V, Io = 3A

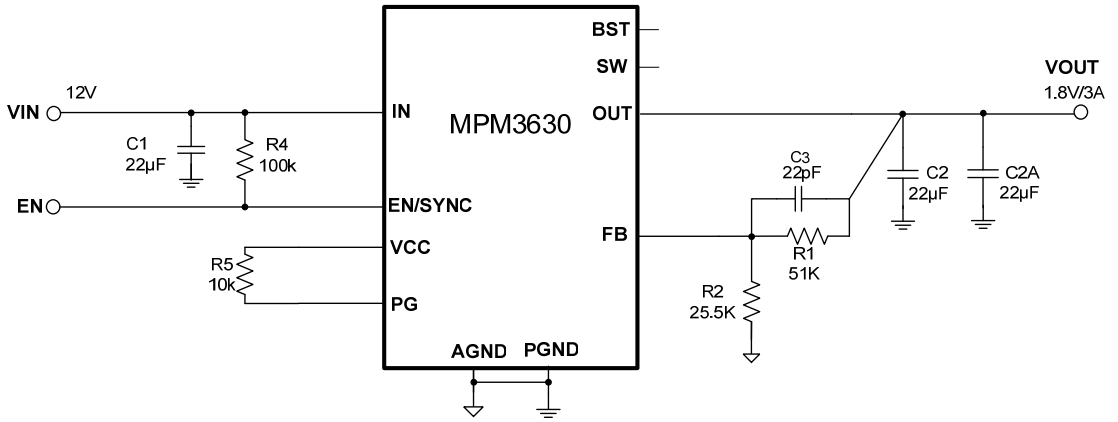


Figure 12: Vo = 1.8V, Io = 3A

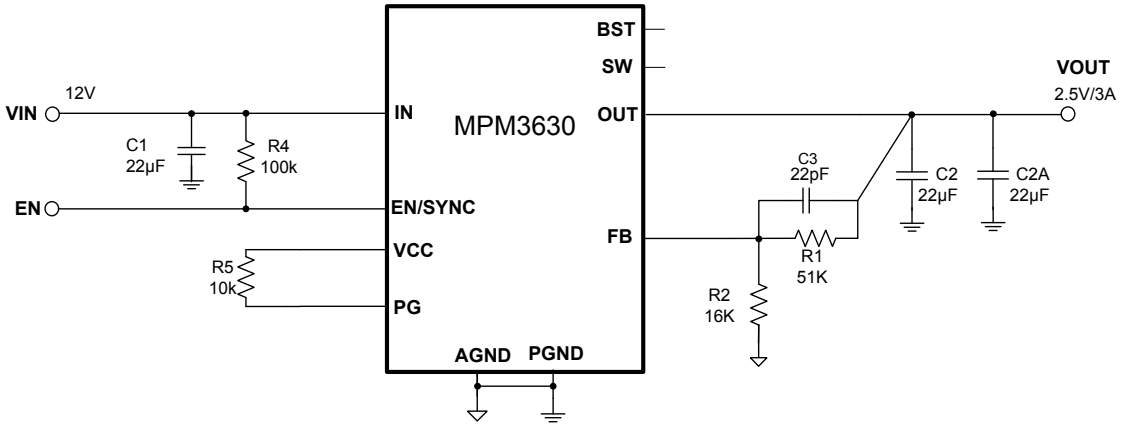


Figure 13: Vo = 2.5V, Io = 3A

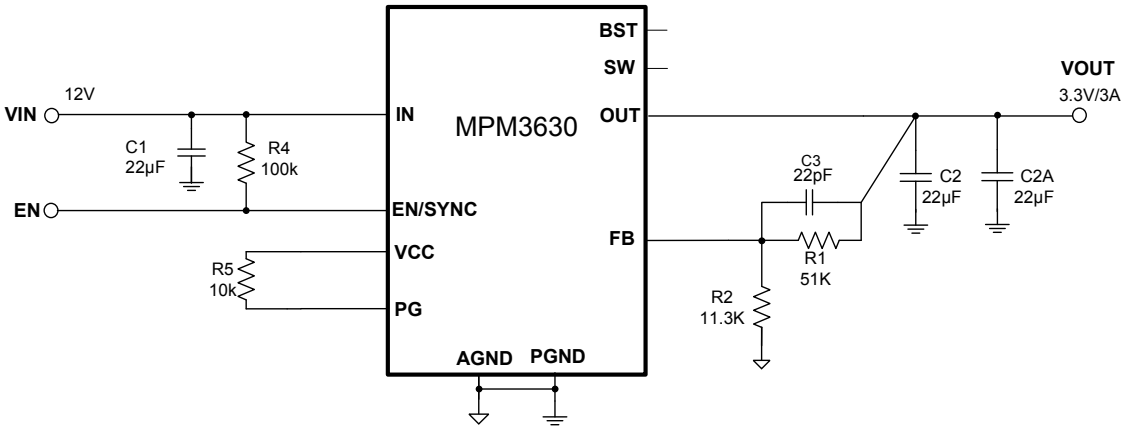


Figure 14: Vo = 3.3V, Io = 3A

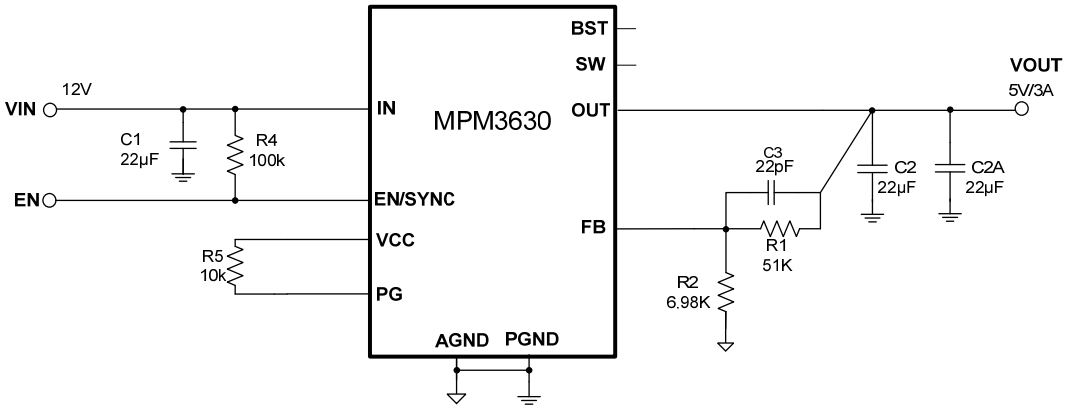
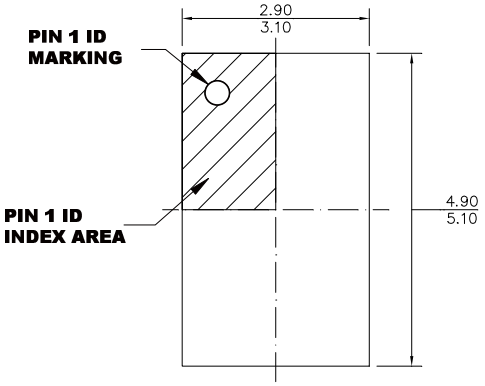


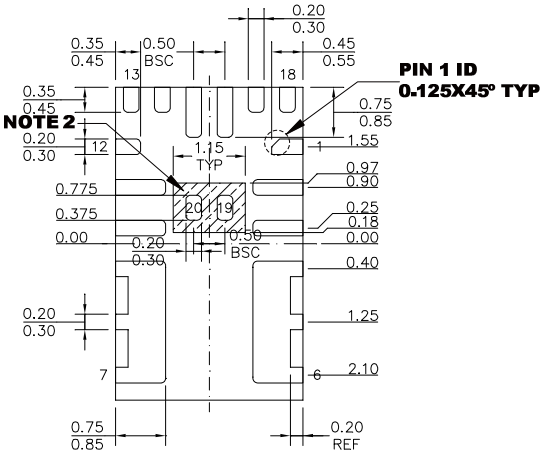
Figure 15: Vo = 5, Io = 3A

PACKAGE INFORMATION

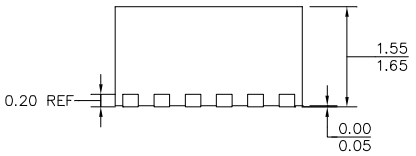
QFN-20 (3mmx5mmx1.6mm)



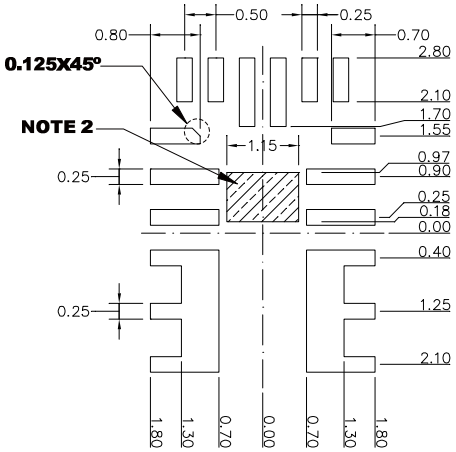
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) SHADED AREA IS THE KEEP-OUT ZONE. ANY PCB METAL TRACE AND VIA ARE NOT ALLOWED TO CONNECT TO THIS AREA ELECTRICALLY OR MECHANICALLY.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

Revision History

Revision #	Revision date	Description	Pages Updated
R1.02	5/26/2020	**Analog ground.** Reference ground of the logic circuit. AGND is connected internally to PGND. There is no need to add external connections to PGND. we need to correct it to: Analog ground. Reference ground of the logic circuit. It needs to be connected to PGND on PCB layout.	Page 9