MP3314

6-Channel, 60mA, 50V, Boost White LED Driver with I²C Interface

DESCRIPTION

The MP3314 is a 6-channel white LED (WLED) driver that operates from a 3V to 30V input voltage (VIN) range. The MP3314 applies six internal current sources in each LED string terminal. The maximum current for each channel is 60mA. The MP3314 is designed to drive WLED arrays for LCD panels in tablets and notebook backlighting applications.

Peak current mode control and pulse-width modulation (PWM) control are employed to regulate the boost converter's output voltage (V_{OUT}).

The MP3314 integrates an I^2C digital interface that can configure the device parameters, such as the operation mode, switching frequency (f_{SW}), dimming mode, dimming duty, phase shift, frequency spread spectrum (FSS), and various protection thresholds.

The device supports a configurable switching slew rate and FSS function to reduce EMI.

The MP3314 achieves high efficiency with a low headroom voltage for LED regulation and a low MOSFET on resistance.

Full protection features include LED open protection, LED short protection, over-current protection (OCP), over-voltage protection (OVP), and over-temperature protection.

The MP3314 is available in QFN-24 (4mmx4mm) and CSP-20 (2.4mmx1.74mm) packages.

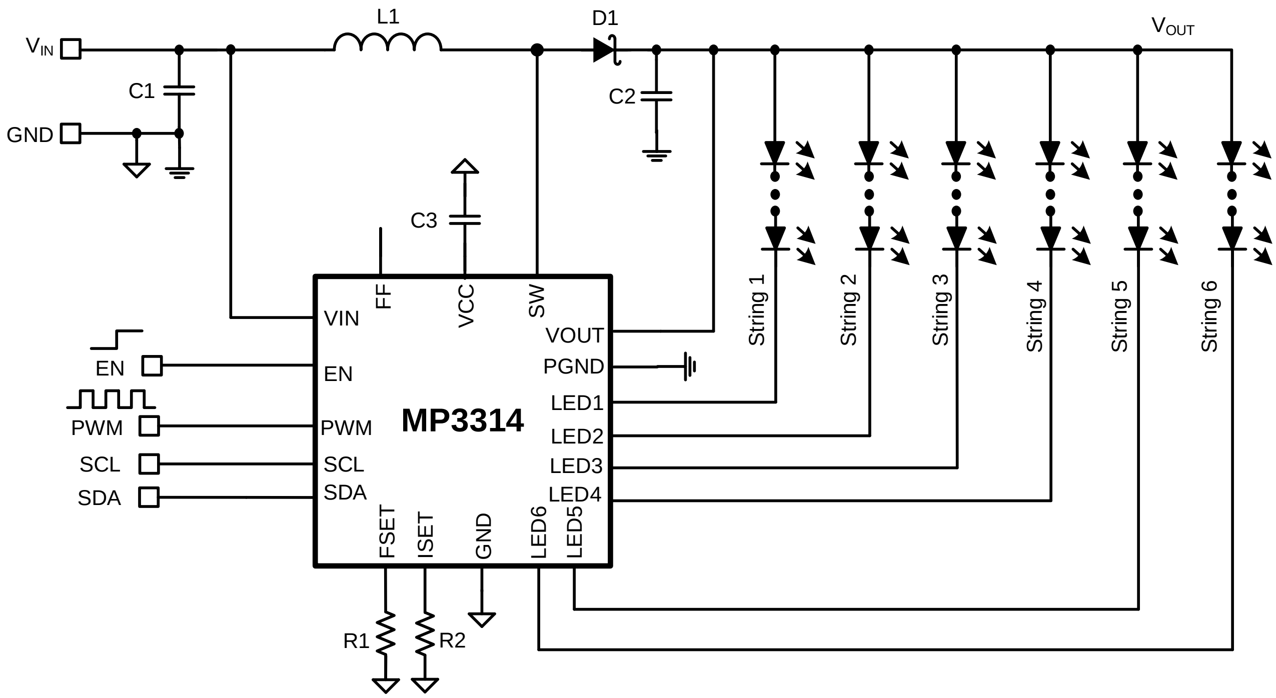
FEATURES

- 3V to 30V Input Voltage (V_{IN}) Range
- 6 Channels, Max 60mA/Ch
- 50V, 150mΩ On Resistance, Integrated Low-Side MOSFET (LS-FET)
- Up to 43V Output Voltage (V_{OUT})
- 187.5mV LED Regulation Voltage at 20mA
- 2% LED Current (I_{LED}) Accuracy at 20mA
  - 1.5% I_{LED} Matching at 20mA (QFN-24)
  - 3% I_{LED} Matching at 20mA (CSP-20)
- Selectable 312kHz, 625kHz, or 1250kHz Switching Frequency (f_{SW})
- Auto-Selected f_{SW} for High Efficiency
- I^2C and External Pulse-Width Modulation (PWM) Brightness Control
- Analog, PWM, and Mix Dimming
- Phase Shift Function to Reduce Noise
- Configurable Switching Slew Rate and Frequency Spread Spectrum (FSS) Function to Reduce EMI
- One-Time Programmable (OTP) Memory to Configure Default Register Values
- LED Open Protection and LED Short Protection
- Over-Temperature Protection
- Over-Current Protection (OCP), Inductor Short Protection, and Diode Short Protection
- Available in QFN-24 (4mmx4mm) and CSP-20 (2.4mmx1.74mm) Packages

APPLICATIONS

- Tablets
- Notebooks
- Small-Size LCD Displays

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number	Package	Top Marking	MSL Rating
MP3314GR*	QFN-24 (4mmx4mm)	*See Below*	1
MP3314GC**	CSP-20 (2.4mmx1.74mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MP3314GR-Z).

** For Tape & Reel, add suffix -Z (e.g. MP3314GC-Z).

TOP MARKING (MP3314GC)

LFY
LLL

LF: Product code
Y: Year code
LLL: Lot number

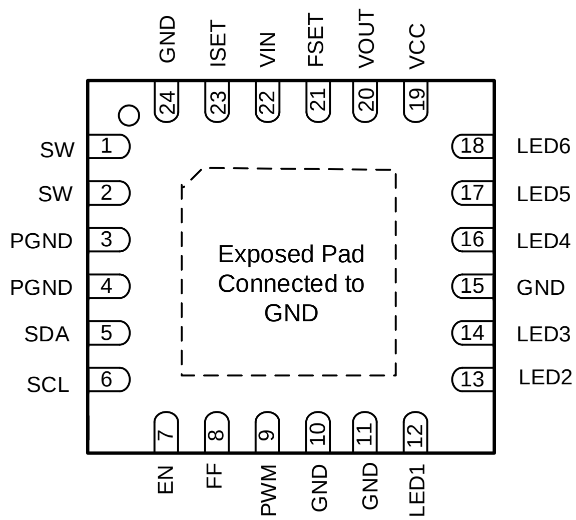
TOP MARKING (MP3314GR)

MPSYWW
MP3314
LLLLLL

MPS: MPS prefix
Y: Year code
WW: Week code
MP3314: Part number
LLLLLL: Lot number

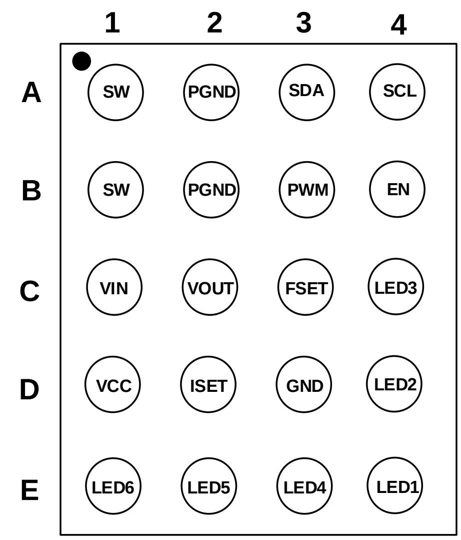
PACKAGE REFERENCE

TOP VIEW



QFN-24 (4mmx4mm)

TOP VIEW



CSP-20 (2.4mmx1.74mm)

PIN FUNCTIONS

Pin #		Name	Description
QFN-24	CSP-20		
1, 2	A1, B1	SW	**Internal low-side MOSFET (LS-FET) drain.**
3, 4	A2, B2	PGND	**Power ground.**
5	A3	SDA	**I²C interface data input/output.**
6	A4	SCL	**I²C interface clock input.**
7	B4	EN	**Enable.** Pull the EN pin high to turn the IC on; pull EN low turn the IC off. Place an RC filter near EN.
8	-	FF	**Fault flag.** The FF pin is the open drain of internal MOSFET. If a fault occurs, FF is pulled to GND.
9	B3	PWM	**External PWM signal input.** Apply a pulse-width modulation (PWM) signal to the PWM pin to control the brightness. If only using I²C dimming, connect the PWM and GND pins.
10, 11, 15, 24	D3	GND	**IC ground.**
12	E4	LED1	**LED channel 1 current input.** Connect the LED string 1 cathode to this pin.
13	D4	LED2	**LED channel 2 current input.** Connect the LED string 2 cathode to this pin.
14	C4	LED3	**LED channel 3 current input.** Connect the LED string 3 cathode to this pin.
16	E3	LED4	**LED channel 4 current input.** Connect the LED string 4 cathode to this pin.
17	E2	LED5	**LED channel 5 current input.** Connect the LED string 5 cathode to this pin.
18	E1	LED6	**LED channel 6 current input.** Connect the LED string 6 cathode to this pin.
19	D1	VCC	**5V LDO output.** The VCC pin supplies power to the internal logic and gate driver. Place a ceramic capacitor as close to VCC as possible to reduce noise.
20	C2	VOUT	**Output voltage detection.** Connect the power diode cathode to the VOUT pin.
21	C3	FSET	**Switching frequency and PWM dimming frequency setting.** Connect a resistor between the FSET and GND pins to set the switching frequency (f_{SW}) and PWM dimming frequency (f_{PWM}).
22	C1	VIN	**Power supply input.** Place a bypass capacitor near the VIN pin.
23	D2	ISET	**LED current setting.** Connect a current-setting resistor between the ISET and GND pins to configure the LED current (I_{LEDx}) for each channel.
Exposed pad	-	EP	**Exposed pad.** Connect the exposed pad to GND.

ABSOLUTE MAXIMUM RATINGS (1)

V_{SW}, V_{LEDx}, V_{OUT} ....-0.3V to +50V
V_{IN} ....-0.3V to +32V
All other pins ....-0.3V to +5.3V
Junction temperature ....150°C
Lead temperature ....260°C
Storage temperature .... -65°C to 150°C
Continuous power dissipation (T_A = 25°C) (2)
QFN-24 (4mmx4mm).............................. 2.97W
CSP-20 (2.4mmx1.74mm)......................... 2.5W

ESD Ratings

Human body model (HBM) .... ±2kV
Charged device model (CDM) ... +1.5kV/-1.25kV

Recommended Operating Conditions (3)

Input voltage (V_{IN}) ....3V to 30V
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}	
QFN-24 (4mmx4mm)	42	9	°C/W
CSP-20 (2.4mmx1.74mm)	50	0.5	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the device to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on a JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 7.6V, V_{EN} = 2V, T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Supply						
Operating input voltage	V_{IN}		3		30	V
Supply current	$I_{STANDBY}$	LDO is enabled, boost is disabled, T_J = -30°C to 85°C		1.6	1.8	mA
	I_{NORMAL}	LDO is enabled, boost is enabled, no load		3.5	3.9	mA
Shutdown supply current	I_{SD}	V_{EN} = 0V, V_{IN} = 12V			1	µA
V_{IN} under-voltage lockout (UVLO) rising low threshold	$V_{IN\_UVLO\_RISING\_LO}$	UVLOH = 0b		2.5		V
V_{IN} UVLO rising high threshold	$V_{IN\_UVLO\_RISING\_HI}$	UVLOH = 1b		5.2		V
V_{IN} UVLO low hysteresis		UVLOH = 0b		125		mV
V_{IN} UVLO high hysteresis		UVLOH = 1b		250		mV
LDO output voltage	V_{CC}	V_{EN} = 2V, 6V < V_{IN} < 30V, 0mA < I_{VCC} < 10mA	4.5	5	5.5	V
EN on threshold	V_{EN_ON}	V_{EN} rising	1.2			V
EN off threshold	V_{EN_OFF}	V_{EN} falling			0.4	V
EN pull-down resistance	R_{EN}			1000		kΩ
Boost Converter						
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)\_LS}$	V_{IN} = 6V		150		mΩ
SW leakage current	I_{SW_LKG}	V_{SW} = 50V			1	µA
Switching frequency	f_{SW}	FSW[1:0] = 10b	1200	1250	1300	kHz
Maximum duty cycle	D_{MAX}	FSW[1:0] = 10b	89			%
		FSW[1:0] = 01b	90			%
Cycle-by-cycle current limit (I_{LIMIT})	I_{LIMIT_SW}	ILIM[2:0] = 000b	0.7	0.9	1.1	A
		ILIM[2:0] = 101b		2.4		A
Latch-off I_{LIMIT}	$I_{LIMIT\_LATCH\text{-}OFF}$	ILIM[2:0] = 101b		5.6		A
Minimum turn on time	t_{ON_MIN}			70		ns
Dimming						
PWM input high threshold	V_{PWM_HI}	V_{PWM} rising	1.2			V
PWM input low threshold	V_{PWM_LO}	V_{PWM} falling			0.4	V
PWM pull-down resistor	R_{PWM}			1000		kΩ
PWM input frequency range	f_{PWM_IN}		75		25000	Hz
Minimum on time	t_{MIN_ON}			1		µs
Minimum off time	t_{MIN_OFF}			1		µs
PWM input low time for standby	$t_{STANDBY}$			55	70	ms
PWM input resolution (5)		f_{PWM_IN} < 9kHz		10		bits
Mix dimming transfer point		DIMT[1:0] = 10b		25		%
PWM dimming frequency	f_{PWM}	FPWM[3:0] = 1100b, configured via the I²C		24.04		kHz

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 7.6V, V_{EN} = 2V, T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
LED Current (I_{LEDx}) Regulation						
Current matching (6)		V_{LEDx} = 187.5mV, I_{LED} = 20mA, CSP-20 package			3	%
		V_{LEDx} = 187.5mV, I_{LED} = 20mA, QFN-24 package			1.5	%
Full-scale current		R_{ISET} = 60kΩ, ILED[11:0] = FFFh, IMAX[2:0] = 111b	49	50.5	52	mA
		R_{ISET} = 60kΩ, ILED[11:0] = FFFh, IMAX[2:0] = 011b	19.6	20	20.4	mA
Maximum LEDx current	I_{LEDx_MAX}	R_{ISET} = 50kΩ		60		mA
LEDx leakage current	I_{LEDx_LKG}	V_{OUT} = 50V			1	µA
Protections						
Over-voltage protection (OVP) threshold	V_{OVP}	Rising edge, OVP[2:0] = 111b, VOHL = 1b		43		V
		Rising edge, OVP[2:0] = 010b, VOHL = 1b		21		V
OVP UVLO threshold	V_{OVP_UVLO}	Step-up converter fails		1		V
LEDx over-voltage threshold	V_{LEDx_OV}	LEDS1:0 = 01b		5		V
LEDx over-voltage fault timer				1.8		ms
LEDx UVLO threshold	V_{LEDx_UVLO}			80		mV
Thermal shutdown threshold	T_{SD}	Rising edge (5)		150		°C
		Hysteresis (5)		20		°C
FF pull-down resistance	R_{FF}	QFN-24 package		100		Ω
I²C Interface						
Logic-low input voltage	V_{IN_LOW}				0.54	V
Logic-high input voltage	V_{IN_HIGH}	QFN-24 package	1.26			V
		CSP-20 package	1.50			V
Logic-low output voltage (5)	V_{OUT_LOW}	I_{LOAD} = 3mA			0.4	V
SCL clock frequency (5)	f_{SCL}		10		1000	kHz
Bus free time (5)	t_{BUS_FREE}	Between stop and start condition	0.5			µs
Repeated start condition hold time (5)	t_{HOLD_START}	After this period, the first clock is generated	0.26			µs
Repeated start condition set-up time (5)	t_{SU_START}		0.26			µs
Stop condition set-up time (5)	t_{SU_STOP}		0.26			µs
Data hold time (5)	t_{HOLD_DATA}		0			ns
Data set-up time (5)	t_{SU_DATA}		50			ns

ELECTRICAL CHARACTERISTICS *(continued)*

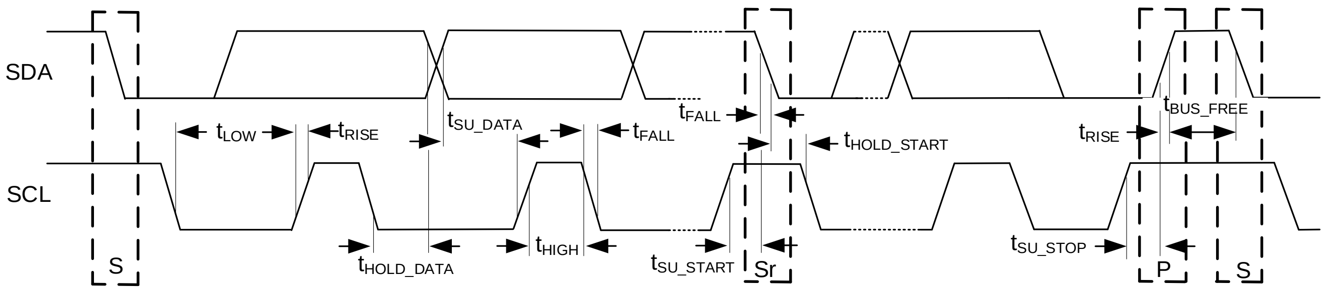
V_{IN} = 7.6V, V_{EN} = 2V, T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Clock low timeout (5)	$t_{TIMEOUT}$		25		35	ms
Clock low time (5)	t_{LOW}		0.5			μs
Clock high time (5)	t_{HIGH}		0.26		50	μs
Clock/data fall time (5)	t_{FALL}				120	ns
Clock/data rising time (5)	t_{RISE}				120	ns

Notes:

5) Not tested in production. Guaranteed by characterization.
6) Matching is defined as the difference of the maximum to minimum current divided by 2 times the average current.

I²C INTERFACE TIMING DIAGRAM



S = Start Condition
Sr = Repeated Start Condition
P = Stop Condition

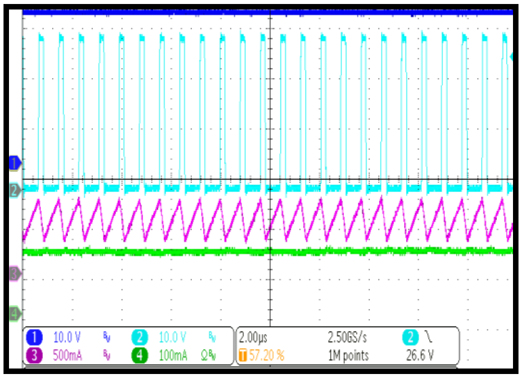
Figure 1: I²C Interface Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 7.6V, 10 LEDs in series, 6 channels, 20mA/channel, L = 10µH, T_A = 25°C, unless otherwise noted.

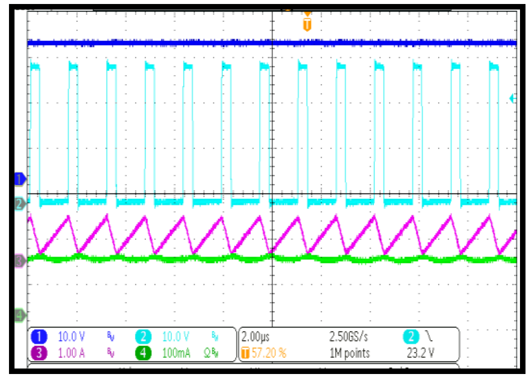
Steady State
f_{SW} = 1250kHz

CH1: V_{OUT}
CH2: V_{SW}
CH3: I_L
CH4: I_{LED}



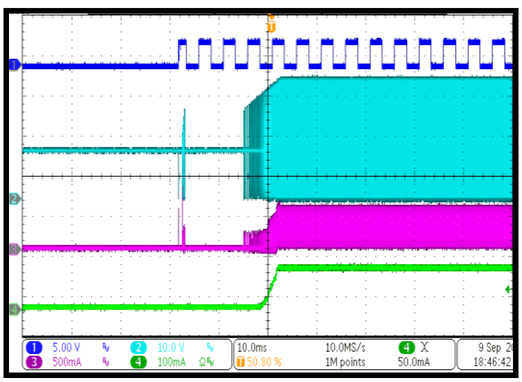
Steady State
f_{SW} = 625kHz

CH1: V_{OUT}
CH2: V_{SW}
CH3: I_L
CH4: I_{LED}



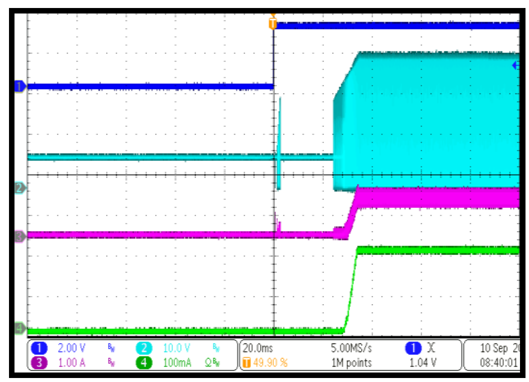
Start-Up through PWM
V_{IN} =12V, f_{PWM} = 200Hz, duty = 50%, 30mA/ch

CH1: PWM
CH2: V_{SW}
CH3: I_L
CH4: I_{LED}



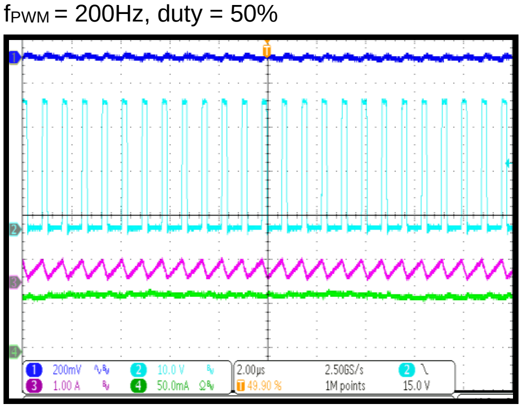
Start-Up through EN
f_{PWM} = 200Hz, duty = 100%, 30mA/ch

CH1: EN
CH2: V_{SW}
CH3: I_L
CH4: I_{LED}



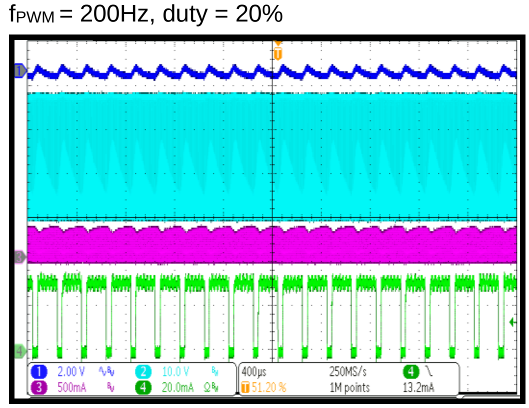
Analog Dimming
f_{PWM} = 200Hz, duty = 50%

CH1: V_{OUT}/AC
CH2: V_{SW}
CH3: I_L
CH4: I_{LED}



Mix Dimming
Transfer point (TP) = 25%, f_{ILED} = 4808Hz,
f_{PWM} = 200Hz, duty = 20%

CH1: V_{OUT}/AC
CH2: V_{SW}
CH3: I_L
CH4: I_{LED}

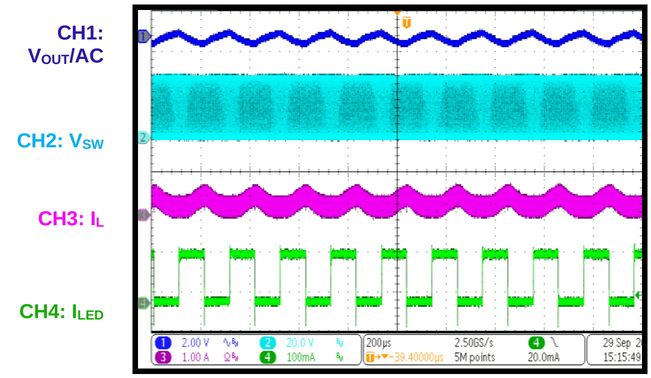


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 7.6V, 10 LEDs in series, 6 channels, 20mA/channel, L = 10µH, T_A = 25°C, unless otherwise noted.

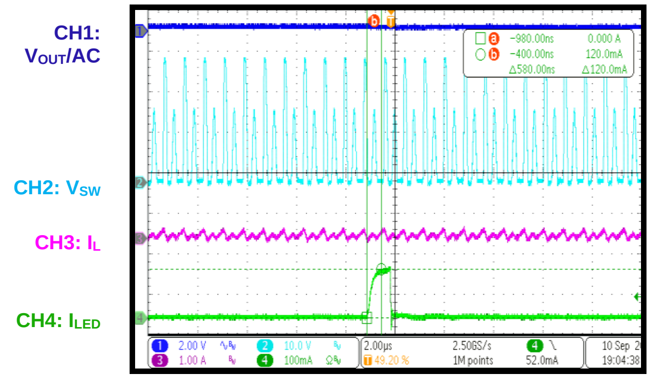
PWM Dimming

f_{ILED} = 4808Hz, f_{PWM} = 200Hz, duty = 50%



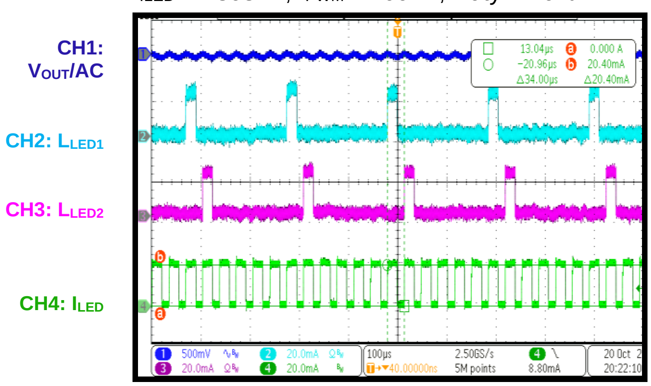
PWM Dimming

f_{ILED} = 4808Hz, f_{PWM} = 200Hz, duty = 0.5%



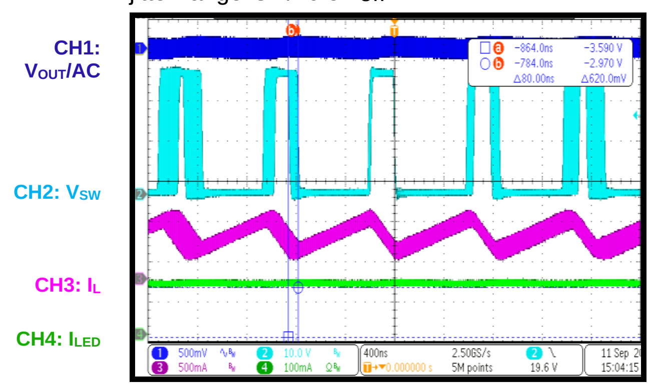
Phase-Shift Function for 6 Channels

f_{ILED} = 4808Hz, f_{PWM} = 200Hz, Duty = 10%



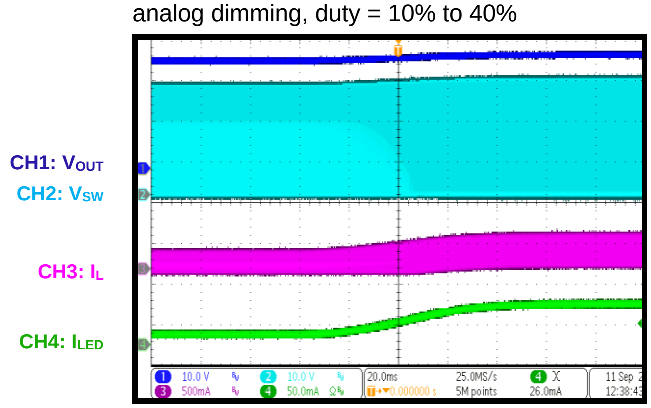
Frequency Spread Spectrum

f_{SW} = 1250kHz, f_{FSS} = 0.01 x f_{SW},
jitter range is 1/10 of f_{SW}



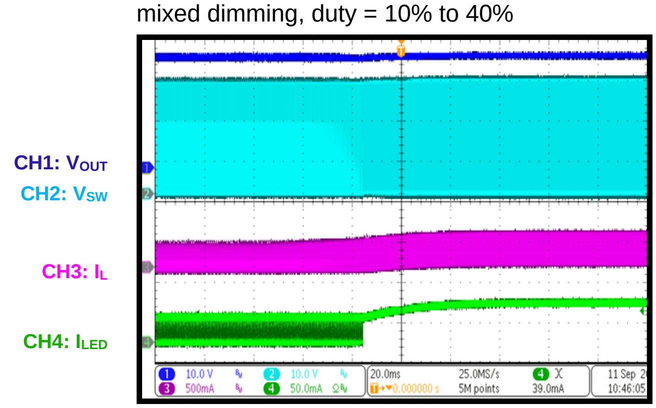
LED Current Transition and Slope

t_{TRANS} = 50ms, medium smoothing,
analog dimming, duty = 10% to 40%



LED Current Transition and Slope

t_{TRANS} = 50ms, medium smoothing,
mixed dimming, duty = 10% to 40%

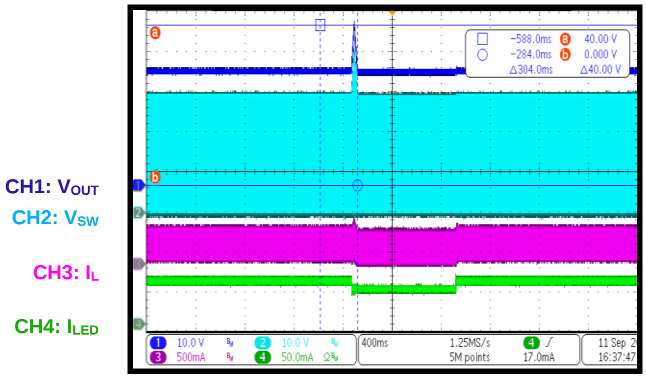


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 7.6V, 10 LEDs in series, 6 channels, 20mA/channel, L = 10µH, T_A = 25°C, unless otherwise noted.

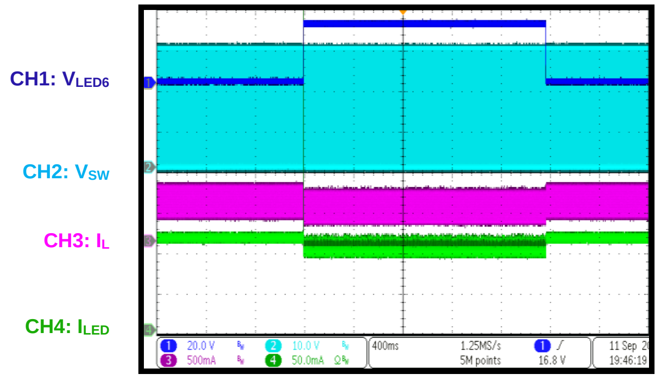
LED Open Protection

Duty = 50%, one channel is open, then recovers

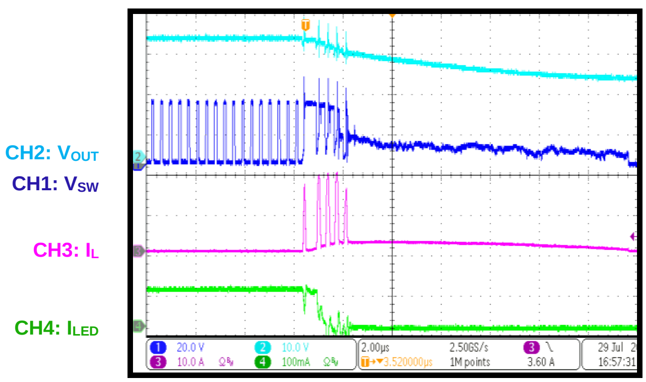


LED Short Protection

Channel 6 LED short occurs, then recovers

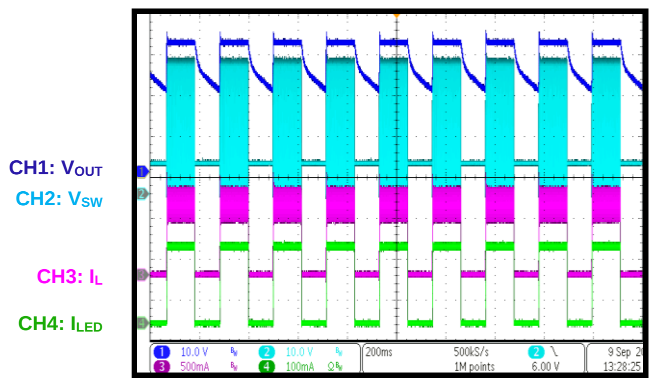


Diode Short Protection



Over-Temperature Protection

30mA/channel, device is heated



FUNCTIONAL BLOCK DIAGRAM

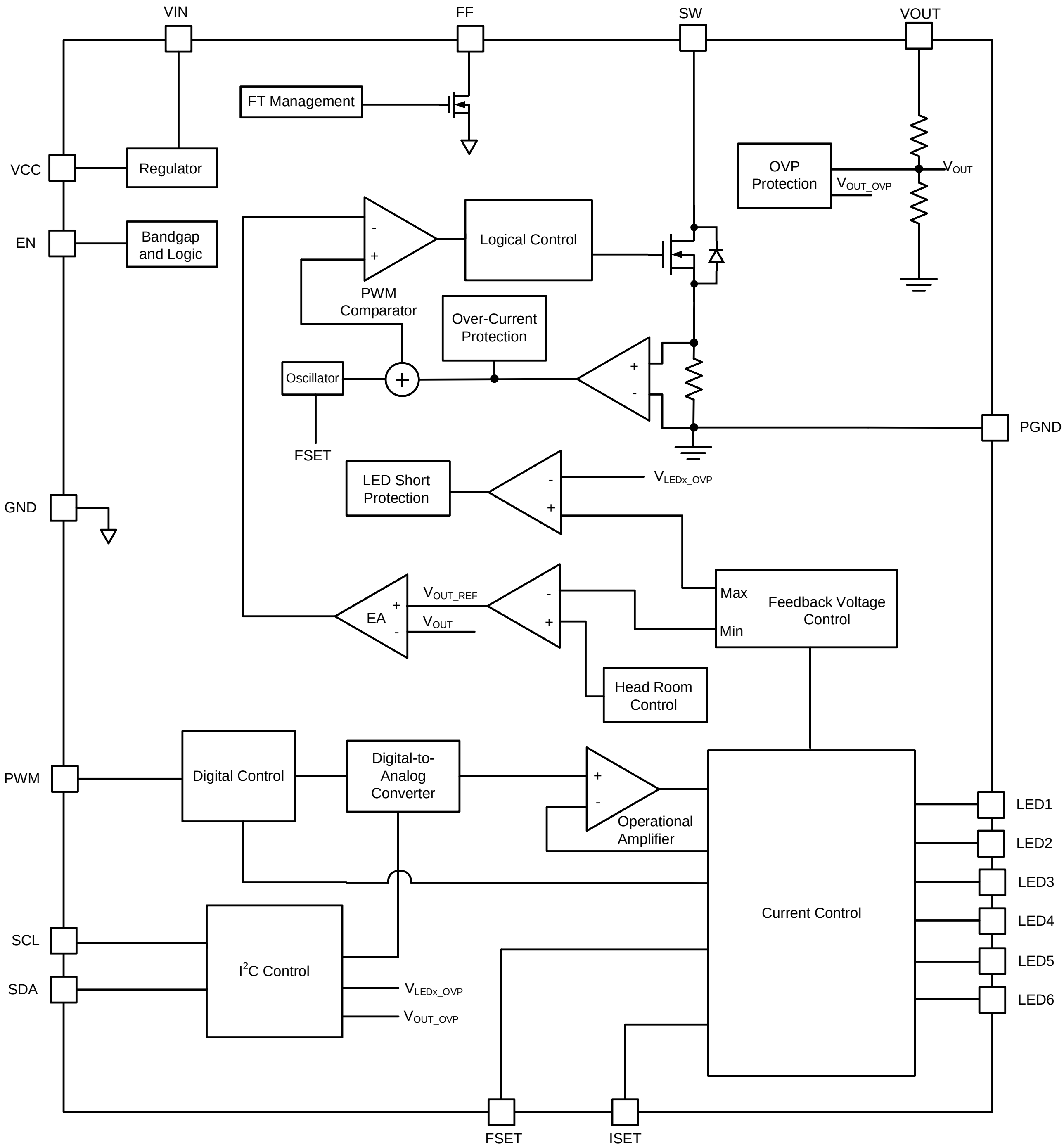


Figure 2: Functional Block Diagram

OPERATION

The MP3314 is a fixed-frequency, 6-channel white LED (WLED) driver with peak current mode control. The MP3314 applies six internal current sources in each LED string terminal. The maximum current for each channel is 60mA. The device integrates a low-side MOSFET (LS-FET) with a 50V voltage rating that supports up to 43V of output voltage (V_{OUT}).

Internal Regulator

The MP3314 integrates an internal linear regulator (VCC). If V_{IN} exceeds 6V and EN is high, the VCC regulator outputs 5V to power the internal MOSFET gate driver and internal control circuitry.

Internal Clock

To achieve a high dimming resolution, the MP3314 has a fixed 20MHz clock for its internal timer and counter.

Boost Converter Switching Frequency

The boost converter's switching frequency (f_{SW}) can be set by an external resistor connected between the FSET pin and GND If the external resistor is enabled (FSETEN1 = 1b). If the external resistor is disabled (FSETEN1 = 0b), f_{SW} can also be set by FSW[1:0] through I^2C. f_{SW} can be set to 312kHz, 625kHz, or 1250kHz.

System Start-Up

When enabled, the MP3314 checks whether the circuit is connected properly and that no short or open circuits are present. The IC monitors V_{OUT} to determine whether an output short to GND has occurred. If V_{OUT} is below 1V, the device is disabled. Then the MP3314 continues to check for other faults, such as an LED open and over-voltage (OV) fault. If the device passes all of the protection tests, the IC initiates an internal soft start (SS) to start-up the boost converter.

The MP3314 starts up regardless of the order in which VIN, PWM, and EN start up. Figure 3 shows the recommended start-up sequence for a quick start-up.

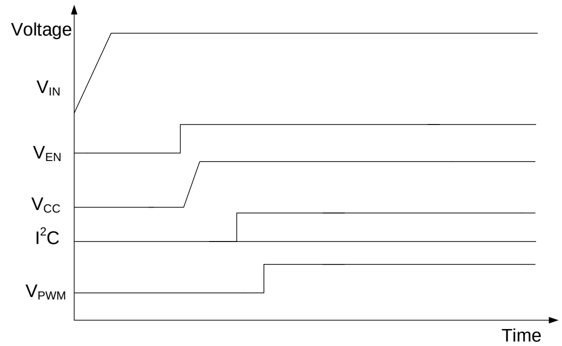


Figure 3: Recommended Start-Up Sequence

The recommended start-up sequence is described below.

1. VIN starts up
2. EN starts up
3. Once EN starts up, the I^2C data is sent after a 2ms delay.
4. The external PWM signal is applied

When using I^2C dimming, the external PWM signal can be ignored.

If the external PWM signal is used to control the brightness and SBY_PWM = 1b, then the PWM input remains low for >70ms, the IC enters standby mode, and all of the blocks are disabled (except the I^2C).

Boost Converter

The MP3314 uses peak current mode control to regulate V_{OUT}. At the beginning of each switching cycle, the internal clock turns on the N-channel LS-FET. During normal operation, the minimum turn-on time (t_{ON_MIN}) is about 70ns. A stabilizing ramp is added to the current-sense amplifier's output to prevent sub-harmonic oscillations at >50% duty cycles. This result is fed into the PWM comparator. Once the summed voltage reaches the error amplifier's (EA's) output, the low-side MOSFET turns off.

Output Voltage Regulation

The MP3314 supports adaptive control and manual control to regulate V_{OUT}.

Adaptive Control

When ADAPTIVE = 1b, the boost loop works in adaptive control mode. In adaptive control mode, the initial V_{OUT} is set by VO[7:0].

The converter automatically chooses the lowest active LEDx voltage (V_{LEDx_MIN}) as the feedback voltage (V_{FB}) to regulate V_{OUT}. V_{LEDx_MIN} is monitored periodically, and is regulated to the optimized voltage set by HEADR[2:0] (which sets the headroom voltage low threshold, HEADR) and CPHYST[1:0] (which sets the comparison hysteresis, CPHYST).

If V_{LEDx_MIN} is below HEADR, V_{OUT} increases by one step. If V_{LEDx_MIN} exceeds (HEADR + CPHYST), V_{OUT} decreases by one step.

The V_{OUT} up and down voltage steps can be configured via STEPUP[1:0] and STEPDN[1:0], respectively.

Manual Control

In manual control mode, V_{OUT} is set by VO[7:0].

Pulse-Skip Mode (PSM)

Under light-load conditions (especially when V_{OUT} is almost equal to V_{IN}), the converter operates in pulse-skip mode (PSM). In PSM, the MOSFET turns on for a minimum on time (t_{ON_MIN}). The MOSFET remains off for several switching cycles to prevent V_{OUT} from exceeding the regulated voltage. Once the device stops switching, the output capacitor (C_{OUT}) discharges to power the LED string. The device starts switching and continues switching until V_{OUT} is boosted again.

Brightness Control

The MP3314 supports flexible brightness control methods that can be configured by the brightness mode setting (BRTM[1:0]) via the I²C (see Figure 4 and Figure 5, and Figure 6, as well as Figure 7 on page 16). Both the external PWM signal and internal PWM[15:0] bits can adjust the brightness.

When PWMDR = 1b, the MP3314 operates in direct PWM dimming mode, and the LED current (I_{LEDx}) directly follows the external PWM input signal.

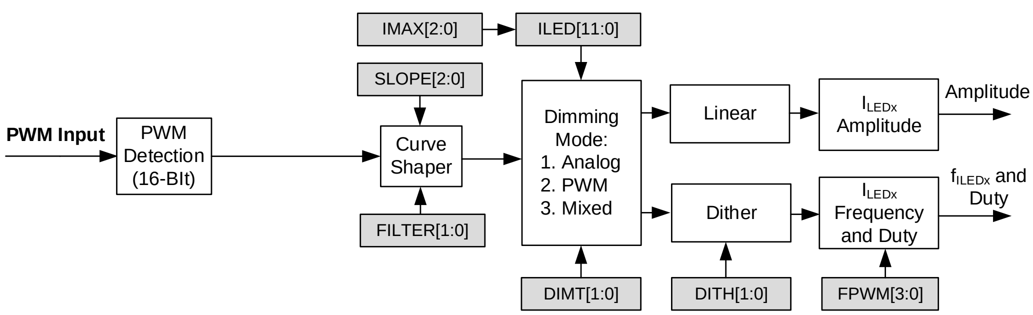


Figure 4: Brightness Control via the External PWM Signal (BRTM[1:0] = 00b)

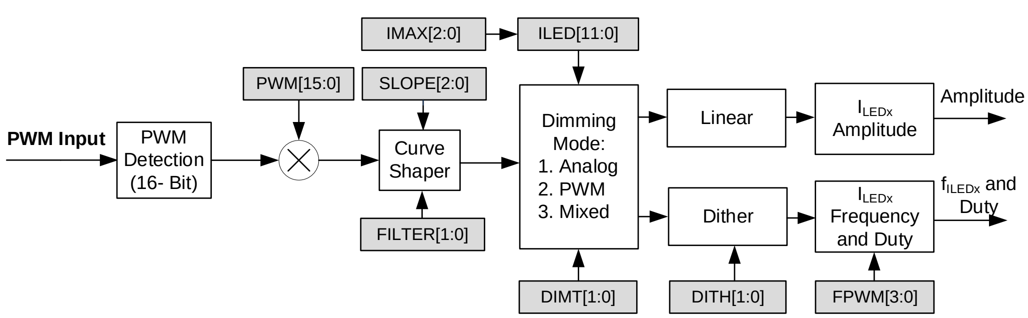


Figure 5: Brightness Control via the External PWM Signal x PWM[15:0] (BRTM[1:0] = 01b)

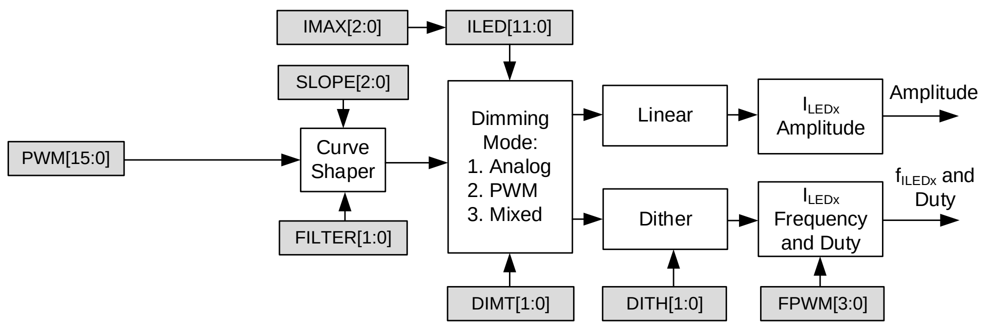


Figure 6: Brightness Control via Internal PWM[15:0] Bits (BRTM1:0 = 10b)

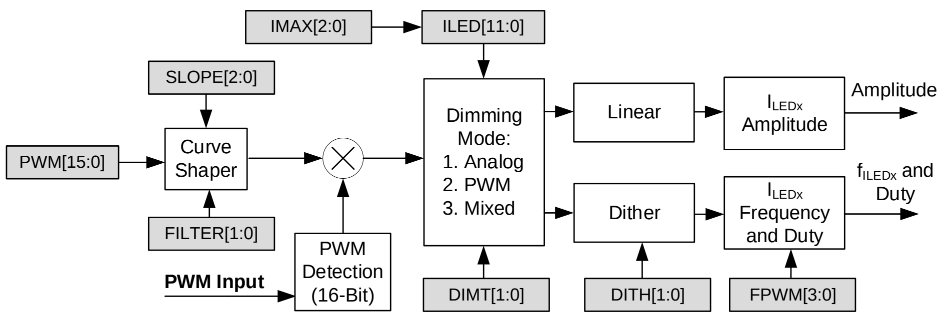


Figure 7: Brightness Control via the External PWM Signal x PWM[15:0] (BRTM1:0 = 11b)

Dimming Modes

The MP3314 has three dimming modes.

Analog Dimming

When DMOD[1:0] = 01b, the MP3314 operates in analog dimming mode. In this mode, the I_{LEDx} amplitude increases linearly as the dimming duty increases.

Auto-Selected Switching Frequency (f_{SW})

In analog dimming mode, the auto-selected f_{SW} function can be employed by comparing the I_{LEDx} amplitude to the set threshold to optimize efficiency at different load currents.

The auto-selected f_{SW} function is implemented by comparing the output brightness code's 8 most-significant bits (MSB) with auto-selected f_{SW} high threshold (HILED[7:0], 0Dh) and low threshold (LILED[7:0], 0Ch) (see Table 1).

Table 1: Auto-Selected Switching Frequency

Output Brightness Code's 8MSB	f_{SW}
Below LILED	312kHz
Between HILED and LILED	625kHz
Exceeds HILED	1.25MHz

To disable the auto-selected f_{SW} function, set the HILED and LILED registers to 0.

PWM Dimming Mode

When DMOD[1:0] = 00b, the MP3314 operates in PWM dimming mode. In this mode, the I_{LEDx} amplitude is configured via ILED[11:0] and IMAX[2:0]. The I_{LEDx} frequency (f_{ILEDx}) can be configured via an external FSET resistor (R_{FSET}) or FPWM[3:0]. If FSETEN = 0b, then f_{ILEDx} follows the register setting. The I_{LEDx} duty follows the dimming duty.

Mix Dimming Mode

When DMOD[1:0] = 10b, the MP3314 operates in mix dimming mode, and the transfer point (TP) is set by DIMT[1:0].

When the dimming duty exceeds TP, the device follows analog dimming, and the I_{LEDx} amplitude increases linearly as the dimming duty increases. When the dimming duty is below TP, the device follows PWM dimming, the I_{LEDx} amplitude remains at the TP value, and the output I_{LEDx} duty can be calculated with Equation (1):

$$(1 / TP) \times \text{Dimming Duty} \quad (1)$$

For example, if TP is 25% and the PWM duty is below 25%, then the I_{LEDx} amplitude is 1/4 of the full-scale current, and the output I_{LEDx} duty is four times the input PWM signal's duty (see Figure 8).

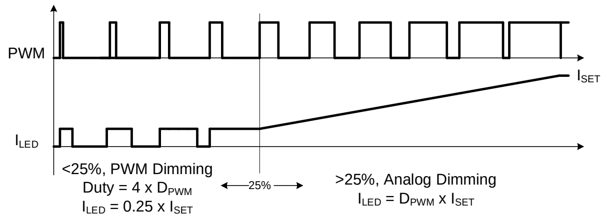


Figure 8: Mix Dimming with 25% Transfer Point

LED Current Transition Time and Slope

The I_{LEDx} amplitude transition time and duty variation can be configured by SLOPE[2:0].

FILTER[1:0] sets the I_{LEDx} amplitude's curvature and duty variation.

Figure 9 shows the LED current transition and smoothing.

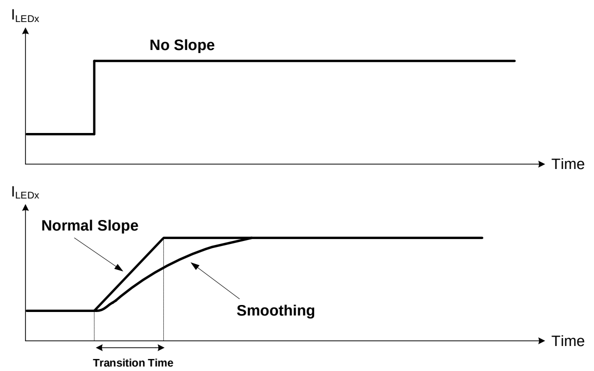


Figure 9: LED Current Transition and Smoothing

Frequency Spread Spectrum (FSS)

The MP3314 uses frequency jittering to spread the f_{SW} spectrum. This reduces the spectrum spike around f_{SW} and its harmonic frequencies.

The frequency spread spectrum (FSS) range is set by the FSPR bit. When FSPR = 0b (default), the FSS range is set to 1/10 of f_{SW}. When FSPR = 1b, the FSS range is set to 1/16 of f_{SW}.

The modulation frequency is set by FSPMF[1:0]. When FSPMF[1:0] = 00b, the modulation frequency is set to 1/100 of f_{SW}. When FSPMF[1:0] = 01b, the modulation frequency is set to 1/150 of f_{SW}. When FSPMF[1:0] = 10b, the modulation frequency is set to 1/200 of f_{SW}.

When FSPMF[1:0] = 11b (default), the FSS function is disabled.

Voltage Jump Function

If an application requires a fast V_{OUT} response to dimming duty variations, the device can employ the voltage jump function. If the dimming duty increases, and the variation exceeds the threshold set by JUMPTH[1:0], then V_{OUT} increases according the voltage set by JUMPV[1:0].

Switching Slew Rate Setting

The internal MOSFET has three types of driving capabilities to reduce EMI. The driving capability can be configured via SRSW[1:0]. The weaker the driving capability, the better the EMI performance. Consider the trade-off between the slow switching speed and efficiency when selecting the driving capability.

Digital Dithering

The MP3314 features a digital dithering scheme to improve the dimming resolution. 3-bit dithering can increase the resolution by 1/8.

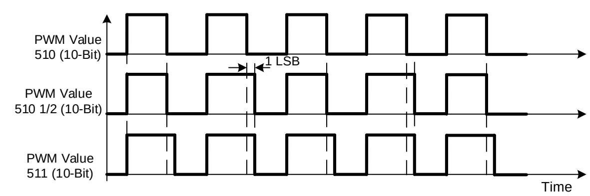


Figure 10: Digital Dithering (1-Bit Dither, 10-Bit Resolution)

Unused LED Channel Setting

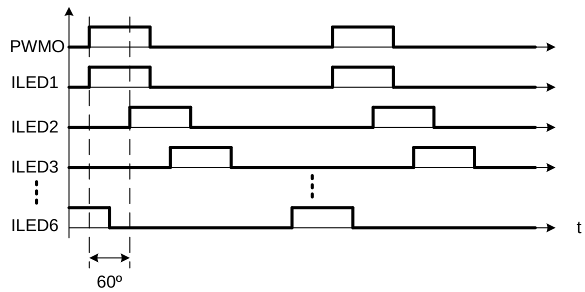
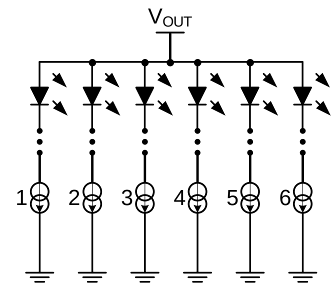
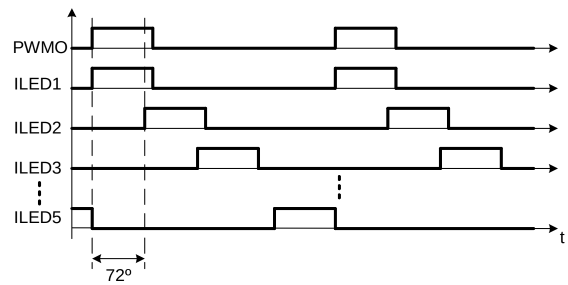
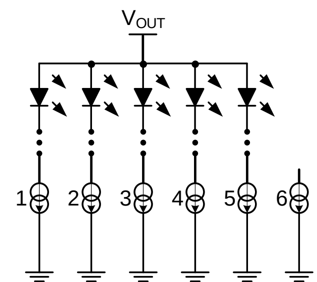
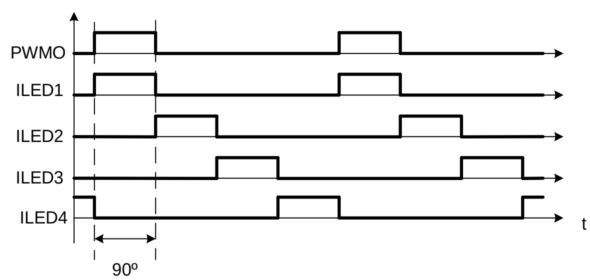
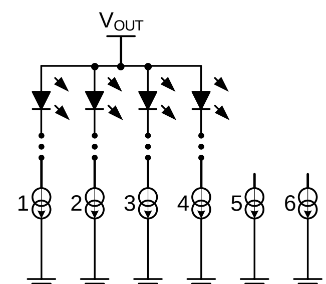
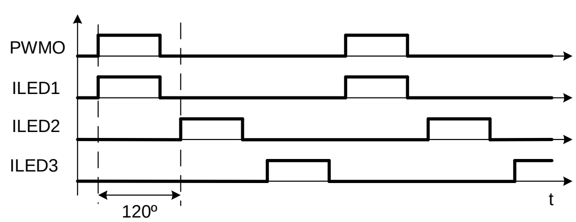
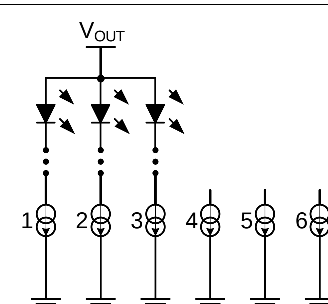
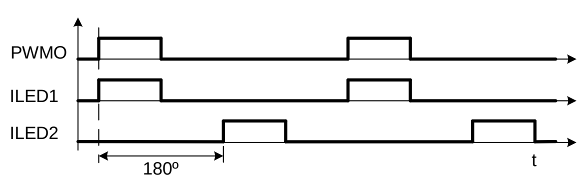
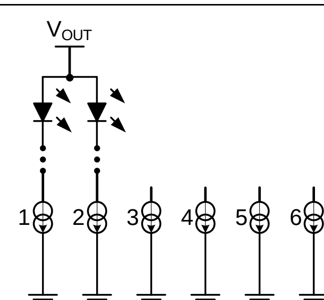
The MP3314 can detect an unused LED channel automatically. It removes the unused channel from the voltage control loop during start-up by setting the corresponding CHENx (x = 0, 1, 2, 3, 4, or 5) bit to 0.

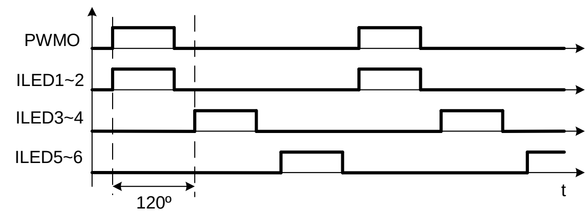
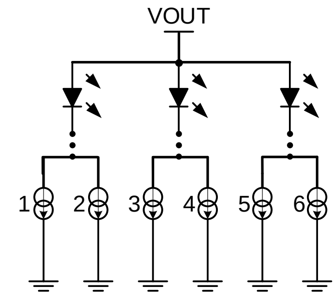
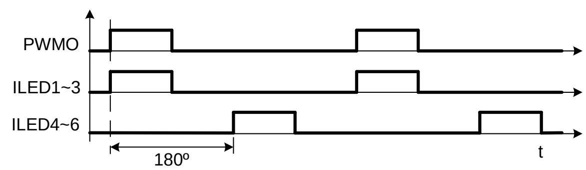
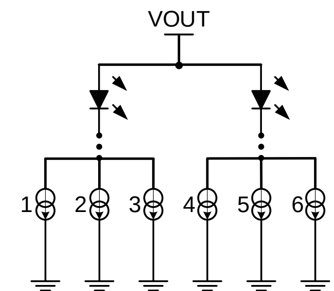
Phase Shift Function

The MP3314 integrates a phase shift function to reduce inrush current and audible noise during PWM dimming.

The phase shift function can be configured via PS[2:0] (see Table 2 on page 18).

Table 2: Phase Shift Function Configurations

PS[2:0]	Phase Shift	Typical Waveforms	Connection
000b	6 LED channels with 60° phase shift, 6 phases		
001b	5 LED channels with 72° phase shift, 5 phases, channel 6 is unused		
010b	4 LED channels with 90° degree phase shift, 4 phases, channels 5~6 are unused		
011b	3 LED channels with 120° phase shift, 3 phases, channels 4~6 are unused		
100b	2 LED channels with 180° phase shift, 2 phases, channels 3~6 are unused		

101b	3 LED strings with 120° phase shift, 3 phases, 2 channels per LED string		
110b	2 LED strings with 180° phase shift, 2 phases, 3 channels per LED string		
111b	Disabled	-	-

Protections

The MP3314 features LED open protection, LED short protection, LEDx pin short to GND protection, over-current protection (OCP), and over-temperature protection. If a protection is triggered, the corresponding fault bit is set to 1.

Input Under-Voltage Lockout (UVLO) Protection

V_{IN} under-voltage lockout (UVLO) can be enabled or disabled via the UVLO_EN bit. If UVLO_EN = 0b, UVLO is disabled, and the status of FT_UVLO is disregarded. If UVLO_EN = 1b, and V_{IN} is below the UVLO threshold set by the UVLOH bit, then the IC shuts down and the I^2C is disabled. If V_{EN} remains high and V_{IN} exceeds its UVLO rising threshold, then the IC recovers and the UVLO fault can be read (showing that a V_{IN} UVLO fault has occurred).

LED Open Protection

LED open protection is achieved by detecting V_{OUT} and the LEDx pins. If one LED channel is open while the part is operating, the respective LEDx pin voltage (V_{LEDx}) is pulled down to AGND, and the IC continues charging V_{OUT} until it reaches the OVP threshold (set by OVP[2:0]). If OVP is triggered, the IC marks any fault channels with V_{LEDx} below 80mV. Once marked, the remaining LED channels force V_{OUT} back to its normal regulation voltage. The LED channel with the largest voltage drop determines V_{OUT}.

In manual mode, if V_{LEDx} is below the LEDx UVLO threshold while dimming is on for about 24ms, LED open protection is triggered. LED open protection has automatic recovery.

LED Short Protection

The MP3314 monitors V_{LEDx} to determine whether an LED short has occurred. If one or more LED channels are shorted, the respective LEDx pins tolerate the high voltage stress. If a V_{LEDx} exceeds the protection threshold set by LEDS[1:0], an internal counter starts. If an LED short lasts for 1.8ms, the fault channel is marked off and disabled. Once a channel is marked off, it is disconnected from the output voltage loop. LED short protection has automatic recovery.

LED short protection only works when at least one V_{LEDx} is regulated to the optimized voltage.

LEDx Short to GND Protection

If an LEDx pin short to GND occurs, the compensation voltage (V_{COMP}) increases and saturates. Once V_{COMP} is saturated for 20ms or 40ms (set by the TCOMP bit), the LEDx short to GND protection is triggered and the IC latches off.

Cycle-by-Cycle Current Limit

To prevent the external components from exceeding the current stress rating, the IC integrates cycle-by-cycle current limit (I_{LIMIT}) protection. The cycle-by-cycle I_{LIMIT} can be selected by ILIM[2:0]. If the current exceeds the I_{LIMIT}, the LS-FET turns off until the next clock cycle begins.

Latch-Off Over-Current Protection (OCP)

To avoid damage to the device caused by a large current (e.g. an inductor or diode short), the MP3314 implements latch-off OCP. If the current flowing through the LS-FET reaches the latch-off I_{LIMIT} and remains there for five consecutive switching cycles, latch-off OCP is triggered and the IC latches off.

Over-Temperature Protection

To prevent the IC from operating at exceedingly high temperatures, the device implements thermal shutdown by detecting the silicon die temperature. If the die temperature exceeds the thermal shutdown threshold (T_{SD}), the IC shuts down. Once the die temperature drops below about 130°C, the device resumes normal operation. There is a typical 20°C hysteresis.

One-Time Programmable (OTP) Memory

The MP3314 can change the register default values one time thru the OTP function. MPS factory can write the customized default register values with different –3314 suffix code.

I²C REGISTER MAP [7]

<table>
<tr><th>Name</th><th>R/W</th><th>Add</th><th>Default</th><th>D[7]</th><th>D[6]</th><th>D[5]</th><th>D[4]</th><th>D[3]</th><th>D[2]</th><th>D[1]</th><th>D[0]</th></tr>
<tr><td>PWM_DUTY_H</td><td>R/W</td><td>00h</td><td>FF</td><td colspan="8">PWM[15:8]</td></tr>
<tr><td>PWM_DUTY_L</td><td>R/W</td><td>01h</td><td>FF</td><td colspan="8">PWM[7:0]</td></tr>
<tr><td>MODE_CTRL</td><td>R/W</td><td>02h</td><td>9D</td><td>ADAPTIVE</td><td>PWMDR</td><td colspan="3">ILIM[2:0]</td><td colspan="2">DMOD[1:0]</td><td>R_EN</td></tr>
<tr><td>SBY_CHEN</td><td>R/W</td><td>03h</td><td>7F</td><td>NC</td><td>SBY_PWM</td><td colspan="6">CHEN[5:0]</td></tr>
<tr><td>FUNC_SET_0</td><td>R/W</td><td>04h</td><td>70</td><td colspan="2">BRTM[1:0]</td><td colspan="3">OVP[2:0]</td><td>TDITH</td><td colspan="2">DITH[1:0]</td></tr>
<tr><td>PHASE_SHIFT</td><td>R/W</td><td>05h</td><td>38</td><td colspan="2">NC</td><td colspan="3">PS[2:0]</td><td colspan="3">NC</td></tr>
<tr><td>ILED_SET_0</td><td>R/W</td><td>06h</td><td>FF</td><td colspan="8">ILED[7:0]</td></tr>
<tr><td>ILED_SET_1</td><td>R/W</td><td>07h</td><td>3F</td><td>NC</td><td colspan="3">IMAX[2:0]</td><td colspan="4">ILED[11:8]</td></tr>
<tr><td>FUNC_SET_1</td><td>R/W</td><td>08h</td><td>A7</td><td colspan="2">DIMT</td><td>UVLO_EN</td><td>UVLOH</td><td>NC</td><td>ISET_EN</td><td>FSETEN1</td><td>FSETEN0</td></tr>
<tr><td>CURVE_SHAPE</td><td>R/W</td><td>09h</td><td>82</td><td>VOHL</td><td colspan="3">SLOP[2:0]</td><td colspan="2">FILTER[1:0]</td><td colspan="2">PWMHY[1:0]</td></tr>
<tr><td>SLEW_FREQ</td><td>R/W</td><td>0Ah</td><td>A0</td><td colspan="2">SRSW[1:0]</td><td colspan="2">FSW[1:0]</td><td colspan="4">FPWM[3:0]</td></tr>
<tr><td>FSS_LEDS</td><td>R/W</td><td>0Bh</td><td>66</td><td>NC</td><td colspan="2">FSPMF[1:0]</td><td>FSPR</td><td colspan="2">LEDS[1:0]</td><td>TCOMP</td><td>NC</td></tr>
<tr><td>AUTO_FSW_L</td><td>R/W</td><td>0Ch</td><td>00</td><td colspan="8">LILED[7:0]</td></tr>
<tr><td>AUTO_FSW_H</td><td>R/W</td><td>0Dh</td><td>00</td><td colspan="8">HILED[7:0]</td></tr>
<tr><td>VOUT_SET</td><td>R/W</td><td>0Eh</td><td>32</td><td colspan="8">VO[7:0]</td></tr>
<tr><td>HEADR_L</td><td>R/W</td><td>0Fh</td><td>2F</td><td colspan="2">NC</td><td colspan="3">HEADR[2:0]</td><td colspan="3">HEADRO[2:0]</td></tr>
<tr><td>CPH_STEP</td><td>R/W</td><td>10h</td><td>C0</td><td colspan="2">CPHYST[1:0]</td><td colspan="2">STEPUP[1:0]</td><td colspan="2">STEPDN[1:0]</td><td colspan="2">NC</td></tr>
<tr><td>VO_JUMP</td><td>R/W</td><td>11h</td><td>00</td><td>JUMPEN</td><td colspan="2">JUMPTH[1:0]</td><td colspan="2">JUMPV[1:0]</td><td colspan="3">NC</td></tr>
<tr><td>ID</td><td>R</td><td>1Dh</td><td>11</td><td colspan="8">ID[7:0]</td></tr>
<tr><td>FAULT</td><td>R</td><td>1Fh</td><td>00</td><td>NC</td><td>FT_UVLO</td><td>FT_LEDG</td><td>FT_OTP</td><td>FT_OCP</td><td>FT_OVP</td><td>FT_LEDO</td><td>FT_LEDS</td></tr>
</table>

Note:

7) All registers can be written to a customized default value one time.

I²C REGISTER DESCRIPTION

PWM_DUTY_H (00h)

The PWM_DUTY_H command sets the 8MSB of the 16-bit, internal dimming duty register.

Bits	Access	Bit Name	Default	Description
7:0	R/W	PWM[15:8]	8'hFF	Sets the 8MSB of the LED current (I_{LEDx}) internal dimming duty register. The internal dimming duty does not change until the 8 least significant bits (LSBs) are written.

PWM_DUTY_L (01h)

The PWM_DUTY_L command sets the 8LSB of 16bits internal dimming duty register.

Bits	Access	Bit Name	Default	Description
7:0	R/W	PWM[7:0]	8'hFF	Sets the 8 LSBs of the I_{LEDx} internal dimming duty register. The internal dimming duty does not change until the 8 LSBs are written.

MODE_CTRL (02h)

The MODE_CTRL command sets the loop control mode, dimming mode, and the boost circuit current limit (I_{LIMIT}). MODE_CTRL can also enable and disable the IC.

Bits	Access	Bit Name	Default	Description
7	R/W	ADAPTIVE	1'b1	This bit sets the boost loop control mode. 1'b1: Adaptive control mode 1'b0: Manual control mode
6	R/W	PWMDR	1'b0	This bit sets the direct PWM dimming mode. 1'b0: See BRTM[1:0] in the FUNC_SET_0 (04h) section for more details 1'b1: Direct PWM dimming, I_{LEDx} follows the external PWM signal
5:3	R/W	ILIM	3'b011	These bits set the cycle-by-cycle I_{LIMIT}. 3'b000: 0.9A 3'b001: 1.2A 3'b010: 1.5A 3'b011: 1.8A 3'b100: 2.1A 3'b101: 2.4A 3'b110: 2.7A 3'b111: 3A
2:1	R/W	DMOD	2'b10	These bits set the dimming mode. 2'b00: PWM dimming mode 2'b01: Analog dimming mode 2'b10: Mix dimming mode
0	R/W	R_EN	1'b1	This bit enables the IC. R_EN is the highest-priority enable (EN) bit. When R_EN = 0, all blocks are disabled, except the I²C. 1'b0: Disable. 1'b1: Enable. If external PWM signal is used for brightness control, it can also be used to enable/disable IC. SBY_PWM bit can program this function.

SBY_CHEN (03h)

The SBY_CHEN command can enables standby mode and the 6 LED current sources separately.

Bits	Access	Bit Name	Default	Description
7	R	RESERVED	N/A	Reserved.
6	R/W	SBY_PWM	1’b1	This bit enables standby mode when the PWM pin is pulled low for at least 70ms. 1’b0: Disabled 1’b1: Enabled
5:0	R/W	CHEN	6’b111111	These bits enable the LED current source. CHEN[5:0] corresponds to channels 6 through 1, respectively. CHENx = 1’b1: LED channel (x + 1) is enabled CHENx = 1’b0: LED channel (x + 1) is disabled

FUNC_SET_0 (04h)

The FUNC_SET_0 command sets the brightness control source, OVP threshold, and digital dithering function.

Bits	Access	Bit Name	Default	Description
7:6	R/W	BRTM	2’b01	These bits select the brightness control source. 2’b00: External PWM signal 2’b01: External PWM signal and internal dimming duty setting register (external PWM signal duty is multiplied before the curve shaper) 2’b10: Internal dimming duty setting register 2’b11: External PWM signal and internal dimming duty setting register (external PWM signal duty is multiplied after the curve shaper)
5:3	R/W	OVP	3’b110	These bits set the V_{OUT} OVP threshold. 3’b010 (VOHL = 0b): N/A 3’b010 (VOHL = 1b): 21V 3’b011 (VOHL = 0b): N/A 3’b011 (VOHL = 1b): 25V 3’b100 (VOHL = 0b): 21V 3’b100 (VOHL = 1b): 30V 3’b101 (VOHL = 0b): 25V 3’b101 (VOHL = 1b): 34.5V 3’b110 (VOHL = 0b): 30V 3’b110 (VOHL = 1b): 39V 3’b111 (VOHL = 0b): 34V 3’b111 (VOHL = 1b): 43V
2	R/W	TDITH	1’b0	This bit sets when the dithering function is active. 1’b0: Dithering is only active during transitions 1’b1: Dithering is active at all times
1:0	R/W	DITH	2’b00	These bits select the dithering function. 2’b00: Dithering is disabled 2’b01: 1-bit dithering 2’b10: 2-bit dithering 2’b11: 3-bit dithering

PHASE_SHIFT (05h)

The PHASE_SHIFT command sets the phase shift function for indirect PWM dimming and mix dimming.

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	N/A	Reserved.
5:3	R/W	PS	3'b111	These bits set the phase shift function. 3'b000: 60° phase shift for 6 channels and 6 phases 3'b001: 72° phase shift for 5 channels and 5 phases 3'b010: 90° phase shift for 4 channels and 4 phases 3'b011: 120° phase shift for 3 channels and 3 phases 3'b100: 180° phase shift for 2 channels and 2 phases 3'b101: 120° phase shift for 6 channels and 3 phases 3'b110: 180° phase shift for 6 channels and 2 phases 3'b111: Phase shift function is disabled See Table 2 on page 18 for more details regarding the phase shift configuration options.
2:0	R	RESERVED	N/A	Reserved.

ILED_SET_0 (06h)

The ILED_SET_0 command sets 8 LSBs of the 12-bit I_{LEDx} amplitude register.

Bits	Access	Bit Name	Default	Description
7:0	R/W	ILED7:0	8'hFF	These bits set the I_{LEDx} amplitude's 8 LSBs. These 12 bits further scale the maximum I_{LEDx} set by IMAX[2:0].

ILED_SET_1 (07h)

The ILED_SET_1 command sets the maximum I_{LEDx} and the 4MSB of the 12-bit I_{LEDx} amplitude register.

Bits	Access	Bit Name	Default	Description
7	R	RESERVED	N/A	Reserved.
6:4	R/W	IMAX	3'b011	These bits set the maximum I_{LEDx}. 3'b000: 5mA 3'b001: 10mA 3'b010: 15mA 3'b011: 20mA 3'b100: 23mA 3'b101: 25mA 3'b110: 30mA 3'b111: 50mA
3:0	R/W	ILED[11:8]	4'b1111	These bits set the I_{LEDx} amplitude's 4MSB. These 12 bits further scale the maximum I_{LEDx} set by IMAX[2:0].

FUNC_SET_1 (08h)

The FUNC_SET_1 command sets the transfer point mix dimming, enabled the UVLO function, and enables the external setting resistor.

Bits	Access	Bit Name	Default	Description
7:6	R/W	DIMT	2'b10	These bits select the mix dimming transfer point. 2'b00: 12.5% 2'b01: 20% 2'b10: 25% 2'b11: 50%

5	R/W	UVLO_EN	1’b1	This bit enables the V_{IN} UVLO function. 1’b0: Disabled 1’b1: Enabled
4	R/W	UVLOH	1’b0	This bit sets the UVLO threshold. 1’b0: 2.5V 1’b1: 5.2V
3	R	RESERVED	N/A	Reserved.
2	R/W	ISET_EN	1’b1	This bit enables the external ILED setting resistor. 1’b0: Disabled 1’b1: Enabled
1	R/W	FSETEN1	1’b1	This bit enables the boost f_{SW} set by the FSET resistor. 1’b0: Disabled 1’b1: Enabled
0	R/W	FSETEN0	1’b1	This bit enables the ILED frequency (f_{ILED}) set by the FSET resistor. 1’b0: Disabled 1’b1: Enabled

CURVE_SHAPE (09h)

The CURVE_SHAPE command sets the V_{OUT} range, the LED current transition time and filter strength, and the PWM input signal hysteresis.

Bits	Access	Bit Name	Default	Description
7	R/W	VOHL	1’b1	This bit sets the V_{OUT} range. 1’b0: 7V to 34V 1’b1: 16V to 43V
6:4	R/W	SLOPE	3’b000	These bits select the brightness change transition duration. 3’b000: 0ms (immediate change) 3’b001: 1ms 3’b010: 2ms 3’b011: 50ms 3’b100: 100ms 3’b101: 200ms 3’b110: 300ms 3’b111: 500ms
3:2	R/W	FILTER	2’b00	These bits select the brightness change transition filtering strength. 2’b00: No filtering 2’b01: Light smoothing 2’b10: Medium smoothing 2’b11: Heavy smoothing
1:0	R/W	PWMHY1:0	2’b10b	These bits select the PWM input signal hysteresis. 2’b00b: No hysteresis 2’b01b: 1-bit hysteresis with a 13-bit resolution 2’b10b: 1-bit hysteresis with a 12-bit resolution 2’b11b: 1-bit hysteresis with a 8-bit resolution

SLEW_FREQ (0Ah)

The SLEW_FREQ command sets the boost switching slew rate, boost f_{SW}, and the LED current dimming frequency (f_{ILED}) in indirect PWM dimming mode and mix dimming mode.

Bits	Access	Bit Name	Default	Description
7:6	R/W	SRSW	2'b10	These bits set the switching slew rate. 2'b00: 1 driver 2'b01: 2 drivers 2'b10: 3 drivers 2'b11: NC
5:4	R/W	FSW	2'b10	These bits set the boost f_{SW}. 2'b00: 312kHz 2'b01: 625kHz 2'b10: 1250kHz 2'b11: NC
3:0	R/W	FPWM	4'b0000	These bits set f_{ILED}. 4'b0000: 4,808Hz (11-bit) 4'b0001: 6,010Hz (10-bit) 4'b0010: 7,212Hz (10-bit) 4'b0011: 8,414Hz (10-bit) 4'b0100: 9,616Hz (10-bit) 4'b0101: 12,020Hz (9-bit) 4'b0110: 13,222Hz (9-bit) 4'b0111: 14,424Hz (9-bit) 4'b1000: 15,626Hz (9-bit) 4'b1001: 16,828Hz (9-bit) 4'b1010: 18,030Hz (9-bit) 4'b1011: 19,232Hz (9-bit) 4'b1100: 24,040Hz (8-bit) 4'b1101: 28,848Hz (8-bit) 4'b1110: 33,656Hz (8-bit) 4'b1111: 38,464Hz (8-bit)

FSS_LEDS (0Bh)

The FSS_LEDS command sets the FSS modulation frequency and frequency spread range. It also sets the LED short protection threshold and the LEDx short to GND protection compensation saturation time.

Bits	Access	Bit Name	Default	Description
7	R	RESERVED	N/A	Reserved.
6:5	R/W	FSPMF	2'b11	These bits set the FSS modulation frequency. 2'b00: 1/100 of f_{SW} 2'b01: 1/150 of f_{SW} 2'b10: 1/200 of f_{SW} 2'b11: FSS is disabled
4	R/W	FSPR	1'b0	This bit sets the FSS range. 1'b0: 1/10 of f_{SW} 1'b1: 1/16 of f_{SW}
3:2	R/W	LEDS	2'b01	These bits set the LED short protection threshold. 2'b00: 2V 2'b01: 5V 2'b10: 7V 2'b11: 10V

1	R/W	TCOMP	1'b1	This bit sets the LEDx short to GND protection compensation saturation time. 1'b0: 20ms 1'b1: 40ms
0	R	RESERVED	N/A	Reserved.

AUTO_FSW_L (0Ch)

The AUTO_FSW_L command sets the auto-selected f_{SW} low threshold.

Bits	Access	Bit Name	Default	Description
7:0	R/W	LILED	8'h00	Sets the auto-selected f_{SW} low threshold (625kHz or 312kHz). Compare with the output brightness code's 8MSB. The auto-selected f_{SW} function is disabled when both HILED and LILED are set 0.

AUTO_FSW_H (0Dh)

The AUTO_FSW_H command sets the high threshold for auto-selecting switching frequency function.

Bits	Access	Bit Name	Default	Description
7:0	R/W	HILED	8'h00	Sets the auto-selected f_{SW} high threshold (625kHz or 1.25MHz). Compare with the with the output brightness code's 8MSB. The auto-selected f_{SW} function is disabled when both HILED and LILED are set to 0.

VOUT_SET (0Eh)

The VOUT_SET command sets the boost circuit's V_{OUT}. When the part is operating in adaptive mode, VOUT_SET sets the boost circuit's initial V_{OUT} when the boost circuit starts up, and the final V_{OUT} is adaptively adjusted to a proper level. When the part is operating in manual mode, VOUT_SET sets the LED strings' final V_{OUT}.

Bits	Access	Bit Name	Default	Description
7:0	R/W	VO	8'h32	When ADAPTIVE = 1'b0, VO[7:0] sets V_{OUT}. When Adaptive = 1'b1, VO[7:0] sets the initial V_{OUT}. 8'h00 (VOHL = 1'b0): 7V 8'h01 (VOHL = 1'b0): 7.106V … 8'hFF (VOHL = 1'b0): 34V 8'h00 (VOHL = 1'b1): 16V 8'h01 (VOHL = 1'b1): 16.106V … 8'hFF (VOHL = 1'b1): 43V 0.106V/step.

HEADR_L (0Fh)

The HEADR_L command sets the V_{LEDx} low comparison threshold in adaptive mode. If V_{LEDx_MIN} is below this threshold, V_{OUT} takes a step up.

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	N/A	Reserved.

5:3	R/W	HEADR	3'b101	These bits set the V_{LEDx} low comparison threshold in adaptive mode. 3'b000: HEADRO + 875mV 3'b001: HEADRO + 750mV 3'b010: HEADRO + 625mV 3'b011: HEADRO + 500mV 3'b100: HEADRO + 375mV 3'b101: HEADRO + 250mV 3'b110: HEADRO + 125mV 3'b111: HEADRO + 0mV
2:0	R/W	HEADRO	3'b111	These bits set the V_{LEDx} threshold offset. 3'b000: 562.5mV 3'b001: 500mV 3'b010: 437.5mV 3'b011: 375mV 3'b100: 312.5mV 3'b101: 250mV 3'b110: 187.5mV 3'b111: 125mV

CPH_STEP (10h)

The CPH_STEP command sets the V_{LEDx} comparison hysteresis and the voltage steps up/down in adaptive mode.

Bits	Access	Bit Name	Default	Description
7:6	R/W	CPHYST	2'b11	These bits set the comparison hysteresis. Below are the corresponding high comparison thresholds. 2'b00: HEADR + 1000mV 2'b01: HEADR + 750mV 2'b10: HEADR + 500mV 2'b11: HEADR + 250mV
5:4	R/W	STEPUP	2'b01	These bits set the voltage step up in adaptive mode. 2'b00: 105mV 2'b01: 210mV 2'b10: 420mV 2'b11: 840mV
3:2	R/W	STEPDN	2'b00	These bits set the voltage step down in adaptive mode. 2'b00: 105mV 2'b01: 210mV 2'b10: 420mV 2'b11: 840mV
1:0	R	RESERVED	N/A	Reserved.

VO_JUMP (11h)

The VO_JUMP command enables the V_{OUT} jump function and sets the duty variation thresholds for triggering voltage jump function and the jump voltage value.

Bits	Access	Bit Name	Default	Description
7	R/W	JumpEN	1'b0	This bit enables the voltage jump function. 1'b0: Disabled 1'b1: Enabled

6:5	R/W	JUMPTH	2'b00	These bits set the triggering voltage jump function's duty variation threshold. 2'b00: 10% 2'b01: 30% 2'b10: 50% 2'b11: 70%
4:3	R/W	JUMPV	2'b00	These bits set the jump voltage value. 2'b00: 0.5V 2'b01: 1V 2'b10: 2V 2'b11: 4V When the dimming duty increases and the variation exceeds the threshold set by JUMPTH[1:0], V_{OUT} rises sharply with the voltage set by JUMPV[1:0].
2:0	R	RESERVED	N/A	Reserved.

ID (1Dh)

The ID register indicates the device ID.

Bits	Access	Bit Name	Default	Description
7:0	R	ID	8'h11	These bits indicate the device ID.

FAULT (1Fh)

The FAULT register indicates the status of each fault type.

Bits	Access	Bit Name	Default	Description
7	R	RESERVED	N/A	Reserved.
6	R	FT_UVLO	1'b0	This bit indicates whether a UVLO fault has occurred. 1'b0: No fault 1'b1: Fault If a UVLO fault has occurred, the fault bit is set to 1 until readback or the power is reset.
5	R	FT_LEDG	1'b0	This bit indicates whether an LEDx short to GND has occurred. 1'b0: No fault 1'b1: Fault If an LEDx short to GND has occurred, the fault bit is set to 1 until readback or the power is reset.
4	R	FT_OTP	1'b0	This bit indicates whether an over-temperature (OT) fault has occurred. 1'b0: No fault 1'b1: Fault If an OT fault has occurred, the fault bit is set to 1 until readback or the power is reset.
3	R	FT_OCP	1'b0	This bit indicates whether an over-current (OC) fault has occurred. 1'b0: No fault 1'b1: Fault If an OC fault has occurred, the fault bit is set to 1 until readback or the power is reset.

2	R	FT_OVP	1'b0	This bit indicates whether an over-voltage (OV) fault has occurred. Trim to enable this function. 1'b0: No fault 1'b1: Fault If an OV fault has occurred, the fault bit is set to 1 until readback or the power is reset.
1	R	FT_LEDO	1'b0	This bit indicates whether an LED open fault has occurred. 1'b0: No fault 1'b1: Fault If an LED open fault has occurred, the fault bit is set to 1 until readback or the power is reset.
0	R	FT_LEDS	1'b0	This bit indicates whether an LED short has occurred. 1'b0: No short 1'b1: Short If an LED short fault has occurred, the fault bit is set to 1 until readback or the power is reset.

APPLICATION INFORMATION

Setting the Full-Scale LED Current

When ISET_EN = 1b, the full-scale LED current (I_{SET}) can be configured by I_{MAX} (set by IMAX[2:0]) and the ISET resistor (R_{ISET}). I_{SET} can be calculated with Equation (2):

$$I_{SET}(mA) = \frac{60}{R_{ISET}(k\Omega)} \times I_{MAX} \quad (2)$$

For example, if I_{MAX} = 20mA (IMAX[2:0] = 011b) and R_{ISET} = 60kΩ, then I_{SET} is 20mA.

When ISET_EN = 0b, R_{ISET} is invalid, and I_{SET} can only be configured by IMAX[2:0].

Switching Frequency and LED Current Dimming Frequency Setting

f_{SW} and the LED current dimming frequency (f_{ILED}) can be set by FSW[1:0] and FPWM[3:0] or an external resistor (R_{FSET}). Table 3 shows common R_{FSET} values for different f_{SW} and f_{ILED}.

Table 3: Common R_{FSET} Values

R_{FSET} (kΩ) (1%)	f_{SW} (kHz)	f_{ILED} (Hz)
0	1250	Direct PWM dimming
15	1250	19232
22.6	1250	16828
27.4	1250	14424
33	1250	12020
39	1250	9616
46.4	1250	6010
54.9	1250	4808
64.9	1250	2404
75	625	19232
86.6	625	16828
97.6	625	14424
113	625	12020
127	625	9616
143	625	6010
162	625	4808
180	625	2404
200	312	19232
221	312	16828
249	312	14424
274	312	12020
309	312	9616
340	312	6010
383	312	4808
442	312	2404
Floating	1250	9616

Note:

8) R_{FSET} is valid and can set f_{SW} and f_{ILED} when FSETEN1 = 1b and FSETEN0 = 1b.

Selecting the Input Capacitor

The input capacitor reduces the surge current drawn from the input supply and the switching noise from the device. The input capacitor impedance at the switching frequency should be less than the input source impedance to prevent the high-frequency switching current from passing through to the input. Use ceramic capacitors with X5R or X7R dielectrics for their low ESR and small temperature coefficients. For most applications, a 10μF ceramic capacitor is sufficient.

Selecting the Inductor

The MP3314 requires an inductor to supply a higher output voltage while being driven by the input voltage. A larger value inductor results in less ripple current, lower peak inductor current and less stress on the internal N-channel MOSFET. However, the larger value inductor has a larger physical size, higher series resistance, and lower saturation current.

Choose an inductor that does not saturate under the worst-case load conditions. Select the minimum inductor value to ensure that the boost converter works in continuous conduction mode with high efficiency and good EMI performance. The inductance (L) can be calculated with Equation (3):

$$L \geq \frac{\eta \times V_{OUT} \times D \times (1-D)^2}{2 \times f_{SW} \times I_{LOAD}} \quad (3)$$

Where D is (1 – [V_{IN} / V_{OUT}]), I_{LOAD} is the LED load current, and η is the efficiency.

For most applications, the inductor's DC current rating should be at least 40% higher than the maximum input peak inductor current. The inductor's DC resistance should be as small as possible to achieve high efficiency.

Selecting the Output Capacitor

The output capacitor keeps the output voltage ripple small and ensures feedback loop stability. The output capacitor impedance must be low at the switching frequency. Ceramic capacitors with X7R dielectrics are recommended for their low ESR characteristics. For most applications, a 10μF ceramic capacitor is sufficient.

I²C Chip Address

The 7-bit MSB device address is 0x28. After the start condition, the I²C-compatible master sends a 7-bit address followed by an eighth read (1) or write (0) bit.

0	1	0	1	0	0	0	R/W

I²C Compatible Device Address

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation (especially placement of the high-frequency switching path to reduce noise and EMI). For the best results, refer to Figure 11 and follow the guidelines below:

1. Reference all logic signals to AGND.
2. Connect PGND to AGND externally.
3. Route PGND away from the logic signals.
4. Keep the loop between the SW to PGND pins, output diode (D1), and output capacitor (C1, C2) as short as possible to reduce noise and EMI due to the high-frequency pulse current.

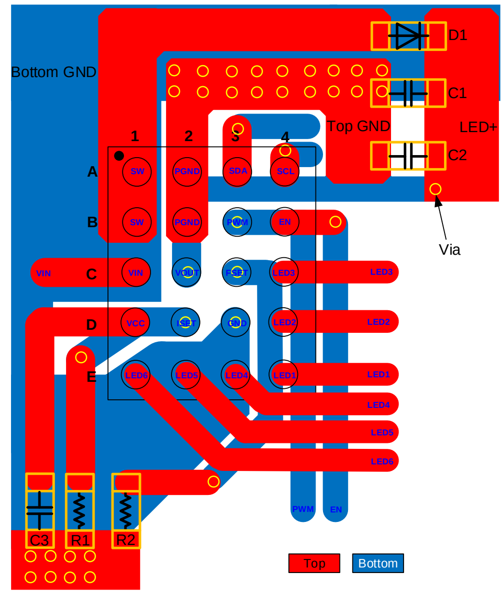


Figure 11: Recommended PCB Layout for the CSP-20 Package

TYPICAL APPLICATION CIRCUIT

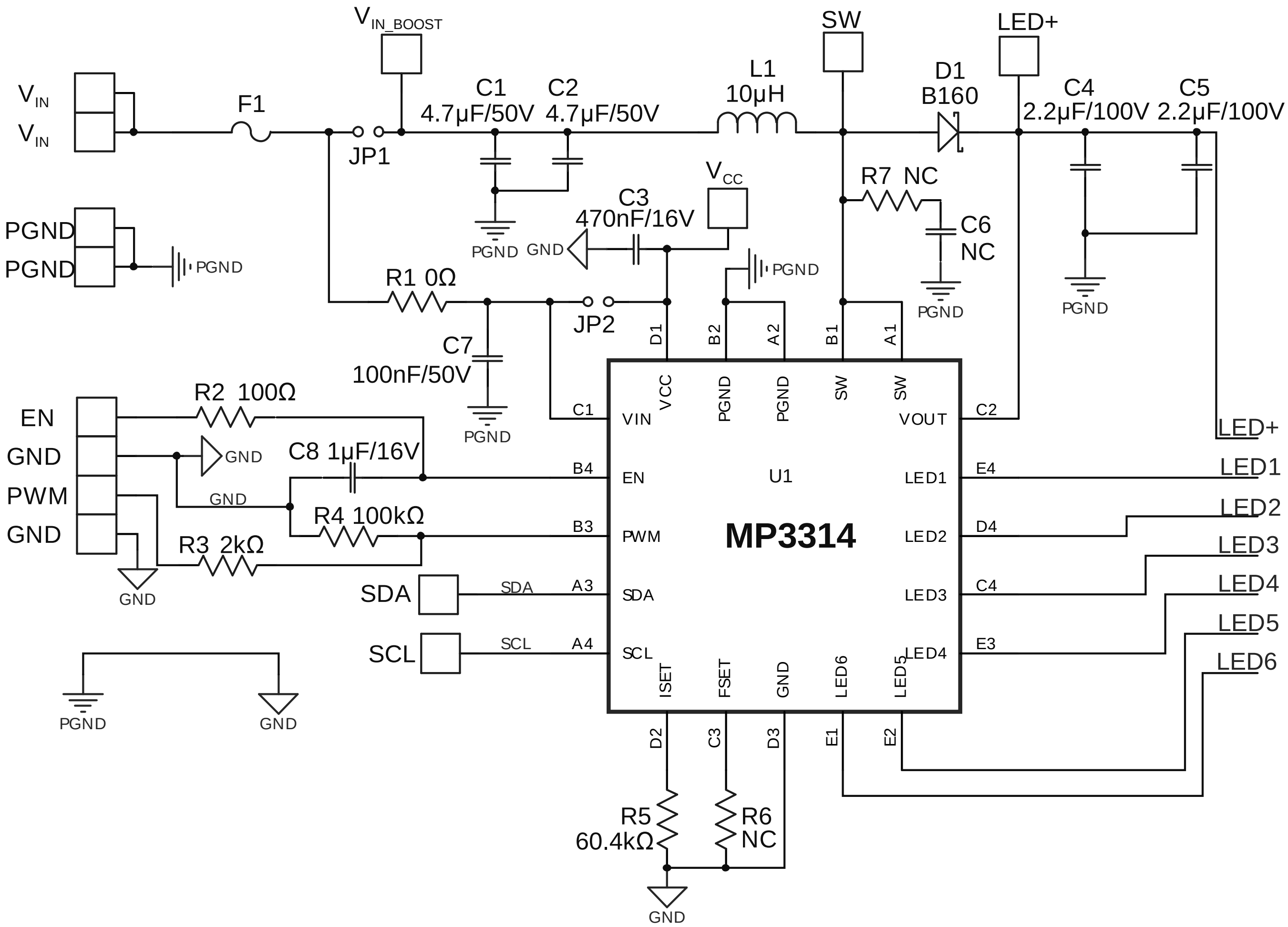
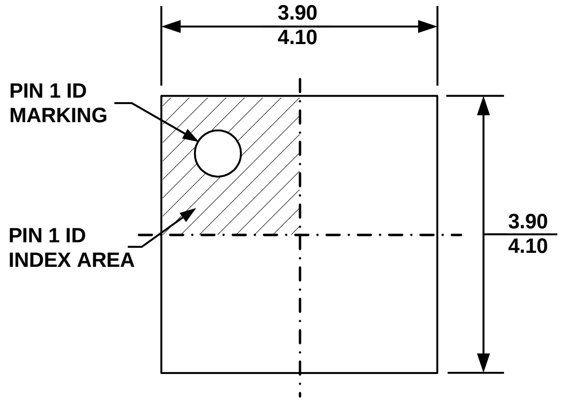


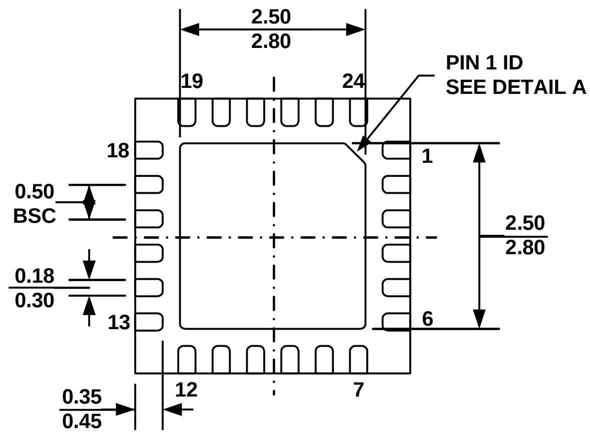
Figure 12: Typical Application Circuit

PACKAGE INFORMATION

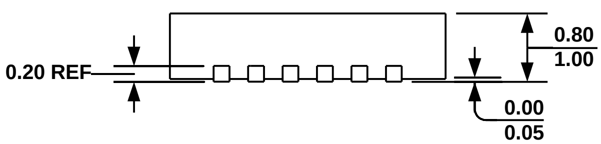
QFN-24 (4mmx4mm)



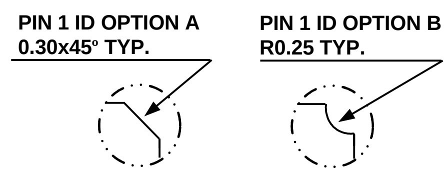
TOP VIEW



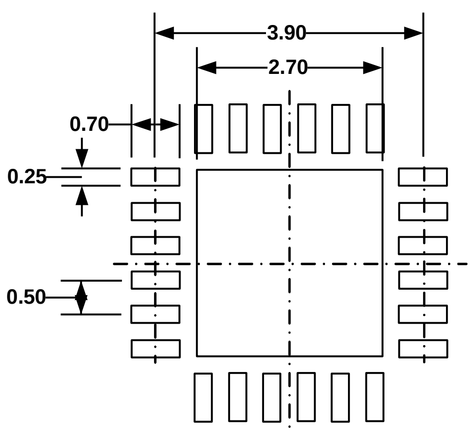
BOTTOM VIEW



SIDE VIEW



DETAIL A



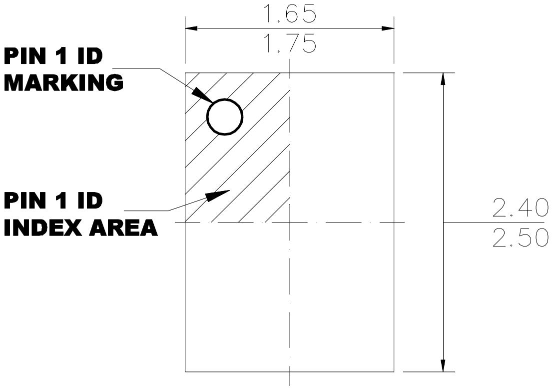
RECOMMENDED LAND PATTERN

NOTE:

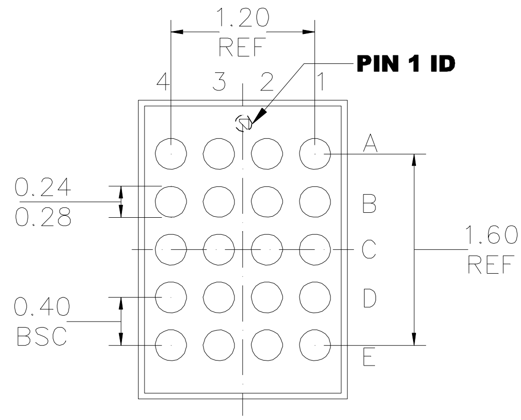
1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) DRAWING CONFIRMS TO JEDEC MO-220, VARIATION VGGD.
5) DRAWING IS NOT TO SCALE.

PACKAGE INFORMATION *(continued)*

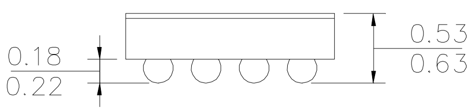
CSP-20 (2.4mmx1.74mm)



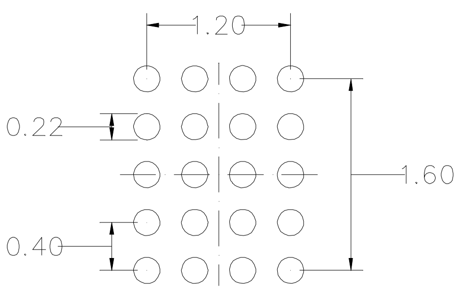
TOP VIEW



BOTTOM VIEW



SIDE VIEW

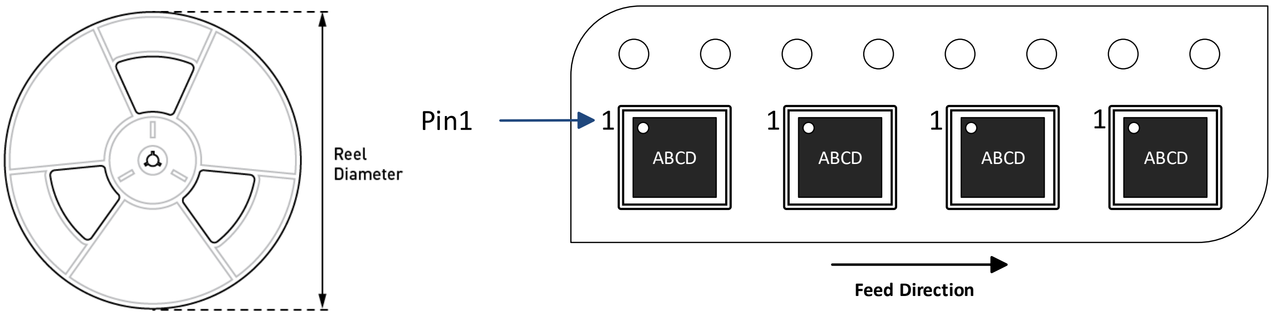


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) BALL COPLANARITY SHALL BE 0.05 MILLIMETER MAX.
3) JEDEC REFERENCE IS MO-211.
4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/Reel	Quantity/Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP3314GR	QFN-24 (4mmx4mm)	5000	N/A	13in	12mm	8mm
MP3314GC	CSP-20 (2.4mmx1.74mm)	3000	N/A	7in	8mm	4mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	4/11/2023	Initial Release	-