MP2395

28V, 3A Peak, High-Efficiency, Synchronous, Step-Down Converter with Power Good in QFN 3x3

The Future of Analog IC Technology

DESCRIPTION

The MP2395 is a high-frequency, synchronous, rectified, step-down, switch-mode converter with built-in power MOSFETs. The MP2395 offers a very compact solution that achieves 3A of peak output current with excellent load and line regulation over a wide input supply range. The MP2395 uses synchronous mode operation for higher efficiency over the output current load range.

Current-mode operation provides fast transient response and eases loop stabilization.

Full protection features include over-current protection (OCP) and thermal shutdown.

The MP2395 requires a minimal number of readily available, standard, external components and is available in a space-saving QFN-8 (3mmx3mm) package.

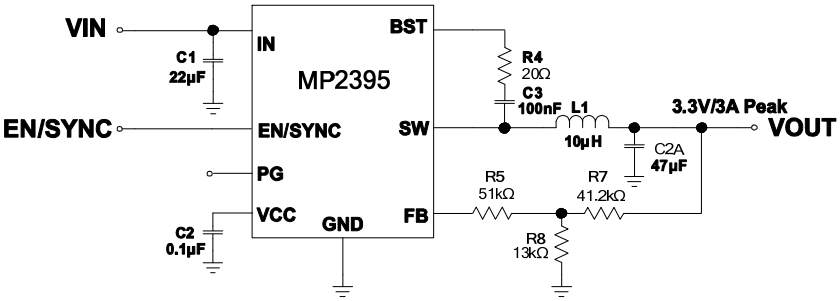
FEATURES

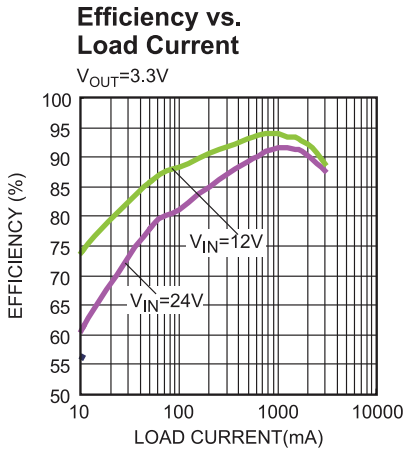
- Wide 4V to 28V Continuous Operating Input Range
- 85mΩ/55mΩ Low $R_{DS(ON)}$ Internal Power MOSFETs
- High-Efficiency Synchronous Mode Operation
- 410kHz Switching Frequency
- Synchronizes from 200kHz to 2.2MHz External Clock
- High Duty Cycle for Automotive Cold Crank
- Internal Power-Save Mode (PSM)
- Internal Soft Start (SS)
- Power Good (PG) Indicator
- Over-Current Protection (OCP) and Hiccup
- Thermal Shutdown
- Output Adjustable from 0.8V
- Available in an QFN-8 (3mmx3mm) Package

APPLICATIONS

- General Consumer
- Multi-Function Printers (MFP)
- Distributed Power Systems

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking
MP2395GQ	QFN-8 (3mmx3mm)	*See Below*

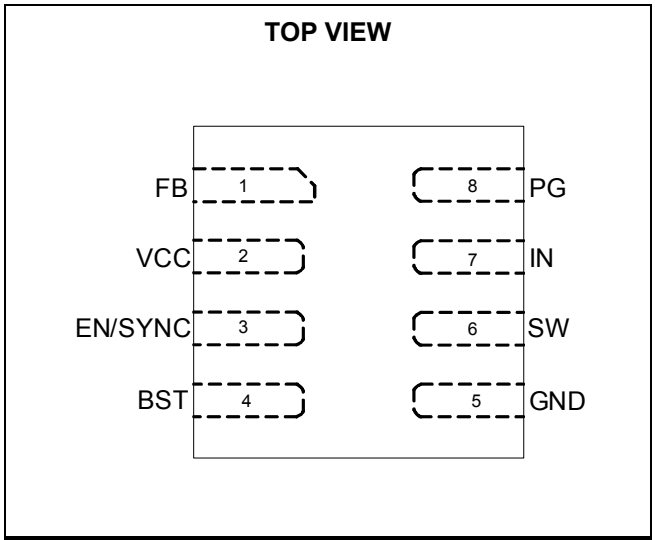
* For Tape & Reel, add suffix –Z (e.g. MP2395GQ–Z)

TOP MARKING

BCPY
LLL

BCP: Product code of MP2395GQ
Y: Year code
LLL: Lot number

PACKAGE REFERENCE



QFN-8 (3mmx3mm)

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} ..... -0.3V to 35V
V_{SW} ..... -0.6V (-5V <10ns) to V_{IN} + 0.3V (38V <10ns)
V_{BST} ..... V_{SW} + 6V
All other pins ..... -0.3V to 6V (2)
Continuous power dissipation (T_A = +25°C) (3)
QFN-8 (3mmx3mm) 2.27W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to 150°C

Recommended Operating Conditions (4)

Continuous supply voltage (V_{IN}) ..... 4V to 28V
Output voltage (V_{OUT}) ..... 0.8V to V_{IN} * D_{MAX}
Operating junction temp (T_J) ..... -40°C to +125°C

Thermal Resistance (5) θ_{JA} θ_{JC}

QFN-8 (3mmx3mm)	55	13 ... °C/W

NOTES:

1) Absolute maximum ratings are rated under room temperature unless otherwise noted. Exceeding these ratings may damage the device.
2) For details on EN/SYNC's ABS MAX rating, please refer to the EN/SYNC Control section on page 11.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operation condition.
5) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply current (shutdown)	I_{SHDN}	$V_{EN/SYNC}$ = 0V			8	μA
Supply current (quiescent)	I_Q	$V_{EN/SYNC}$ = 2V, V_{FB} = 1V		0.5	0.7	mA
HS switch on resistance	R_{ON_HS}	V_{BST-SW} = 5V		85	105	mΩ
LS switch on resistance	R_{ON_LS}	VCC = 5V		55	75	mΩ
Switch leakage	I_{LKG_SW}	$V_{EN/SYNC}$ = 0V, V_{SW} = 12V			1	μA
Current limit	I_{LIMIT}	Under 40% duty cycle	3.2	4.4	5.5	A
Oscillator frequency	f_{SW}	V_{FB} = 750mV	320	410	500	kHz
Foldback frequency	f_{FB}	V_{FB} < 400mV	70	100	130	kHz
Maximum duty cycle	D_{MAX}	V_{FB} = 750mV, 410kHz	92	95		%
Minimum on time (6)	t_{ON_MIN}			70		ns
Sync frequency range	f_{SYNC}		0.2		2.4	MHz
Feedback voltage	V_{FB}		778	792	806	mV
Feedback current	I_{FB}	V_{FB} = 820mV		10	100	nA
EN/SYNC rising threshold	V_{EN_RISING}		1.15	1.4	1.65	V
EN/SYNC falling threshold	$V_{EN\_FALLING}$		1.05	1.25	1.45	V
EN/SYNC threshold hysteresis	V_{EN_HYS}			150		mV
EN/SYNC input current	I_{EN}	$V_{EN/SYNC}$ = 2V		4	6	μA
		$V_{EN/SYNC}$ = 0V		0	0.2	μA
IN under-voltage lockout threshold rising	$INUV_{RISING}$		3.3	3.5	3.7	V
IN under-voltage lockout threshold falling	$INUV_{FALLING}$		3.1	3.3	3.5	V
IN under-voltage lockout threshold hysteresis	$INUV_{HYS}$			200		mV
VCC regulator	V_{CC}	I_{CC} = 0mA	4.6	4.9	5.2	V
VCC load regulation		I_{CC} = 5mA		1.5	4	%
Soft-start period	t_{SS}	V_{OUT} from 10% to 90%	0.45	1. 5	2.55	ms
Thermal shutdown (6)	T_{SD}		150	170		°C
Thermal hysteresis (6)	T_{SD_HYS}			30		°C
PG rising threshold	PG_{Vth_RISING}	As a percentage of V_{FB}	86	90	94	%
PG falling threshold	$PG_{Vth\_FALLING}$	As a percentage of V_{FB}	80	84	88	%
PG threshold hysteresis	PG_{Vth_HYS}	As a percentage of V_{FB}		6		%
PG rising delay	PG_{Td_RISING}		40	90	160	μs
PG falling delay	$PG_{Td\_FALLING}$		30	55	95	μs
PG sink current capability	V_{PG}	Sink 4mA		0.1	0.3	V
PG leakage current	I_{LKG_PG}			10	100	nA

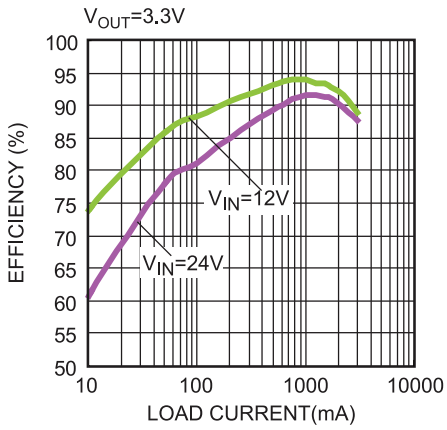
NOTE:

6) Derived from bench characterization. Not tested in production.

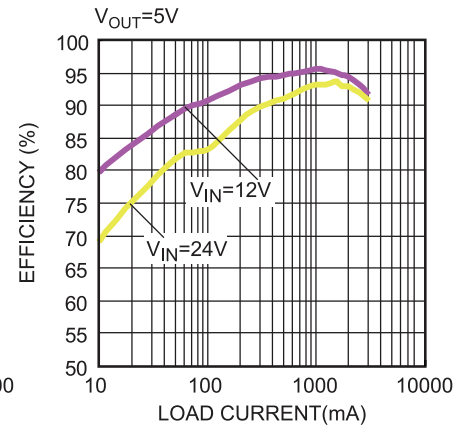
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 3.3V, L = 10µH, R_{BST} = 20Ω, T_A = +25°C, unless otherwise noted.

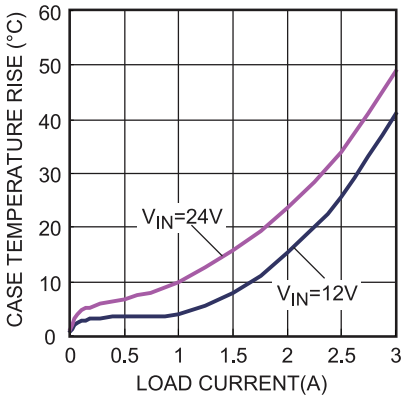
Efficiency vs. Load Current



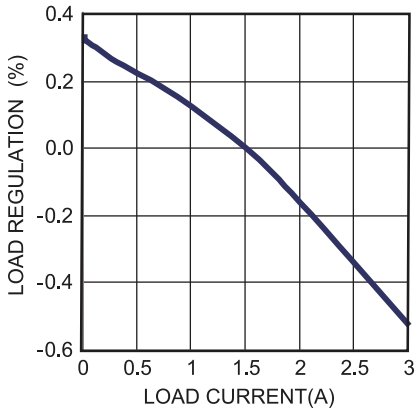
Efficiency vs. Load Current



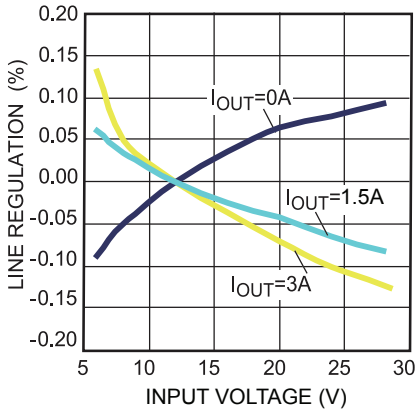
Thermal Rise



Load Regulation



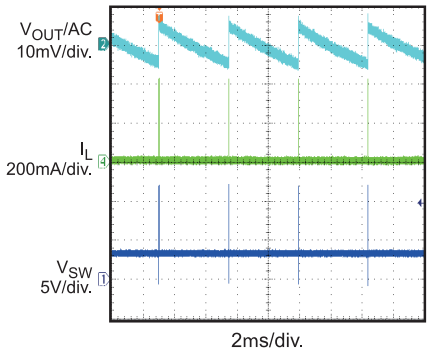
Line Regulation



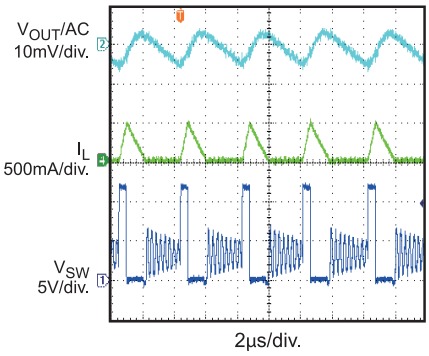
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 10µH, R_{BST} = 20Ω, T_A = +25°C, unless otherwise noted.

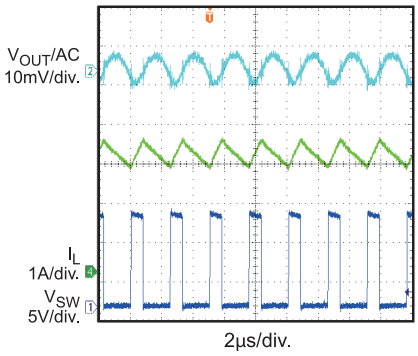
Steady State
I_{OUT}=0A



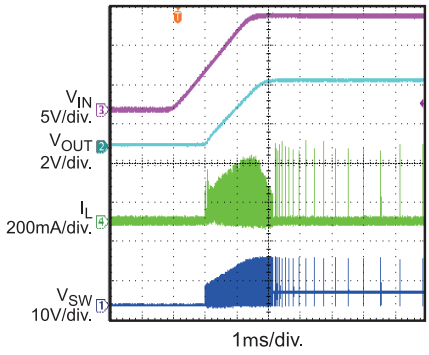
Steady State
I_{OUT} = 0.1A



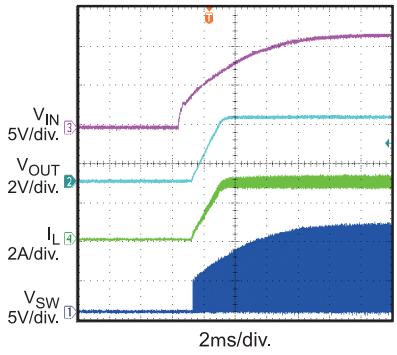
Steady State
I_{OUT}=3A



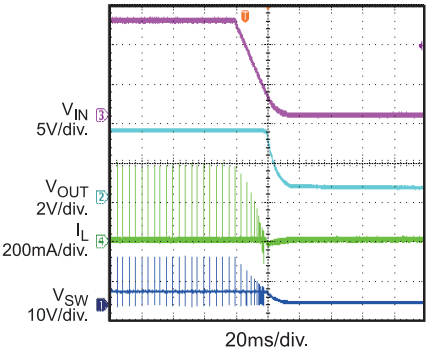
Start-Up through V_{IN}
I_{OUT}=0A



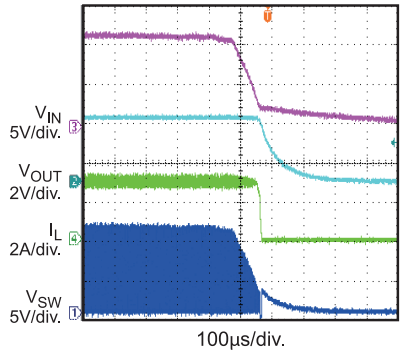
Start-Up through V_{IN}
I_{OUT}=3A



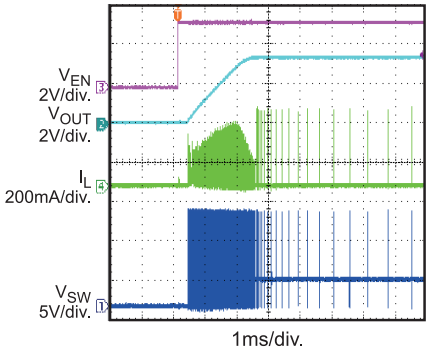
Shutdown through V_{IN}
I_{OUT}=0A



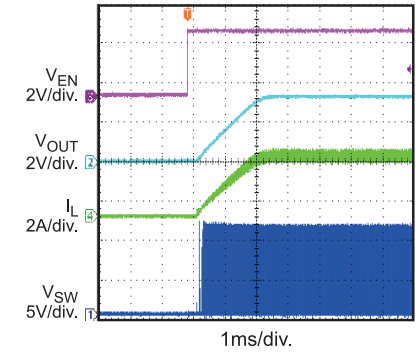
Shutdown through V_{IN}
I_{OUT}=3A



Start-Up through EN/SYNC
I_{OUT}=0A



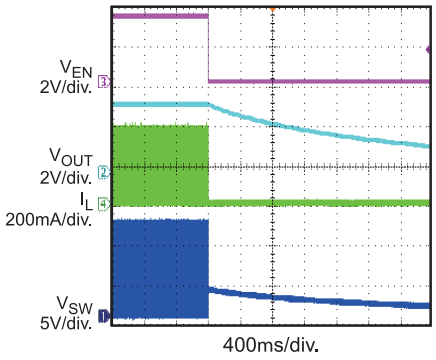
Start-Up through EN/SYNC
I_{OUT}=3A



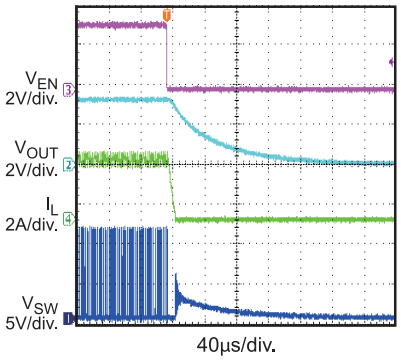
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 10µH, R_{BST} = 20Ω, T_A = +25°C, unless otherwise noted.

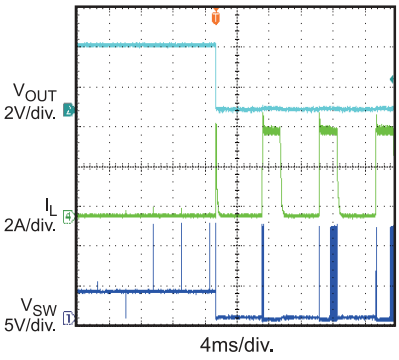
Shutdown through EN
I_{OUT}=0A



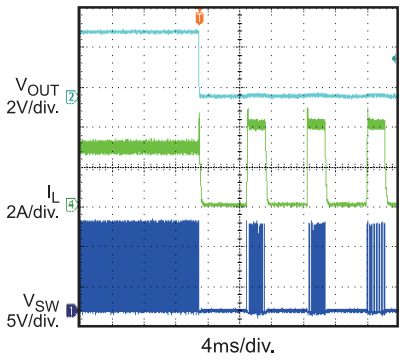
Shutdown through EN
I_{OUT}=3A



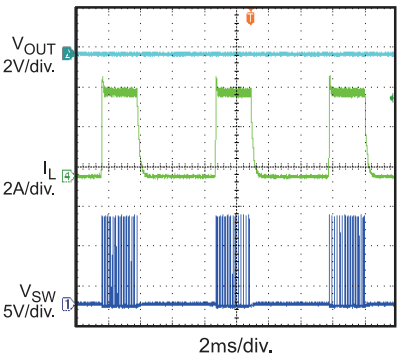
SCP Entry
I_{OUT}=0A to Short Circuit



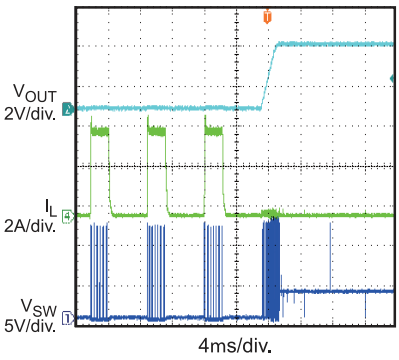
SCP Entry
I_{OUT}=3A to Short Circuit



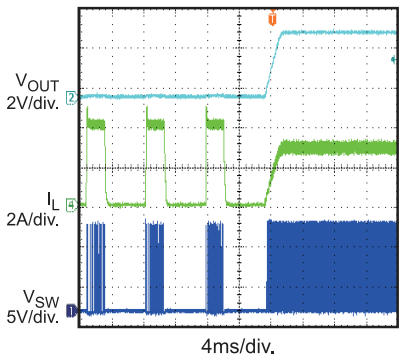
SCP Steady State



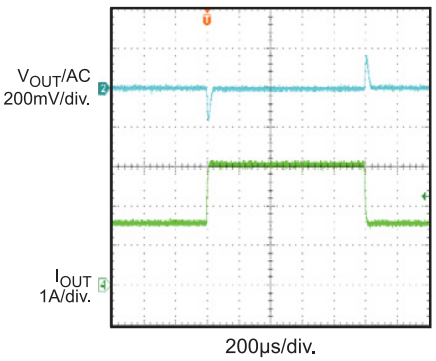
SCP Recovery
Short Circuit to I_{OUT}=0A



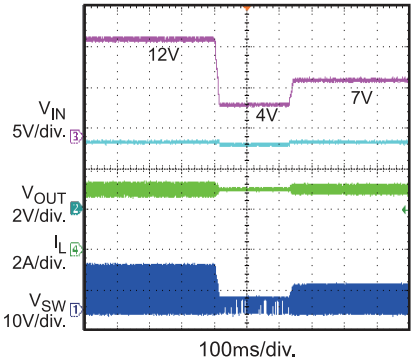
SCP Recovery
Short Circuit to I_{OUT}=3A



Load Transient
I_{OUT}=1.5A<->3A, 1.6A/µs



Cold Crank
V_{OUT}=3.3V, I_{OUT}=3A

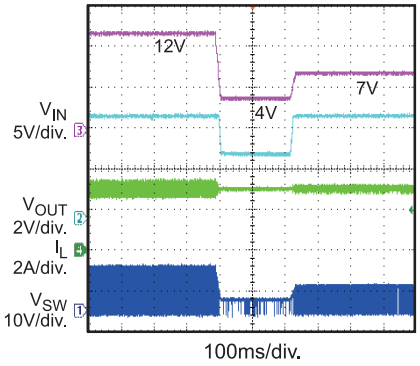


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 10µH, R_{BST} = 20Ω, T_A = +25°C, unless otherwise noted.

Cold Crank

V_{OUT}=5V, I_{OUT}=3A



PIN FUNCTIONS

Package Pin #	Name	Description
1	FB	**Feedback.** Connect FB to the tap of an external resistor divider from the output to GND to set the output voltage. The frequency foldback comparator lowers the oscillator frequency when the FB voltage is below 660mV to prevent current limit runaway during a short-circuit fault condition.
2	VCC	**Bias supply.** Decouple VCC with a 0.1 - 0.22μF capacitor.
3	EN/SYNC	**Enable/synchronize.** Drive EN/SYNC high to enable the MP2395. Apply an external clock to EN/SYNC to change the switching frequency.
4	BST	**Bootstrap.** Connect a capacitor between SW and BST to form a floating supply across the high-side switch driver. A 20Ω resistor placed between the SW and BST cap is strongly recommended to reduce SW voltage spikes.
5	GND	**System ground.** GND is the reference ground of the regulated output voltage and requires special care during the PCB layout. For best results, connect GND with copper traces and vias.
6	SW	**Switch output.** Connect SW with a wide PCB trace.
7	IN	**Supply voltage input.** The MP2395 operates from a 4V to 28V input rail. A capacitor (C1) is required to decouple the input rail. Connect IN using a wide PCB trace.
8	PG	**Power good.** The output of PG is an open drain. PG goes high if the output voltage exceeds 90% of the nominal voltage.

BLOCK DIAGRAM

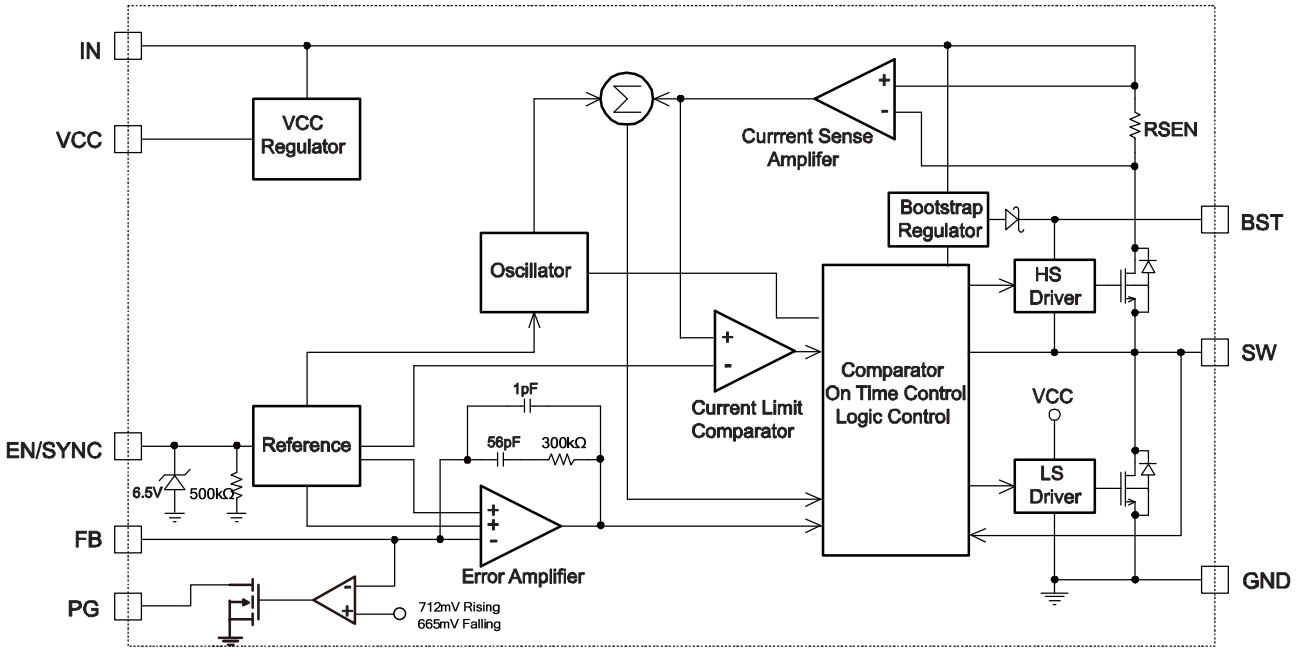


Figure 1: Functional Block Diagram

OPERATION

The MP2395 is a high-frequency, synchronous, rectified, step-down, switch-mode converter with built-in power MOSFETs. The MP2395 offers a very compact solution that achieves 3A of peak output current with excellent load and line regulation over a wide input supply range.

The MP2395 operates in a fixed-frequency, peak-current-control mode to regulate the output voltage. An internal clock initiates a pulse-width modulation (PWM) cycle. The integrated high-side power MOSFET (HS-FET) turns on and remains on until its current reaches the value set by the COMP voltage (V_{COMP}). When the power switch is off, it remains off until the next clock cycle begins. If the current in the power MOSFET does not reach the current value set by COMP within 95% of one PWM period, the power MOSFET is forced off.

Internal Regulator

The 5V internal regulator powers most of the internal circuitries. This regulator is supplied by the V_{IN} input and operates in the full V_{IN} range. When V_{IN} exceeds 5.0V, the output of the regulator is in full regulation. When V_{IN} falls below 5.0V, the output of the regulator decreases following V_{IN}. A 0.1μF decoupling ceramic capacitor is needed at VCC.

Error Amplifier (EA)

The error amplifier compares the FB voltage (V_{FB}) against the internal 0.8V reference and outputs a V_{COMP} value. This V_{COMP} controls the power MOSFET current. The optimized internal compensation network minimizes the external component count and simplifies the control loop design.

Power-Save Mode (PSM) for Light-Load Condition

The MP2395 has an advanced asynchronous mode (AAM) power-save mode (PSM) for light-load conditions (see Figure 2). The AAM threshold is fixed internally. Under heavy-load conditions, V_{COMP} is higher than the AAM voltage (V_{AAM}). When the clock goes high, the HS-FET turns on and remains on until $V_{ILsense}$ reaches the value set by V_{COMP}. The internal clock resets whenever V_{COMP} is higher than V_{AAM}. Under light-load conditions, the value of V_{COMP} is low. When V_{COMP} is less than V_{AAM} and V_{FB} is less than V_{REF}, V_{COMP} ramps up until it exceeds V_{AAM}. During this time, the internal clock is blocked, making the MP2395 skip some pulses for pulse-frequency modulation (PFM) mode, achieving light-load power save.

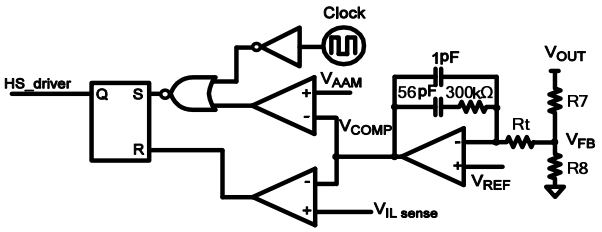


Figure 2: Simplified AAM Control Logic

Enable/Synchronize (EN/SYNC) Control

EN/SYNC is a digital control pin that turns the regulator on and off. Drive EN/SYNC high to turn on the regulator. Drive EN/SYNC low to turn off the regulator. An internal 500kΩ resistor from EN/SYNC to GND allows EN/SYNC to be floated to shut down the chip.

EN/SYNC is clamped internally using a 6.5V series Zener diode (see Figure 3). Connect the EN/SYNC input through a pull-up resistor to any voltage connected to V_{IN}. The pull-up resistor limits the EN/SYNC input current to less than 150μA. For example, with 12V connected to V_{IN}, $R_{PULLUP} \geq (12V - 6.5V) \div 150\mu A = 36.7k\Omega$.

Connecting EN/SYNC directly to a voltage source without a pull-up resistor requires limiting the voltage amplitude to ≤6V to prevent damage to the Zener diode.

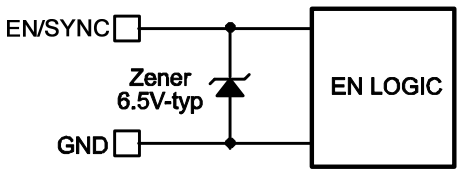


Figure 3: 6.5V Type Zener Diode

Connect a 200kHz to 2.2MHz external clock to EN/SYNC 2ms after the output voltage is set to synchronize the internal clock rising edge to the external clock rising edge. The pulse width of external clock signal should be less than 2μs.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The MP2395 UVLO comparator monitors the output voltage of the internal regulator (VCC). The UVLO rising threshold is about 3.5V, while its falling threshold is 3.3V.

Internal Soft Start (SS)

Soft start prevents the converter output voltage from overshooting during start-up. When the chip starts up, the internal circuitry generates a soft-start voltage (SS) that ramps up from 0V to 1.2V. When SS is lower than REF, SS overrides REF, so the error amplifier uses SS as the reference. When SS exceeds REF, the error amplifier uses REF as the reference. The SS time is set to 1.5ms internally.

Over-Current Protection (OCP) and Hiccup

The MP2395 has a cycle-by-cycle over-current limit when the inductor current peak value exceeds the set current limit threshold. If the output voltage starts to drop until FB is below the under-voltage (UV) threshold (typically 84% below the reference), the MP2395 enters hiccup mode to restart the part periodically. This protection mode is especially useful when the output is dead-shorted to ground. The average short-circuit current is reduced greatly to alleviate thermal issues and protect the regulator. The MP2395 exits hiccup mode once the over-current condition is removed.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 170°C, the entire chip shuts down. When the temperature drops below its lower threshold (typically 140°C), the chip is enabled again.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. A dedicated internal regulator charges and regulates the bootstrap capacitor voltage to ~5V (see Figure 4). When the voltage between the BST and SW nodes drops below the regulation, a PMOS pass transistor connected from V_{IN} to BST turns on. The charging current path is from V_{IN} to BST to SW. The external circuit provides enough voltage headroom to facilitate charging. As long as V_{IN} is higher than SW significantly, the bootstrap capacitor remains charged. When the HS-FET is on, $V_{IN} \approx V_{SW}$, so the bootstrap capacitor cannot be charged. When the LS-FET is on, $V_{IN} - V_{SW}$ reaches its maximum for fast charging. When there is no inductor current, $V_{SW} = V_{OUT}$, so the difference between V_{IN} and V_{OUT} can charge the bootstrap capacitor. The floating driver has its own UVLO protection with a rising threshold of 2.2V and hysteresis of 150mV. A 20Ω resistor placed between the SW and BST cap is strongly recommended to reduce SW voltage spikes.

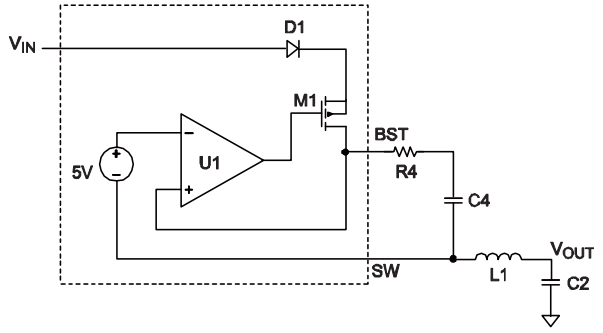


Figure 4: Internal Bootstrap Charging Circuit

Start-Up and Shutdown

If both V_{IN} and EN/SYNC exceed their appropriate thresholds, the chip starts up. The reference block starts first, generating a stable reference voltage and current, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

Three events can shut down the chip: EN/SYNC low, V_{IN} low, and thermal shutdown. In the shutdown procedure, the signaling path is first blocked to avoid any fault triggering. V_{COMP} and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

Power Good (PG)

The MP2395 has a power good (PG) output. PG is the open drain of a MOSFET. Connect PG to VCC or another voltage source through a resistor (e.g.: 100kΩ). In the presence of an input voltage, the MOSFET turns on so that PG is pulled low before SS is ready. After V_{FB} reaches 90% x REF, PG is pulled high after a delay (typically 90μs). When V_{FB} drops to 84% x REF, PG is pulled low. PG is also pulled low if thermal shutdown or EN/SYNC is pulled low.

APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider sets the output voltage (see the Typical Application on page 1). Choose R7 to be around 41.2kΩ. Then calculate R8 with Equation (1):

$$R8 = \frac{R7}{\frac{V_{OUT}}{0.792V} - 1} \quad (1)$$

A T-type network is highly recommended when V_{OUT} is low (see Figure 5).

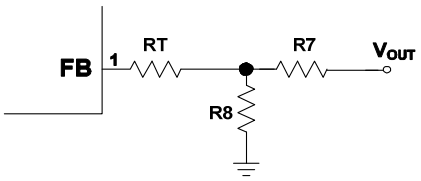


Figure 5: T-Type Network

RT + R7 is used to set the loop bandwidth. The higher RT + R7 is, the lower the bandwidth will be. To ensure loop stability, it is strongly recommended to limit the bandwidth below 40kHz based on the 410kHz default f_{SW}. Table 1 lists the recommended T-type resistor values for common output voltages.

Table 1: Resistor Selection for Common Output Voltages (7)

V_{OUT} (V)	R7 (kΩ)	R8 (kΩ)	RT (kΩ)
3.3	41.2 (1%)	13 (1%)	51 (1%)
5	41.2 (1%)	7.68 (1%)	51 (1%)

NOTES:

7) The recommended parameters are based on a 410kHz switching frequency. A different input voltage, output inductor value, or output capacitor value may affect the selection of R7, R8, and RT. For other components' parameters, please refer to the Typical Application Circuits on page 17.

Selecting the Inductor

Use a 1μH to 10μH inductor with a DC current rating at least 25% higher than the maximum load current for most applications. For the highest efficiency, use an inductor with a small DC resistance. For most designs, the inductance value can be derived from Equation (2):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (2)$$

Where ΔI_L is the inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation (3):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (3)$$

Use a larger inductor for improved efficiency under light-load conditions below 100mA.

V_{IN} UVLO Setting

The MP2395 has an internal, fixed, UVLO threshold. The rising threshold is 3.5V, while the falling threshold is about 3.3V. For applications that require a higher UVLO point, an external resistor divider between EN/SYNC and V_{IN} can be used to achieve a higher equivalent UVLO threshold (see Figure 6).

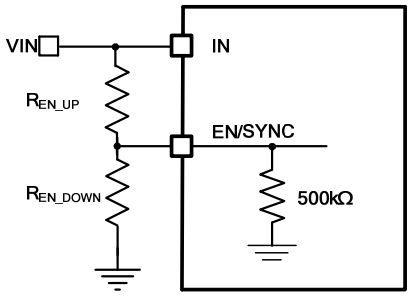


Figure 6: Adjustable UVLO using EN/SYNC Divider

The UVLO threshold can be calculated with Equation (4) and Equation (5):

$$INUV_{RISING} = (1 + \frac{R_{EN\_UP}}{500k // R_{EN\_DOWN}}) \times V_{EN\_RISING} \quad (4)$$

$$INUV_{FALLING} = (1 + \frac{R_{EN\_UP}}{500k // R_{EN\_DOWN}}) \times V_{EN\_FALLING} \quad (5)$$

Where V_{EN_RISING} is 1.4V, and $V_{EN\_FALLING}$ is 1.25V.

When choosing R_{EN_UP}, ensure that it is large enough to limit the current flowing into EN/SYNC below 150μA.

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are recommended because of their low ESR and small temperature coefficients.

For most applications, a 22µF ceramic capacitor is sufficient for maintaining the DC input voltage. It is strongly recommended to use another lower-value capacitor (e.g.: 1µF) with a small package size (0603) to absorb high frequency switching noise. Place the smaller capacitor as close to IN and GND as possible (see the PCB Layout Guidelines section on page 16).

Since C1 absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (6):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (6)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (7):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (7)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g.: 1µF) placed as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple caused by the capacitance can be estimated with Equation (8):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (8)$$

Selecting the Output Capacitor

The output capacitor (C2) maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right) \quad (9)$$

Where L_1 is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes the majority of the output voltage ripple. For simplification, estimate the output voltage ripple with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (10)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (11)$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MP2395 can be optimized for a wide range of capacitance and ESR values.

BST Resistor and External BST Diode

A 20Ω resistor in series with a BST capacitor is recommended to reduce SW voltage spikes. A higher resistance is better for SW spike reduction but compromises efficiency. The BST voltage may become insufficient at some particular specs. In this case, an external bootstrap diode can enhance the efficiency of the regulator and avoid BST voltage insufficiency at light-load PFM operation. BST voltage insufficiency is more likely to occur under either of the following conditions:

- V_{IN} is below 5V
- V_{OUT} is 5V or 3.3V
- Duty cycle is high: $D = \frac{V_{OUT}}{V_{IN}} > 65\%$

In these cases, if the BST voltage becomes insufficient, the output ripple voltage may become extremely large in light-load condition. Add an external BST diode from VCC or V_{OUT} to BST (see Figure 7).

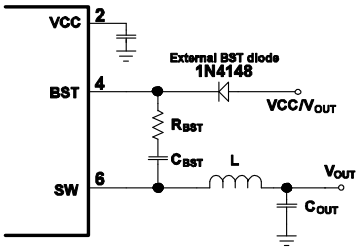


Figure 7: Optional External Bootstrap Diode to Enhance Efficiency

The recommended external BST diode is 1N4148, and the recommended BST capacitor value is 0.1µF to 1µF.

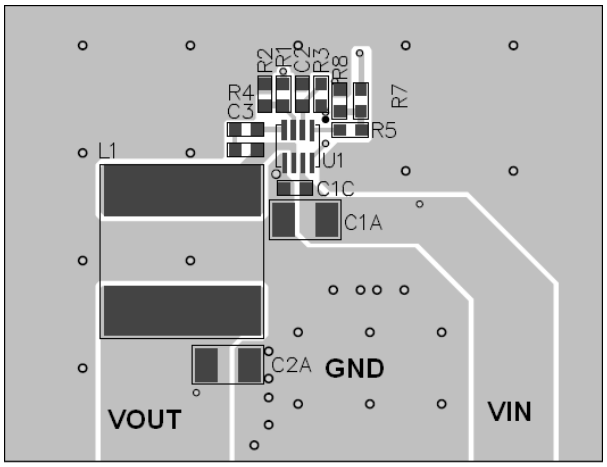
PCB Layout Guidelines (8)

Efficient PCB layout is critical for stable operation, especially for the input capacitor and VCC capacitor placement. For best results, refer to Figure 8 and follow the guidelines below.

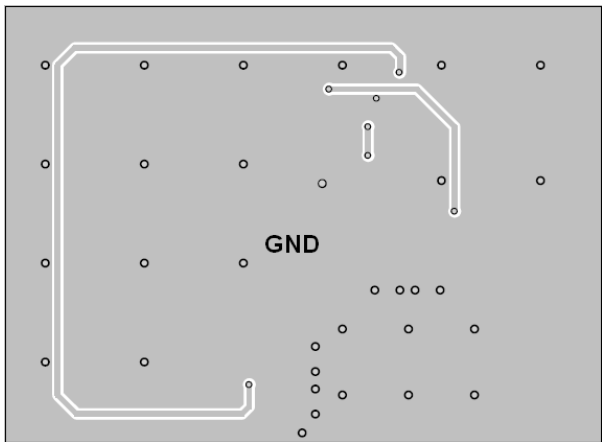
1) Place the ceramic input capacitor, especially the small package size (0603) input bypass capacitor, as close to IN and GND as possible.
2) Keep the connection of the input capacitor and IN as short and wide as possible.
3) Place the VCC capacitor as close to VCC and GND as possible.
4) Make the trace length of VCC to the VCC capacitor anode to the VCC capacitor cathode to GND as short as possible.
5) Connect GND to a large ground plane directly.
6) Add vias near GND if the bottom layer is a ground plane.
7) Route SW and BST away from sensitive analog areas, such as FB.
8) Place the T-type feedback resistor close to the chip to ensure that the trace connecting FB is as short as possible.

NOTE:

8) The recommended layout is based on the F9 Typical Application Circuits on page 17.



Top Layer



Bottom Layer

Figure 8: Recommended Layout

Design Example

Table 2 is a design example following the application guidelines for the specifications below.

Table 2: Design Example

V_{IN}	12V
V_{OUT}	5V
I_{OUT}	3A Peak

The detailed application schematic is shown in Figure 9 and Figure 10. The typical performance and circuit waveforms are shown in the Typical Performance Characteristics section. For more device applications, please refer to the related evaluation board datasheets.

TYPICAL APPLICATION CIRCUITS

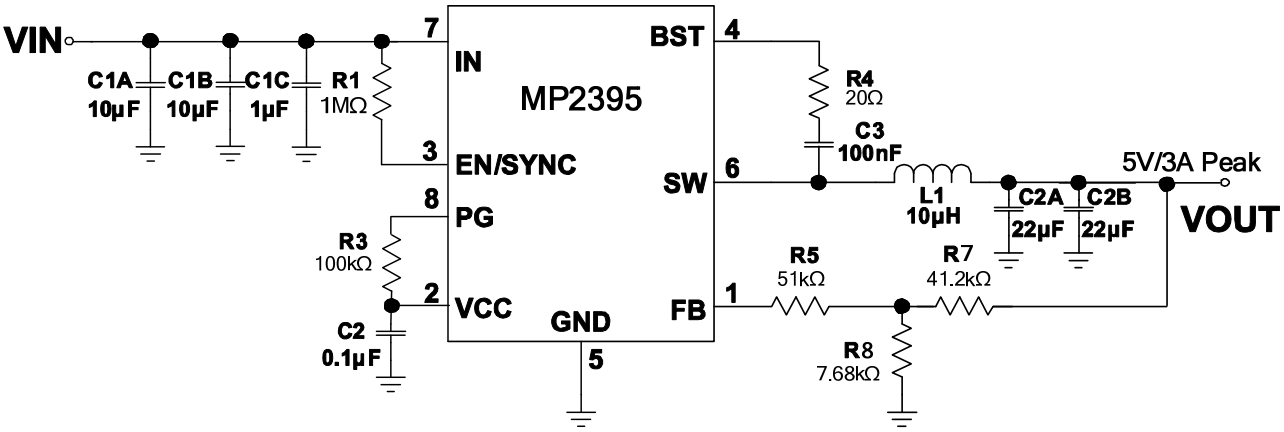


Figure 9: 12V$_{IN}$, 5V/3A Peak Output

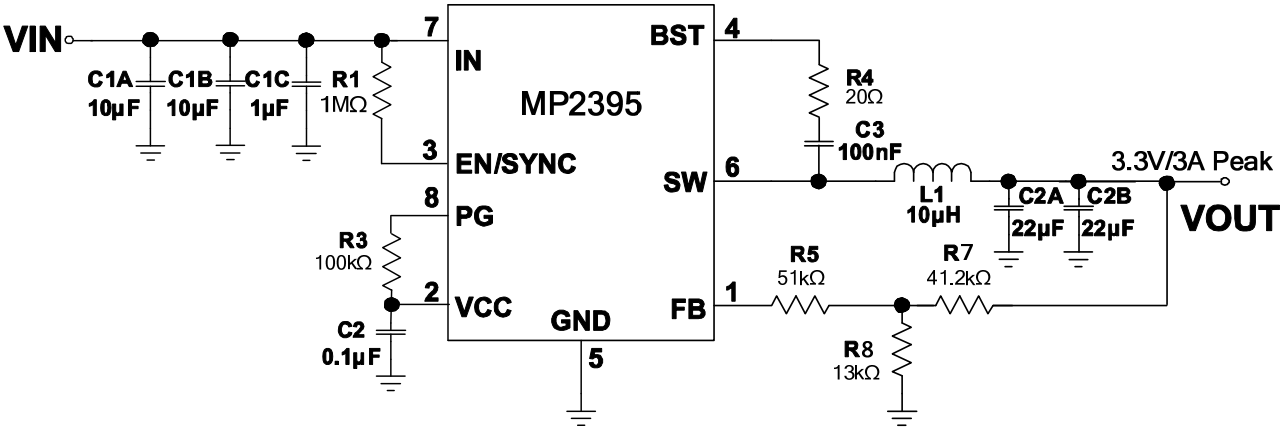
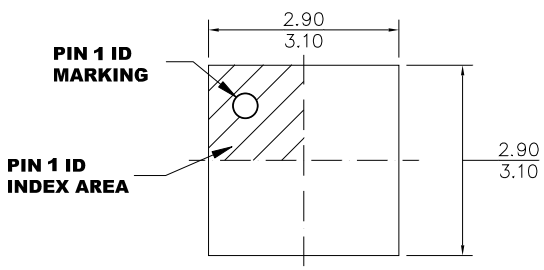
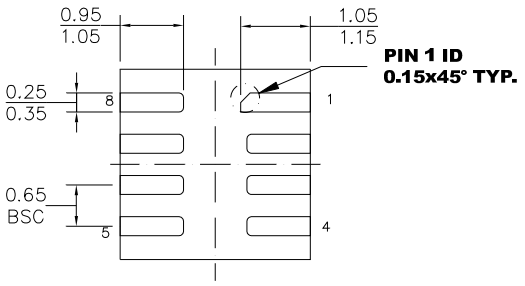


Figure 10: 12V$_{IN}$, 3.3V/3A Peak Output

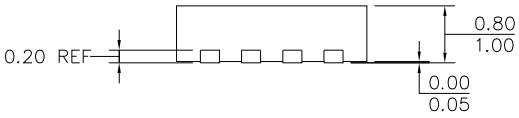
PACKAGE INFORMATION

QFN-8 (3mmx3mm)

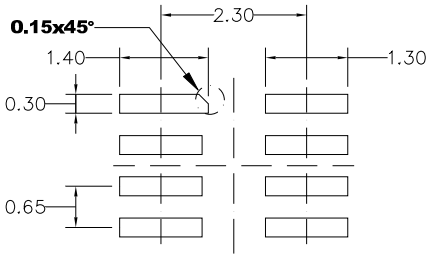




TOP VIEW **BOTTOM VIEW**



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.