MP2349

24V, 6.5A, Low-I_Q, Synchronous Buck Converter with Mode Selection

DESCRIPTION

The MP2349 is a fully integrated, high-frequency, synchronous, rectified, step-down switch-mode converter. It offers a very compact solution to achieve up to 6.5A of continuous output current (I_{OUT}) and 7.5A of peak output current (I_{OUT_MAX}) across a wide input voltage (V_{IN}) range.

The MP2349 operates at high efficiency across a wide I_{OUT} load range based on MPS's proprietary switching loss reduction technology and internal, low on resistance ($R_{DS(ON)}$) power MOSFETs.

Adaptive constant-on-time (COT) control provides fast transient response and eases loop stabilization. The DC auto-tune loop combined with the remote differential sense provides good load and line regulation.

Full protection features include over-current protection (OCP), over-voltage protection (OVP), under-voltage protection (UVP), and thermal shutdown.

The MP2349 requires a minimal number of external components, and is available in a QFN-11 (2mmx2mm) package.

FEATURES

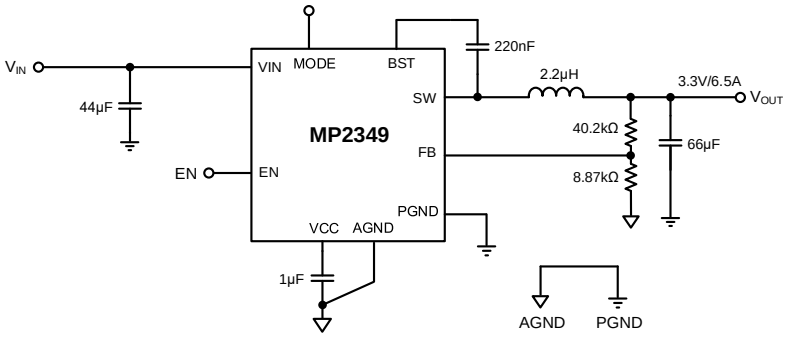
- Wide 4.5V to 24V Operating Input Voltage (V_{IN}) Range
- 105μA Low Quiescent Current (I_Q)
- 6.5A Continuous Output Current (I_{OUT})
- 7.5A Peak Output Current (I_{OUT_MAX})
- Adaptive Constant-On-Time (COT) for Fast Transient Response
- DC Auto-Tune Loop
- Low On Resistance ($R_{DS(ON)}$) Internal Power MOSFETs
- Proprietary Switching Loss Reduction Technology
- Selectable Forced Continuous Conduction Mode (FCCM), Automatic Pulse-Frequency Modulation (PFM)/Pulse-Width Modulation (PWM) Mode, and Ultrasonic Mode (USM)
- Fixed 700kHz Switching Frequency (f_{SW})
- Stable with POSCAP and Ceramic Capacitors
- Internal Soft Start (SS)
- Output Discharge
- Over-Current Protection (OCP), Over-Voltage Protection (OVP), Under-Voltage Protection (UVP), and Thermal Shutdown with Automatic Retry
- Available in a QFN-11 (2mmx2mm) Package

MPL Optimized Performance with MPS Inductor MPL-AL6050 and MPL-AL4020 Series

APPLICATIONS

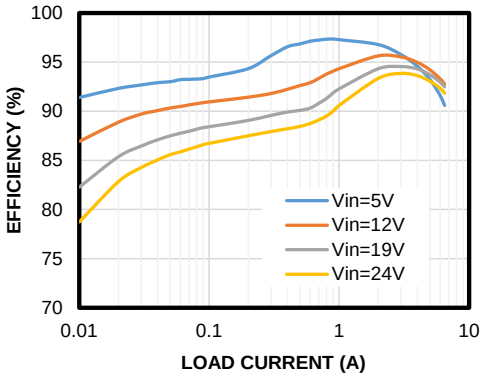
- Security Cameras
- Portable Devices and xDSL Devices
- Digital Set-Top Boxes
- Flat-Panel Televisions and Monitors
- General-Purpose Power Supplies

TYPICAL APPLICATION



Efficiency vs. Load Current

V_{OUT} = 3.3V, L = 2.2µH, DCR = 3mΩ, PFM mode without USM



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP2349GG	QFN-11 (2mmx2mm)	*See Below*	1

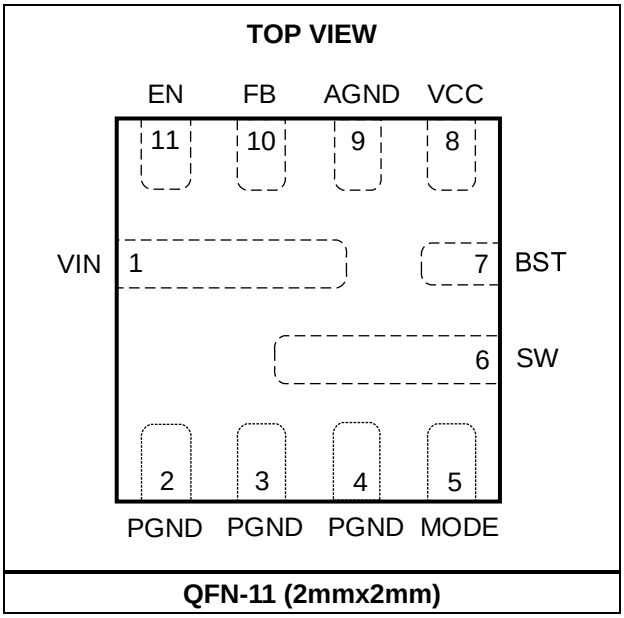
* For Tape & Reel, add suffix -Z (e.g. MP2349GG-Z).

TOP MARKING

JCY
LLL

JC: Product code of MP2349GG
Y: Year code
LLL: Lot number

PACKAGE REFERENCE



QFN-11 (2mmx2mm)

PIN FUNCTIONS

Pin #	Name	Description
1	VIN	**Supply voltage.** The VIN pin supplies power for the internal MOSFET and regulator. The MP2349 operates from a 4.5V to 24V input rail. An input capacitor (C_{IN}) is required to decouple the input rail, using wide PCB traces and multiple vias. Apply a minimum of two layers for this input trace.
2, 3, 4	PGND	**Power ground.** Connect the PGND pin to the PCB's ground layer using wide PCB traces and multiple vias.
5	MODE	**Ultrasonic mode (USM), pulse-frequency modulation (PFM) mode, forced continuous conduction mode (FCCM) selection.** Pull the MODE pin above 3.2V to operate in FCCM. Float MODE to operate in PFM mode with USM at light loads. Connect MODE to ground to operate in PFM mode without USM.
6	SW	**Switch output.** Connect the SW pin to the inductor and bootstrap (BST) capacitor using short, wide PCB traces. If the high-side MOSFET (HS-FET) is on during the pulse-width modulation (PWM) duty cycle, then pull SW to the input voltage (V_{IN}). If the HS-FET is off during the PWM duty cycle, then the inductor current (I_L) pulls SW to a negative voltage. The on resistance ($R_{DS(ON)}$) of the low-side MOSFET (LS-FET) and the internal diode fixes the negative voltage.
7	BST	**Bootstrap.** A capacitor connected between the SW and BST pins is required to form a floating supply across the HS-FET driver.
8	VCC	**Internal VCC low-dropout (LDO) output.** The VCC pin supplies power for the driver and control circuits. Decouple VCC by placing a minimum 1µF ceramic capacitor as close to the pin as possible. X7R or X5R grade dielectric ceramic capacitors are recommended for their stable temperature characteristics.
9	AGND	**Signal logic ground.** The AGND pin provides the Kelvin connection to the PGND pin.
10	FB	**Feedback.** Connect the FB pin to an external resistor divider from the output to AGND (tapped to FB) to set the output voltage (V_{OUT}). Place the resistor divider as close to FB as possible. Avoid placing vias on the FB traces. Keep the V_{OUT} sense trace far away from the SW node.
11	EN	**Buck enable.** The EN pin is a digital input that turns the buck regulator on and off. When the power supply of the control circuit is ready, pull EN high to turn the buck regulator on; pull EN low to turn the regulator off. Connect EN with VIN through a voltage resistor divider for automatic start-up. The EN voltage (V_{EN}) should not exceed 4.5V. Do not float this pin.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) 26V
SW voltage (V_{SW}) (DC) ..... -1V to V_{IN} + 0.3V
V_{SW} (25ns)..... -3.6V to V_{IN} + 4V (2)
BST voltage (V_{BST}) ..... V_{SW} + 4.5V
All other pins .....-0.3V to + 4.5V
Continuous power dissipation (T_A = 25°C) (3) (5)
QFN-11 (2mmx2mm)…….……..……3.6W
Junction temperature (T_J) .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to +150°C

ESD Ratings

Human body model (HBM) 1.8kV
Charged-device model (CDM) 2kV

Recommended Operating Conditions (4)

V_{IN}…….……..……4.5V to 24V
Output voltage (V_{OUT}).....0.6V to 13V
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

EV2349-G-00A (5)	34	9 °C/W
QFN-11 (2mmx2mm) (6)	80	16 °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) Measured by using a differential oscilloscope probe.
3) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can generate an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on the EV2349-G-00A, 4-layer PCB (64mmx64mm).
6) The θ_{JA} value given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7 and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C [7], typical value is tested at T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Current						
Quiescent supply current	I_Q	V_{EN} = 3.3V, V_{FB} = 0.62V		105	145	µA
Shutdown supply current	I_{SD}	V_{EN} = 0V			2	µA
MOSFETs						
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)\_HS}$			36		mΩ
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)\_LS}$			12		mΩ
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 0V		0	5	µA
Current Limit						
Low-side (LS) valley current limit	I_{LIMIT_LS}		6	7.5	9	A
Zero-current detection (ZCD) threshold	I_{ZCD}	Pulse-frequency modulation (PFM) mode, V_{OUT} = 3.3V, L = 2.2µH	-50	150	+300	mA
LS sink current limit [8]	$I_{LIMIT\_SINK\_LS}$	Forced continuous conduction mode (FCCM)		-1.5		A
Switching Frequency and Minimum Off Time						
Switching frequency	f_{SW}	FCCM, V_{OUT} = 3.3V, I_{OUT} = 0A	600	700	800	kHz
Minimum on time [8]	t_{ON_MIN}			50		ns
Minimum off time [8]	t_{OFF_MIN}			200		ns
Over-Voltage Protection (OVP) and Under-Voltage Protection (UVP)						
Over-voltage protection (OVP) threshold	V_{OVP}	V_{FB}	125%	130%	135%	% of V_{REF}
Under-voltage protection (UVP) threshold 1	V_{UVP1}	V_{FB}	70%	75%	80%	% of V_{REF}
UVP1 hold-off timer [8]	t_{OC1}	V_{OUT} = 60% of V_{REF}		32		µs
UVP threshold 2	V_{UVP2}	V_{FB}	45%	50%	55%	% of V_{REF}
Reference Voltage and Soft Start (SS)						
Reference voltage	V_{REF}		590	600	610	mV
Soft-start time [8]	t_{SS}		1.1	1.7	2.3	ms
Mode						
FCCM input logic low threshold	V_{MODE_H}		3.2		V_{CC}	V
PFM mode with USM threshold	V_{MODE_MID}		1		2.6	V
PFM mode without USM threshold	V_{MODE_L}		0		0.5	V

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C (7), typical value is tested at T_J = 25°C, the over-temperature (OT) limit is derived by characterization, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Enable (EN) and Under-Voltage Lockout (UVLO)						
EN rising threshold	V_{EN_RISING}		1.15	1.25	1.35	V
EN hysteresis	V_{EN_HYS}			150		mV
EN input current	I_{EN}	V_{EN} = 3.3V		3.3		µA
V_{CC} under-voltage lockout (UVLO) rising threshold	$V_{CC\_VTH\_R}$		3.1	3.3	3.5	V
V_{CC} UVLO hysteresis	V_{CC_HYS}			420		mV
V_{IN} UVLO rising threshold	$V_{IN\_VTH\_R}$		4.2	4.35	4.48	V
V_{IN} UVLO threshold hysteresis	V_{IN_HYS}			550		mV
VCC Regulator						
VCC voltage	V_{CC}		3.45	3.65	3.85	V
VCC load regulation	V_{CC_REG}	I_{VCC} = 5mA		5		%
Thermal Protection						
Thermal shutdown (8)	T_{SD}			150		°C
Thermal shutdown hysteresis (8)	T_{SD_HYS}			25		°C

Notes:

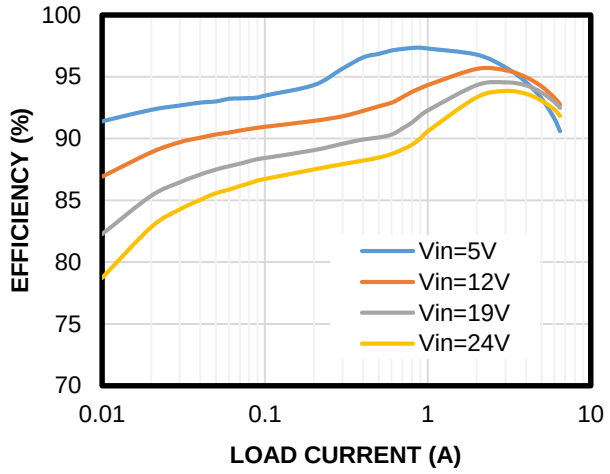
7) Not tested in production. Derived by over-temperature correlation.
8) Derived by sample characterization. Not tested in production.

TYPICAL CHARACTERISTICS

V_{IN} = 19V, V_{OUT} = 3.3V, L = 2.2µH, T_A = 25°C, PFM mode without USM, unless otherwise noted.

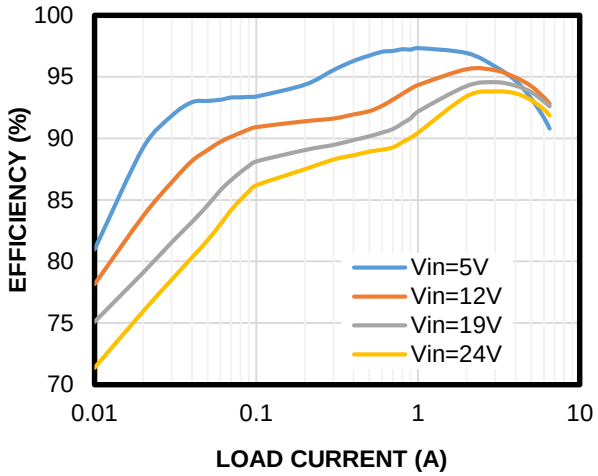
Efficiency

PFM mode without USM, DCR = 3mΩ



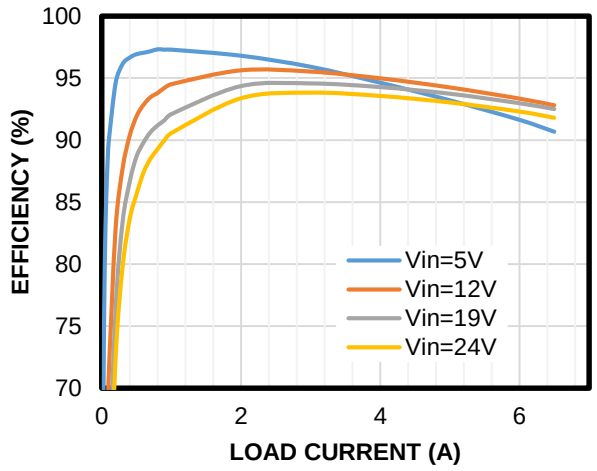
Efficiency

USM, DCR = 3mΩ

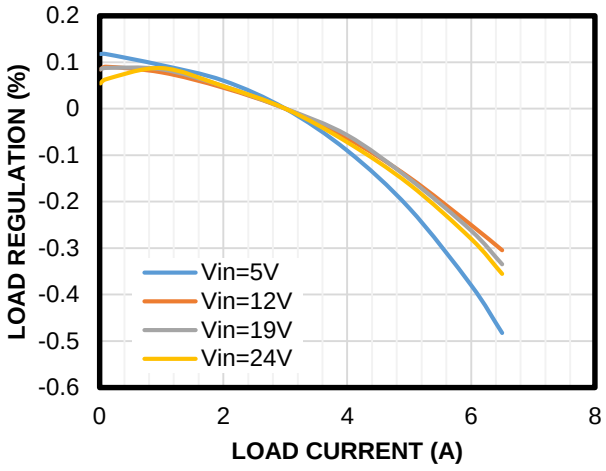


Efficiency

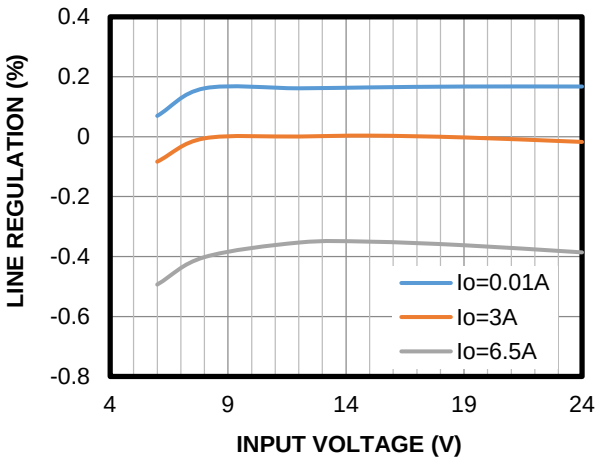
FCCM, DCR = 3mΩ



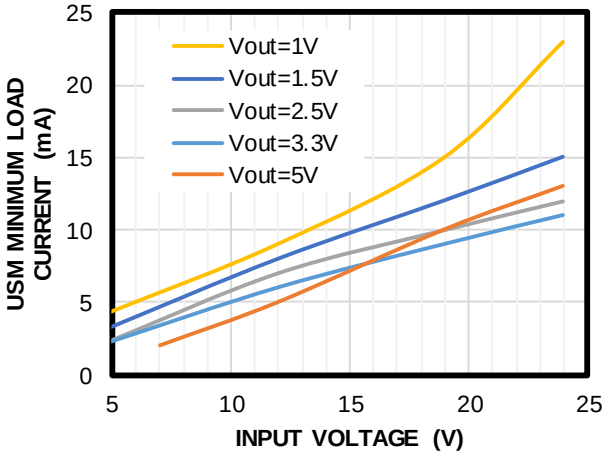
Load Regulation



Line Regulation



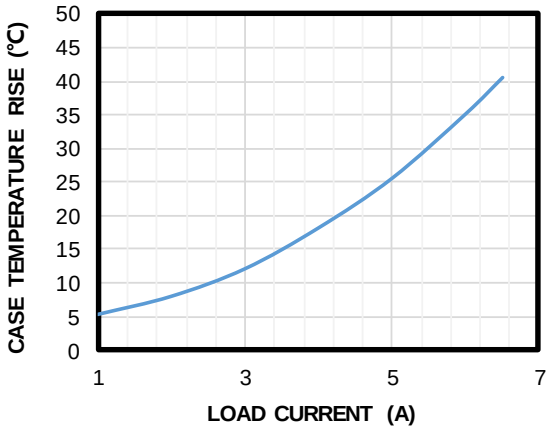
USM Minimum Load Current vs. Input Voltage



TYPICAL CHARACTERISTICS *(continued)*

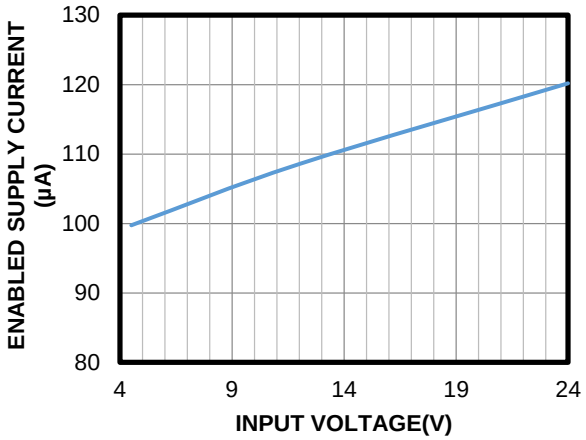
V_{IN} = 19V, V_{OUT} = 3.3V, L = 2.2µH, T_A = 25°C, PFM mode without USM, unless otherwise noted.

Case Temperature Rise vs. Load Current



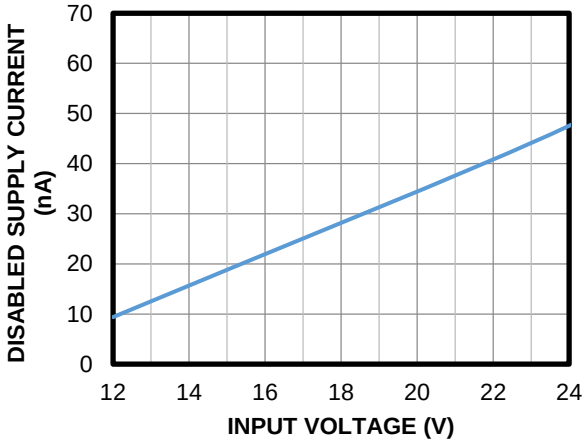
Enabled Supply Current vs. Input Voltage

V_{EN} = 3.3V, V_{FB} = 0.62V

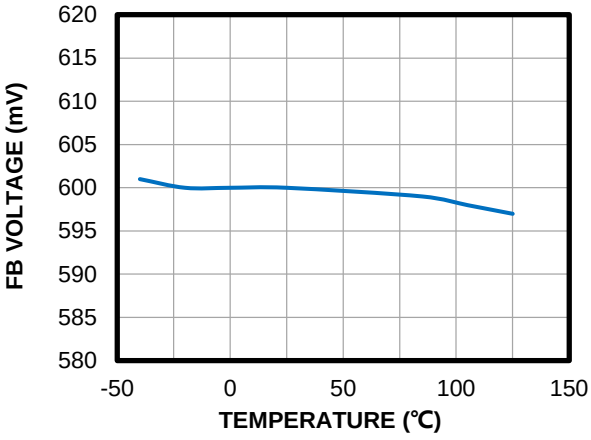


Disabled Supply Current vs. Input Voltage

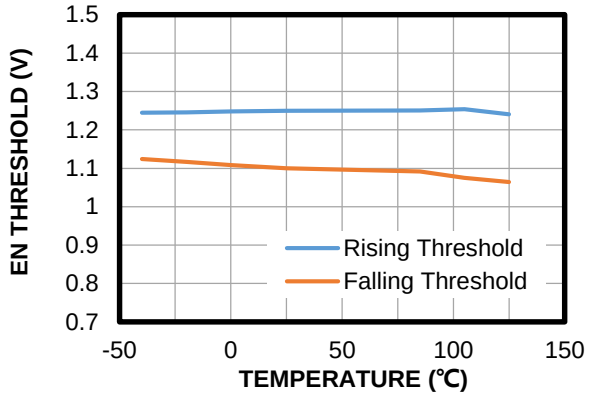
V_{EN} = 0V



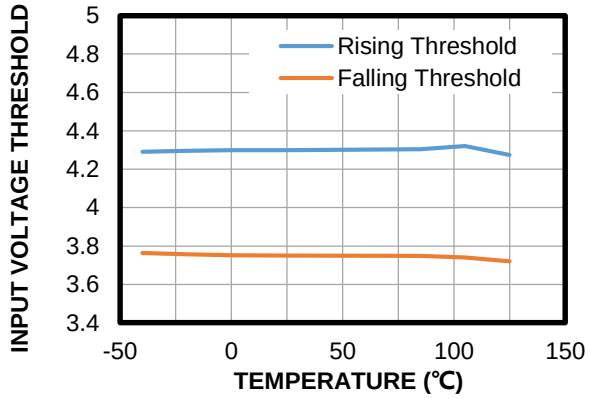
FB Voltage vs. Temperature



EN Threshold vs. Temperature



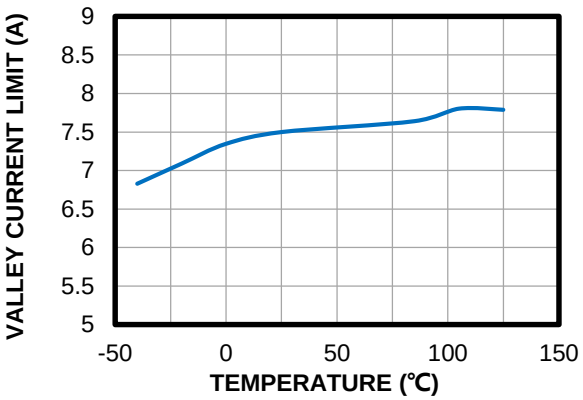
Input Voltage Threshold vs. Temperature



TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 19V, V_{OUT} = 3.3V, L = 2.2µH, T_A = 25°C, PFM mode without USM, unless otherwise noted.

Valley Current Limit vs. Temperature

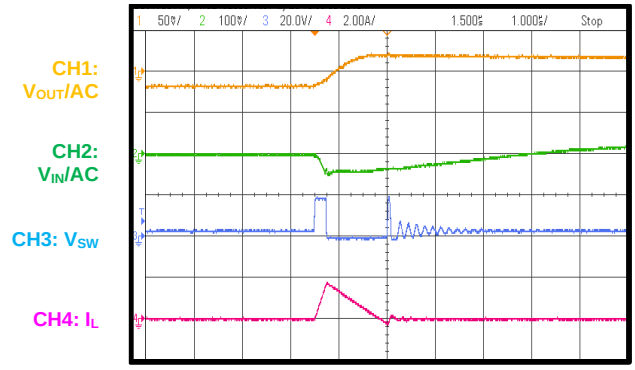


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 19V, V_{OUT} = 3.3V, L = 2.2µH, T_A = 25°C, PFM mode without USM, unless otherwise noted.

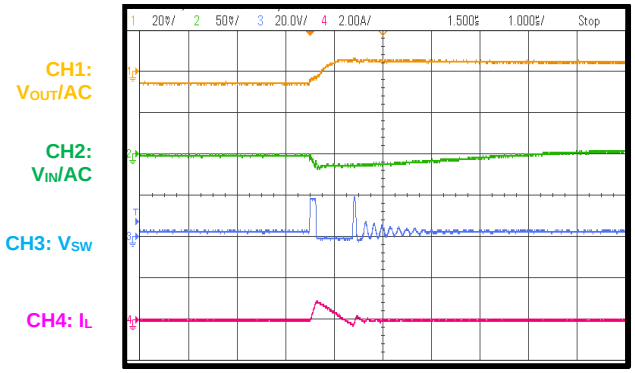
Input and Output Ripple

I_{OUT} = 0A, PFM mode without USM



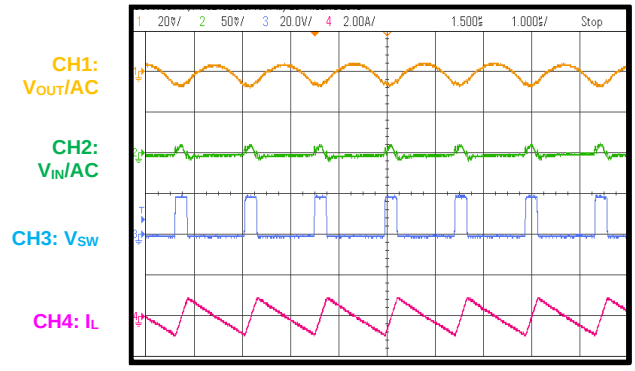
Input and Output Ripple

I_{OUT} = 0A, USM



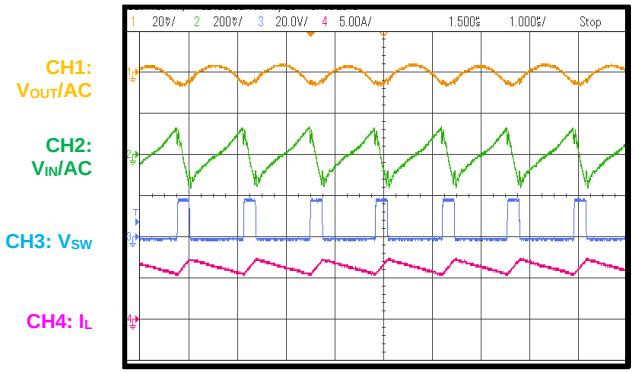
Input and Output Ripple

I_{OUT} = 0A, FCCM



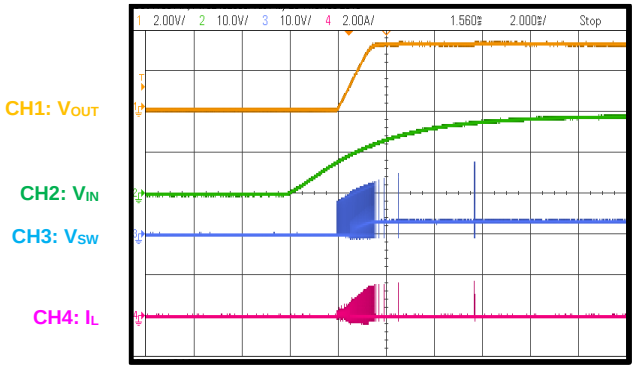
Input and Output Ripple

I_{OUT} = 6.5A



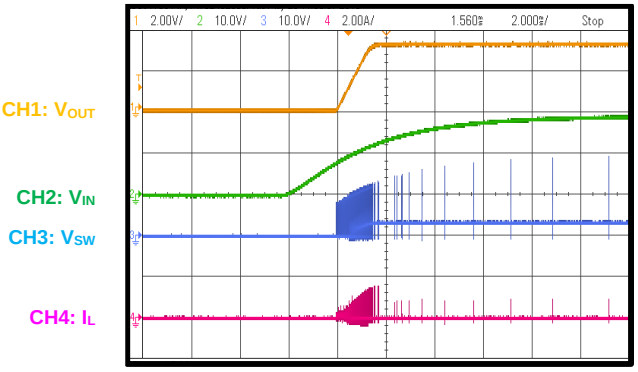
Start-Up through VIN

I_{OUT} = 0A, PFM mode without USM



Start-Up through VIN

I_{OUT} = 0A, USM

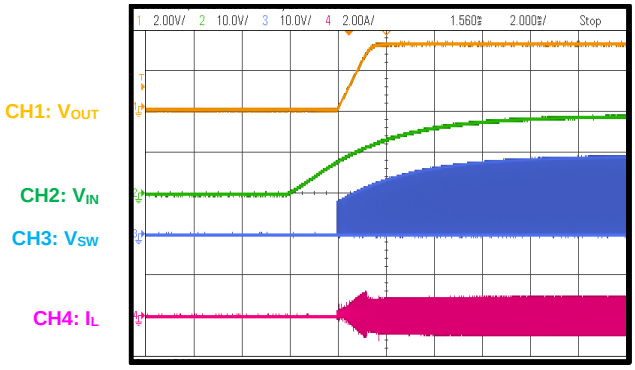


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 19V, V_{OUT} = 3.3V, L = 2.2µH, T_A = 25°C, PFM mode without USM, unless otherwise noted.

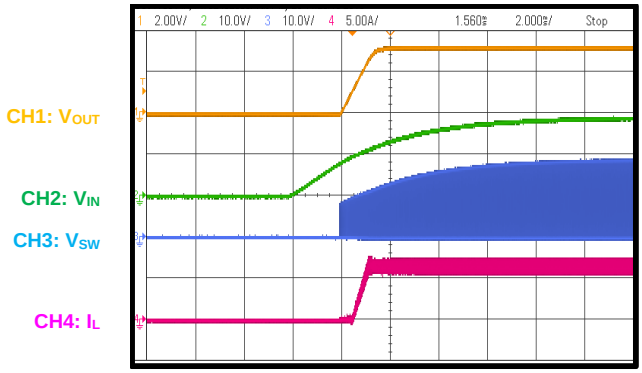
Start-Up through VIN

I_{OUT} = 0A, FCCM



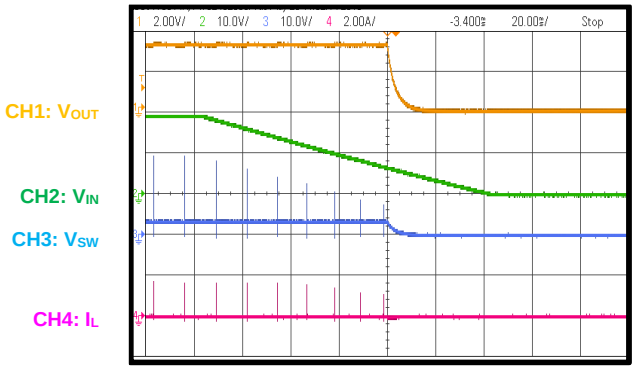
Start-Up through VIN

I_{OUT} = 6.5A



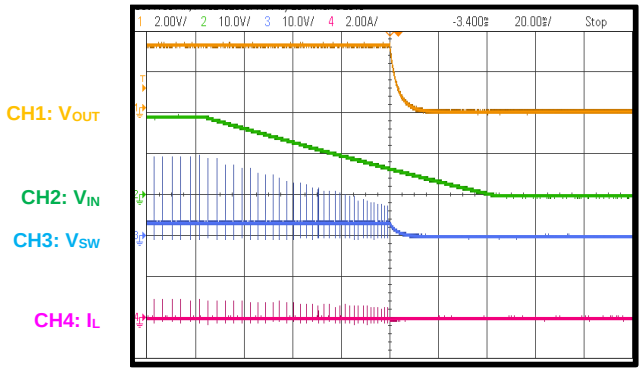
Shutdown through VIN

I_{OUT} = 0A, PFM mode without USM



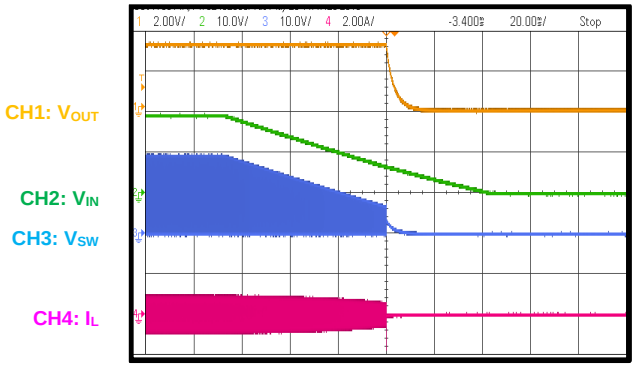
Shutdown through VIN

I_{OUT} = 0A, USM



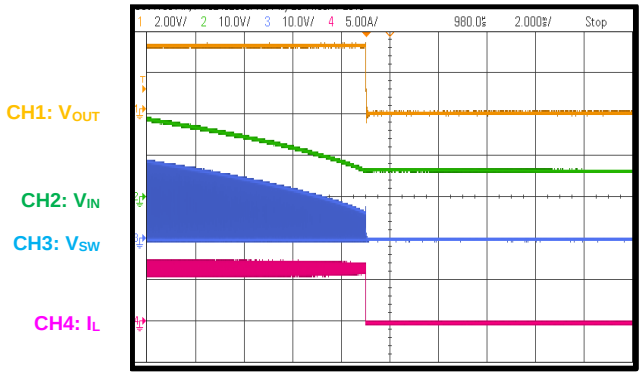
Shutdown through VIN

I_{OUT} = 0A, FCCM



Shutdown through VIN

I_{OUT} = 6.5A

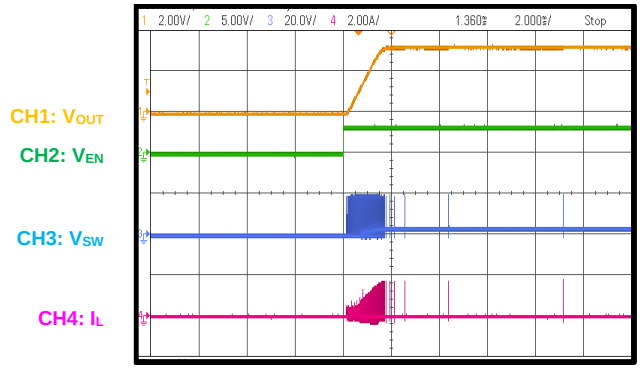


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 19V, V_{OUT} = 3.3V, L = 2.2µH, T_A = 25°C, PFM mode without USM, unless otherwise noted.

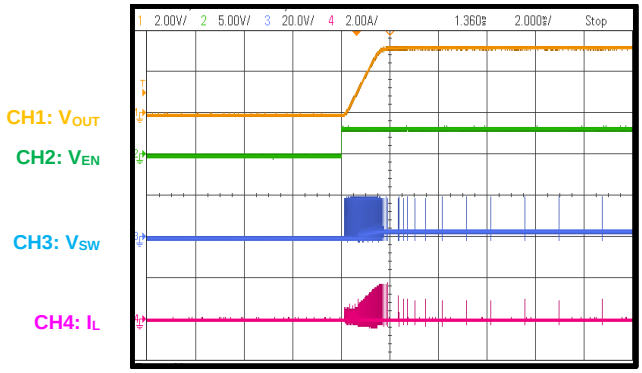
Start-Up through EN

I_{OUT} = 0A, PFM mode without USM



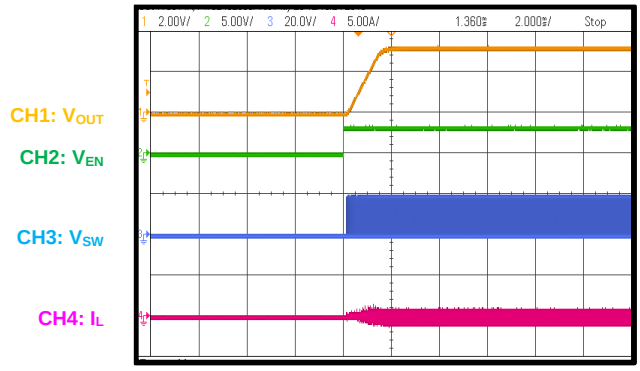
Start-Up through EN

I_{OUT} = 0A, USM



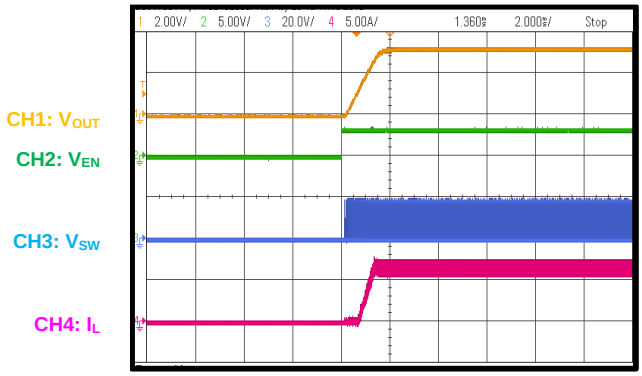
Start-Up through EN

I_{OUT} = 0A, FCCM



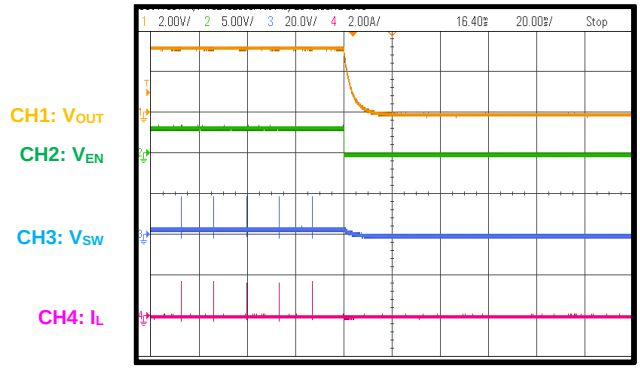
Start-Up through EN

I_{OUT} = 6.5A



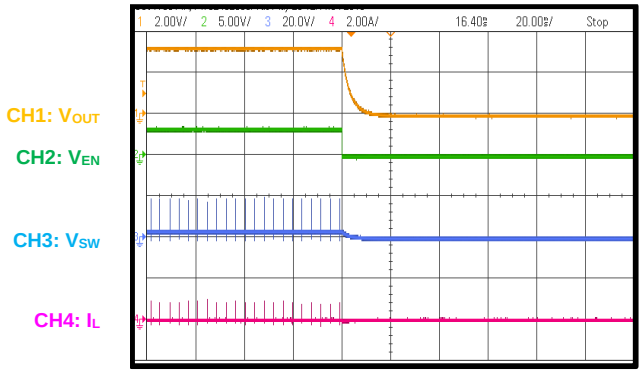
Shutdown through EN

I_{OUT} = 0A, PFM mode without USM



Shutdown through EN

I_{OUT} = 0A, USM

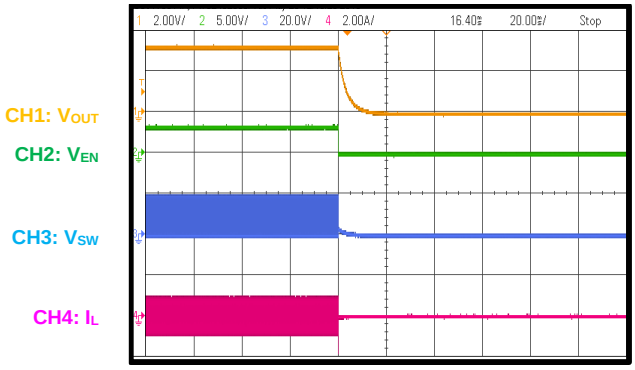


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 19V, V_{OUT} = 3.3V, L = 2.2µH, T_A = 25°C, PFM mode without USM, unless otherwise noted.

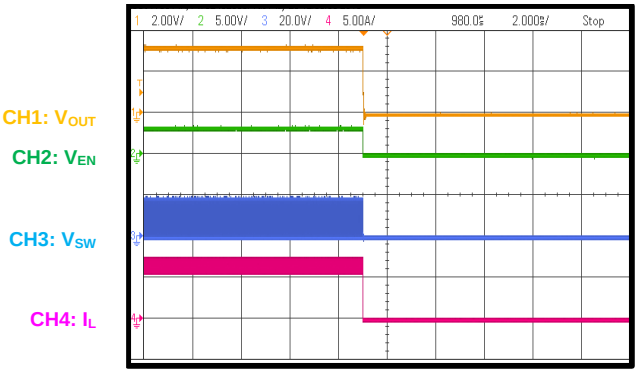
Shutdown through EN

I_{OUT} = 0A, FCCM



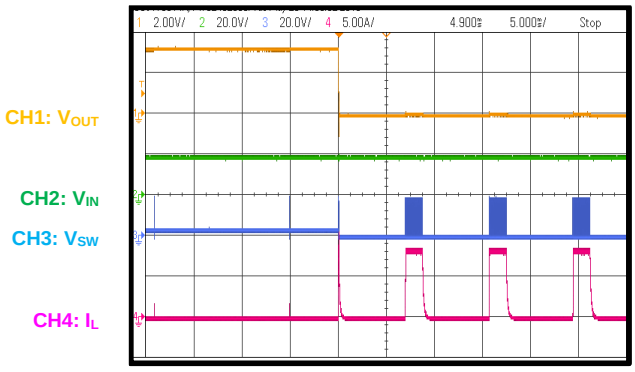
Shutdown through EN

I_{OUT} = 6.5A



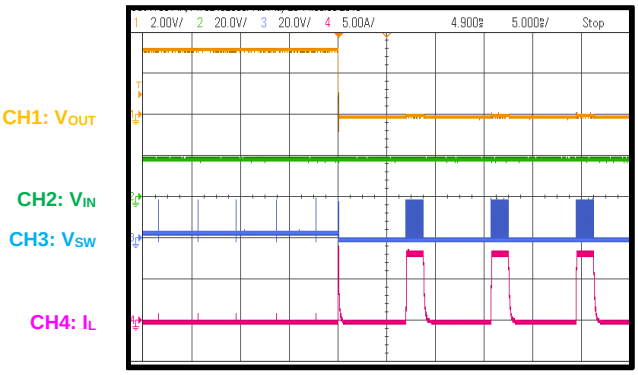
Short-Circuit Protection Entry

I_{OUT} = 0A, PFM mode without USM



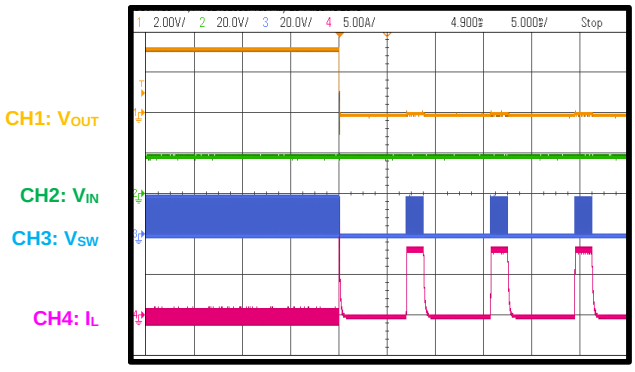
Short-Circuit Protection Entry

I_{OUT} = 0A, USM



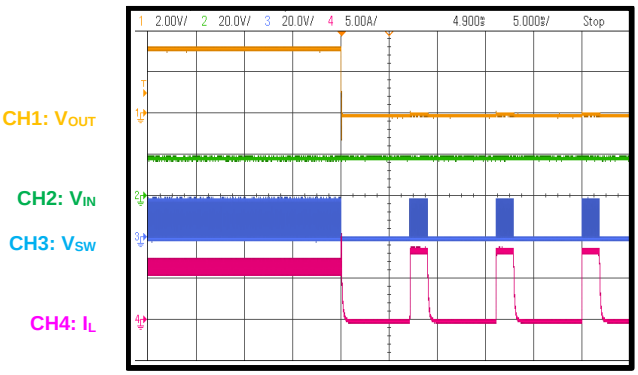
Short-Circuit Protection Entry

I_{OUT} = 0A, FCCM



Short-Circuit Protection Entry

I_{OUT} = 6.5A

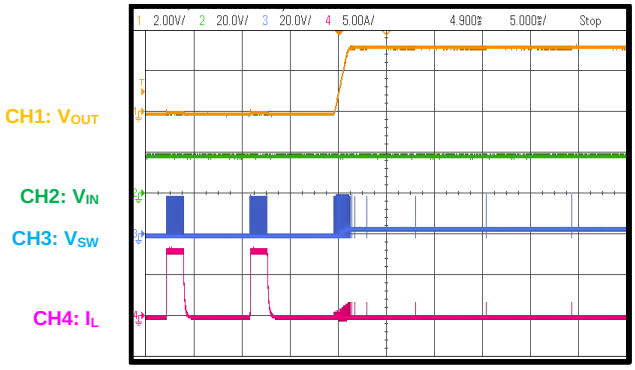


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 19V, V_{OUT} = 3.3V, L = 2.2µH, T_A = 25°C, PFM mode without USM, unless otherwise noted.

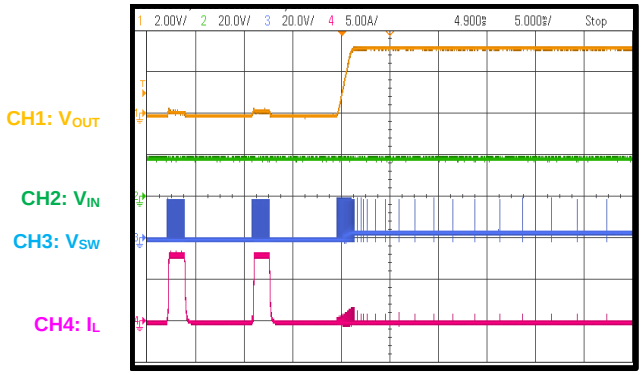
Short-Circuit Protection Recovery

I_{OUT} = 0A, PFM mode without USM



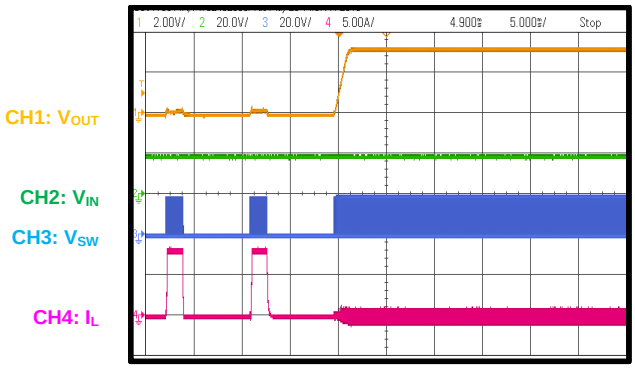
Short-Circuit Protection Recovery

I_{OUT} = 0A, USM



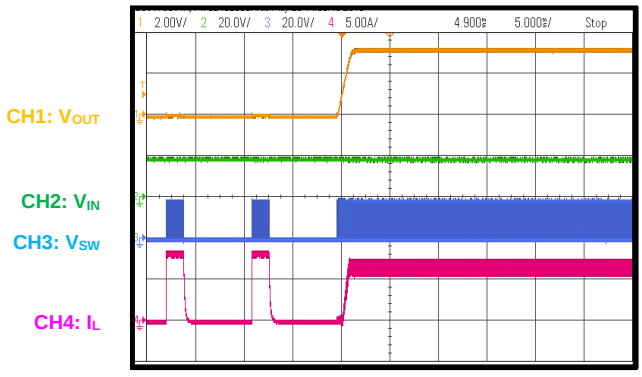
Short-Circuit Protection Recovery

I_{OUT} = 0A, FCCM



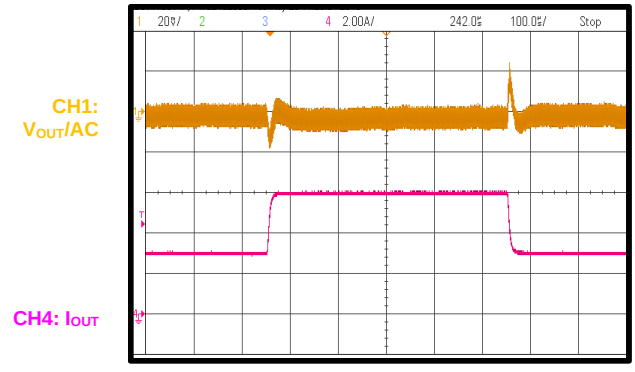
Short-Circuit Protection Recovery

I_{OUT} = 6.5A



Load Transient

I_{OUT} = 3A to 6A



FUNCTIONAL BLOCK DIAGRAM

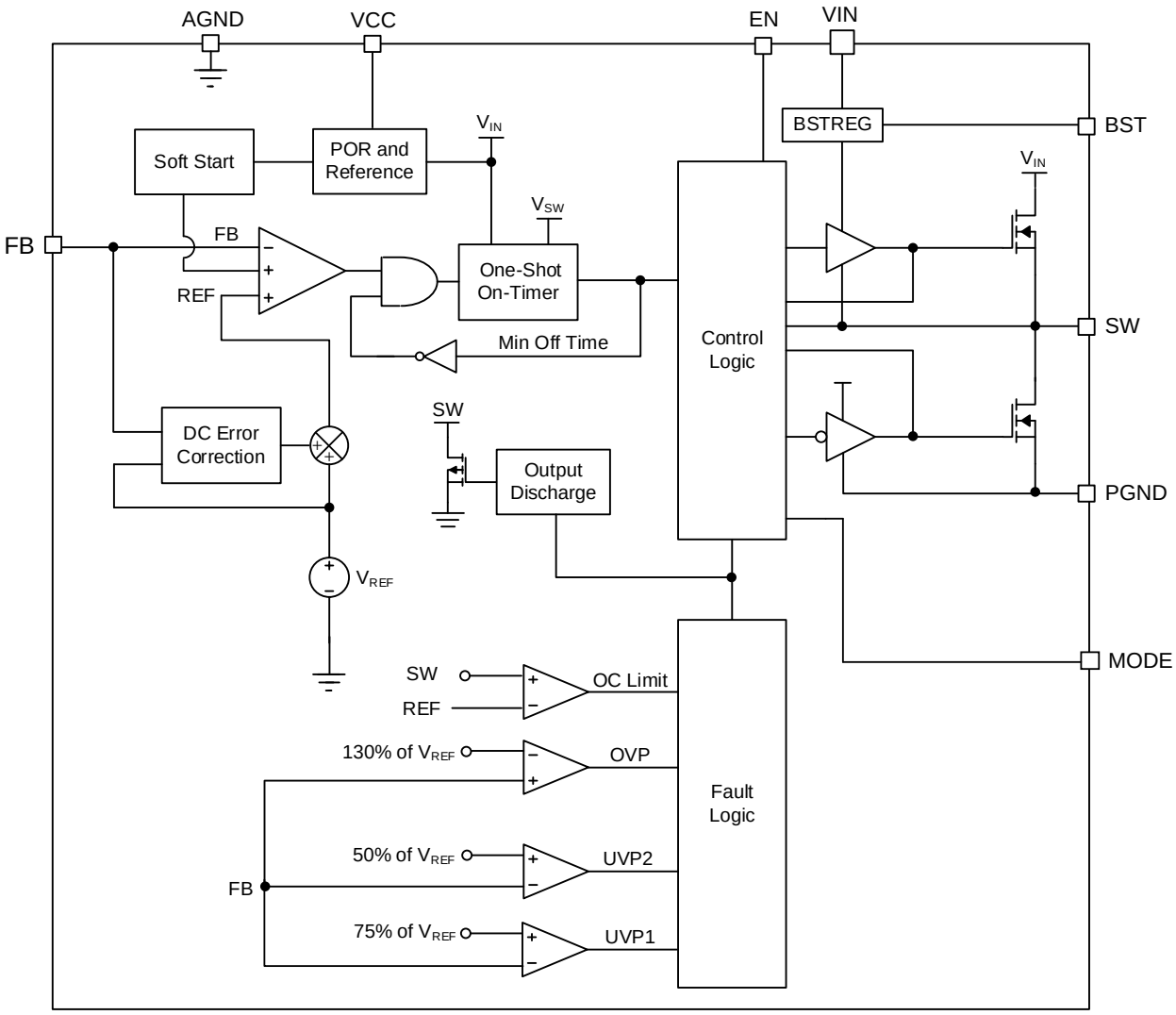


Figure 1: Functional Block Diagram

OPERATION

The MP2349 is a fully integrated, synchronous, rectified, step-down switch-mode converter. Constant-on-time (COT) control is implemented to provide fast transient response and ease loop stabilization. At the beginning of each cycle, the high-side MOSFET (HS-FET) turns on once the feedback (FB) voltage (V_{FB}) drops below the reference voltage (V_{REF}), which indicates an insufficient output voltage (V_{OUT}). The on period is determined by both V_{OUT} and the input voltage (V_{IN}) to make the switching frequency (f_{SW}) fairly constant across the V_{IN} range.

After the on period elapses, the HS-FET turns off. Once V_{FB} drops below V_{REF}, the HS-FET turns on again. By repeating the operation, the converter regulates V_{OUT}. The integrated low-side MOSFET (LS-FET) turns on when the HS-FET is off to minimize conduction loss. If the HS-FET and LS-FET are turned on at the same time, a dead short occurs between the input and PGND; this is called shoot-through. To avoid shoot-through, the MP2349 generates a dead time (DT) internally between the HS-FET off and LS-FET on period, and vice versa.

The MP2349 applies internal compensation for COT control to provide more stable operation, even when ceramic capacitors are used as output capacitors (C_{OUT}). This internal compensation improves jitter performance without affecting the line or load regulation.

Heavy-Load Operation

If the output current (I_{OUT}) is high and the inductor current (I_L) remains above 0A, then the MP2349 enters continuous conduction mode (CCM) (see Figure 2).

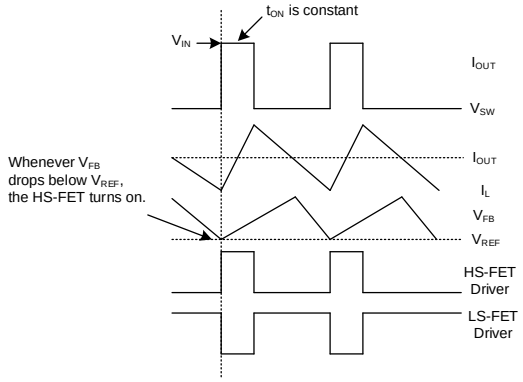


Figure 2: Heavy-Load Operation

If V_{FB} is below V_{REF}, then the HS-FET turns on for a fixed interval. If the HS-FET turns off, then the LS-FET turns on until the next period begins.

During CCM, f_{SW} is fairly constant; this is called pulse-width modulation (PWM) mode.

Light-Load Operation

If the load decreases, then I_L also decreases. When I_L reaches 0A, the operation transitions from CCM to discontinuous conduction mode (DCM). Figure 3 shows light-load operation.

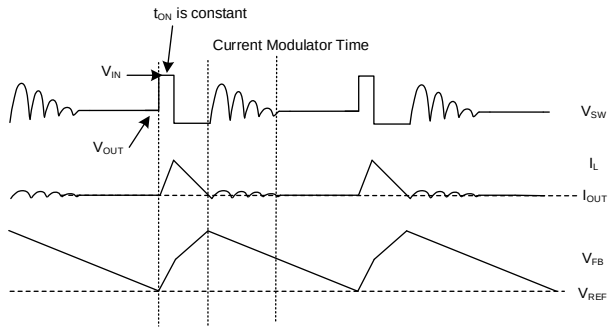


Figure 3: Light-Load Operation

If V_{FB} is below V_{REF}, then the HS-FET turns on for a fixed interval. If the HS-FET turns off, then the LS-FET turns on until I_L reaches 0A. During DCM, V_{FB} cannot reach V_{REF} while I_L approaches 0A. When I_L reaches 0A, the LS-FET driver enters tri-state (Hi-Z). As a result, the efficiency under light-load conditions improves significantly. Under light-load conditions, the HS-FET does not turn on as frequently compared to heavy-load conditions; this is called skip mode.

Under light-load or no-load conditions, the output drops very slowly, and the MP2349 reduces f_{SW} to achieve high efficiency at light loads.

As I_{OUT} increases under light-load conditions, the current modulator regulation time becomes shorter. The HS-FET turns on more frequently and f_{SW} increases accordingly. I_{OUT} reaches its critical level when the current modulator time is 0s. The critical level of I_{OUT} ($I_{OUT\_CRITICAL}$) can be calculated with Equation (1):

$$I_{OUT\_CRITICAL} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times f_{SW} \times V_{IN}} \quad (1)$$

When I_{OUT} exceeds the critical level, the device enters PWM mode. Afterward, f_{SW} stays fairly constant across the I_{OUT} range.

Light-Load Ultrasonic Mode (USM)

Ultrasonic mode (USM) maintains f_{SW} above the audible frequency range during light-load conditions. Once the MP2349 enters light-load conditions, the on time (t_{ON}) decreases to prevent f_{SW} from dropping below 20kHz.

Large Duty Cycle Operation

If V_{IN} is below 7V, then V_{OUT} exceeds 4.2V, and the MP2349 reduces f_{SW} to about 280kHz to support large duty operation. If V_{OUT} is below 3.9V, then the MP2349 returns to f_{SW} during normal operation.

Jitter and FB Ramp

Jitter occurs during PWM and skip modes when V_{FB} ripple noise propagates a delay to the HS-FET driver. Jitter can affect system stability with noise immunity proportional to the V_{FB} downward slope steepness. Thus, jitter during DCM is typically larger than during CCM. However, V_{FB} ripple does not affect noise immunity directly.

Figure 4 shows the jitter in PWM mode.

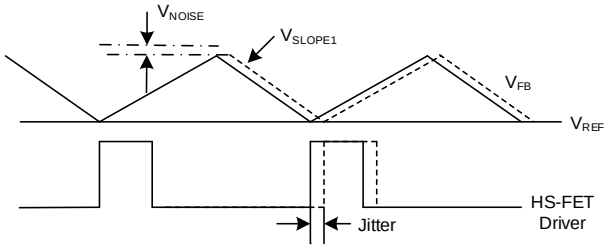


Figure 4: Jitter in PWM Mode

Figure 5 shows the jitter in skip mode.

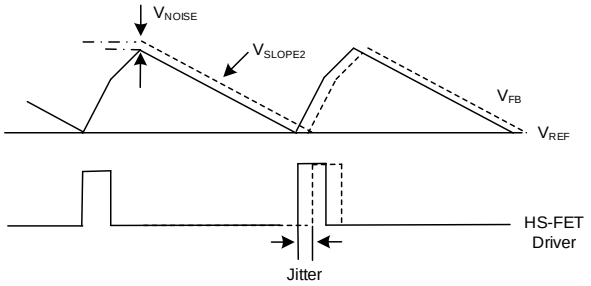


Figure 5: Jitter in Skip Mode

Operation with External Ramp Compensation

The MP2349 is typically able to support ceramic C_{OUT} without an external ramp. If the internal ramp is not sufficient to stabilize the system or the jitter is too large, then external ramp compensation is required. See the Application Information section on page 20 for more details on external ramp compensation.

Configuring the EN Control

The EN pin can enable or disable the entire chip. Pull EN high to turn on the regulator; pull EN low to turn it off. Do not float the pin.

For automatic start-up, EN can be pulled up to V_{IN} via a voltage resistor divider. There is an internal 1MΩ resistor from EN to AGND. To calculate the automatic start-up input voltage (V_{IN_START}), determine the values of the pull-up resistor (R_{UP}, from VIN to EN) and the pull-down resistor (R_{DOWN}, from EN to AGND). V_{IN_START} can be calculated with Equation (2):

$$V_{IN\_START} = 1.25 \times \frac{R_{UP} + R_{DOWN}//1000k\Omega}{R_{DOWN}//1000k\Omega} (V) \quad (2)$$

For example, if R_{UP} = 150kΩ and R_{DOWN} = 51kΩ, then set V_{IN_START} to 5.11V.

The EN voltage (V_{EN}) must not exceed a maximum of 4.5V to prevent damage to the internal circuit.

MODE Selection

Pull the MODE pin above 3.2V to operate in forced continuous conduction mode (FCCM). Float MODE to operate in pulse-frequency modulation (PFM) mode with USM at light loads. Connect MODE to ground to operate in PFM mode without USM.

Soft Start (SS)

The MP2349 employs soft start (SS) to ensure smooth output during start-up. When the device starts up, the internal V_{REF} ramps up gradually. As a result, V_{OUT} ramps up smoothly as well. Once V_{REF} reaches the target voltage, SS finishes and the device enters steady state operation.

If the output is pre-biased to a set voltage during start-up, the IC disables the switching on the HS-FET and LS-FET until the internal V_{REF} exceeds the sensed V_{OUT} at the FB node.

Over-Current Limit (OCL)

The MP2349 provides cycle-by-cycle over-current limit (OCL) control. The current-limit circuit employs a valley current sensing algorithm, where the LS-FET's on resistance ($R_{DS(ON)}$) is used as a current-sensing element. If the magnitude of the current-sense signal exceeds the current-limit threshold, then PWM is not allowed to initiate a new cycle, even if V_{FB} is below V_{REF} (see Figure 6).

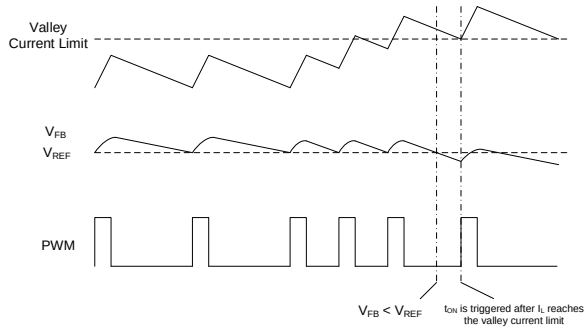


Figure 6: Valley Current Limit Control

Since the comparison occurs when the LS-FET is on, the over-current (OC) trip level sets the I_L valley level. The maximum load current at the OC threshold (I_{OC}) can be calculated with Equation (3):

$$I_{OC} = I_{LIMIT} + \frac{\Delta I_L}{2} \quad (3)$$

The OCL limits I_L and does not latch off. Under an OC condition, the current to the load exceeds the current to C_{OUT}, which causes V_{OUT} to fall off. Eventually, the V_{OUT} crosses the under-voltage protection (UVP) threshold and enters hiccup protection mode.

Over-Voltage Protection (OVP) and Under-Voltage Protection (UVP)

The MP2349 monitors a resistor-divided V_{FB} to detect over-voltage (OV) and under-voltage (UV) conditions. If V_{FB} exceeds 130% of the target voltage, then the over-voltage protection (OVP) comparator output goes high and the circuit latches as the HS-FET driver turns off. A discharge FET on the SW pin then turns on to discharge the voltage on C_{OUT}.

If V_{FB} drops between below 50% and 75% of V_{REF}, then the UVP1 comparator output goes high. If V_{FB} remains within this range for about 32µs, then the part enters hiccup mode. During this period, the valley current limit helps control I_L.

If V_{FB} drops below 50% of V_{REF}, then the UVP2 comparator output goes high and the part enters hiccup mode immediately after the comparator and logic delay.

Under-Voltage Lockout (UVLO) Protection

The MP2349 has two under-voltage lockout (UVLO) protections: V_{CC} UVLO and V_{IN} UVLO. The MP2349 can start up when V_{CC} and V_{IN} exceed their respective UVLO thresholds. The device shuts down when either V_{CC} is below its falling threshold or V_{IN} is below its falling threshold. Both UVLO protections are non-latch protections.

If an application requires a higher UVLO threshold, use EN to adjust the V_{IN} UVLO threshold via two external resistors (see Figure 7).

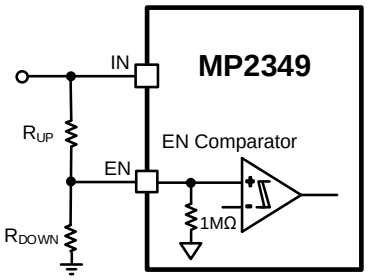


Figure 7: Adjustable UVLO

Thermal Shutdown

The MP2349 provides thermal shutdown. The IC's junction temperature (T_J) is monitored internally. If T_J exceeds the threshold (typically 150°C), then the converter shuts off. This is a non-latch protection. There is a hysteresis of about 25°C. Once T_J drops to about 125°C, a new SS is initiated, and the device resumes normal operation.

Output Discharge

The MP2349 discharges the output when the controller is turned off by VIN, EN, or the protection functions (OVP, UVLO, and thermal shutdown). The discharge current on the output is typically 40mA.

APPLICATION INFORMATION

Setting the Output Voltage without External Ramp Compensation

The MP2349 has an internal ramp. When internal compensation is sufficient for stable operation using the ceramic C_{OUT}, the device does not require external ramp compensation. V_{OUT} can be set via the FB resistors (R1 and R2) (see Figure 8).

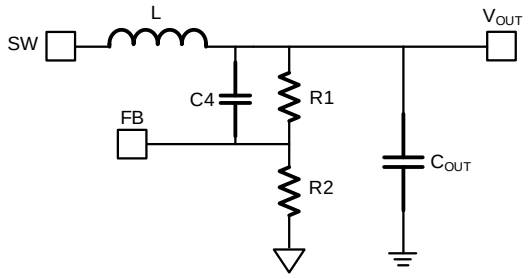


Figure 8: Simplified Circuit without External Ramp Compensation

First, select a proper value for R2 since a small R2 leads to considerable quiescent current (I_Q) loss, while a large R2 makes FB sensitive to noise. R2 is recommended to be between 5kΩ and 100kΩ. Considering the output ripple, R1 can be determined with Equation (4):

$$R1 = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R2 \quad (4)$$

When C4 functions as a feed-forward capacitor, the transient response improves. A larger C4 leads to improved transient response, but more noise sensitivity.

Table 1 shows the recommended resistances for common V_{OUT} values.

Table 1: Parameter Selection for Common Output Voltages (9)

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	C4 (pF)	L (μH)
5	40.2	5.49	33	2.2
3.3	40.2	8.87	33	2.2
2.5	40.2	12.7	33	1.5
1.8	40.2	20	33	1.5
1.5	40.2	26.7	33	1
1.2	40.2	40.2	33	1
1	40.2	60.4	33	0.68

Note:

9) For additional component parameters, see the Typical Application Circuits section on pages 24 thorugh 26.

Setting the Output Voltage with External Ramp Compensation

Figure 9 shows the simplified circuit with external ramp compensation.

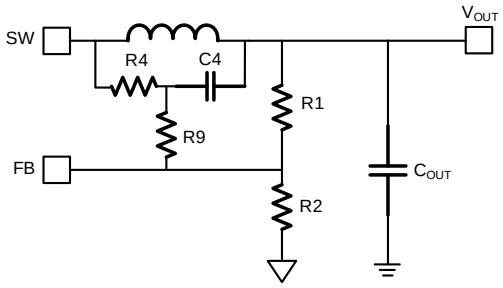


Figure 9: Simplified Circuit with External Ramp Compensation

If the system is not stable enough or the jitter is too big using a ceramic C_{OUT}, add an external voltage ramp to FB via R4 and C4. Since there is an internal ramp included in the system, a 1MΩ ramp for R4 and 220pF ramp for C4 is typically sufficient for the ramp.

V_{OUT} is impacted by R4 in addition to R1 and R2 shown in Figure 9. R1 can be determined with Equation (5):

$$R1 = \frac{1}{\frac{V_{REF}}{V_{OUT} - V_{REF}} - \frac{R2}{R4}} \times R2 \quad (5)$$

R9 is typically set to 0Ω. To obtain a pole for improved noise immunity, R9 can be calculated with Equation (6):

$$R9 = \frac{1}{2\pi \times C4 \times 2 \times f_{SW}} \quad (6)$$

R9 is recommended to be between 100Ω and 1kΩ to reduce its influence on the ramp.

Selecting the Input Capacitor

The step-down converter has a discontinuous input current (I_{IN}), and requires a capacitor to supply AC current to the converter while maintaining the DC V_{IN}. For the best performance, use ceramic capacitors placed as

close to VIN as possible. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable amid temperature fluctuations.

The capacitors must also have a ripple current rating greater than the converter's maximum input ripple current (I_{CIN}). I_{CIN} can be estimated with Equation (7):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (7)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, which can be calculated with Equation (8):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (8)$$

For simplification, choose an input capacitor (C_{IN}) with an RMS current rating greater than half of the maximum load current.

C_{IN} determines the converter's input voltage ripple (ΔV_{IN}). If the system has a ΔV_{IN} requirement, select C_{IN} to meet the specifications. ΔV_{IN} can be estimated with Equation (9):

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (9)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, which can be calculated with Equation (10):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{f_{SW} \times C_{IN}} \quad (10)$$

Selecting the Output Capacitor

C_{OUT} is required to maintain the DC V_{OUT}. Ceramic or POSCAP capacitors are recommended. The output voltage ripple (ΔV_{OUT}) can be estimated using Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \quad (11)$$

In the case of ceramic capacitors, the capacitance dominates the impedance at f_{SW} and cause the majority of ΔV_{OUT}.

For simplification, ΔV_{OUT} can be estimated with Equation (12):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (12)$$

In the case of POSCAP capacitors, the ESR dominates the impedance at f_{SW}. ΔV_{OUT} can be estimated with Equation (13):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (13)$$

The maximum C_{OUT} limitation should also be considered in the design application. The MP2349 has an SS time (t_{SS}) around 1.7ms. If C_{OUT} is too high, then V_{OUT} cannot reach the design value during t_{SS}, and the device fails to regulate. The maximum C_{OUT} (C_{OUT_MAX}) can be calculated with Equation (14):

$$C_{OUT\_MAX} = (I_{LIM\_AVG} - I_{OUT}) \times t_{SS} / V_{OUT} \quad (14)$$

Where I_{LIM_AVG} is the average start-up current during the SS period.

Selecting the Inductor

An inductor is required to supply constant current to the output load while being driven by the switched V_{IN}. A larger-value inductor results in reduced ripple current and ΔV_{OUT}; however, it also has a larger physical footprint, higher series resistance, and lower saturation current (I_{SAT}). A good rule for determining the inductance (L) is to design the inductor's peak-to-peak ripple current to be 30% to 50% of the maximum I_{OUT} and to keep the peak I_L below the maximum switch current limit. L can be calculated with Equation (15):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (13)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

The inductor should not saturate under the maximum peak inductor current, including short current. MPS inductors are optimized and tested for use with a complete line of integrated circuits.

Table 2 lists our power inductor recommendations. Select a part number based on the relevant design requirements.

Table 2: Power Inductor Selection

MPS Part Number	Inductance	Manufacturer
MPL-AL4020-R68	0.68µH	MPS
MPL-AL6050-1R0	1µH	MPS
MPL-AL6050-1R5	1.5µH	MPS
MPL-AL6050-2R2	2.2µH	MPS

Visit MonolithicPower.com under Products > Inductors for more information.

Design Example

Table 3 shows a design example when the ceramic capacitors are applied.

Table 3: Design Example

V_{IN}	V_{OUT}	I_{OUT}
8V to 24V	3.3V	6.5A

For the detailed application schematic, see Figure 12 on page 24. For the typical performance and circuit waveforms, see the Typical Performance Characteristics section on page 8. For more device applications, refer to the related evaluation board datasheet.

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. A 4-layer layout is strongly recommended for improved thermal performance. For the best results, refer to Figure 10 on page 23 and follow the guidelines below:

1. Place the high-current paths (PGND, VIN, and SW) very close to the device using short, direct, and wide traces.
2. Place the input capacitors as close to VIN and PGND as possible.
3. Put the decoupling capacitor as close to VCC and AGND as possible.
4. Keep the switching node (SW) short and away from the FB network.
5. Keep the BST voltage path as short as possible.
6. Connect the VIN and PGND pads with large coppers to achieve improved thermal performance.
7. Add several vias close to the VIN and PGND pads to help with thermal dissipation.

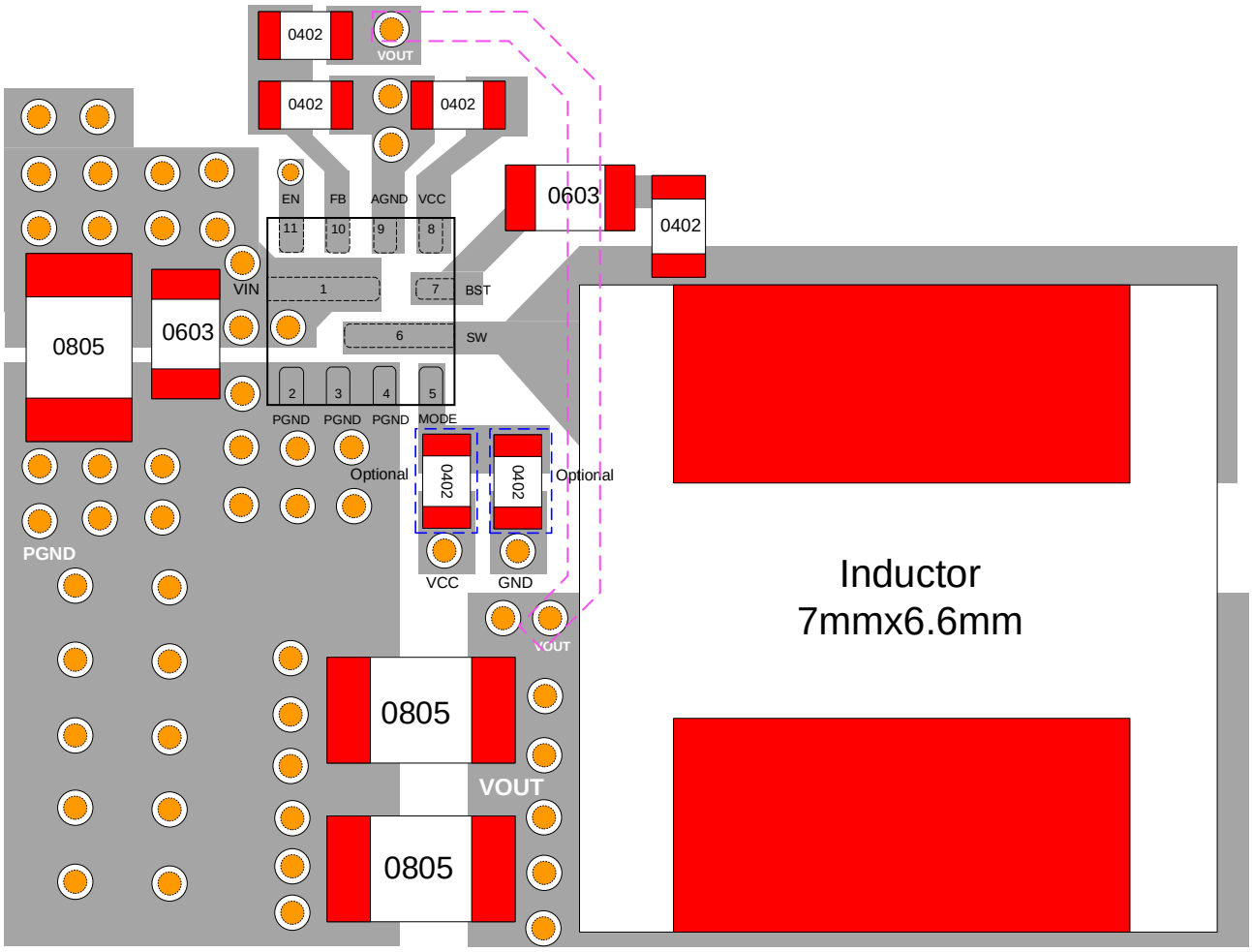


Figure 10: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS (10)

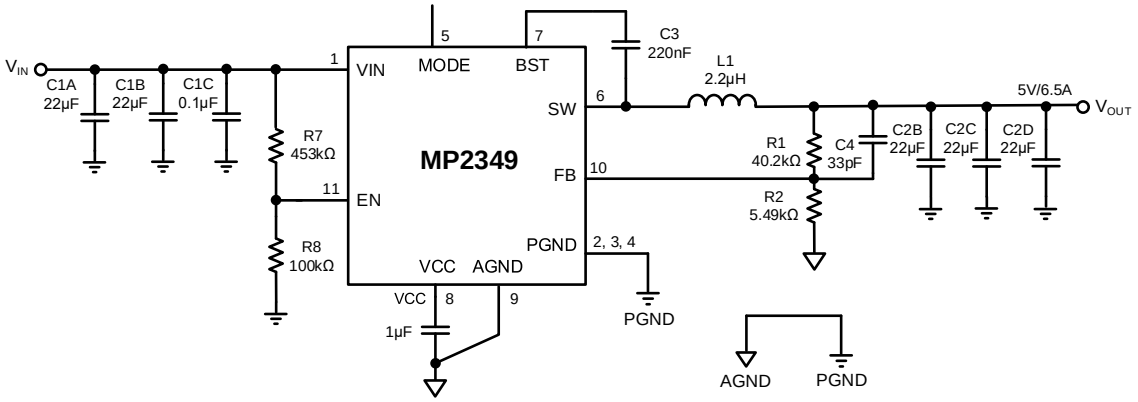


Figure 11: Typical Application Circuit (V_{IN} = 19V, V_{OUT} = 5V/6.5A)

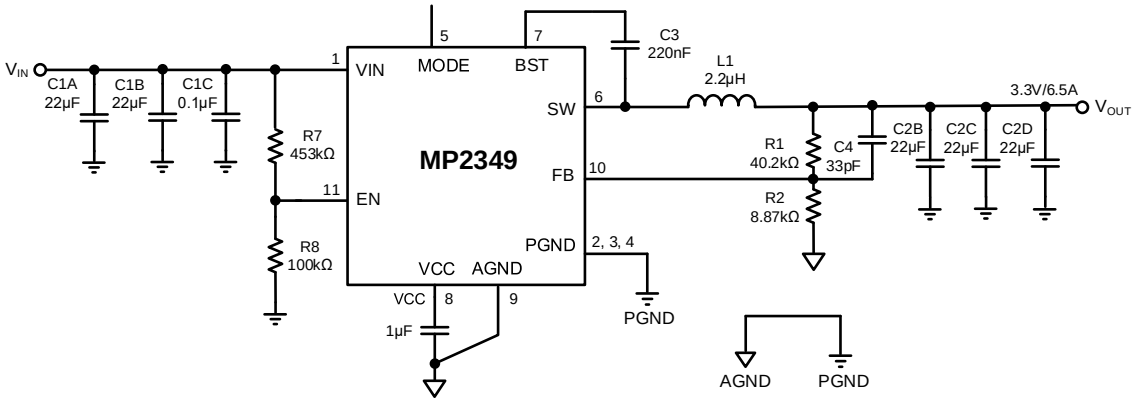


Figure 12: Typical Application Circuit (V_{IN} = 19V, V_{OUT} = 3.3V/6.5A)

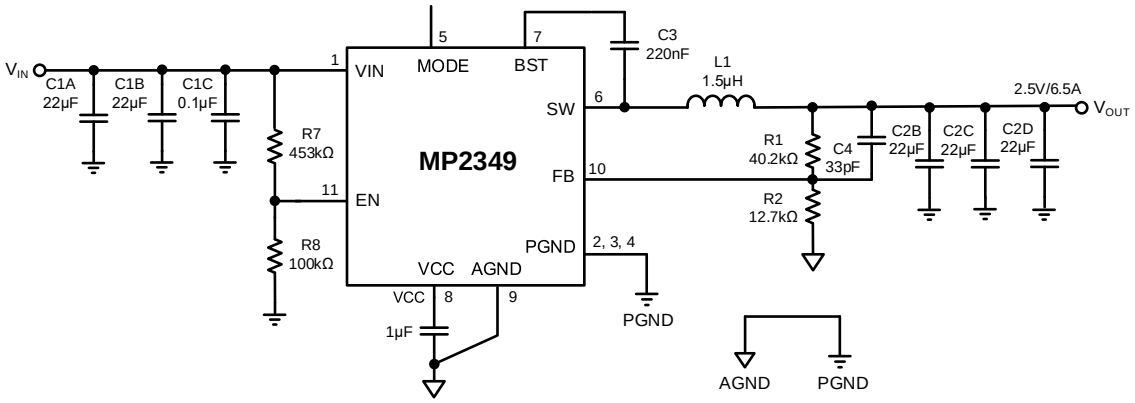


Figure 13: Typical Application Circuit (V_{IN} = 19V, V_{OUT} = 2.5V/6.5A)

TYPICAL APPLICATION CIRCUITS *(continued)* (10)

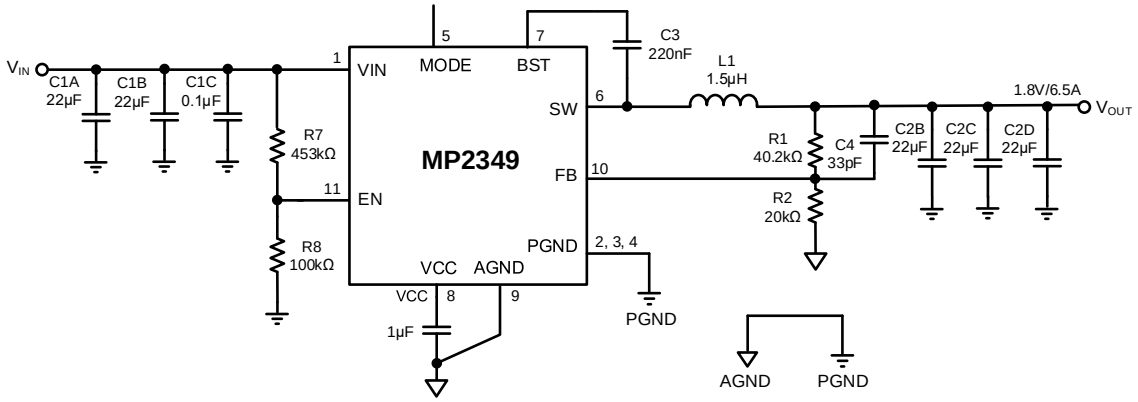


Figure 14: Typical Application Circuit (V_{IN} = 19V, V_{OUT} = 1.8V/6.5A)

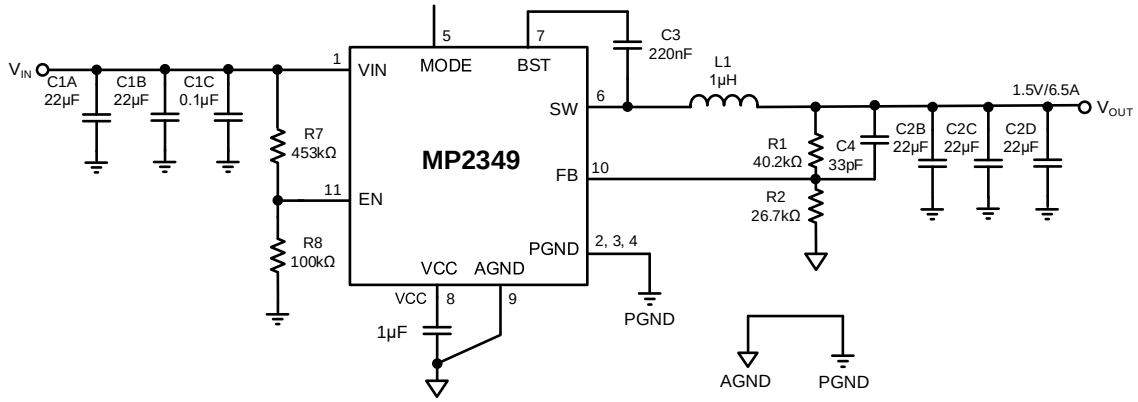


Figure 15: Typical Application Circuit (V_{IN} = 19V, V_{OUT} = 1.5V/6.5A)

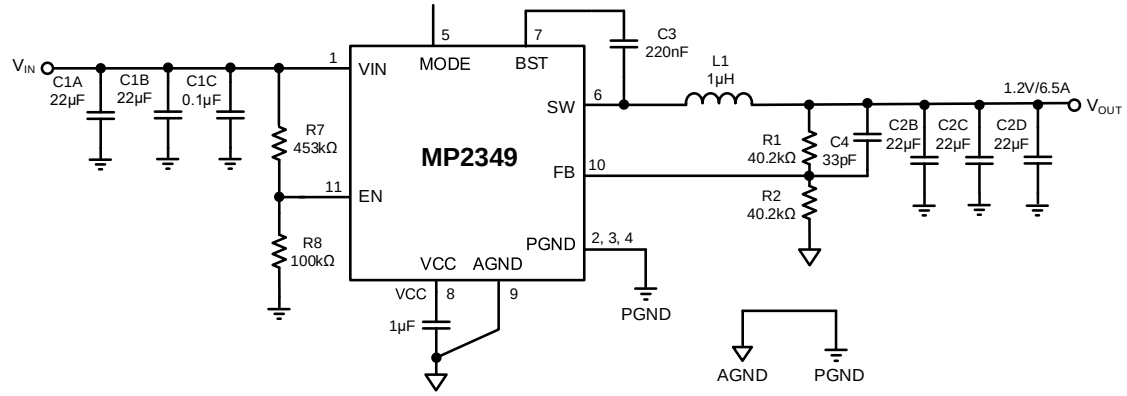


Figure 16: Typical Application Circuit (V_{IN} = 19V, V_{OUT} = 1.2V/6.5A)

TYPICAL APPLICATION CIRCUITS *(continued)* (10)

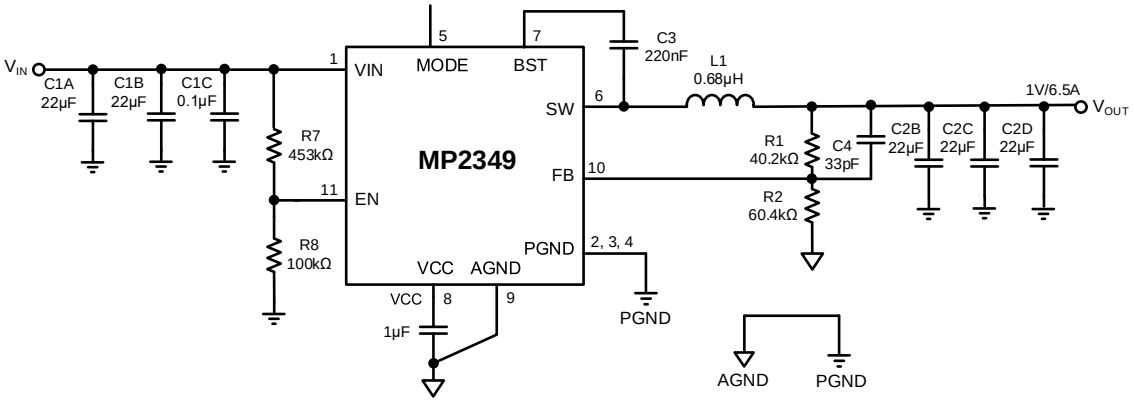


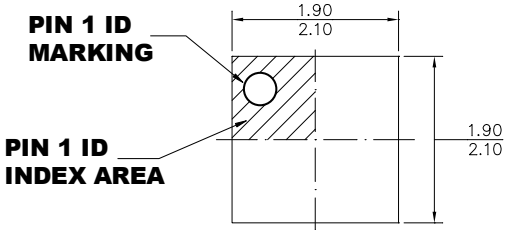
Figure 17: Typical Application Circuit (V_{IN} = 19V, V_{OUT} = 1V/6.5A)

Note:

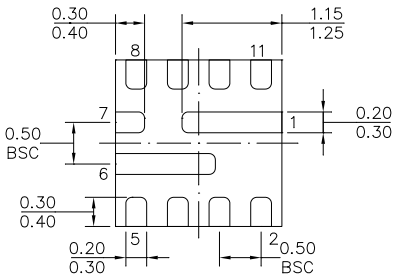
10) The EN resistor divider sets the V_{IN} threshold to 7.5V. For 5V input applications, the EN resistor must be adjusted accordingly.

PACKAGE INFORMATION

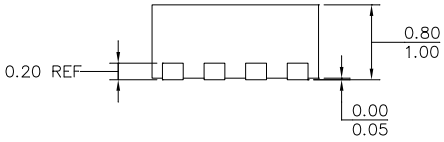
QFN-11 (2mmx2mm)



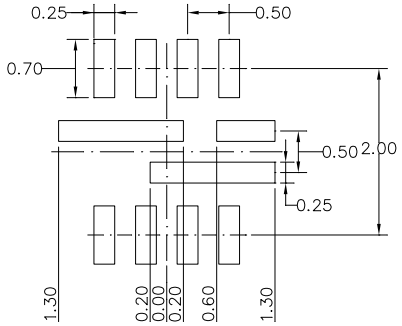
TOP VIEW



BOTTOM VIEW



SIDE VIEW

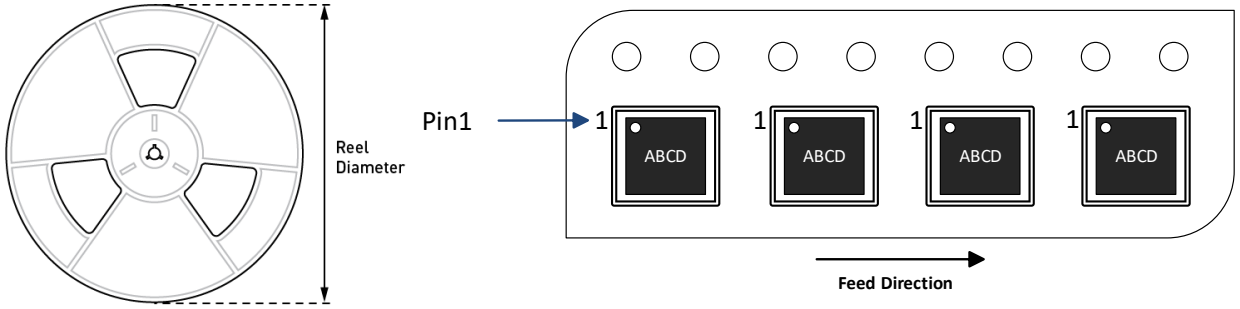


RECOMMENDED LAND PATTERN

NOTE:

1) LAND PATTERNS OF PIN1 AND PIN6 HAVE THE SAME LENGTH AND WIDTH.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP2349GG-Z	QFN-11 (2mmx2mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	5/22/2023	Initial Release	-