MP2152D

2.5V to 5.5V, 2A Synchronous, Step-Down Converter with Fast Output Discharge

DESCRIPTION

The MP2152D is a monolithic, step-down switch-mode converter with integrated internal power MOSFETs. It can achieve up to 2A of continuous output current (I_{OUT}) across a wide 2.5V to 5.5V input voltage (V_{IN}) range, with excellent load and line regulation. The output voltage (V_{OUT}) can be regulated to as low as 0.6V.

The device is ideal for a wide range of applications, including solid-state drives (SSDs), portable devices, as well as other low-power and low-voltage systems.

Constant-on-time (COT) control provides fast transient response and eases loop stabilization.

Full protection features include cycle-by-cycle over-current protection (OCP), over-voltage protection (OVP), short-circuit protection (SCP) with hiccup mode, and thermal shutdown.

The MP2152D requires a minimal number of readily available, standard external components, and is available in ultra-small SOT563 package and UTQFN-6 (1.2mmx1.6mm) package.

FEATURES

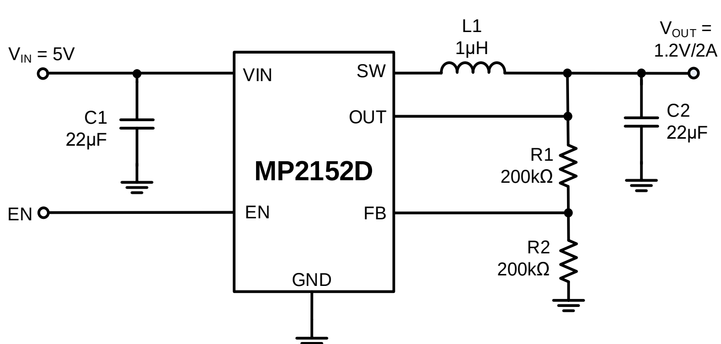
- Wide 2.5V to 5.5V Operating Input Voltage (V_{IN}) Range
- Up to 2A Output Current (I_{OUT})
- Adjustable Output Voltage (V_{OUT}) from 0.6V
- 25µA Low Quiescent Current (I_Q)
- 1.1MHz Switching Frequency (f_{SW})
- Enable (EN) for Power Sequencing
- 1% Feedback (FB) Accuracy
- 75mΩ and 45mΩ Internal Power MOSFETs
- 100% Duty Cycle
- Fast Output Discharge
- Output Over-Voltage Protection (OVP)
- Short-Circuit Protection (SCP) with Hiccup Mode
- Available in an SOT563 Package or UTQFN-6 (1.2mmx1.6mm) Package

MPL Optimized Performance with MPS Inductor MPL-AL4020 Series

APPLICATIONS

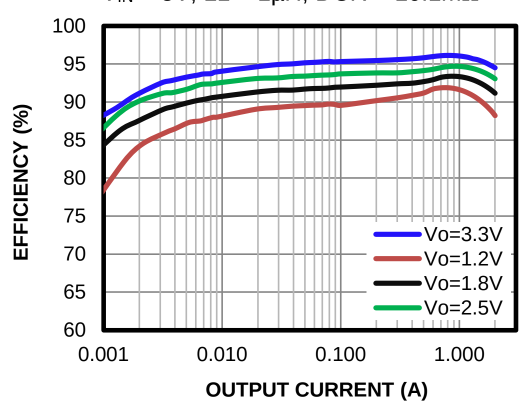
- Solid-State Drives
- Portable Instruments
- Battery-Powered Devices
- Multi-Function Printers

TYPICAL APPLICATION



Efficiency vs. Output Current

V_{IN} = 5V, L1 = 1µH, DCR = 10.1mΩ



ORDERING INFORMATION

Part Number*	Package	Top Marking	V_{OUT} Range	MSL Rating
MP2152DGQFU	UTQFN-6 (1.2mmx1.6mm)	*See Below*	Adjustable	1
MP2152DGTF	SOT563	*See Below*	Adjustable	1

* For Tape & Reel, add suffix -Z (e.g. MP2152DGTF-Z).

TOP MARKING (MP2152DGQFU)

$\overline{\text{LA}}$
LL

LA: Product code of MP2152DGQFU
LL: Lot number

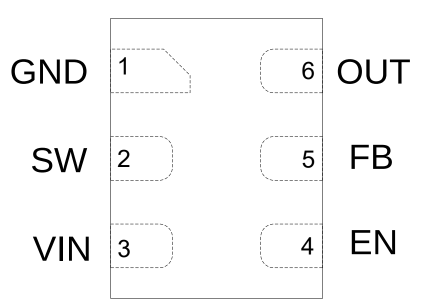
TOP MARKING (MP2152DGTF)

BQDY
LLL

BDQ: Product code of MP2152DGTF
Y: Year code
LLL: Lot number

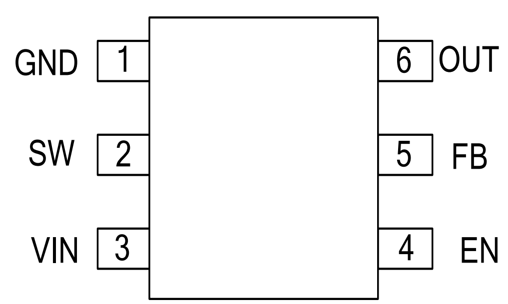
PACKAGE REFERENCE

TOP VIEW



UTQFN-6 (1.2mmx1.6mm)
MP2152DGQFU

TOP VIEW



SOT563 (1.6mmx1.6mm)
MP2152DGTF

PIN FUNCTIONS

Pin #	Name (SOT563 and UTQFN-6)	Description
1	GND	**Power ground.**
2	SW	**Output switching node.** The SW pin is the drain of the internal, P-Channel high-side MOSFET (HS-FET). Connect SW to the inductor to complete the converter.
3	VIN	**Supply voltage.** The MP2152D operates from a 2.5V to 5.5V unregulated input voltage (V_{IN}). Use a decoupling capacitor to prevent large voltage spikes at the input.
4	EN	**On/off control.**
5	FB	**Feedback.** To set the output voltage (V_{OUT}), connect an external resistor divider tapped to the FB pin between the output and GND.
6	OUT	**Output sense.** The OUT pin is the voltage power rail and input sense for V_{OUT}. Use an output capacitor (C2) to reduce the output voltage ripple (ΔV_{OUT}).

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) 6.5V
V_{SW} .... -0.3V (-5V for <10ns) to +6.5V (10V for <10ns)
All other pins .... -0.3V to +6.5V
Junction temperature .... 150°C
Lead temperature .... 260°C
Continuous power dissipation (T_A = 25°C)
SOT563 .... 1.5W (2) (4)
QFN 2W (2) (5)
Storage temperature .... -65°C to +150°C

ESD Rating

SOT563
Human body model (HBM) 2000V
Charged device model (CDM) 1500V
UTQFN-6 (1.2mmx1.6mm)
Human body model (HBM) 2000V
Charged device model (CDM) 1500V

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) .... 2.5V to 5.5V
Operating junction temp (T_J) ..... -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

SOT563
EVL2152D-TF-00A (4) .... 80 .... 50 ... °C/W
JESD51-7 (6) (7) (8) .... 130 .... 60 ... °C/W
UTQFN-6 (1.2mmx1.6mm)
EVL2152D-QFU-00A (5) .... 65 .... 30 ... °C/W
JESD51-7 (6) (7) (8) .... 173 ...... 127 ... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on EVL2152D-TF-00A, 2-layer PCB.
5) Measured on EVL2152D-QFU-00A, 2-layer PCB.
6) Measured on JESD51-7, 4-layer PCB.
7) The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes.
8) These values are calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN} = 3.6V, T_J = -40°C to +125°C (9), typical value is tested at T_J = 25°C. The limit over temperature is guaranteed by characterization, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input voltage	V_{IN}		2.5		5.5	V
Under-voltage lockout (UVLO) rising threshold	V_{UVLO_RISING}			2.3	2.45	V
UVLO threshold hysteresis	V_{UVLO_HYS}			200		mV
Feedback (FB) voltage	V_{FB}	2.5V ≤ V_{IN} ≤ 5.5V	594	600	606	mV
		T_J = -40°C to +125°C	591	600	609	
FB current	I_{FB}	V_{FB} = 0.63V		50	100	nA
P-channel high-side MOSFET (HS-FET) on resistance	$R_{DS(ON)\_HS}$	V_{IN} = 5V		75		mΩ
N-channel low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)\_LS}$	V_{IN} = 5V		45		mΩ
Switch leakage		V_{SW} = 0V and 6V, V_{EN} = 0V, V_{IN} = 6V, T_J = 25°C		0	1	μA
HS-FET peak current limit	I_{PEAK_HS}		2.8		4	A
LS-FET valley current limit	I_{PEAK_LS}			2.5		A
Zero-current detection (ZCD)				50		mA
On time	t_{ON}	V_{IN} = 5V, V_{OUT} = 1.2V	180	220	260	ns
		V_{IN} = 3.6V, V_{OUT} = 1.2V	240	300	360	
Switching frequency	f_{SW}	V_{OUT} = 1.2V		1100		kHz
Minimum off time	t_{MIN_OFF}			100		ns
Minimum on time (10)	t_{MIN_ON}			60		ns
Soft-start time	t_{SS}	10% to 90% V_{OUT} rise		0.5		ms
Maximum duty cycle			100			%
Enable (EN) start-up delay		EN on to SW active		150		μs
EN input logic low voltage					0.4	V
EN input logic high voltage			1.2			V
Output discharge resistor	$R_{DISCHARGE}$	V_{EN} = 0V, V_{OUT} = 1.2V		13		Ω
EN input current		V_{EN} = 2V		1.2		μA
		V_{EN} = 0V		0		μA
Shutdown current	I_{SD}	V_{EN} = 0V, T_J = 25°C		0	1	μA
Quiescent current	I_Q	V_{EN} = 2V, V_{FB} = 0.63V, V_{IN} = 5V, T_J = 25°C		25	30	μA
Output over-voltage protection (OVP) threshold	V_{OVP}		110	115	120	% of V_{FB}
Output OVP hysteresis	V_{OVP_HYS}			10		% of V_{FB}
OVP delay	t_{DELAY_OVP}			12		μs
Low-side current		Current flows from SW to GND		1.5		A
Absolute V_{IN} OVP		After V_{OUT} OVP is enabled		6.1		V
Absolute V_{IN} OVP hysteresis				400		mV

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 3.6V, T_J = -40°C to +125°C (9), typical value is tested at T_J = 25°C. The limit over temperature is guaranteed by characterization, unless otherwise noted.

Thermal shutdown (10)				160		°C
Thermal hysteresis (10)				30		°C

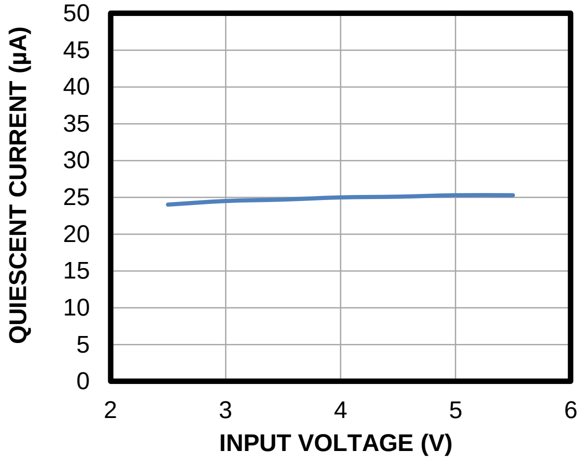
Notes:

9) Guaranteed by over-temperature correlation. Not tested in production.
10) Guaranteed by engineering sample characterization.

TYPICAL CHARACTERISTICS

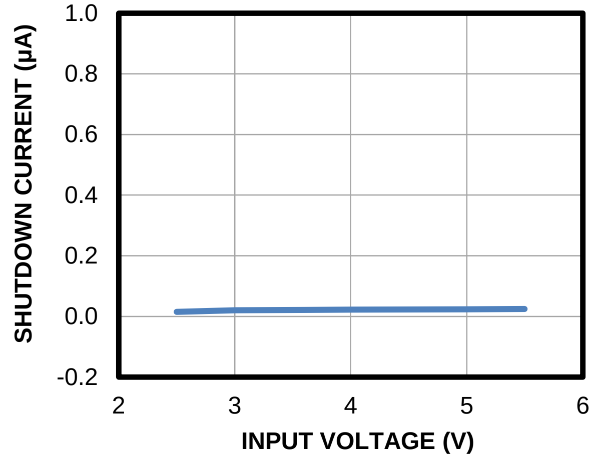
V_{IN} = 3.6V, V_{OUT} = 1.2V, L = 1µH, C_{OUT} = 22µF, T_A = 25°C, unless otherwise noted.

Quiescent Current vs. Input Voltage

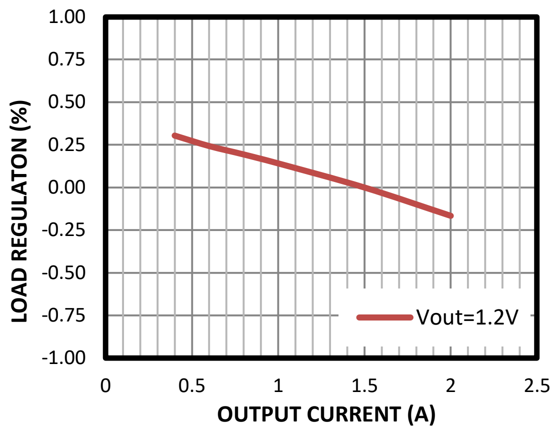


Shutdown Current vs. Input Voltage

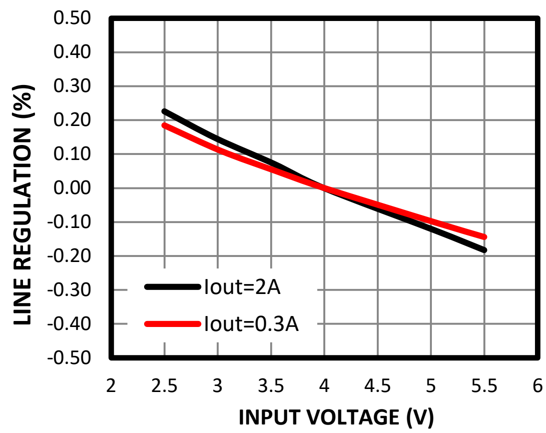
V_{EN} = 0V



Load Regulation

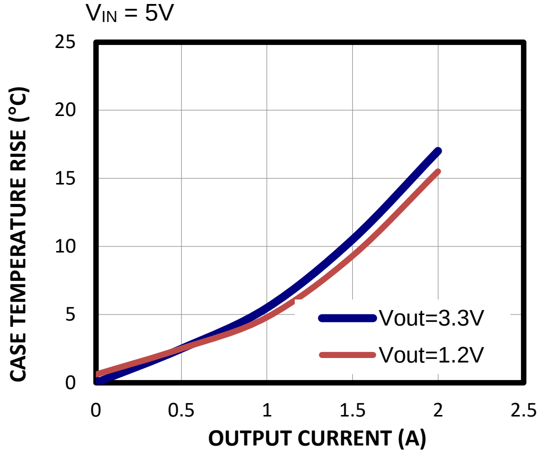


Line Regulation



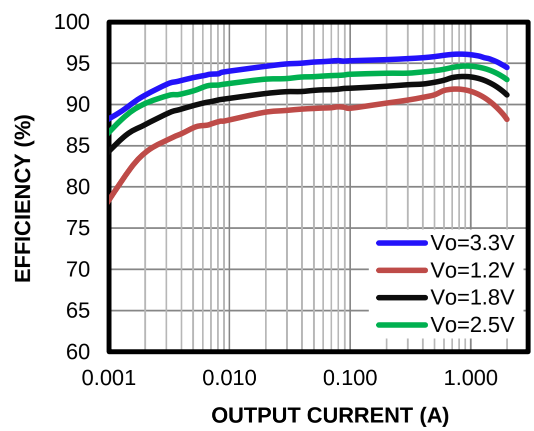
Case Temperature Rising

V_{IN} = 5V



Efficiency vs. Output Current

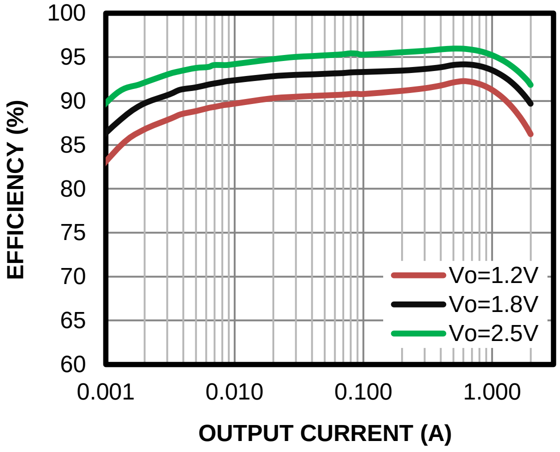
V_{IN} = 5V



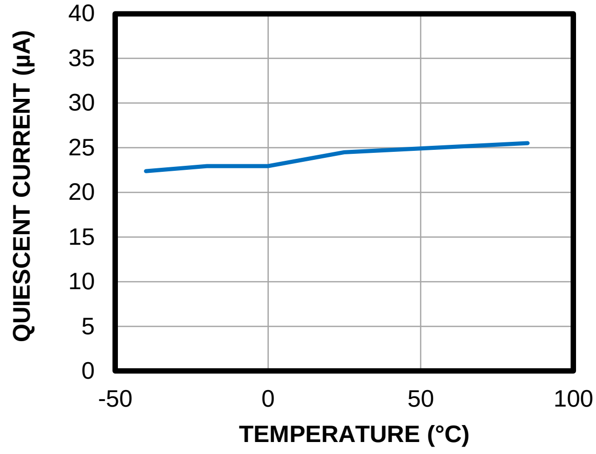
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 3.6V, V_{OUT} = 1.2V, L = 1µH, C_{OUT} = 22µF, T_A = 25°C, unless otherwise noted.

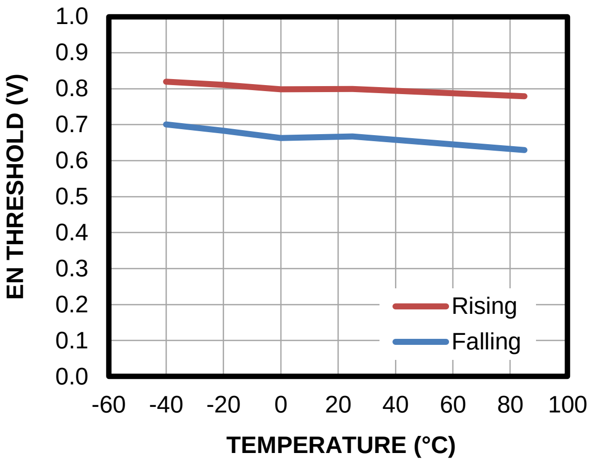
Efficiency vs. Output Current
V_{IN} = 3.6V



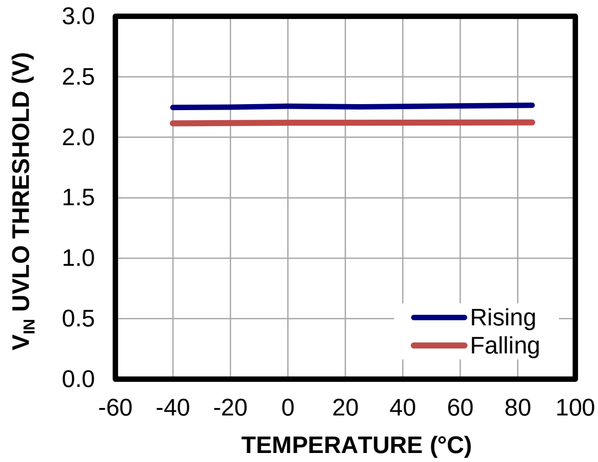
Quiescent Current vs. Temperature



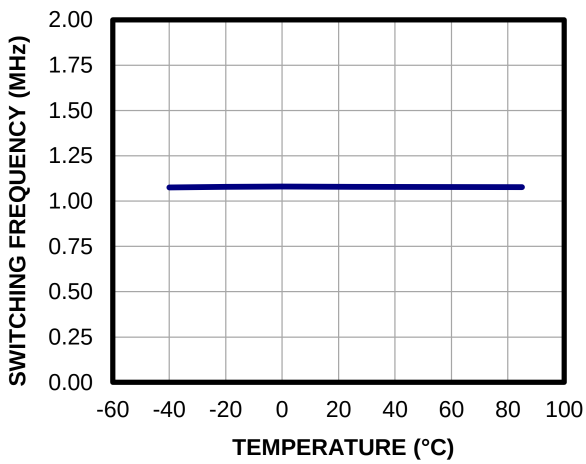
EN Threshold vs. Temperature



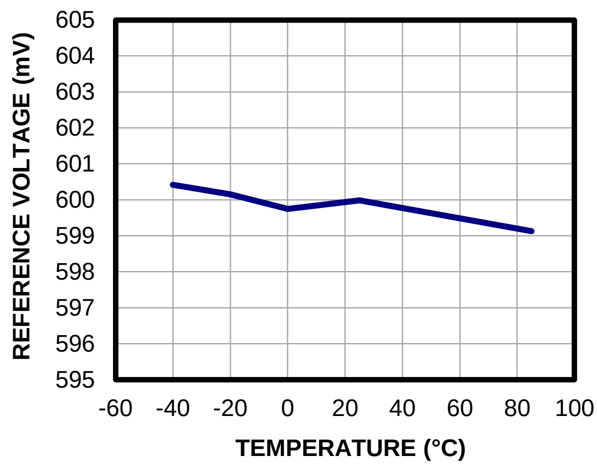
V_{IN} Threshold vs. Temperature



Switching Frequency vs. Temperature



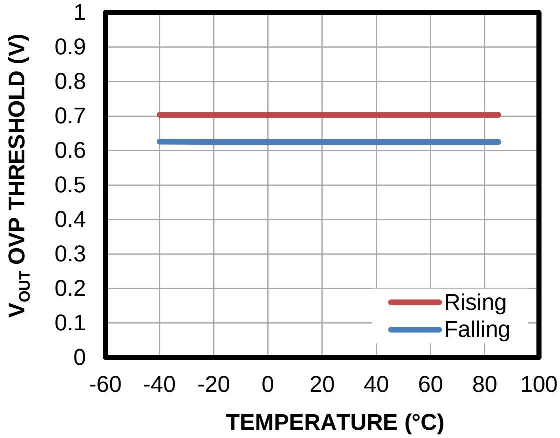
Reference Voltage vs. Temperature



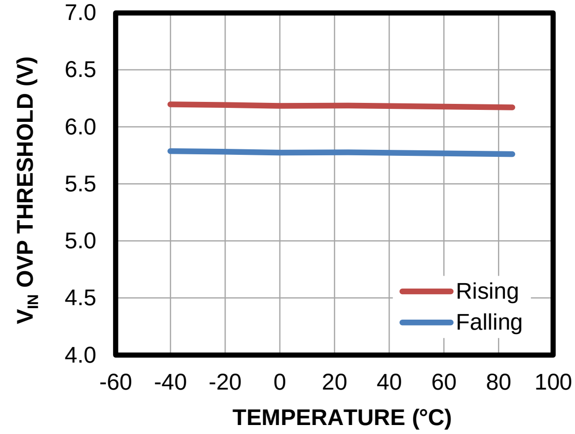
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 3.6V, V_{OUT} = 1.2V, L = 1µH, C_{OUT} = 22µF, T_A = 25°C, unless otherwise noted.

V_{OUT} OVP Threshold vs. Temperature

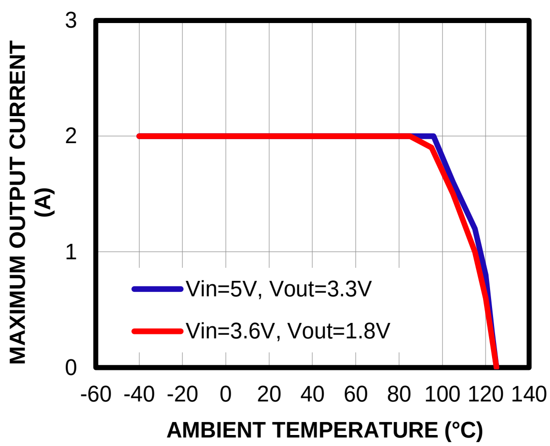


V_{IN} OVP Threshold vs. Temperature



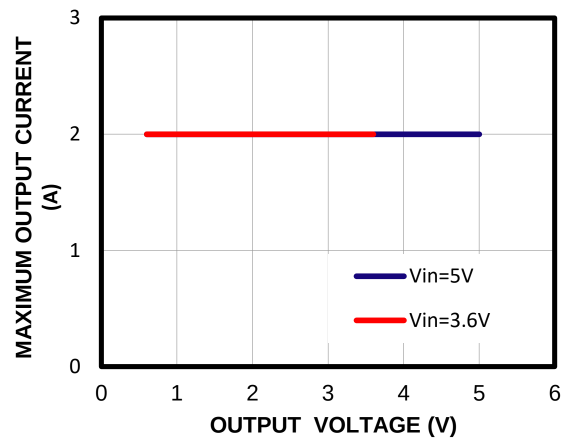
Maximum Output Current vs. Ambient Temperature

T_J ≤ 125°C

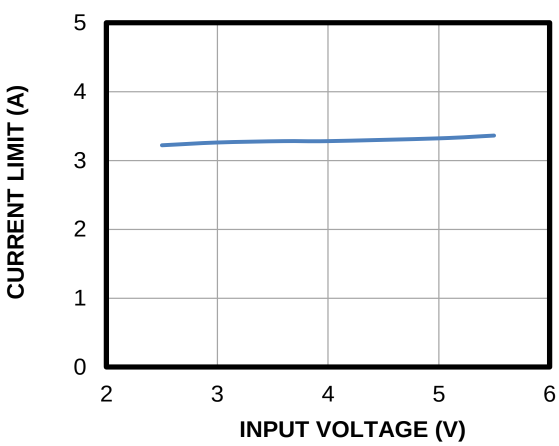


Output Current Derating vs. Output Voltage

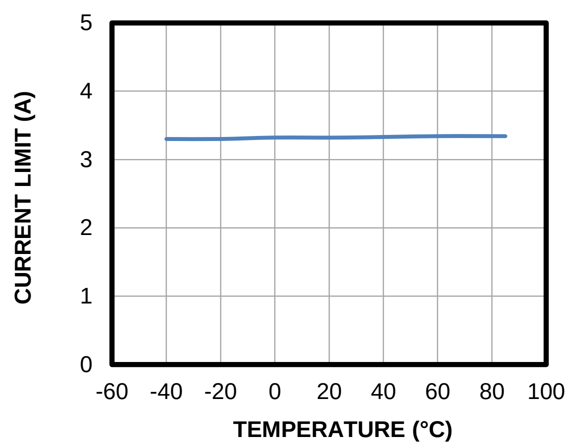
T_J ≤ 125°C



Peak Current Limit vs. Input Voltage



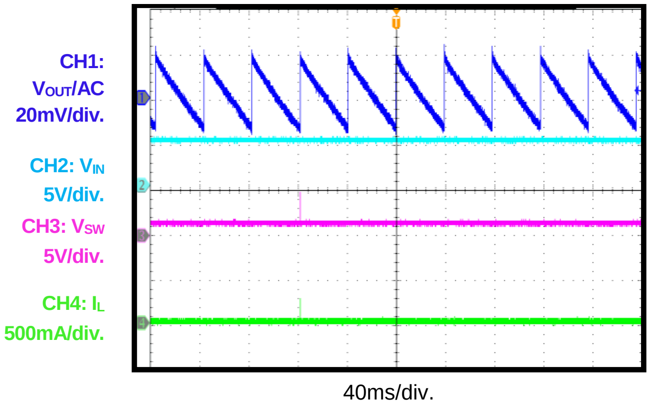
Peak Current Limit vs. Temperature



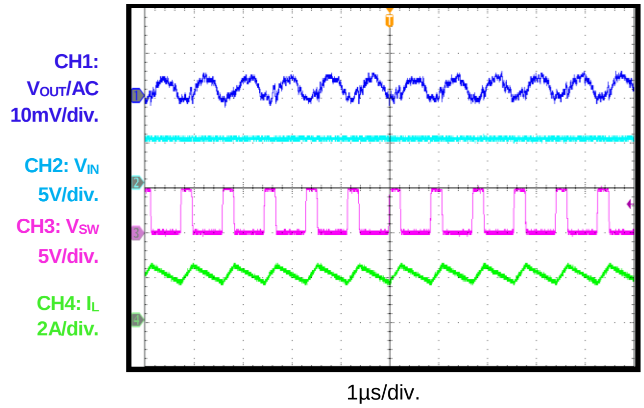
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, V_{OUT} = 1.2V, L = 1µH, C_{OUT} = 22µF, T_A = 25°C, unless otherwise noted.

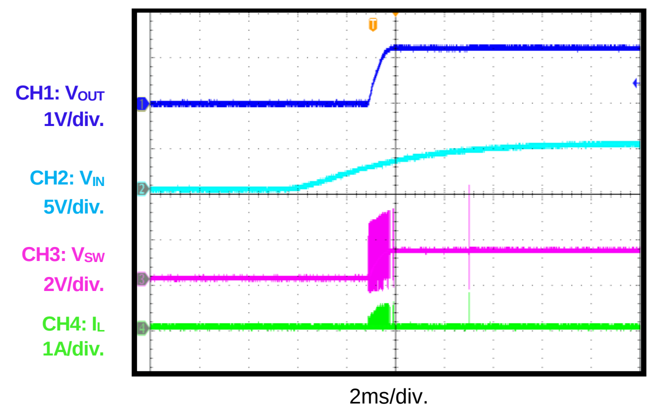
Steady State
I_{OUT} = 0A



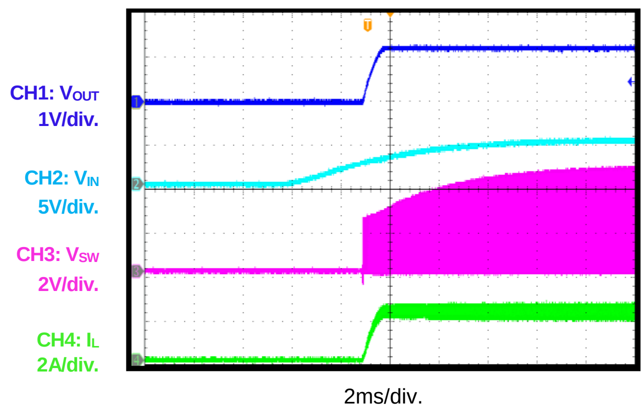
Steady State
I_{OUT} = 2A



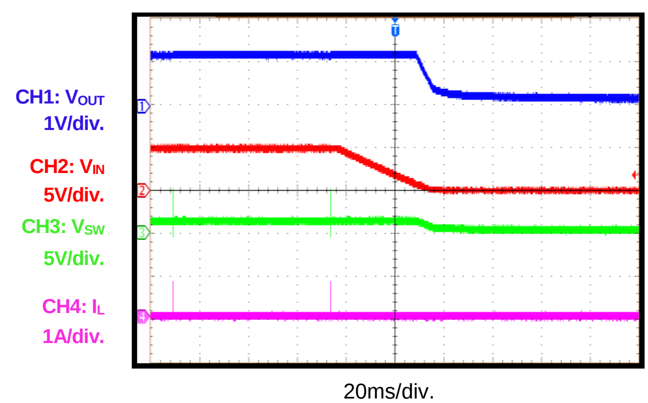
Start-Up through VIN
I_{OUT} = 0A



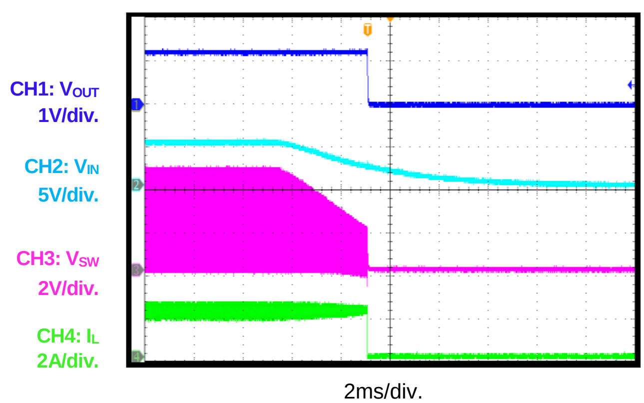
Start-Up through VIN
I_{OUT} = 2A



Shutdown through VIN
I_{OUT} = 0A



Shutdown through VIN
I_{OUT} = 2A

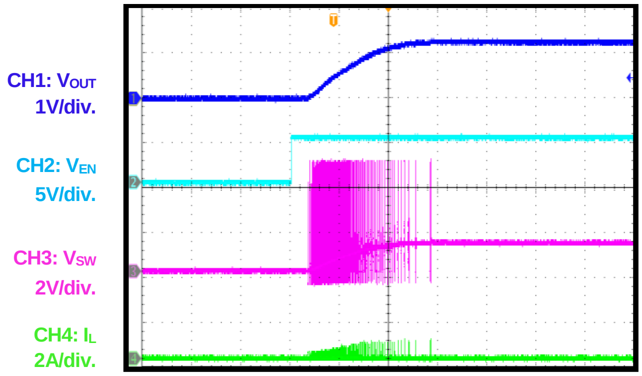


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.2V, L = 1µH, C_{OUT} = 22µF, T_A = 25°C, unless otherwise noted.

Start-Up through EN

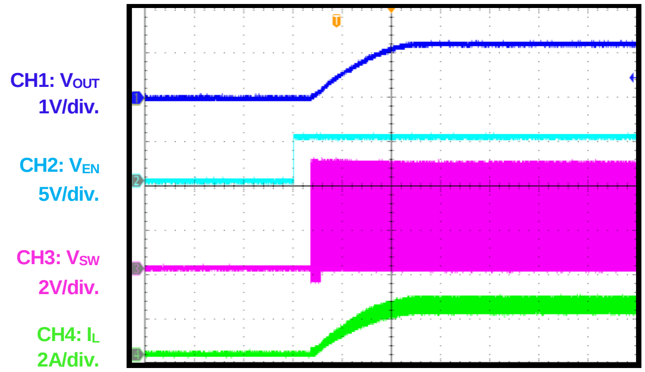
I_{OUT} = 0A



400µs/div.

Start-Up through EN

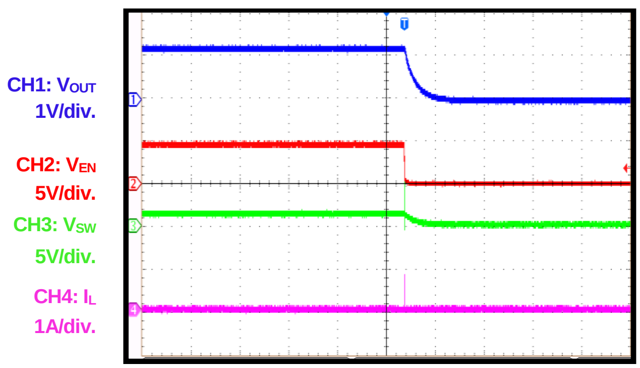
I_{OUT} = 2A



400µs/div.

Shutdown through EN

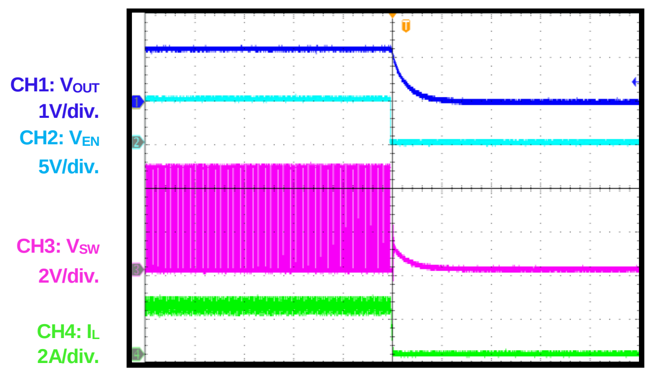
I_{OUT} = 0A



800µs/div.

Shutdown through EN

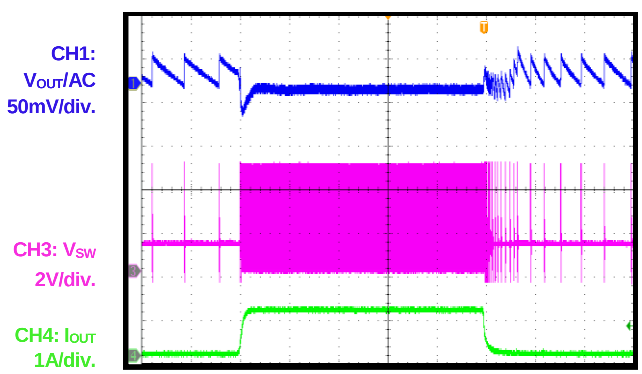
I_{OUT} = 2A



40µs/div.

Load Transient

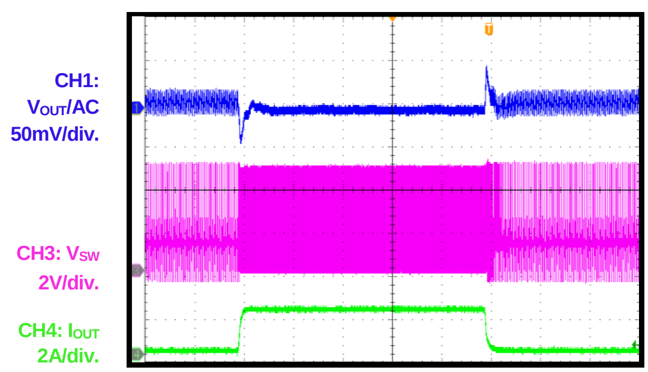
I_{OUT} = 0A to 1A, 1A/µs



100µs/div.

Load Transient

I_{OUT} = 0.1A to 2A, 1A/µs

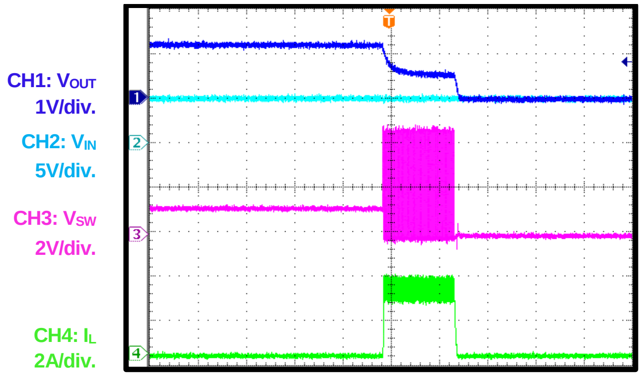


100µs/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

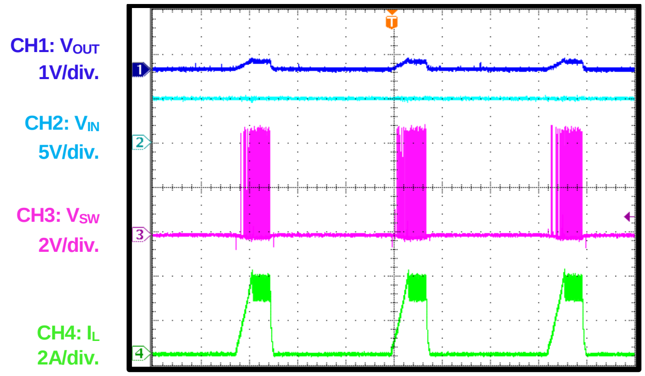
V_{IN} = 5V, V_{OUT} = 1.2V, L = 1µH, C_{OUT} = 22µF, T_A = 25°C, unless otherwise noted.

Short-Circuit Entry



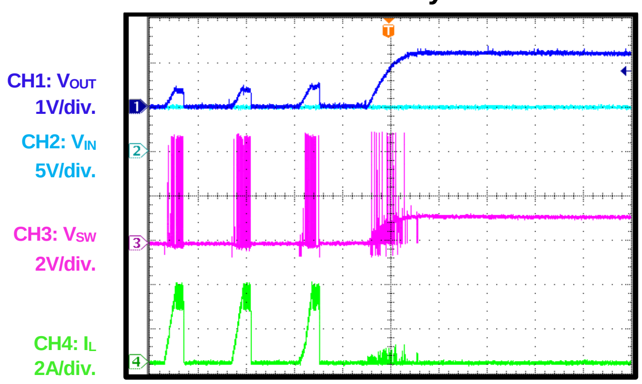
100µs/div.

Short-Circuit Protection



400µs/div.

Short-Circuit Recovery



1ms/div.

FUNCTIONAL BLOCK DIAGRAM

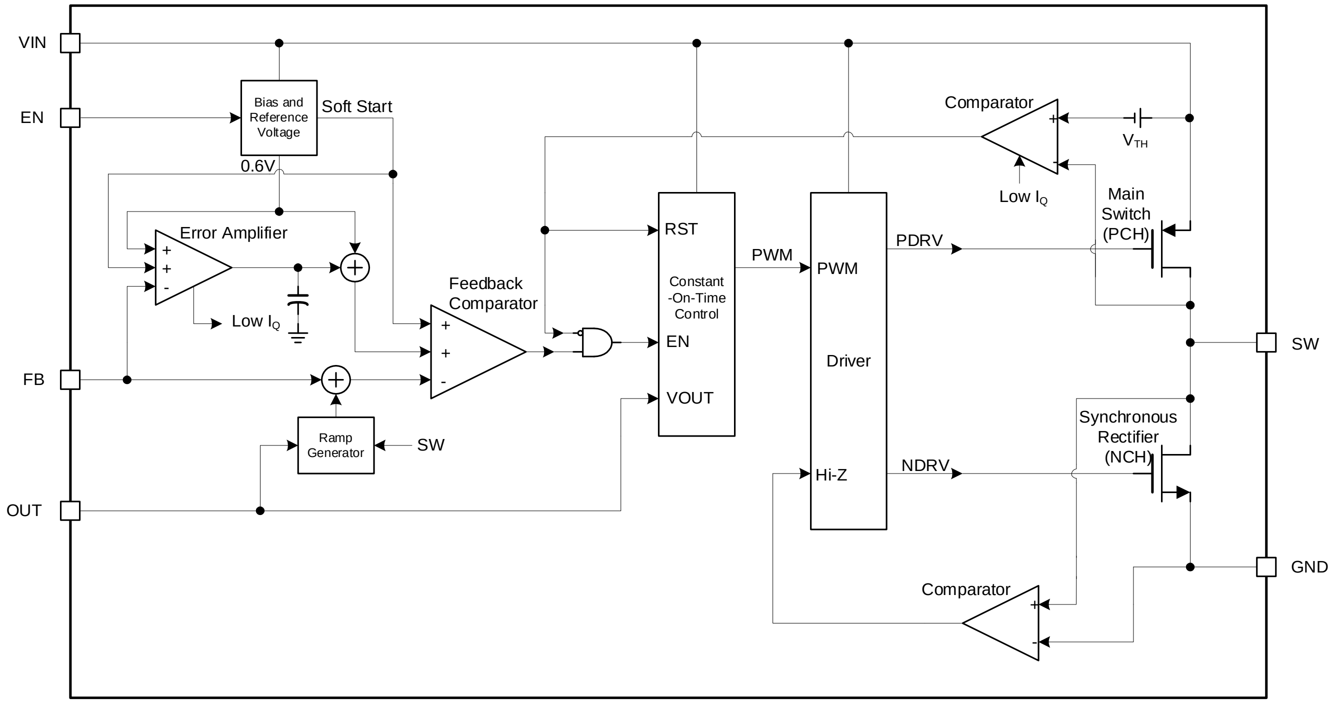


Figure 1: Functional Block Diagram

OPERATION

The MP2152D employs constant-on-time control (COT) and input voltage (V_{IN}) feed-forward to stabilize the switching frequency (f_{SW}) across the entire V_{IN} range. The device can achieve up to 2A of continuous output current (I_{OUT}) across a wide 2.5V to 5.5V V_{IN} range, with excellent load and line regulation. The output voltage (V_{OUT}) can be regulated to as low as 0.6V.

Constant-On-Time (COT) Control

Constant-on-time (COT) control offers a simpler control loop and fast transient response, compared to fixed-frequency pulse-width modulation (PWM) control. By using V_{IN} feed-forward, the MP2152D can maintain a fairly constant f_{SW} across the entire V_{IN} and V_{OUT} ranges. The switching pulse on time (t_{ON}) can be estimated with Equation (1):

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times 0.91\mu s \quad (1)$$

The IC has a fixed minimum off time (t_{MIN_OFF}) (100ns) to prevent inductor current (I_L) runaway during load transient.

Sleep Mode

The MP2152D employs sleep mode for high efficiency at extremely light loads. In sleep mode, most of the circuit blocks are turned off to reduce the input current to a minimum value (see Figure 2). The error amplifier (EA) and the PWM comparator remain on during sleep mode.

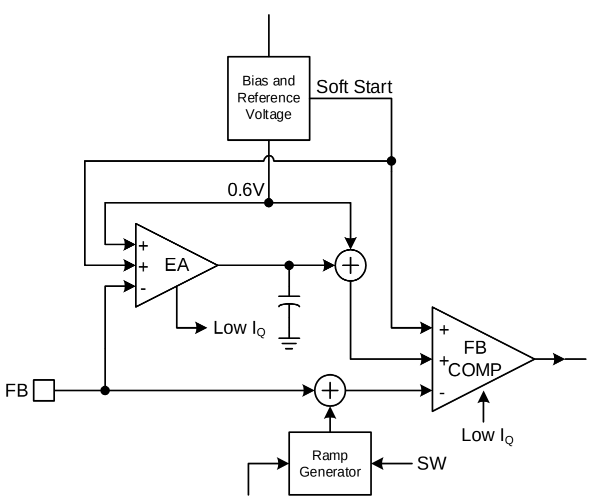


Figure 2: Operation Blocks in Sleep Mode

As the load decreases, the output voltage ripple (ΔV_{OUT}) increases and drives the EA output (EAO) low. If the EAO reaches its internal low threshold, then it clamps at this level and the device enters sleep mode. During sleep mode, the valley of the feedback (FB) voltage (V_{FB}) is regulated to the internal reference voltage (V_{REF}). This means that the average V_{OUT} is slightly exceeds the V_{OUT} in discontinuous conduction mode (DCM) or continuous conduction mode (CCM). The on-time pulse in sleep mode slightly exceeds that in DCM or CCM. Figure 3 shows the relationship between the average V_{FB} and V_{REF} in sleep mode.

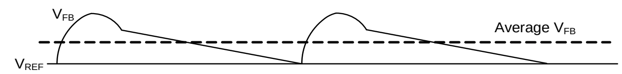


Figure 3: Average V_{FB} in Sleep Mode

In sleep mode, the average V_{OUT} exceeds the internal V_{REF}. The EAO is clamped low. If the load increases, the PWM switching t_{ON} decreases to regulate V_{OUT}. ΔV_{OUT} decreases relatively. Once the EAO exceeds its internal low threshold, the IC exits sleep mode and enters either DCM or CCM, depending on the load. In DCM or CCM, the EA regulates the average V_{OUT} to the internal V_{REF} (see Figure 4).

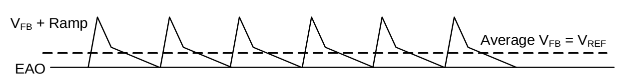


Figure 4: Discontinuous Conduction Mode

Due to the EA's clamping response time, there is a loading hysteresis while entering or exiting sleep mode.

Advanced Asynchronous Modulation (AAM) Mode under Light-Load Conditions

The MP2152D employs advanced asynchronous modulation (AAM) power-save mode together with zero current detection (ZCD) for light-load operation (see Figure 5).

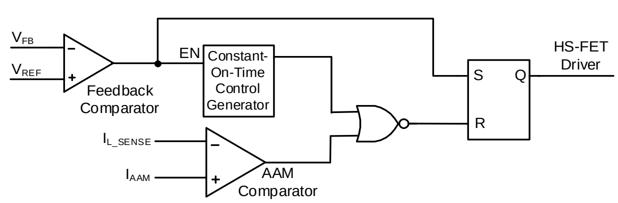


Figure 5: Simplified AAM Control Logic

The AAM current (I_{AAM}) is set internally. The SW on-time pulse is determined by the on-timer generator and AAM comparator. If the AAM comparator pulse is longer than the on-timer generator pulse, then the part operates in AAM mode (see Figure 6).

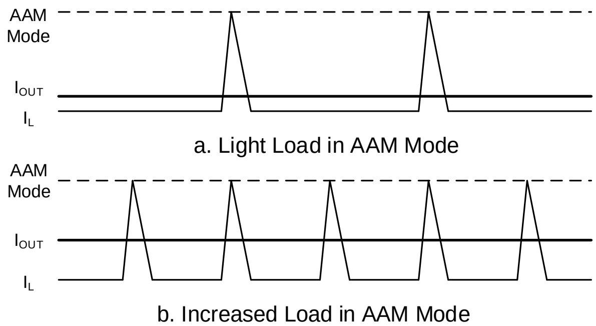


Figure 6: Simplified AAM Control Logic

If the AAM comparator pulse is shorter than the COT generator pulse, then the part operates in AAM mode (see Figure 7).

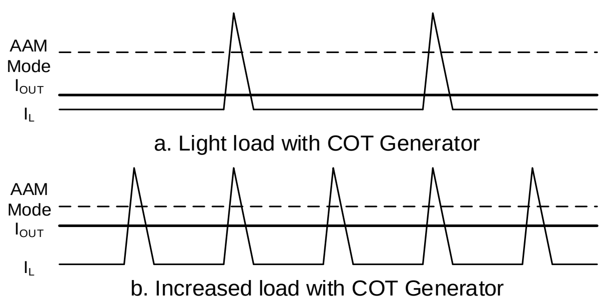


Figure 7: On-Time Control t_{ON}

Figure 8 shows that the AAM threshold decreases as t_{ON} increases gradually. In CCM, I_{OUT} should be at least half of the AAM threshold. Typically, the AAM threshold is below I_L during a normal duty cycle.

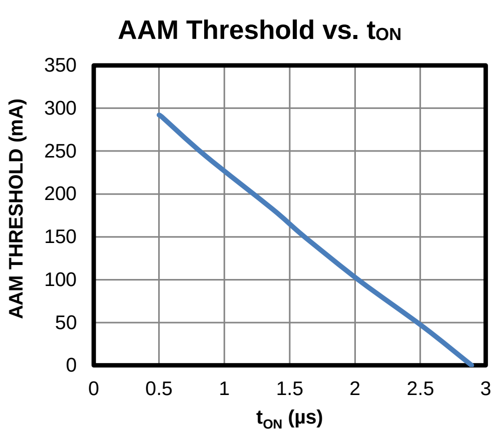


Figure 8: AAM Threshold Decreases as t_{ON} Increases

ZCD determines whether I_L has reversed. If I_L reaches the ZCD threshold, then the low-side MOSFET (LS-FET) turns off.

AAM mode and a ZCD circuit allow the MP2152D to operate in DCM at light loads, even if V_{OUT} is close to V_{IN}.

Enable (EN)

The enable (EN) pin enables and disables the MP2152D. Pull EN above 1.2V to turn the converter on; float EN or pull EN to GND to turn it off. If V_{IN} exceeds the under-voltage lockout (UVLO) threshold (typically 2.3V), then the part turns off. It can be turned on again once EN exceeds 1.2V. There is an internal 1MΩ resistor connected between the EN pin and GND.

If the MP2152D turns off, then the IC enters output discharge mode. Its internal discharge MOSFET provides a resistive discharge path for the output capacitor (C2).

Soft Start (SS)

The MP2152D has a built-in soft start (SS) that ramps up V_{OUT} at a controlled slew rate to avoid overshoot during start-up. The soft-start time (t_{SS}) is typically 1ms.

Current Limit

The MP2152D's HS-FET has a 4A maximum current limit (I_{LIMIT}). If the HS-FET exceeds its current limit, then the MP2152D operates in hiccup mode until the current drops below 4A. This prevents I_L from rising and damaging components.

Short Circuit Protection (SCP) and Recovery

If I_{LIMIT} has been exceeded, then short-circuit protection (SCP) is triggered. SCP hiccup mode is used to recover from the over-current (OC) fault. In hiccup mode, the output power stage is disabled and the soft-start capacitor (C_{SS}) is discharged, then the IC initiates an SS. If the short circuit remains once SS is complete, then the IC repeats the operation until the short circuit is removed and V_{OUT} rises to its regulation level.

Output Over-Voltage Protection (OVP)

The MP2152D monitors V_{FB} to detect over-voltage (OV) faults. If V_{FB} exceeds 115% of its target voltage, then the converter enters a dynamic regulation period. During this period, the LS-FET turns off once the LS-FET current

(I_{LS-FET}) drops to -1.5A. This discharges V_{OUT} to keep it within its normal range. If the OV condition remains, then the LS-FET turns on after a delay (1µs). The MP2152D exits this regulation period once the V_{FB} drops below 105% of V_{REF}.

If the dynamic regulation cannot limit the increasing V_{OUT} once V_{IN} exceeds 6.1V, then input over-voltage protection (OVP) is triggered. The MP2152D stops switching until V_{IN} drops below 5.7V. Once V_{IN} drops below 5.7V, then the IC resumes normal operation.

APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider sets V_{OUT} (see Figure 11 on page 17). Choose a FB resistor (R1) that reduces the V_{OUT} leakage current to between 100kΩ and 200kΩ. There is no strict requirement for the R1. The FB resistor (R2) can then be calculated with Equation (2):

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.6} - 1} \quad (2)$$

Where R1 is 10kΩ.

Figure 9 shows the feedback circuit.

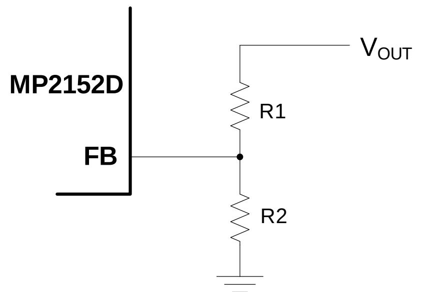


Figure 9: Feedback Network

Table 1 lists the recommended resistor values for common output voltages.

Table 1: Resistor Values for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
1	200 (1%)	300 (1%)
1.2	200 (1%)	200 (1%)
1.8	200 (1%)	100 (1%)
2.5	200 (1%)	63.2 (1%)
3.3	200 (1%)	44.2 (1%)

Selecting the Inductor

Most applications work best with a 1-2.2µH inductor. Select an inductor with a DC resistance less than 50mΩ to optimize efficiency.

Select an inductor with a DC resistance below 50mΩ to improve efficiency. For most applications, a 1µH to 2.2µH inductor is sufficient.

A high-frequency, switch-mode power supply with a magnetic device has strong electromagnetic inference. Unshielded power inductors should not be used in application. It is recommended to use metal alloy or multi-layer chip shielded power inductors, as they can reduce the electromagnetic interference.

For most designs, the inductance (L_1) can be calculated with Equation (3):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{SW}} \quad (3)$$

Where ΔI_L is the inductor ripple current.

Choose I_L to be approximately 30% of the maximum load current (I_{LOAD_MAX}). The maximum inductor peak current ($I_{L\_PEAK\_MAX}$) can be calculated with Equation (4):

$$I_{L\_PEAK\_MAX} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (4)$$

MPS inductors are optimized and tested for use with our complete line of integrated circuits. Table 2 lists the recommended inductor.

Table 2: Suggested Inductor

Manufacturer P/N	Inductance	Manufacturer
MPL-AL4020-1R0	1µH	MPS

Visit MonolithicPower.com under Products > Inductors for more information.

Selecting the Input Capacitor (C1)

The step-down converter has a discontinuous input current (I_{IN}), and requires a capacitor to supply AC current to the step-down converter while maintaining the DC V_{IN}. Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are recommended due to their low ESR and small temperature coefficients. For most applications, a 22µF capacitor is sufficient. Higher output voltages may require a 44µF capacitor to increase system stability.

C1 requires an adequate ripple current rating to absorb the switching I_{IN}. The RMS current in C1 (I_{C1}) can be estimated with Equation (5):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (5)$$

The worst case condition occurs at $V_{IN} = 2V_{OUT}$, which can be calculated with Equation (6):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (6)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of I_{LOAD_MAX}. C1 can be electrolytic, tantalum, or ceramic.

When using electrolytic or tantalum capacitors, add a small, high-quality, 0.1μF ceramic capacitor as close to the IC as possible.

When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge and prevent excessive voltage ripple at the input. The input voltage ripple (ΔV_{IN}) caused by the capacitance can be estimated with Equation (7):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (7)$$

Selecting the Output Capacitor (C2)

The output capacitor (C2) stabilizes the DC V_{OUT}. Low ESR ceramic capacitors are recommended to limit ΔV_{OUT}. ΔV_{OUT} can be estimated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C2}\right) \quad (8)$$

Where R_{ESR} is the equivalent series resistance (ESR) of C2.

When using ceramic capacitors, the capacitance dominates the impedance at f_{SW} and causes most of ΔV_{OUT}. For simplification, ΔV_{OUT} can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (9)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at f_{SW}. For simplification, ΔV_{OUT} can be estimated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (10)$$

The characteristics of C2 also affect the stability of the regulation system.

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. A poor layout design can result in poor line and load regulation, as well as stability issues. For the best results, refer to Figure 10 and follow the guidelines below:

1. Place the high-current paths (GND, VIN, and SW) as close to the device as possible using short, direct, and wide traces.
2. Place the input capacitor (C1) as close to VIN and GND as possible.
3. Place the external feedback resistors close to the FB pin.
4. Keep the switching node (SW) short and away from the feedback network.
5. Keep the output voltage sense line as short as possible and away from the power inductor, especially the surrounding inductor.

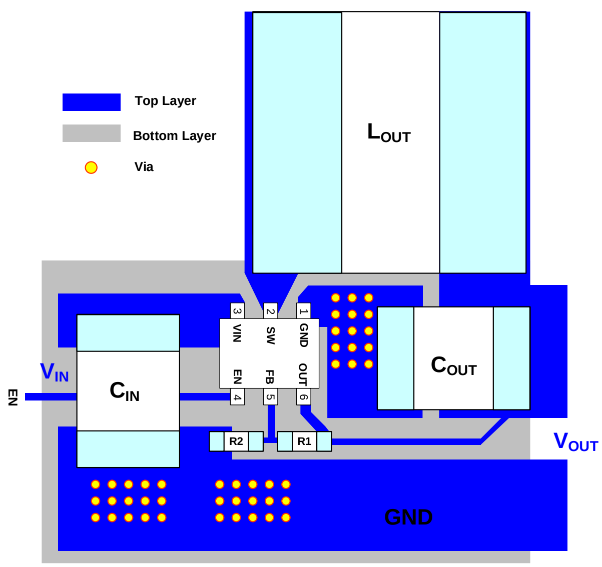


Figure 10: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

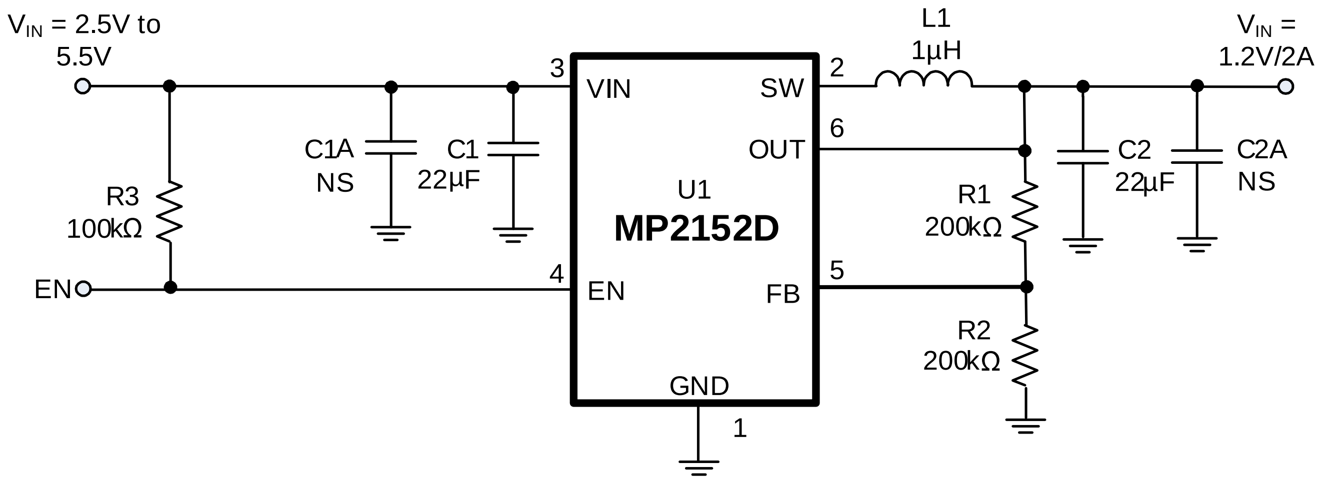


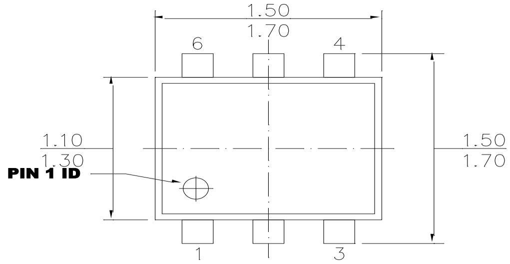
Figure 11: Typical Application Circuit

Note:

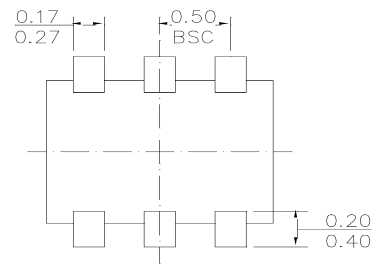
11) If V_{IN} is below 3.3V, then the application circuit may require more input capacitors.

PACKAGE INFORMATION

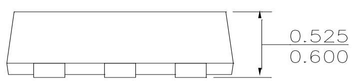
SOT563



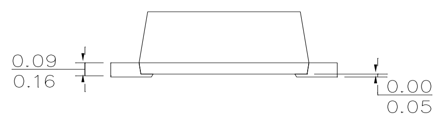
TOP VIEW



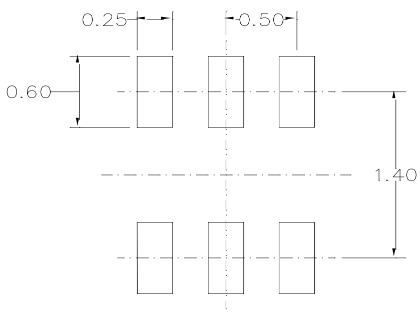
BOTTOM VIEW



FRONT VIEW



SIDE VIEW



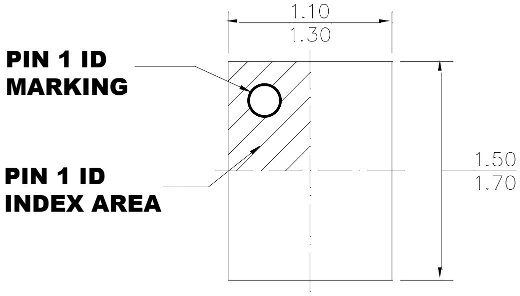
RECOMMENDED LAND PATTERN

NOTE:

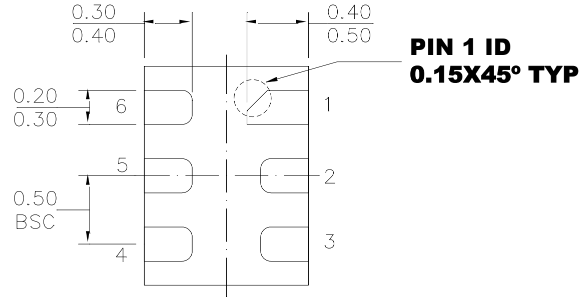
1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING IS NOT TO SCALE.

PACKAGE INFORMATION *(continued)*

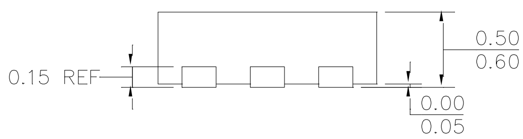
UTQFN-6 (1.2mmx1.6mm)



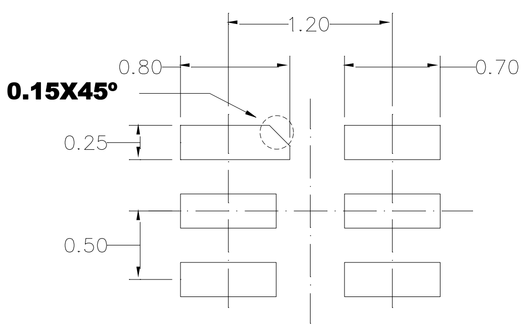
TOP VIEW



BOTTOM VIEW



SIDE VIEW

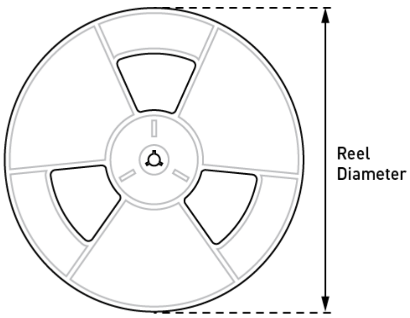


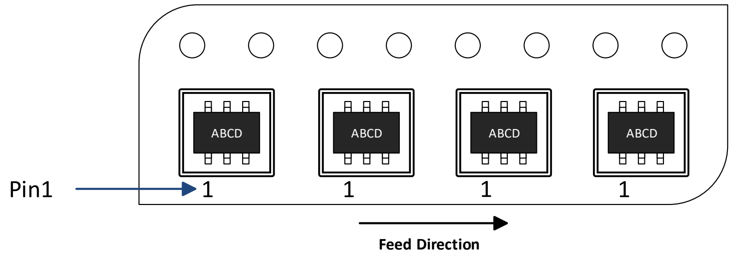
RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION





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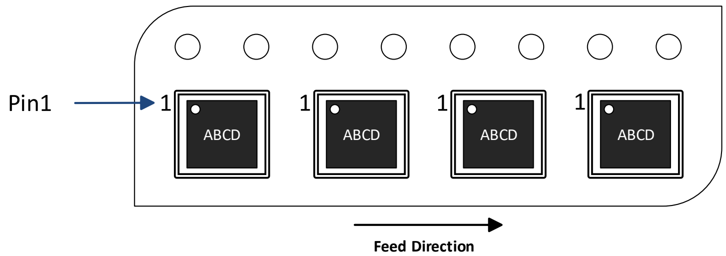

UTQFN-6 (1.2mmx1.6mm)

Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP2152DGTF-Z	SOT563	5000	N/A	7in	8mm	4mm
MP2152DGQFU-Z	UTQFN-6 (1.2mmx1.6mm)	5000	N/A	13in	8mm	4mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	11/18/2021	Initial Release	-