LPDDR SDRAM

512K x 32 Bit x 4 Banks
Low Power DDR SDRAM

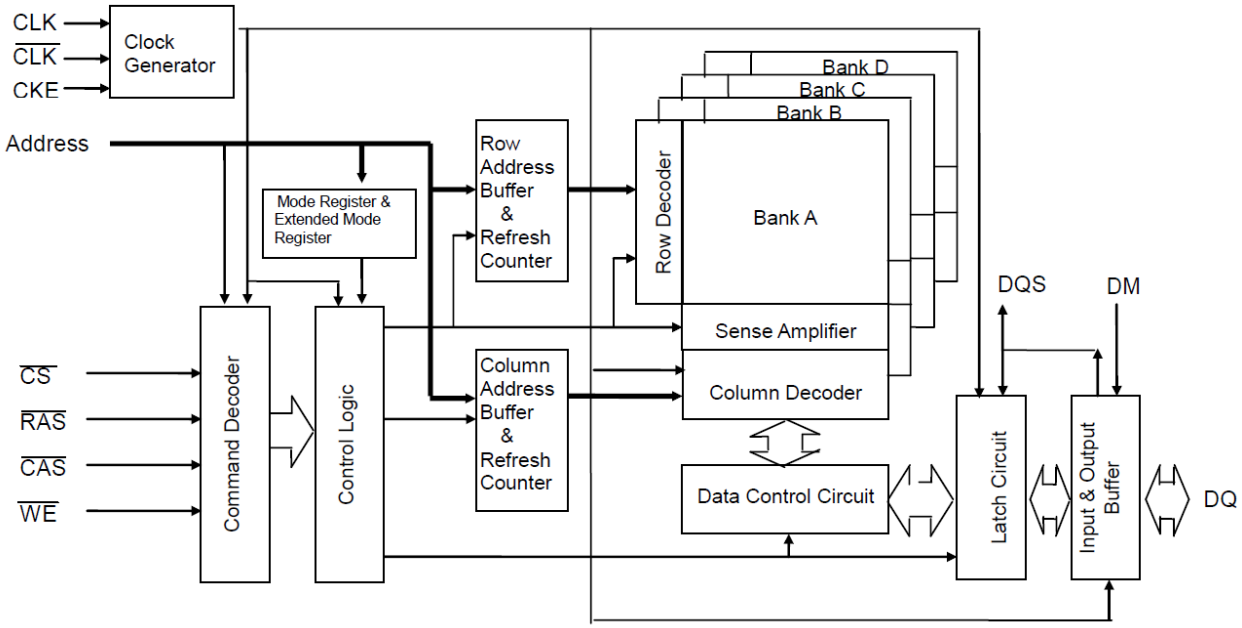
Features

- JEDEC Standard
- Internal pipelined double-data-rate architecture, two data access per clock cycle
- Bi-directional data strobe (DQS)
- No DLL; CLK to DQS is not synchronized.
- Differential clock inputs (CLK and $\overline{CLK}$)
- Four bank operation
- CAS Latency : 2, 3
- Burst Type : Sequential and Interleave
- Burst Length : 2, 4, 8, 16 & full page
- Special function support
  - DS (Drive Strength)
  - Deep Power Down Mode (DPD Mode)
- All inputs except data & DM are sampled at the rising edge of the system clock(CLK)
- DQS is edge-aligned with data for READ; center-aligned with data for WRITE
- Data mask (DM) for write masking only
- V_{DD} = 1.7V ~ 1.95V
- V_{DDQ} = 1.7V ~ 1.95V
- Auto & Self refresh
- 15.6us refresh interval (64ms refresh period, 4K cycle)
- LVCMOS-compatible inputs

Ordering Information

Product ID	Max Freq.	V_{DD}	Package	Comments
M13D64322A -4BG2S	250MHz	1.8V	144 ball FBGA	Pb-free
M13D64322A -4.5BG2S	222MHz			
M13D64322A -5BG2S	200MHz			

Functional Block Diagram



BALL CONFIGURATION (TOP VIEW)

(BGA144, 12mmX12mmX1.4m Body, 0.8mm Ball Pitch)

	2	3	4	5	6	7	8	9	10	11	12	13
B	DQS0	DM0	VSSQ	DQ3	DQ2	DQ0	DQ31	DQ29	DQ28	VSSQ	DM3	DQS3
C	DQ4	VDDQ	NC	VDDQ	DQ1	VDDQ	VDDQ	DQ30	VDDQ	NC	VDDQ	DQ27
D	DQ6	DQ5	VSSQ	VSSQ	VSSQ	VDD	VDD	VSSQ	VSSQ	VSSQ	DQ26	DQ25
E	DQ7	VDDQ	VDD	VSS	VSSQ	VSS	VSS	VSSQ	VSS	VDD	VDDQ	DQ24
F	DQ17	DQ16	VDDQ	VSSQ	VSS Thermal	VSS Thermal	VSS Thermal	VSS Thermal	VSSQ	VDDQ	DQ15	DQ14
G	DQ19	DQ18	VDDQ	VSSQ	VSS Thermal	VSS Thermal	VSS Thermal	VSS Thermal	VSSQ	VDDQ	DQ13	DQ12
H	DQS2	DM2	NC	VSSQ	VSS Thermal	VSS Thermal	VSS Thermal	VSS Thermal	VSSQ	NC	DM1	DQS1
J	DQ21	DQ20	VDDQ	VSSQ	VSS Thermal	VSS Thermal	VSS Thermal	VSS Thermal	VSSQ	VDDQ	DQ11	DQ10
K	DQ22	DQ23	VDDQ	VSSQ	VSS	VSS	VSS	VSS	VSSQ	VDDQ	DQ9	DQ8
L	$\overline{CAS}$	$\overline{WE}$	VDD	VSS	A10/AP	VDD	VDD	NC	VSS	VDD	NC	NC
M	$\overline{RAS}$	NC	NC	BA1	A2	NC	A9	A5	NC	CLK	$\overline{CLK}$	NC
N	$\overline{CS}$	NC	BA0	A0	A1	A3	A4	A6	A7	A8	CKE	NC

Ball Description

Ball Name	Function	Ball Name	Function
A0~A10, BA0~BA1	Address inputs - Row address A0~A10 - Column address A0~ A7 A10/AP : AUTO Precharge BA0~BA1 : Bank selects (4 Banks)	DM0~DM3	DM is an input mask signal for write data. DM0 corresponds to the data on DQ0~DQ7; DM1 correspond to the data on DQ8~DQ15; DM2 correspond to the data on DQ16~DQ23; DM3 correspond to the data on DQ24~DQ31.
DQ0~DQ31	Data-in/Data-out	CLK, $\overline{CLK}$	Clock input
$\overline{RAS}$	Row address strobe	CKE	Clock enable
$\overline{CAS}$	Column address strobe	$\overline{CS}$	Chip select
$\overline{WE}$	Write enable	V_{DDQ}	Supply Voltage for DQ
V_{SS}	Ground	V_{SSQ}	Ground for DQ
V_{DD}	Power	NC	No connection
DQS0~DQS3	Bi-directional Data Strobe. DQS0 corresponds to the data on DQ0~DQ7; DQS1 correspond to the data on DQ8~DQ15; DQS2 correspond to the data on DQ16~DQ23; DQS3 correspond to the data on DQ24~DQ31.		

Absolute Maximum Rating

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 ~ 2.7	V
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}	-0.5 ~ 2.7	V
Voltage on V_{DDQ} supply relative to V_{SS}	V_{DDQ}	-0.5 ~ 2.7	V
Operating ambient temperature	T_A	0 ~ +70	℃
Storage temperature	T_{STG}	-55 ~ +150	℃
Power dissipation	P_D	1.0	W
Short circuit current	I_{OS}	50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommend operation condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC Operation Condition & Specifications

DC Operation Condition

Recommended operating conditions (Voltage reference to V_{SS} = 0V)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage	V_{DD}	1.7	1.95	V	
I/O Supply voltage	V_{DDQ}	1.7	1.95	V	
Input logic high voltage (for Address and Command)	V_{IH} (DC)	0.8 x V_{DDQ}	V_{DDQ} + 0.3	V	
Input logic low voltage (for Address and Command)	V_{IL} (DC)	-0.3	0.2 x V_{DDQ}	V	
Input logic high voltage (for DQ, DM, DQS)	V_{IHD} (DC)	0.7 x V_{DDQ}	V_{DDQ} + 0.3	V	
Input logic low voltage (for DQ, DM, DQS)	V_{ILD} (DC)	-0.3	0.3 x V_{DDQ}	V	
Output logic high voltage	V_{OH} (DC)	0.9 x V_{DDQ}	-	V	I_{OH} = -0.1mA
Output logic low voltage	V_{OL} (DC)	-	0.1 x V_{DDQ}	V	I_{OL} = 0.1mA
Input Voltage Level, CLK and $\overline{CLK}$ inputs	V_{IN} (DC)	-0.3	V_{DDQ} + 0.3	V	
Input Differential Voltage, CLK and $\overline{CLK}$ inputs	V_{ID} (DC)	0.4 x V_{DDQ}	V_{DDQ} + 0.6	V	1
Input leakage current	I_I	-2	2	μ A	
Output leakage current	I_{OZ}	-5	5	μ A	

Note:

1. V_{ID} is the magnitude of the difference between the input level on CLK and the input level on $\overline{CLK}$.

DC Characteristics

Recommended operating condition (Voltage reference to V_{SS} = 0V)

Parameter	Symbol	Test Condition		Version			Unit
				-4	-4.5	-5	
Operating Current (One Bank Active)	I_{DD0}	t_{RC}= t_{RC} (min); t_{CK} = t_{CK} (min); CKE = HIGH; $\overline{CS}$ = HIGH between valid commands; address inputs are SWITCHING; data input signals are STABLE		35	35	30	mA
Precharge Standby Current in power-down mode	I_{DD2P}	All banks idle, CKE = LOW; $\overline{CS}$ = HIGH, t_{CK} = t_{CK} (min); address & control inputs are SWITCHING; data input signals are STABLE		600			μ A
	I_{DD2PS}	All banks idle, CKE = LOW; $\overline{CS}$ = HIGH, CLK = LOW, $\overline{CLK}$ = HIGH; address & control inputs are SWITCHING; data input signals are STABLE		600			μ A
Precharge Standby Current in non power-down mode	I_{DD2N}	All banks idle, CKE = HIGH; $\overline{CS}$ = HIGH, t_{CK} = t_{CK} (min); address & control inputs are SWITCHING; data input signals are STABLE		15	15	15	mA
	I_{DD2NS}	All banks idle, CKE = HIGH; $\overline{CS}$ = HIGH, CLK = LOW, $\overline{CLK}$ = HIGH; address & control inputs are SWITCHING; data input signals are STABLE		7	6	6	mA
Active Standby Current in power-down mode	I_{DD3P}	One bank active, CKE = LOW; $\overline{CS}$ = HIGH, t_{CK} = t_{CK} (min); address & control inputs are SWITCHING; data input signals are STABLE		4			mA
	I_{DD3PS}	One bank active, CKE = LOW; $\overline{CS}$ = HIGH, CLK = LOW, $\overline{CLK}$ = HIGH; address & control inputs are SWITCHING; data input signals are STABLE		3			mA
Active Standby Current in non power-down mode (One Bank Active)	I_{DD3N}	One bank active, CKE = HIGH, $\overline{CS}$ = HIGH, t_{CK} = t_{CK} (min); address & control inputs are SWITCHING; data input signals are STABLE		15	15	15	mA
	I_{DD3NS}	One bank active, CKE = HIGH; $\overline{CS}$ = HIGH, CLK= LOW, $\overline{CLK}$ = HIGH; address & control inputs are SWITCHING; data input signals are STABLE		8	8	8	mA
Operating Current (Burst Mode)	I_{DD4R}	One bank active; BL=4; CL=3; t_{CK} = t_{CK} (min); continuous read bursts; I_{OUT} = 0 mA; address inputs are SWITCHING; 50% data changing each burst		60	60	50	mA
	I_{DD4W}	One bank active; BL=4; t_{CK} = t_{CK} (min); continuous write bursts; I_{OUT} = 0 mA; address inputs are SWITCHING; 50% data changing each burst		60	60	55	mA
Auto Refresh Current	I_{DD5}	Burst refresh; t_{CK} = t_{CK} (min); CKE = HIGH; address inputs are SWITCHING; data input signals are STABLE	t_{RFC}= t_{RFC}(min)	55	55	50	mA
	I_{DD5A}		t_{RFC}= t_{REFI}	15	15	10	mA

Self Refresh Current	I_{DD6}	CKE = LOW, CLK = LOW, $\overline{CLK}$ = HIGH; EMRS set to all 0's; address & control & data bus inputs are STABLE	700	700	700	μA
Deep Power Down Current	I_{DD8}	address & control & data inputs are STABLE	30			μA

Note: 1. Input slew rate is 1V/ns.

2. I_{DD} specifications are tested after the device is properly initialized.

3. Definitions for I_{DD}: LOW is defined as $V_{IN} \leq 0.1 * V_{DDQ}$;

HIGH is defined as $V_{IN} \geq 0.9 * V_{DDQ}$;

STABLE is defined as inputs stable at a HIGH or LOW level;

SWITCHING is defined as: - address and command: inputs changing between HIGH and LOW once per two clock cycles;

- data bus inputs: DQ changing between HIGH and LOW once per clock cycle; DM and DQS are STABLE.

AC Operation Conditions & Timing Specification

AC Operation Conditions

Parameter	Symbol	Min	Max	Unit	Note
Input High (Logic 1) Voltage, DQ, DQS and DM signals	V_{IHD}(AC)	0.8 x V_{DDQ}	V_{DDQ}+0.3	V	
Input Low (Logic 0) Voltage, DQ, DQS and DM signals	V_{ILD}(AC)	-0.3	0.2 x V_{DDQ}	V	
Input Differential Voltage, CLK and $\overline{CLK}$ inputs	V_{ID}(AC)	0.6 x V_{DDQ}	V_{DDQ}+0.6	V	1
Input Crossing Point Voltage, CLK and $\overline{CLK}$ inputs	V_{IX}(AC)	0.4 x V_{DDQ}	0.6 x V_{DDQ}	V	2

Note: 1. V_{ID} is the magnitude of the difference between the input level on CLK and the input on $\overline{CLK}$.
2. The value of V_{IX} is expected to equal 0.5*V_{DDQ} of the transmitting device and must track variations in the DC level of the same.

Input / Output Capacitance

(V_{DD} = 1.8V, V_{DDQ} =1.8V, T_A = 25 °C , f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0~A10, BA0~BA1, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN1}	2	4	pF
Input capacitance (CLK, $\overline{CLK}$)	C_{IN2}	2	4	pF
Data & DQS input/output capacitance	C_{OUT}	2	6	pF
Input capacitance (DM)	C_{IN3}	2	4	pF

AC Operating Test Conditions (V_{DD} = 1.7V~ 1.95V)

Parameter	Value	Unit
Input signal minimum slew rate	1.0	V/ns
Input levels (V_{IH}/V_{IL})	0.8 x V_{DDQ} / 0.2 x V_{DDQ}	V
Input timing measurement reference level	0.5 x V_{DDQ}	V
Output timing measurement reference level	0.5 x V_{DDQ}	V

AC Timing Parameter & Specifications

(V_{DD} = 1.7V~1.95V, V_{DDQ}=1.7V~1.95V)

Parameter		Symbol	-4		-4.5		-5		Unit	Note
			min	max	min	max	min	max		
Clock Period	CL3	t_{CK}	4		4.5		5		ns	12
	CL2		12		12		12		ns	
Access time from CLK/ $\overline{CLK}$	CL3	t_{AC}(3)	2	4.2	2	4.5	2	4.5	ns	
	CL2	t_{AC}(2)	2	6.5	2	6.5	2	6.5	ns	
CLK high-level width		t_{CH}	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}	
CLK low-level width		t_{CL}	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}	
Data strobe edge to clock edge	CL3	t_{DQSCK} (3)	2	4.2	2	4.5	2	4.5	ns	
	CL2	t_{DQSCK} (2)	2	6.5	2	6.5	2	6.5	ns	
Clock to first rising edge of DQS delay		t_{DQSS}	0.85	1.15	0.85	1.15	0.75	1.25	t_{CK}	
Data-in and DM setup time (to DQS) (fast slew rate)		t_{DS}	0.48		0.48		0.48		ns	13,14 ,15
Data-in and DM hold time (to DQS) (fast slew rate)		t_{DH}	0.48		0.48		0.48		ns	13,14 ,15
Data-in and DM setup time (to DQS) (slow slew rate)		t_{DS}	0.58		0.58		0.58		ns	13,14 ,16
Data-in and DM hold time (to DQS) (slow slew rate)		t_{DH}	0.58		0.58		0.58		ns	13,14 ,16
DQ and DM input pulse width (for each input)		t_{DIPW}	1.8		1.8		1.8		ns	17

AC Timing Parameter & Specifications-continued

Parameter		Symbol	-4		-4.5		-5		Unit	Note
			min	max	min	max	min	max		
Input setup time (fast slew rate)		t_{IS}	0.9		0.9		0.9		ns	15,18
Input hold time (fast slew rate)		t_{IH}	0.9		0.9		0.9		ns	15,18
Input setup time (slow slew rate)		t_{IS}	1.1		1.1		1.1		ns	16,18
Input hold time (slow slew rate)		t_{IH}	1.1		1.1		1.1		ns	16,18
Control and Address input pulse width		t_{IPW}	2.0		2.0		2.3		ns	17
DQS input high pulse width		t_{DQSH}	0.4		0.4		0.4		t_{CK}	
DQS input low pulse width		t_{DQSL}	0.4		0.4		0.4		t_{CK}	
DQS falling edge to CLK rising-setup time		t_{DSS}	0.2		0.2		0.2		t_{CK}	
DQS falling edge from CLK rising-hold time		t_{DSH}	0.2		0.2		0.2		t_{CK}	
Data strobe edge to output data edge		t_{DQSQ}		0.4		0.4		0.4	ns	20
Data-out high-impedance window from CLK/ $\overline{CLK}$	CL3	t_{HZ} (3)		3.75		4.25		4.5	ns	19
	CL2	t_{HZ} (2)		6.5		6.5		6.5	ns	19
Data-out low-impedance window from CLK/ $\overline{CLK}$		t_{LZ}	1.0		1.0		1.0		ns	19
Half Clock Period		t_{HP}	t_{CL}min or t_{CH}min		t_{CL}min or t_{CH}min		t_{CL}min or t_{CH}min		ns	10,11
DQ-DQS output hold time		t_{QH}	t_{HP} - t_{QHS}		t_{HP} - t_{QHS}		t_{HP} - t_{QHS}		ns	11
Data hold skew factor		t_{QHS}		0.45		0.45		0.5	ns	11

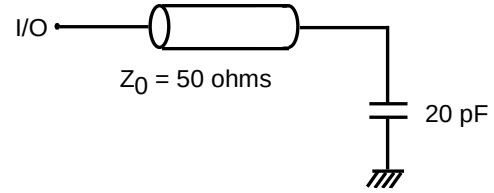
AC Timing Parameter & Specifications-continued

Parameter		Symbol	-4		-4.5		-5		Unit	Note
			min	max	min	max	min	max		
ACTIVE to PRECHARGE command		t_{RAS}	40	70K	40	70K	40	70K	ns	
Row Cycle Time		t_{RC}	55		55		55		ns	
AUTO REFRESH Row Cycle Time		t_{RFC}	72		72		72		ns	
ACTIVE to READ,WRITE delay		t_{RCD}	15		15		15		ns	
PRECHARGE command period		t_{RP}	15		15		15		ns	
Minimum t_{CKE} High/Low time		t_{CKE}	3		3		2		t_{CK}	
ACTIVE bank A to ACTIVE bank B command		t_{RRD}	10		10		10		ns	
WRITE recovery time		t_{WR}	15		15		15		ns	
Write data in to READ command delay		t_{WTR}	2		2		2		t_{CK}	
Col. Address to Col. Address delay		t_{CCD}	1		1		1		t_{CK}	
Refresh period		t_{REF}		64		64		64	ms	
Average periodic refresh interval		t_{REFI}		15.6		15.6		15.6	μ s	9
Write preamble		t_{WPRE}	0.25		0.25		0.25		t_{CK}	
Write postamble		t_{WPST}	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}	22
DQS read preamble	CL3	t_{RPRE} (3)	0.9	1.1	0.9	1.1	0.9	1.1	t_{CK}	23
	CL2	t_{RPRE} (2)	0.5	1.1	0.5	1.1	0.5	1.1	t_{CK}	23
DQS read postamble		t_{RPST}	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}	
Clock to DQS write preamble setup time		t_{WPRES}	0		0		0		ns	21
Load Mode Register / Extended Mode register cycle time		t_{MRD}	2		2		2		t_{CK}	
Exit self refresh to first valid command		t_{XSR}	120		120		120		ns	24
Exit power-down mode to first valid command		t_{XP}	25		25		25		ns	25
Auto precharge write recovery + Precharge time		t_{DAL}	(t_{WR}/t_{CK}) + (t_{RP}/t_{CK})		(t_{WR}/t_{CK}) + (t_{RP}/t_{CK})		(t_{WR}/t_{CK}) + (t_{RP}/t_{CK})		ns	26

Notes:

1. All voltages referenced to V_{SS}.
2. All parameters assume proper device initialization.
3. Tests for AC timing may be conducted at nominal supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage and temperature range specified.

4. The circuit shown below represents the timing reference load used in defining the relevant timing parameters of the part. It is not intended to be either a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester. System designers will use IBIS or other simulation tools to correlate the timing reference load to system environment. Manufacturers will correlate to their production test conditions (generally a coaxial transmission line terminated at the tester electronics). For the half strength driver with a nominal 10 pF load parameters t_{AC} and t_{QH} are expected to be in the same range. However, these parameters are not subject to production test but are estimated by design / characterization. Use of IBIS or other simulation tools for system design validation is suggested.



Timing Reference Load

5. The CLK/$\overline{\text{CLK}}$ input reference voltage level (for timing referenced to CLK/$\overline{\text{CLK}}$) is the point at which CLK and $\overline{\text{CLK}}$ cross; the input reference voltage level for signals other than CLK/$\overline{\text{CLK}}$ is $V_{DDQ}/2$.
6. The timing reference voltage level is $V_{DDQ}/2$.
7. AC and DC input and output voltage levels are defined in AC/DC operation conditions.
8. A CLK/$\overline{\text{CLK}}$ differential slew rate of 2.0 V/ns is assumed for all parameters.
9. A maximum of eight consecutive AUTO REFRESH commands (with t_{RFC}(min)) can be posted to any given LPDDR, meaning that the maximum absolute interval between any AUTO REFRESH command and the next AUTO REFRESH command is 8 x t_{REFI}.
10. Refer to the smaller of the actual clock low time and the actual clock high time as provided to the device.
11. $t_{QH} = t_{HP} - t_{QHS}$, where t_{HP} = minimum half clock period for any given cycle and is defined by clock high or clock low (t_{CL}, t_{CH}). t_{QHS} accounts for 1) the pulse duration distortion of on-chip clock circuits; and 2) the worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are, separately, due to data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers.
12. The only time that the clock frequency is allowed to change is during power-down or self-refresh modes.
13. The transition time for DQ, DM and DQS inputs is measured between V_{IL}(DC) to V_{IH}(AC) for rising input signals, and V_{IH}(DC) to V_{IL}(AC) for falling input signals.
14. DQS, DM and DQ input slew rate is specified to prevent double clocking of data and preserve setup and hold times. Signal transitions through the DC region must be monotonic.
15. Input slew rate ≥ 1.0 V/ns.
16. Input slew rate ≥ 0.5 V/ns and < 1.0 V/ns.
17. These parameters guarantee device timing but they are not necessarily tested on each device.
18. The transition time for address and command inputs is measured between V_{IH} and V_{IL}.
19. t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referred to a specific voltage level, but specify when the device is no longer driving (HZ), or begins driving (LZ).
20. t_{DQSQ} consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers for any given cycle.
21. The specific requirement is that DQS be valid (HIGH, LOW, or some point on a valid transition) on or before the corresponding CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from Hi-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on t_{DQSS}.
22. The maximum limit for this parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.
23. A low level on DQS may be maintained during High-Z states (DQS drivers disabled) by adding a weak pull-down element in the system. It is recommended to turn off the weak pull-down element during read and write bursts (DQS drivers enabled).
24. There must be at least two clock pulses during the t_{XSR} period.
25. There must be at least one clock pulse during the t_{XP} period.
26. Minimum 3 clocks of t_{DAL} (= t_{WR} + t_{RP}) is required because it need minimum 2 clocks for t_{WR} and minimum 1 clock for t_{RP}. $t_{DAL} = (t_{WR}/t_{CK}) + (t_{RP}/t_{CK})$: for each of the terms above, if not already an integer, round to the next higher integer.

Command Truth Table

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DM	BA0,1	A10/AP	A9~A0	Note
Register	Extended MRS		H	X	L	L	L	L	X	OP CODE			1,2
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1,2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A0~A7)	4
	Auto Precharge Enable										H		4
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	V	V	L	Column Address (A0~A7)	4,8
	Auto Precharge Enable										H		4,6,8
Deep Power Down Mode		Entry	H	L	L	H	H	L	X	X			
		Exit	L	H	H	X	X	X	X				
					L	H	H	H					
Burst Terminate			H	X	L	H	H	L	X	X			7
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	All Banks									X	H		5
Active Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	H	H	H					
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	H	H	H					
Deselect (NOP)			H	X	H	X	X	X	X	X			
No Operation (NOP)					L	H	H	H					

(V = Valid, X = Don't Care, H = Logic High, L = Logic Low)

Notes:

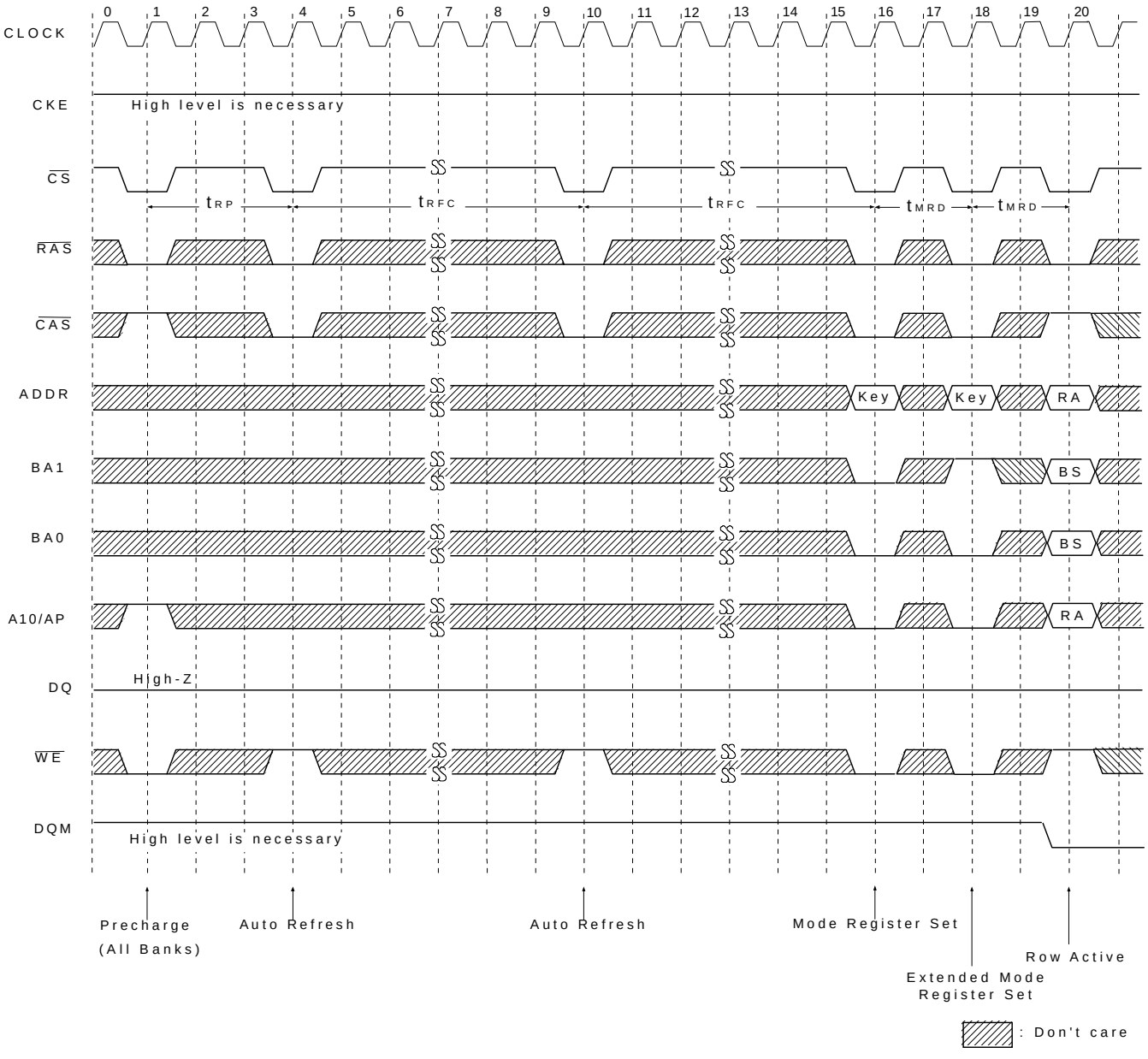
1. OP Code: Operand Code. A0~A10 & BA0~BA1: Program keys. (@EMRS/MRS)
2. EMRS/MRS can be issued only at all banks precharge state.
   A new command can be issued 2 clock cycles after EMRS or MRS.
3. Auto refresh functions are same as the CBR refresh of DRAM.
   The automatical precharge without row precharge command is meant by "Auto"..
   Auto/self refresh can be issued only at all banks precharge state.
4. BA0~BA1: Bank select addresses.
   If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.
   If BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank B is selected.
   If BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank C is selected.
   If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.
5. If A10/AP is "High" at row precharge, BA0 and BA1 are ignored and all banks are selected.
6. New row active of the associated bank can be issued at t_{RP} after end of burst.
7. Burst Terminate command is valid at every burst length.
8. DM and Data-in are sampled at the rising and falling edges of the DQS. Data-in byte are masked if the corresponding and coincident DM is "High". (Write DM latency is 0).

Basic Functionality

Power-Up and Initialization Sequence

The following sequence is required for POWER UP and Initialization.

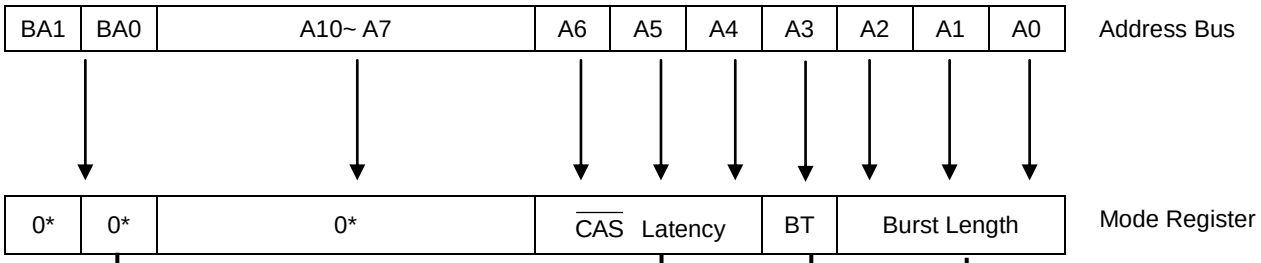
1. Apply power and attempt to maintain CKE at a high state (all other inputs may be undefined.)
   - Apply V_{DD} before or at the same time as V_{DDQ}.
2. Start clock and maintain stable condition for a minimum.
3. The minimum of 200us after stable power and clock (CLK, $\overline{CLK}$), apply NOP.
4. Issue precharge commands for all banks of the device.
5. Issue 2 or more auto-refresh commands.
6. Issue mode register set command to initialize the mode register.
7. Issue extended mode register set command to set DS.



Mode Register Definition

Mode Register Set (MRS)

The mode register stores the data for controlling the various operating modes of LPDDR SDRAM. It programs $\overline{CAS}$ latency, addressing mode, burst length and various vendor specific options to make LPDDR SDRAM useful for variety of different applications. The default value of the register is not defined, therefore the mode register must be written in the power up sequence of LPDDR SDRAM. The mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and BA0~BA1 (The LPDDR SDRAM should be in all bank precharge with CKE already high prior to writing into the mode register). The state of address pins A0~A10 in the same cycle as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and BA0~BA1 going low is written in the mode register. Two clock cycles are requested to complete the write operation in the mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. The mode register is divided into various fields depending on functionality. The burst length uses A0~A2, addressing mode uses A3, $\overline{CAS}$ latency (read latency from column address) uses A4~A6. A7~A10 is used for test mode. A7~A10 must be set to low for normal MRS operation. Refer to the table for specific codes for various burst length, addressing modes and $\overline{CAS}$ latencies.



A3	Burst Type
0	Sequential
1	Interleave

BA1	BA0	Operating Mode
0	0	MRS Cycle
1	0	EMRS Cycle

CAS Latency			
A6	A5	A4	Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Burst Length

A2	A1	A0	Latency	
			Sequential	Interleave
0	0	0	Reserved	Reserved
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	16
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Reserved	Full page

Full Page Length: 256

* BA0~BA1 and A10~A7 should stay “0” during MRS cycle

Burst Address Ordering for Burst Length

Burst Length	Starting Column Address				Sequential Mode	Interleave Mode
	A3	A2	A1	A0		
2				0	0, 1	0, 1
				1	1, 0	1, 0
4			0	0	0, 1, 2, 3	0, 1, 2, 3
			0	1	1, 2, 3, 0	1, 0, 3, 2
			1	0	2, 3, 0, 1	2, 3, 0, 1
			1	1	3, 0, 1, 2	3, 2, 1, 0
8		0	0	0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
		0	0	1	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
		0	1	0	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
		0	1	1	3, 4, 5, 6, 7, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4
		1	0	0	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
		1	0	1	5, 6, 7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
		1	1	0	6, 7, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1
		1	1	1	7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0
16	0	0	0	0	-	0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, F
	0	0	0	1	-	1, 0, 3, 2, 5, 4, 7, 6, 9, 8, B, A, D, C, F, E
	0	0	1	0	-	2, 3, 0, 1, 6, 7, 4, 5, A, B, 8, 9, E, F, C, D
	0	0	1	1	-	3, 2, 1, 0, 7, 6, 5, 4, B, A, 9, 8, F, E, D, C
	0	1	0	0	-	4, 5, 6, 7, 0, 1, 2, 3, C, D, E, F, 8, 9, A, B
	0	1	0	1	-	5, 4, 7, 6, 1, 0, 3, 2, D, C, F, E, 9, 8, B, A
	0	1	1	0	-	6, 7, 4, 5, 2, 3, 0, 1, E, F, C, D, A, B, 8, 9
	0	1	1	1	-	7, 6, 5, 4, 3, 2, 1, 0, F, E, D, C, B, A, 9, 8
	1	0	0	0	-	8, 9, A, B, C, D, E, F, 0, 1, 2, 3, 4, 5, 6, 7
	1	0	0	1	-	9, 8, B, A, D, C, F, E, 1, 0, 3, 2, 5, 4, 7, 6
	1	0	1	0	-	A, B, 8, 9, E, F, C, D, 2, 3, 0, 1, 6, 7, 4, 5
	1	0	1	1	-	B, A, 9, 8, F, E, D, C, 3, 2, 1, 0, 7, 6, 5, 4
	1	1	0	0	-	C, D, E, F, 8, 9, A, B, 4, 5, 6, 7, 0, 1, 2, 3
	1	1	0	1	-	D, C, F, E, 9, 8, B, A, 5, 4, 7, 6, 1, 0, 3, 2
	1	1	1	0	-	E, F, C, D, A, B, 8, 9, 6, 7, 4, 5, 2, 3, 0, 1
	1	1	1	1	-	F, E, D, C, B, A, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0

Extended Mode Register Set (EMRS)

The extended mode register stores for selecting DS. The extended mode register set must be done before any active command after the power up sequence. The extended mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, BA0 and high on BA1 (The LPDDR SDRAM should be in all bank precharge with CKE already high prior to writing into the extended more register). The state of address pins A0~An in the same cycle as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ going low is written in the extended mode register. Refer to the table for specific codes.

The extended mode register can be changed by using the same command and clock cycle requirements during operations as long as all banks are in the idle state.

BA1	BA0	A10 ~ A8	A7 A6 A5	A4 ~ A0	Address bus
1	0*	0*	DS	0*	Extended Mode Register Set

	A7-A5	Drive Strength
DS	000	Full Strength
	001	1/2 Strength
	010	1/4 Strength
	011	1/8 Strength

* BA0 and A10~ A8 should stay “0” during EMRS cycle

Precharge

The precharge command is used to precharge or close a bank that has activated. The precharge command is issued when $\overline{CS}$, $\overline{RAS}$ and $\overline{WE}$ are low and $\overline{CAS}$ is high at the rising edge of the clock. The precharge command can be used to precharge each bank respectively or all banks simultaneously. The bank select addresses (BA0, BA1) are used to define which bank is precharged when the command is initiated. For write cycle, t_{WR}(min.) must be satisfied until the precharge command can be issued. After t_{RP} from the precharge, an active command to the same bank can be initiated.

Burst Selection for Precharge by Bank address bits

A10/AP	BA1	BA0	Precharge
0	0	0	Bank A Only
0	0	1	Bank B Only
0	1	0	Bank C Only
0	1	1	Bank D Only
1	X	X	All Banks

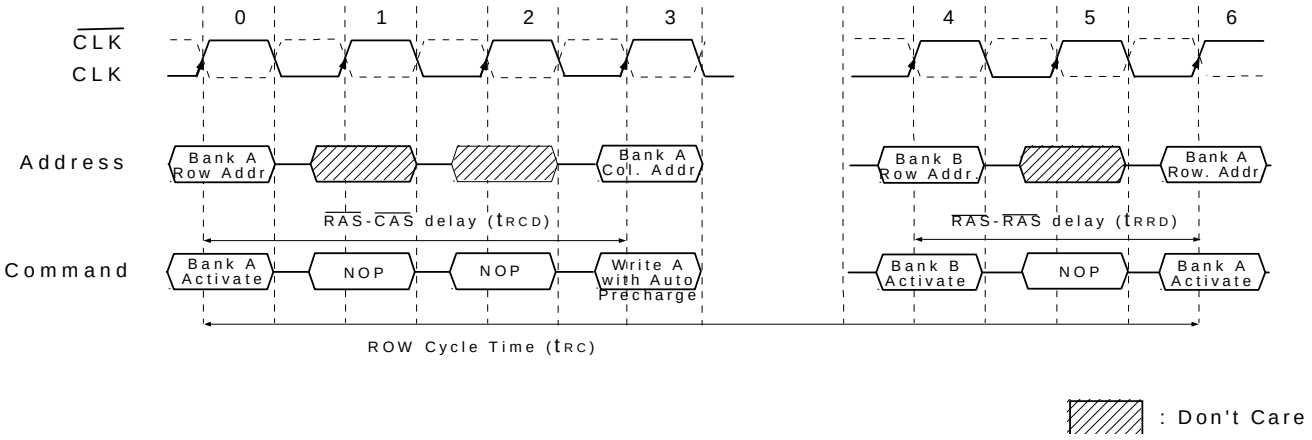
NOP & Device Deselect

The device should be deselected by deactivating the $\overline{CS}$ signal. In this mode, LPDDR SDRAM should ignore all the control inputs. The LPDDR SDRAM is put in NOP mode when $\overline{CS}$ is actived and by deactivating $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$. For both Deselect and NOP, the device should finish the current operation when this command is issued.

Row Active

The Bank Activation command is issued by holding $\overline{CAS}$ and $\overline{WE}$ high with $\overline{CS}$ and $\overline{RAS}$ low at the rising edge of the clock (CLK). The LPDDR SDRAM has four independent banks, so Bank Select addresses (BA0, BA1) are required. The Bank Activation command to the first read or write command must meet or exceed the minimum of $\overline{RAS}$ to $\overline{CAS}$ delay time (t_{RCD} min). Once a bank has been activated, it must be precharged before another Bank Activation command can be applied to the same bank. The minimum time interval between interleaved Bank Activation command (Bank A to Bank B and vice versa) is the Bank to Bank delay time (t_{RRD} min).

Bank Activation Command Cycle ($\overline{CAS}$ Latency = 3)



Read Bank

This command is used after the row activate command to initiate the burst read of data. The read command is initiated by activating $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, and deasserting $\overline{WE}$ at the same clock sampling (rising) edge as described in the command truth table. The length of the burst and the CAS latency time will be determined by the values programmed during the MRS command.

Write Bank

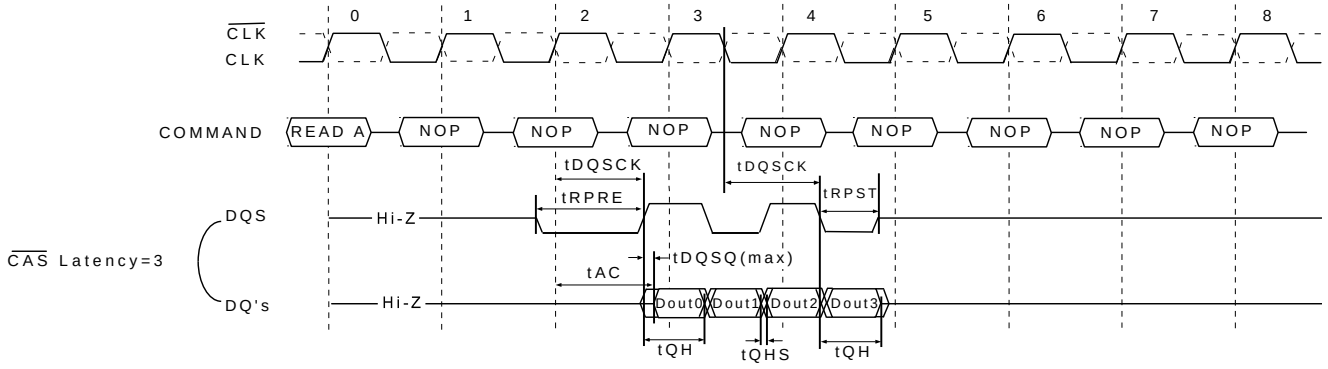
This command is used after the row activate command to initiate the burst write of data. The write command is initiated by activating $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ at the same clock sampling (rising) edge as describe in the command truth table. The length of the burst will be determined by the values programmed during the MRS command.

Essential Functionality for LPDDR SDRAM

Burst Read Operation

Burst Read operation in LPDDR SDRAM is in the same manner as the current LPDDR SDRAM such that the Burst read command is issued by asserting $\overline{CS}$ and $\overline{CAS}$ low while holding $\overline{RAS}$ and $\overline{WE}$ high at the rising edge of the clock (CLK) after t_{RCD} from the bank activation. The address inputs determine the starting address for the Burst, The Mode Register sets type of burst and burst length. The first output data is available after the $\overline{CAS}$ Latency from the READ command, and the consecutive data are presented on the falling and rising edge of Data Strobe (DQS) adopted by LPDDR SDRAM until the burst length is completed.

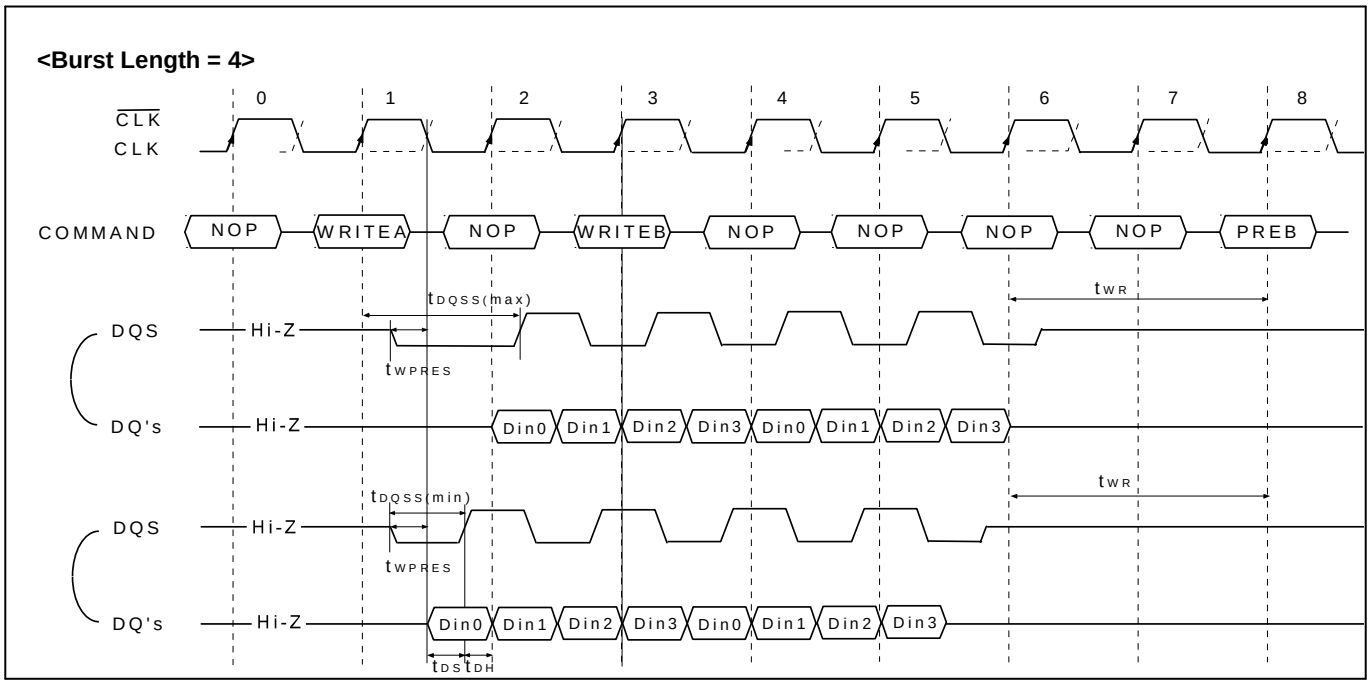
<Burst Length = 4, $\overline{CAS}$ Latency = 3>



Burst Write Operation

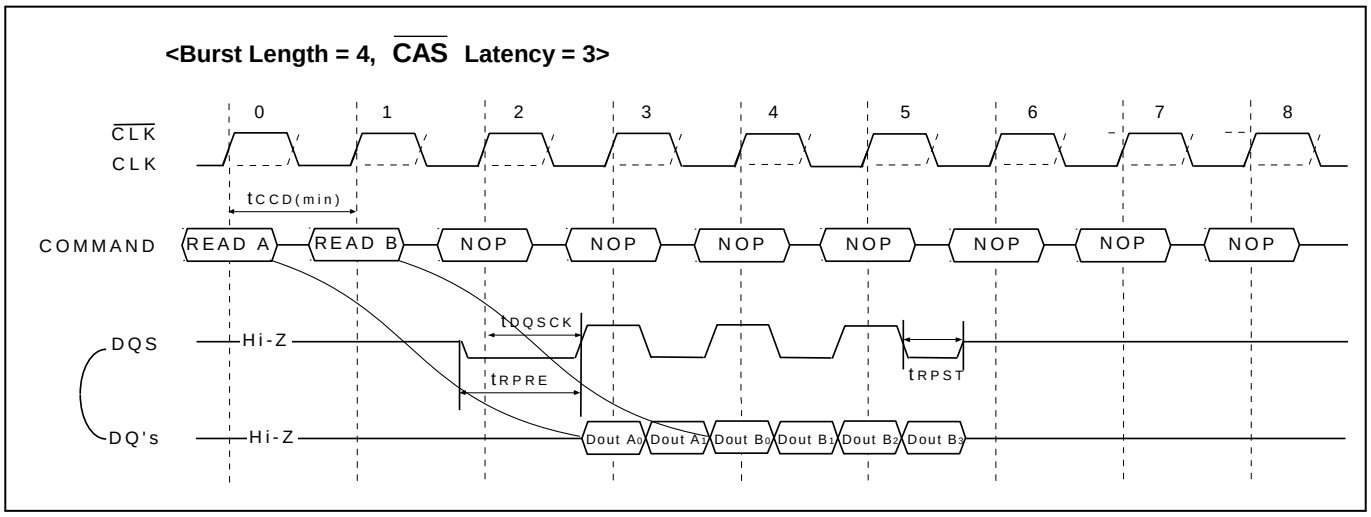
The Burst Write command is issued by having $\overline{CS}$, $\overline{CAS}$ and $\overline{WE}$ low while holding $\overline{RAS}$ high at the rising edge of the clock (CLK). The address inputs determine the starting column address. There is no write latency relative to DQS required for burst write cycle. The first data of a burst write cycle must be applied on the DQ pins t_{DS} (Data-in setup time) prior to data strobe edge enabled after t_{DQSS} from the rising edge of the clock (CLK) that the write command is issued. The remaining data inputs must be supplied on each subsequent falling and rising edge of Data Strobe until the burst length is completed. When the burst has been finished, any additional data supplied to the DQ pins will be ignored.

<Burst Length = 4>



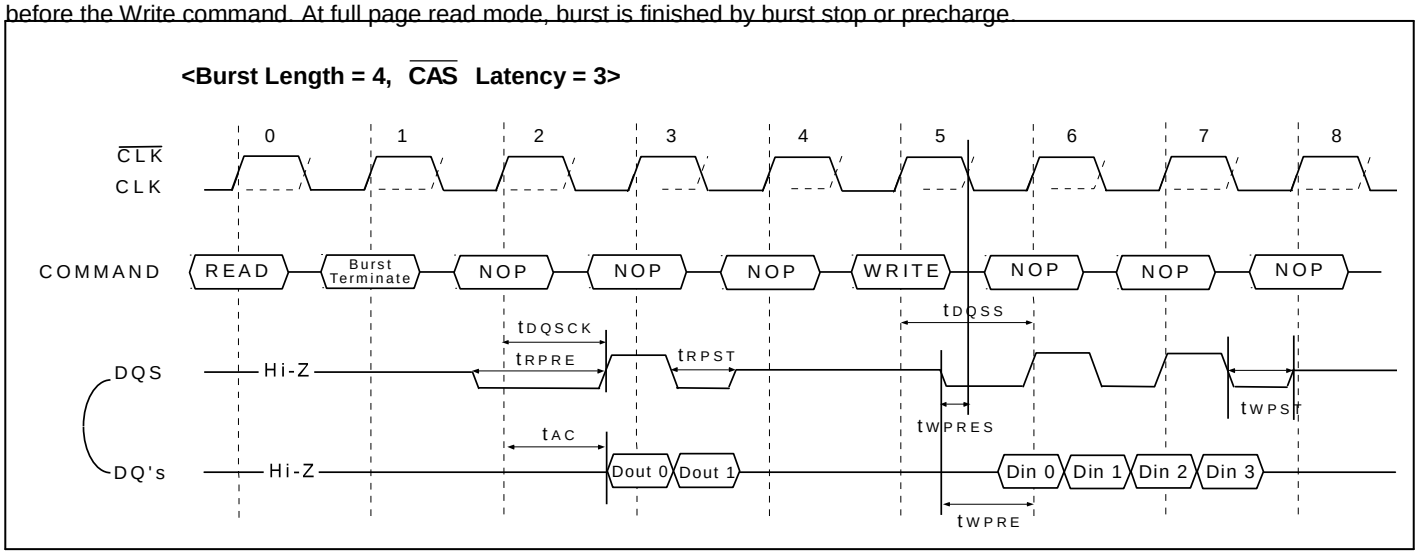
Read Interrupted by a Read

A Burst Read can be interrupted before completion of the burst by new Read command of any bank. When the previous burst is interrupted, the remaining addresses are overridden by the new address with the full burst length. The data from the first Read command continues to appear on the outputs until the $\overline{CAS}$ latency from the interrupting Read command is satisfied. At this point the data from the interrupting Read command appears. Read to Read interval is minimum 1 clock.



Read Interrupted by a Write & Burst Terminate

To interrupt a burst read with a write command, Burst Terminate command must be asserted to avoid data contention on the I/O bus by placing the DQ's(Output drivers) in a high impedance state. To insure the DQ's are tri-stated one cycle before the beginning the write operation, Burt Terminate command must be applied at least RU(CL) clocks 〔RU means round up to the nearest integer〕 before the Write command. At full page read mode, burst is finished by burst stop or precharge.

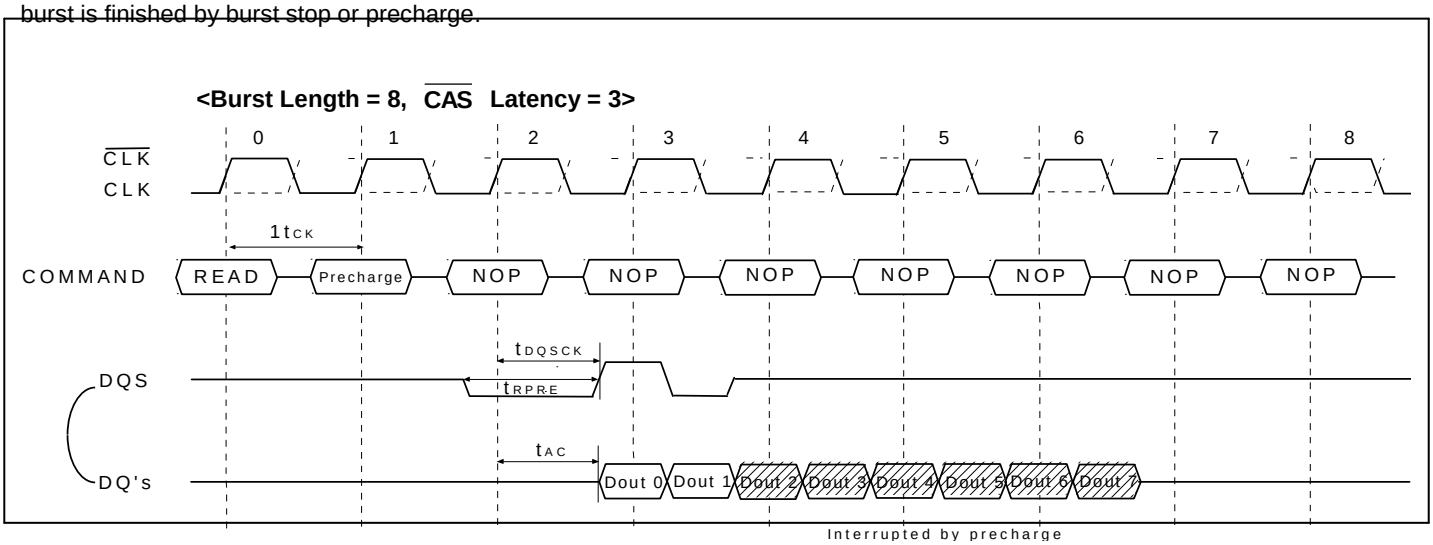


The following functionality establishes how a Write command may interrupt a Read burst.

1. For Write commands interrupting a Read burst, a Burst Terminate command is required to stop the read burst and tristate the DQ bus prior to valid input write data. Once the Burst Terminate command has been issued, the minimum delay to a Write command = RU (CL) [CL is the $\overline{CAS}$ Latency and RU means round up to the nearest integer].
2. It is illegal for a Write and Burst Terminate command to interrupt a Read with auto precharge command.

Read Interrupted by a Precharge

A Burst Read operation can be interrupted by precharge of the same bank. The minimum 1 clock is required for the read to precharge intervals. A precharge command to output disable latency is equivalent to the $\overline{CAS}$ latency. At full page read mode, burst is finished by burst stop or precharge.



When a burst Read command is issued to a LPDDR SDRAM, a Precharge command may be issued to the same bank before the Read burst is complete. The following functionality determines when a Precharge command may be given during a Read burst and when a new Bank Activate command may be issued to the same bank.

1. For the earliest possible Precharge command without interrupting a Read burst, the Precharge command may be given on the rising clock edge which is CL clock cycles before the end of the Read burst where CL is the $\overline{CAS}$ Latency. A new Bank Activate command may be issued to the same bank after t_{RP} (RAS precharge time).

2. When a Precharge command interrupts a Read burst operation, the Precharge command may be given on the rising clock edge which is CL clock cycles before the last data from the interrupted Read burst where CL is the $\overline{CAS}$ Latency. Once the last data word has been output, the output buffers are tristated. A new Bank Activate command may be issued to the same bank after t_{RP}.

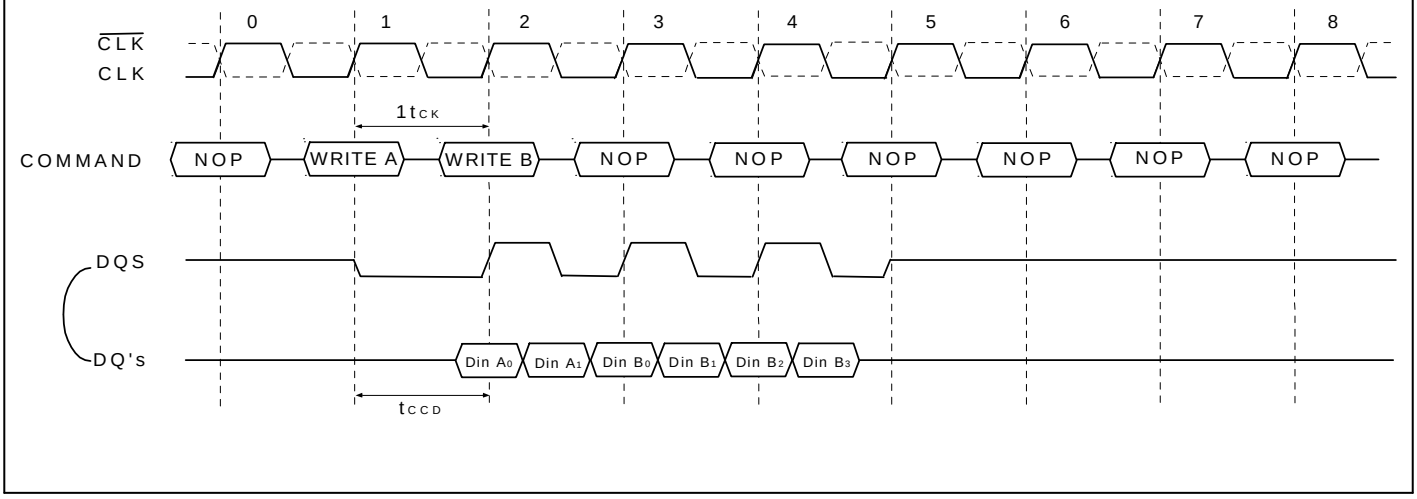
3. For a Read with auto precharge command, a new Bank Activate command may be issued to the same bank after t_{RP} where t_{RP} begins on the rising clock edge which is CL clock cycles before the end of the Read burst where CL is the $\overline{CAS}$ Latency. During Read with auto precharge, the initiation of the internal precharge occurs at the same time as the earliest possible external Precharge command would initiate a precharge operation without interrupting the Read burst as described in 1 above.

4. For all cases above, t_{RP} is an analog delay that needs to be converted into clock cycles. The number of clock cycles between a Precharge command and a new Bank Activate command to the same bank equals t_{RP} / t_{CK} (where t_{CK} is the clock cycle time) with the result rounded up to the nearest integer number of clock cycles.
   In all cases, a Precharge operation cannot be initiated unless t_{RAS}(min) [minimum Bank Activate to Precharge time] has been satisfied. This includes Read with auto precharge commands where t_{RAS}(min) must still be satisfied such that a Read with auto precharge command has the same timing as a Read command followed by the earliest possible Precharge command which does not interrupt the burst.

Write Interrupted by a Write

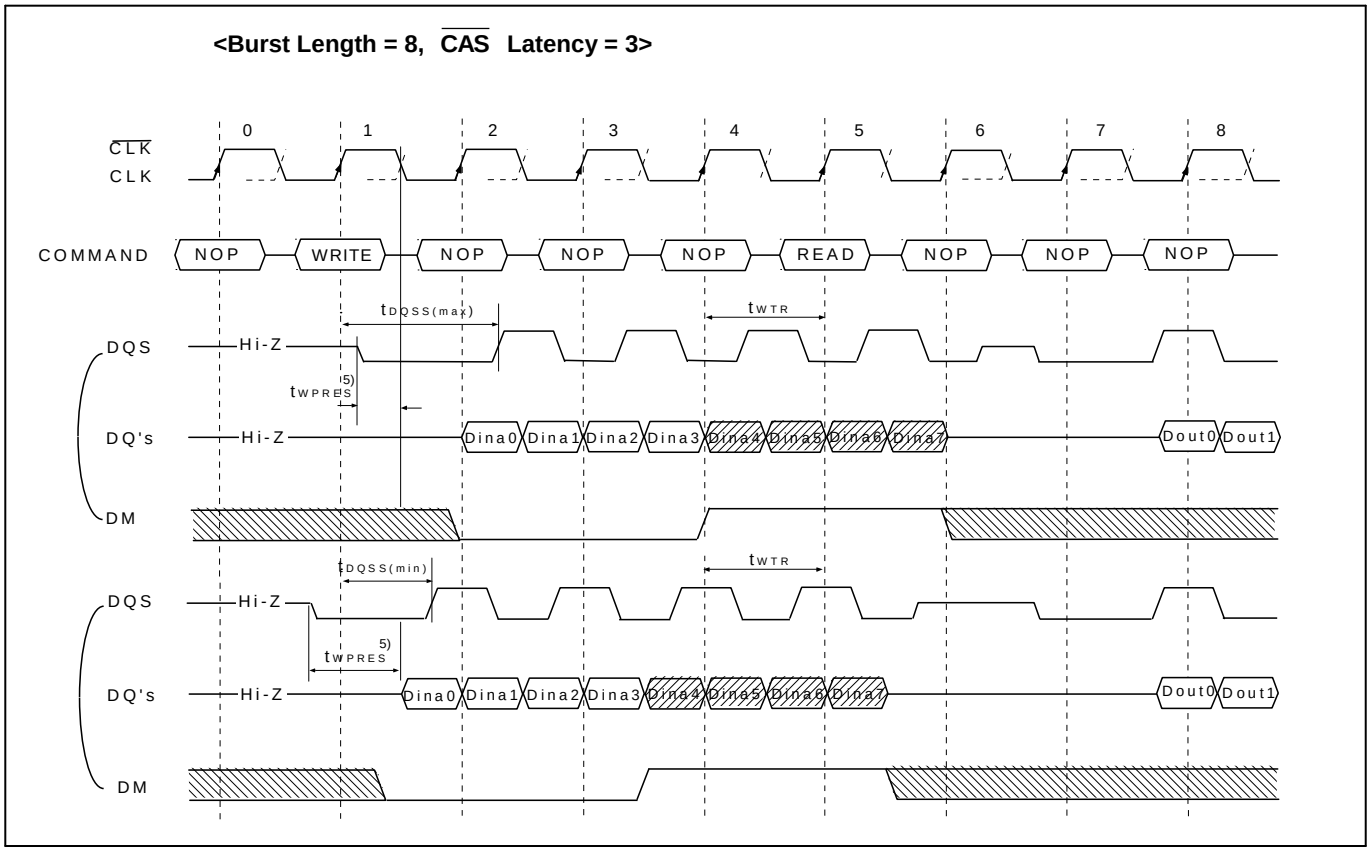
A Burst Write can be interrupted before completion of the burst by a new Write command, with the only restriction that the interval that separates the commands must be at least one clock cycle. When the previous burst is interrupted, the remaining addresses are overridden by the new address and data will be written into the device until the programmed burst length is satisfied.

<Burst Length = 4>



Write Interrupted by a Read & DM

A burst write can be interrupted by a read command of any bank. The DQ's must be in the high impedance state at least one clock cycle before the interrupting read data appear on the outputs to avoid data contention. When the read command is registered, any residual data from the burst write cycle must be masked by DM. The delay from the last data to read command (t_{WTR}) is required to avoid the data contention LPDDR SDRAM inside. Data that are presented on the DQ pins before the read command is initiated will actually be written to the memory. Read command interrupting write can not be issued at the next clock edge of that of write command.

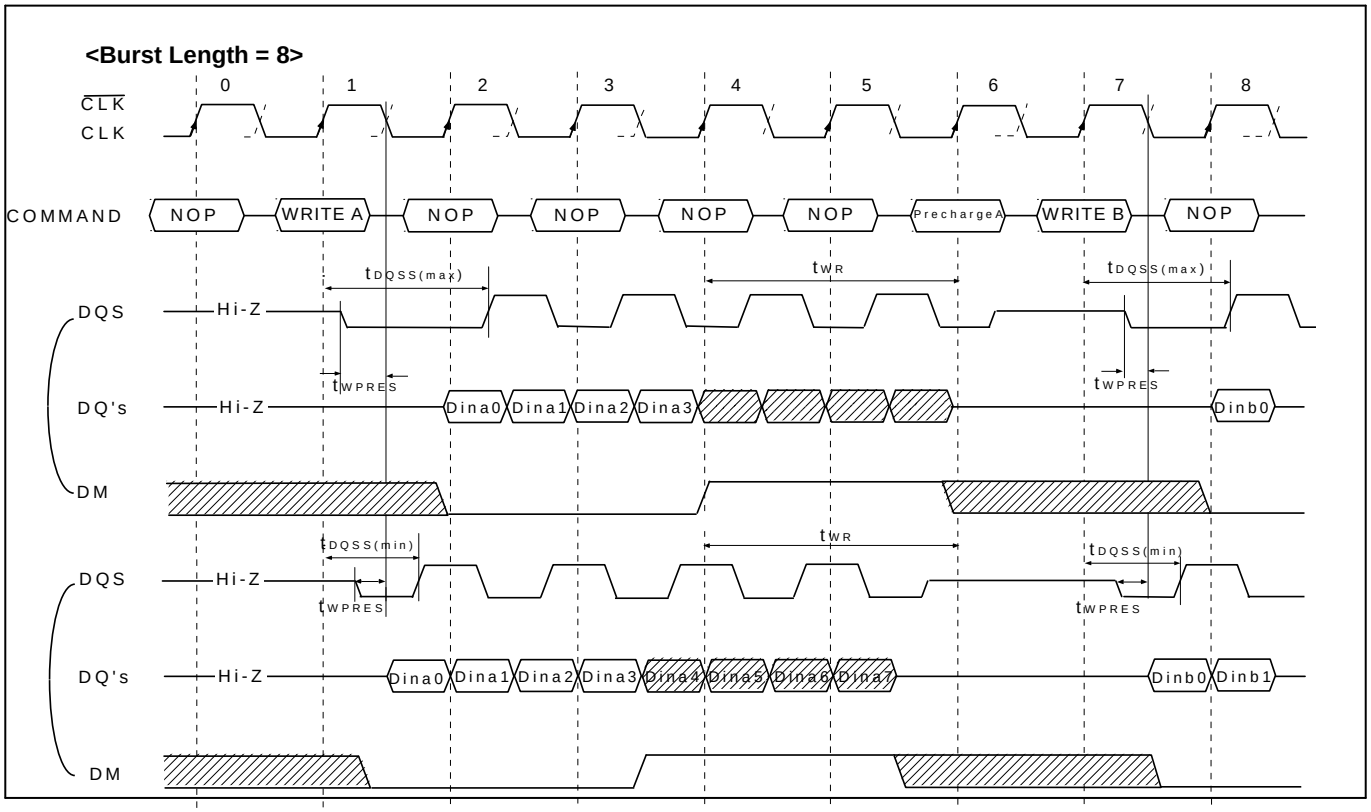


The following functionality established how a Read command may interrupt a Write burst and which input data is not written into the memory.

1. For Read commands interrupting a Write burst, the minimum Write to Read command delay is 2 clock cycles. The case where the Write to Read delay is 1 clock cycle is disallowed.
2. For read commands interrupting a Write burst, the DM pin must be used to mask the input data words which immediately precede the interrupting Read operation and the input data word which immediately follows the interrupting Read operation.
3. For all cases of a Read interrupting a Write, the DQ and DQS buses must be released by the driving chip (i.e., the memory controller) in time to allow the buses to turn around before the LPDDR SDRAM drives them during a read operation.
4. If input Write data is masked by the Read command, the DQS inputs are ignored by the LPDDR SDRAM.
5. It is illegal for a Read command interrupt a Write with auto precharge command.

Write Interrupted by a Precharge & DM

A burst write operation can be interrupted before completion of the burst by a precharge of the same bank. Random column access is allowed. A write recovery time (t_{WR}) is required from the last data to precharge command. When precharge command is asserted, any residual data from the burst write cycle must be masked by DM. At full page write mode, burst is finished by precharge.



Precharge timing for Write operations in LPDDR SDRAM requires enough time to allow “Write recovery” which is the time required by a LPDDR SDRAM core to properly store a full “0” or “1” level before a Precharge operation. For LPDDR SDRAM, a timing parameter, t_{WR}, is used to indicate the required of time between the last valid write operation and a Precharge command to the same bank.

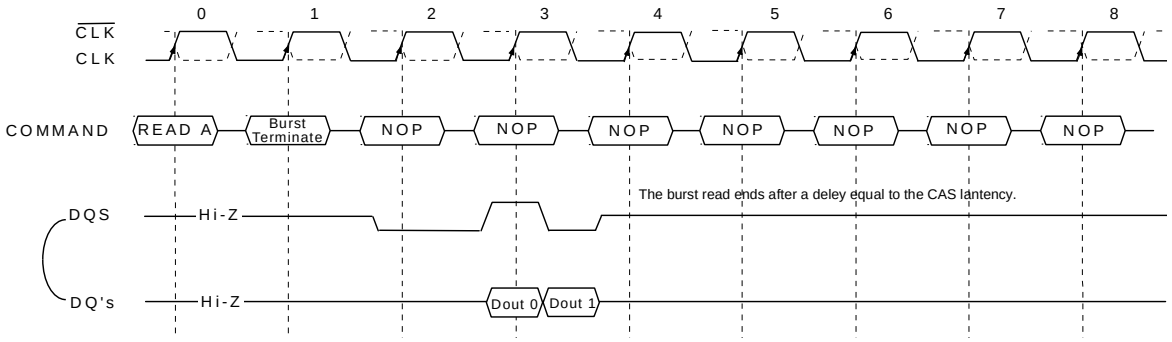
t_{WR} starts on the rising clock edge after the last possible DQS edge that strobed in the last valid and ends on the rising clock edge that strobes in the precharge command.

1. For the earliest possible Precharge command following a Write burst without interrupting the burst, the minimum time for write recovery is defined by t_{WR}.
2. When a precharge command interrupts a Write burst operation, the data mask pin, DM, is used to mask input data during the time between the last valid write data and the rising clock edge in which the Precharge command is given. During this time, the DQS input is still required to strobe in the state of DM. The minimum time for write recovery is defined by t_{WR}.
3. For a Write with auto precharge command, a new Bank Activate command may be issued to the same bank after $t_{WR} + t_{RP}$ where $t_{WR} + t_{RP}$ starts on the falling DQS edge that strobed in the last valid data and ends on the rising clock edge that strobes in the Bank Activate commands. During write with auto precharge, the initiation of the internal precharge occurs at the same time as the earliest possible external Precharge command without interrupting the Write burst as described in 1 above.
4. In all cases, a Precharge operation cannot be initiated unless t_{RAS}(min) [minimum Bank Activate to Precharge time] has been satisfied. This includes Write with auto precharge commands where t_{RAS}(min) must still be satisfied such that a Write with auto precharge command has the same timing as a Write command followed by the earliest possible Precharge command which does not interrupt the burst.

Burst Terminate

The Burst Terminate command is initiated by having $\overline{RAS}$ and $\overline{CAS}$ high with $\overline{CS}$ and $\overline{WE}$ low at the rising edge of the clock (CLK). The Burst Terminate command has the fewest restriction making it the easiest method to use when terminating a burst read operation before it has been completed. When the Burst Terminate command is issued during a burst read cycle, the pair of data and DQS (Data Strobe) go to a high impedance state after a delay which is equal to the CAS latency set in the mode register. The Burst Terminate command, however, is not supported during a write burst operation.

<Burst Length = 4, $\overline{CAS}$ Latency = 3 >



The Burst Terminate command is a mandatory feature for LPDDR SDRAM. The following functionality is required.

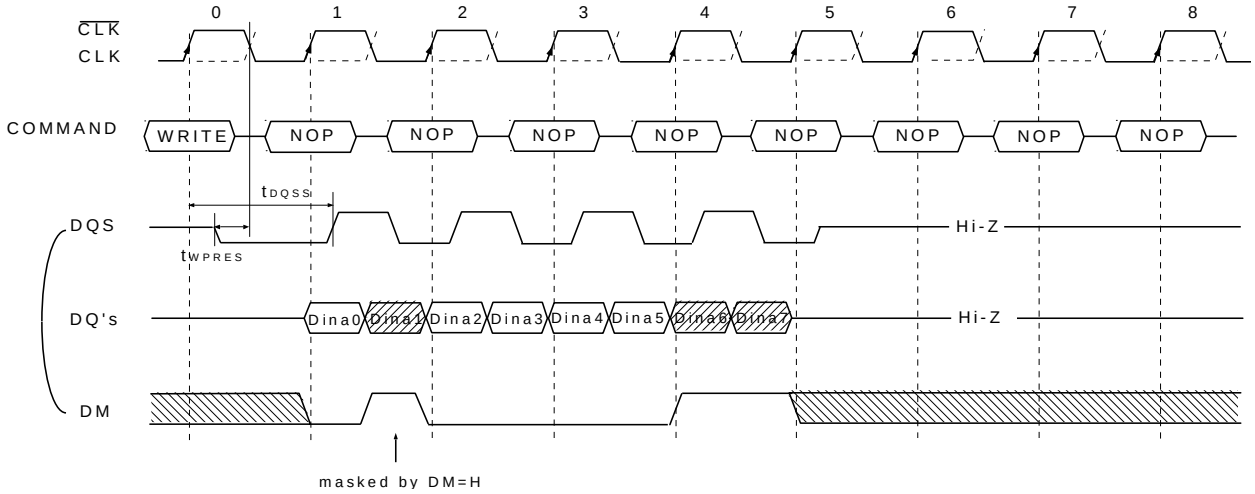
1. The BST command may only be issued on the rising edge of the input clock, CLK.
2. BST is only a valid command during Read burst.
3. BST during a Write burst is undefined and shall not be used.
4. BST applies to all burst lengths.
5. BST is an undefined command during Read with auto precharge and shall not be used.
6. When terminating a burst Read command, the BST command must be issued L_{BST} ("BST Latency") clock cycles before the clock edge at which the output buffers are tristated, where L_{BST} equals the $\overline{CAS}$ latency for read operations.
7. When the burst terminates, the DQ and DQS pins are tristated.

The BST command is not byte controllable and applies to all bits in the DQ data word and the (all) DQS pin(s).

DM masking

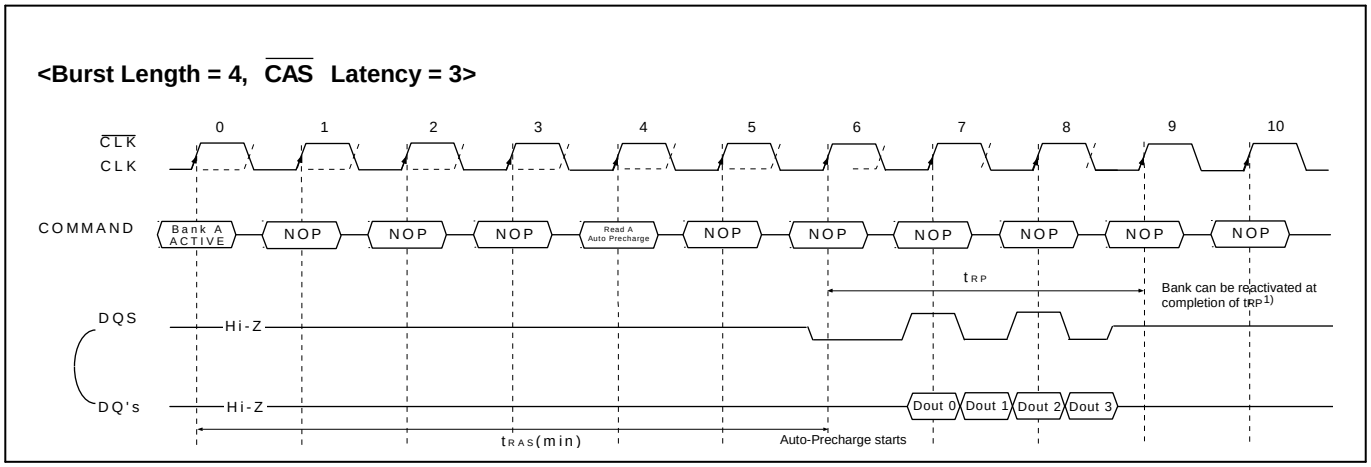
The LPDDR SDRAM has a data mask function that can be used in conjunction with data write cycle. Not read cycle. When the data mask is activated (DM high) during write operation, LPDDR SDRAM does not accept the corresponding data. (DM to data-mask latency is zero) DM must be issued at the rising or falling edge of data strobe.

<Burst Length = 8>



Read with Auto Precharge

If a read with auto precharge command is initiated, the LPDDR SDRAM automatically enters the precharge operation BL/2 clock later from a read with auto precharge command when t_{RAS}(min) is satisfied. If not, the start point of precharge operation will be delayed until t_{RAS}(min) is satisfied. Once the precharge operation has started the bank cannot be reactivated and the new command can not be asserted until the precharge time (t_{RP}) has been satisfied



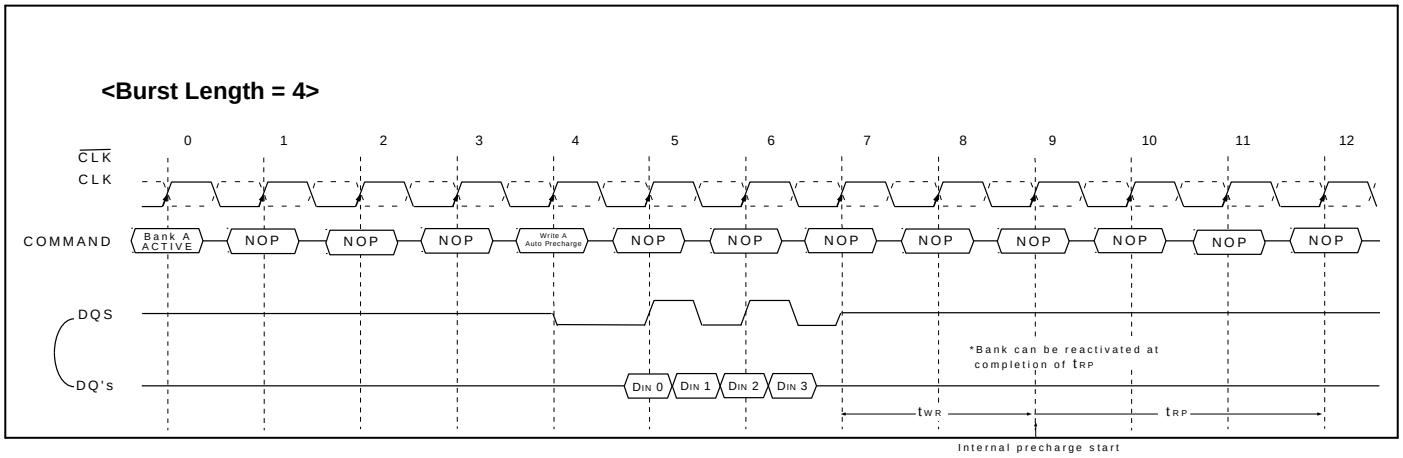
Note: The row active command of the precharge bank can be issued after t_{RP} from this point.

Asserted Command	For Same Bank			For Different Bank		
	5	6	7	5	6	7
READ	READ + No AP	Illegal	Illegal	Legal	Legal	Legal
READ + AP[1]	READ + AP	Illegal	Illegal	Legal	Legal	Legal
Active	Illegal	Illegal	Illegal	Legal	Legal	Legal
Precharge	Legal	Legal	Illegal	Legal	Legal	Legal

Note: 1. AP = Auto Precharge

Write with Auto Precharge

If A10 is high when write command is issued, the write with auto precharge function is performed. Any new command to the same bank should not be issued until the internal precharge is completed. The internal precharge begins at the rising edge of the CLK with the t_{WR} delay after the last data-in.



Note: The row active command of the precharge bank can be issued after t_{RP} from this point.

Asserted Command	For Same Bank						For Different Bank				
	5	6	7	8	9	10	5	6	7	8	9
WRITE	WRITE + NO AP	WRITE + NO AP	Illegal	Illegal	Illegal	Illegal	Legal	Legal	Legal	Legal	Legal
WRITE + AP[1]	WRITE + AP	WRITE + AP	Illegal	Illegal	Illegal	Illegal	Legal	Legal	Legal	Legal	Legal
READ	Illegal	READ + No AP + DM[2]	READ + No AP+ DM	READ + No AP	Illegal	Illegal	Illegal	Illegal	Illegal	Legal	Legal
READ + AP	Illegal	READ + AP+ DM	READ + AP+ DM	READ + AP	Illegal	Illegal	Illegal	Illegal	Illegal	Legal	Legal
Active	Illegal	Illegal	Illegal	Illegal	Illegal	Illegal	Legal	Legal	Legal	Legal	Legal
Precharge	Illegal	Illegal	Illegal	Illegal	Illegal	Illegal	Legal	Legal	Legal	Legal	Legal

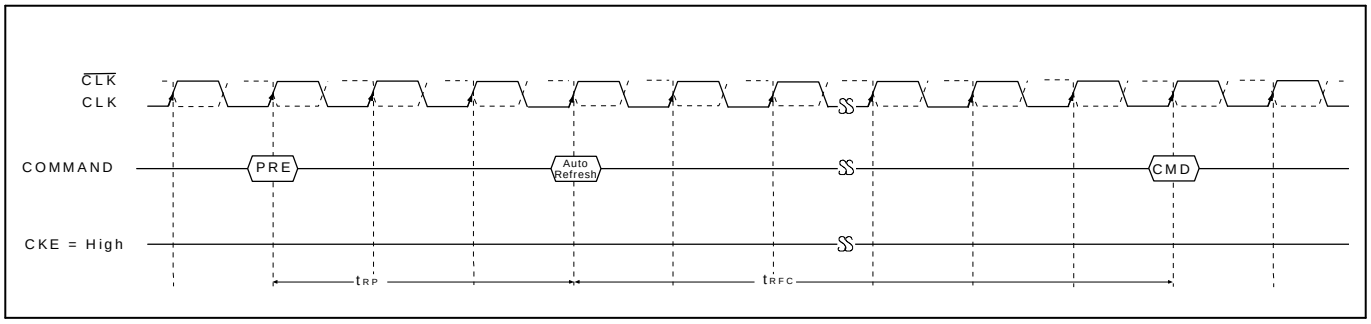
Note: 1. AP = Auto Precharge
2. DM: Refer to “Write Interrupted by Precharge & DM”

Auto Refresh & Self Refresh

Auto Refresh

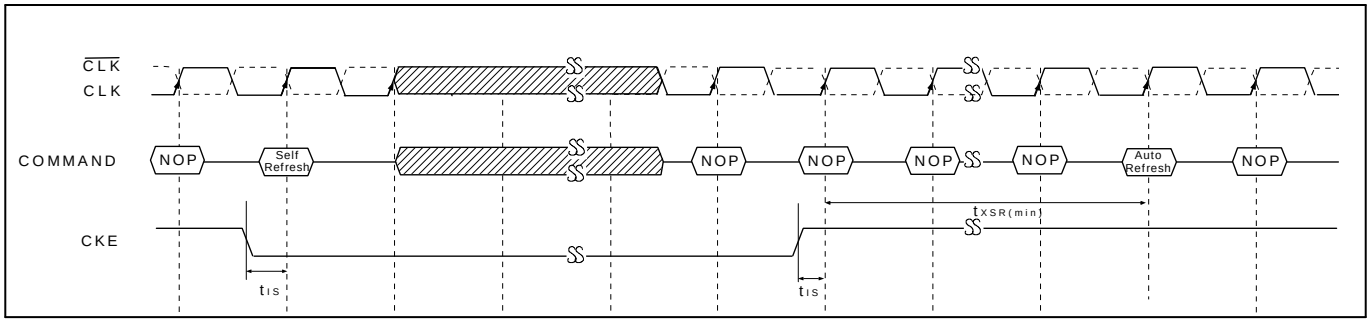
An auto refresh command is issued by having $\overline{CS}$, $\overline{RAS}$ and $\overline{CAS}$ held low with CKE and $\overline{WE}$ high at the rising edge of the clock(CLK). All banks must be precharged and idle for t_{RP}(min) before the auto refresh command is applied. No control of the external address pins is requires once this cycle has started because of the internal address counter. When the refresh cycle has completed, all banks will be in the idle state. A delay between the auto refresh command and the next activate command or subsequent auto refresh command must be greater than or equal to the t_{RFC}(min).

A maximum of eight consecutive AUTO REFRESH commands (with t_{RFC}(min)) can be posted to any given LPDDR, meaning that the maximum absolute interval between any AUTO REFRESH command and the next AUTO REFRESH command is 8 x t_{REFI}.



Self Refresh

A self refresh command is defines by having $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and CKE held low with $\overline{WE}$ high at the rising edge of the clock (CLK). Once the self refresh command is initiated, CKE must be held low to keep the device in self refresh mode. During the self refresh operation, all inputs except CKE are ignored. The clock is internally disabled during self refresh operation to reduce power consumption. The self refresh is exited by supplying stable clock input before returning CKE high, asserting deselect or NOP command and then asserting CKE high for longer than t_{XSR}.



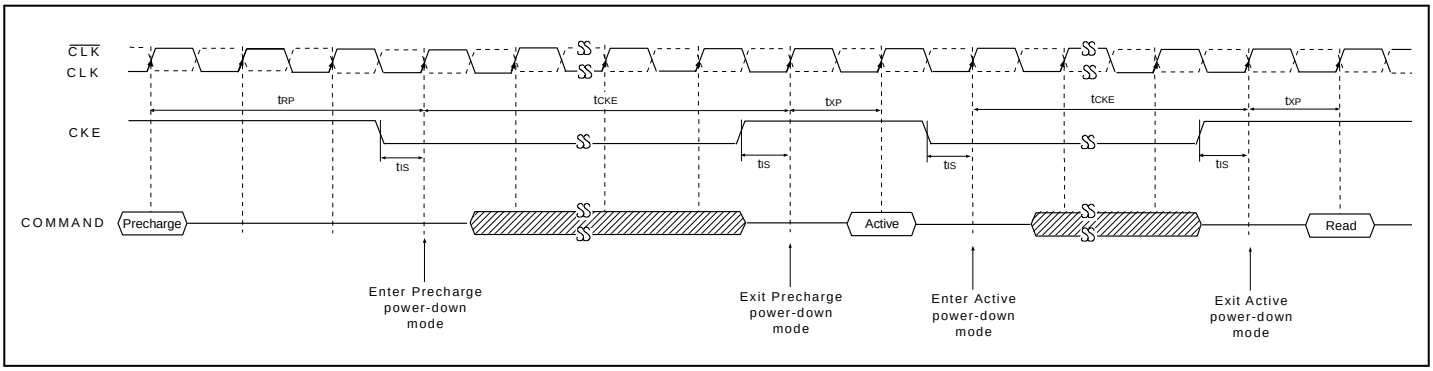
Note: After self refresh exit, input an auto refresh command immediately.

Power Down

Power down is entered when CKE is registered Low (no accesses can be in progress). If power down occurs when all banks are idle, this mode is referred to as precharge power-down; if power down occurs when there is a row active in any bank, this mode is referred to as active power-down.

Entering power down deactivates the input and output buffers, excluding CLK, $\overline{CLK}$ and CKE. In power down mode, CKE Low must be maintained, and all other input signals are "Don't Care". The minimum power down duration is specified by t_{CKE}. However, power down duration is limited by the refresh requirements of the device.

The power down state is synchronously exited when CKE is registered High (along with a NOP or DESELECT command). A valid command may be applied t_{XP} after exit from power down.



Functional Truth Table

Truth Table – CKE [Note 1~10]

CKE n-1	CKE n	Current State	COMMAND n	ACTION n	NOTE
L	L	Power Down	X	Maintain Power Down	
L	L	Self Refresh	X	Maintain Self Refresh	
L	L	Deep Power Down	X	Maintain Deep Power Down	
L	H	Power Down	NOP or DESELECT	Exit Power Down	5,6,9
L	H	Self Refresh	NOP or DESELECT	Exit Self Refresh	5,7,10
L	H	Deep Power Down	NOP or DESELECT	Exit Deep Power Down	5,8
H	L	All Banks Idle	NOP or DESELECT	Precharge Power Down Entry	5
H	L	Bank(s) Active	NOP or DESELECT	Active Power Down Entry	5
H	L	All Banks Idle	AUTO REFRESH	Self Refresh Entry	
H	L	All Banks Idle	BURST TERMINATE	Enter Deep Power Down	
H	H	See the other Truth Tables			

Notes:

1. CKE n is the logic state of CKE at clock edge n; CKE n-1 was the state of CKE at the previous clock edge.
2. Current state is the state of LPDDR immediately prior to clock edge n.
3. COMMAND n is the command registered at clock edge n, and ACTION n is the result of COMMAND n.
4. All states and sequences not shown are illegal or reserved.
5. DESELECT and NOP are functionally interchangeable.
6. Power Down exit time (t_{XP}) should elapse before a command other than NOP or DESELECT is issued.
7. SELF REFRESH exit time (t_{XSR}) should elapse before a command other than NOP or DESELECT is issued.
8. The Deep Power Down exit procedure must be followed the figure of Deep Power Down Mode Entry & Exit Cycle.
9. The clock must toggle at least once during the t_{XP} period.
10. The clock must toggle at least once during the t_{XSR} time.

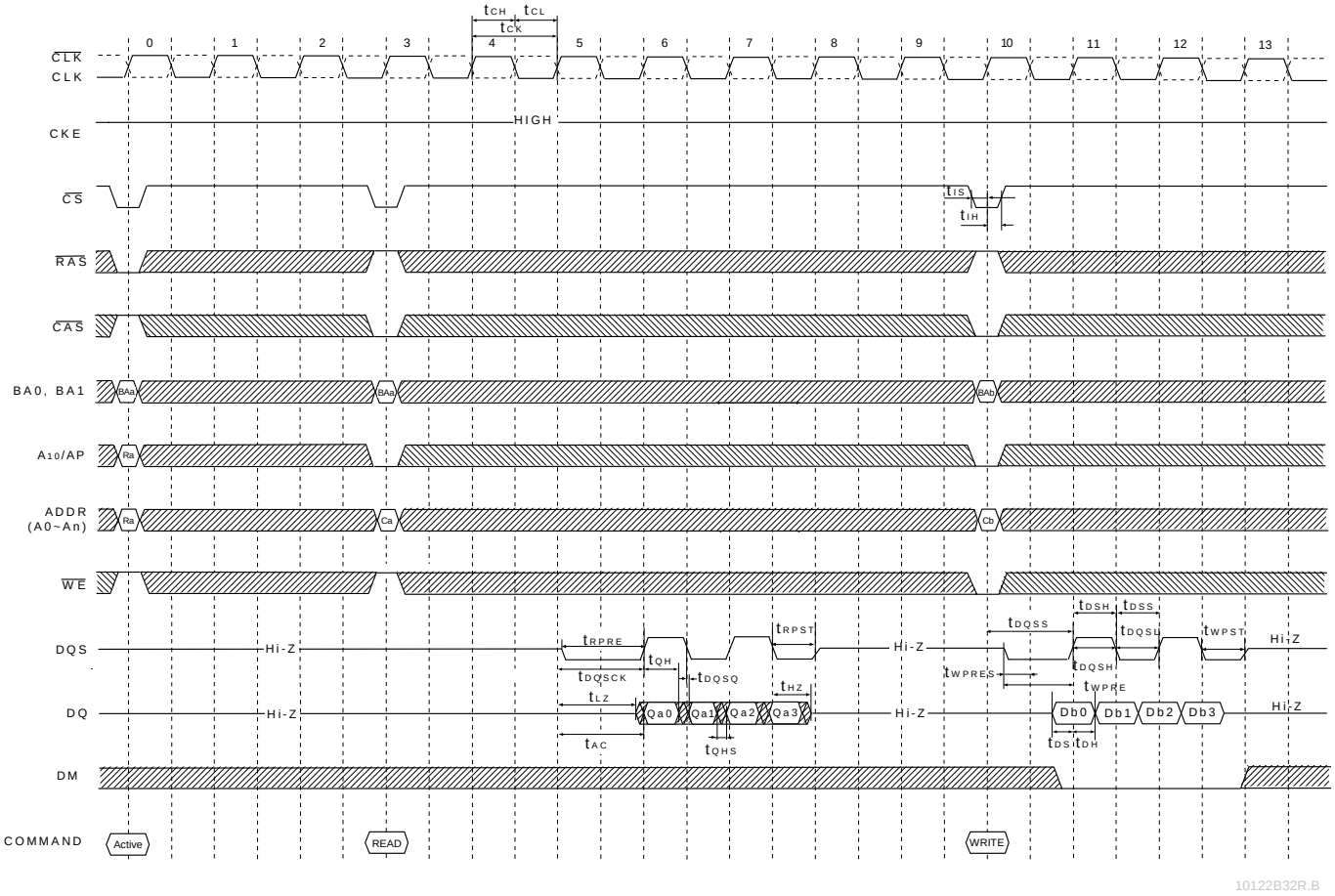
Truth Table – Current State Bank n

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	COMMAND / ACTION	NOTE
Command to Bank n [Note 1~12]						
Any	H	X	X	X	DESELECT (NOP / continue previous operation)	
	L	H	H	H	No Operation (NOP / continue previous operation)	
Idle	L	L	H	H	ACTIVE (select and activate row)	
	L	L	L	H	AUTO REFRESH	9
	L	L	L	L	MODE REGISTER SET	9
Row Active	L	H	L	H	READ (select column & start read burst)	
	L	H	L	L	WRITE (select column & start write burst)	
	L	L	H	L	PRECHARGE (deactivate row in bank or banks)	4
Read (Auto Precharge Disabled)	L	H	L	H	READ (select column & start new read burst)	5
	L	H	L	L	WRITE (select column & start write burst)	5, 12
	L	L	H	L	PRECHARGE (truncate read burst, start precharge)	
	L	H	H	L	BURST TERMINATE	10
Write (Auto Precharge Disabled)	L	H	L	H	READ (select column & start read burst)	5,11
	L	H	L	L	WRITE (select column & start new write burst)	5
	L	L	H	L	PRECHARGE (truncate write burst, start precharge)	11
Command to Bank m [Note 1~3,6, 11~16]						
Any	H	X	X	X	DESELECT (NOP / continue previous operation)	
	L	H	H	H	No Operation (NOP / continue previous operation)	
Idle	X	X	X	X	Any command allowed to bank m	
Row Activating, Active, or Precharging	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column & start read burst)	16
	L	H	L	L	WRITE (select column & start write burst)	16
	L	L	H	L	PRECHARGE	
Read (Auto Precharge disabled)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column & start new read burst)	16
	L	H	L	L	WRITE (select column & start write burst)	12,16
	L	L	H	L	PRECHARGE	
Write (Auto Precharge disabled)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column & start read burst)	11,16
	L	H	L	L	WRITE (select column & start new write burst)	16
	L	L	H	L	PRECHARGE	
Read with Auto Precharge	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column & start new read burst)	13,16
	L	H	L	L	WRITE (select column & start write burst)	12,13,16
	L	L	H	L	PRECHARGE	
Write with Auto Precharge	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column & start read burst)	13,16
	L	H	L	L	WRITE (select column & start new write burst)	13,16
	L	L	H	L	PRECHARGE	

Notes:

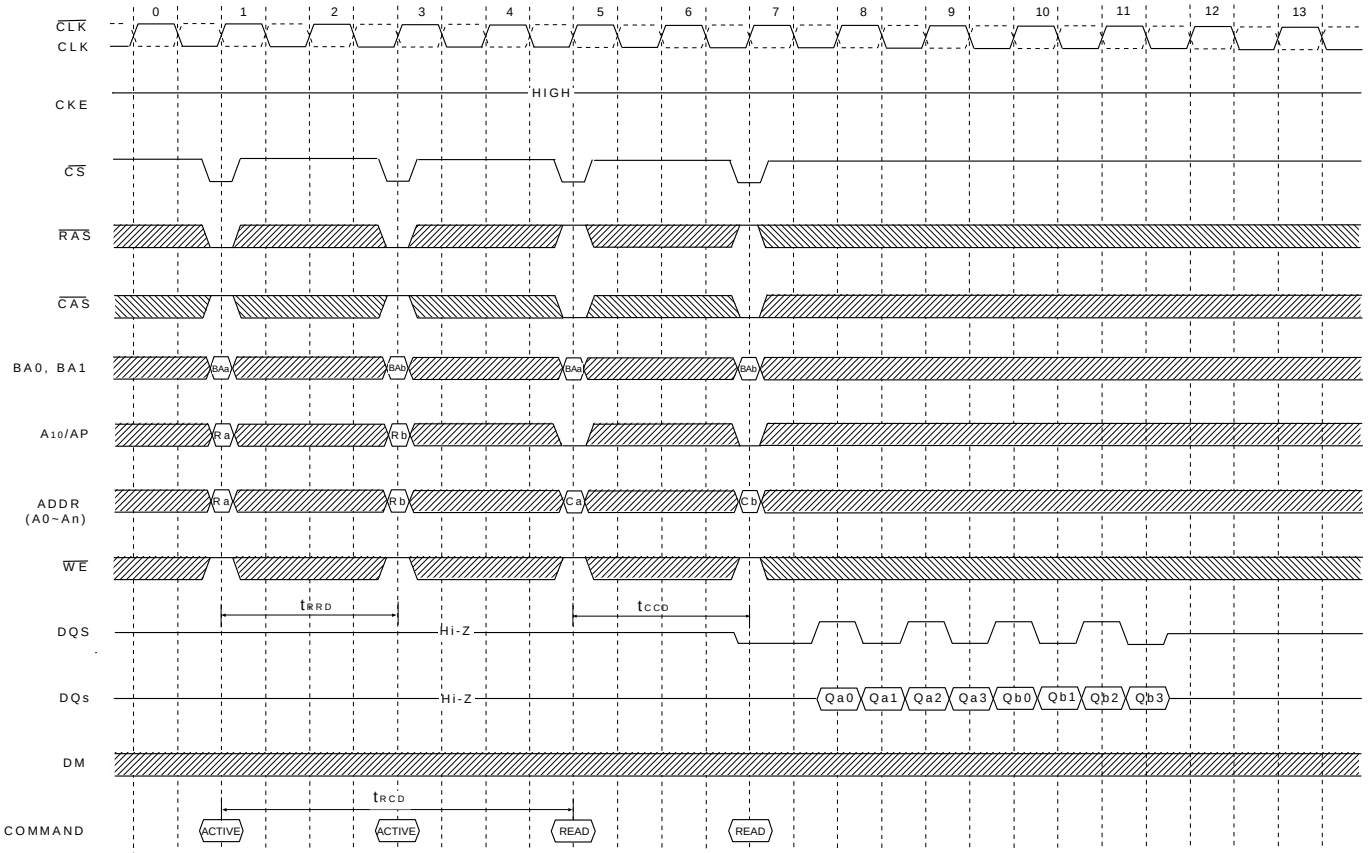
1. The table applies when both CKE n-1 and CKE n are HIGH, and after t_{XSR} or t_{XP} has been met if the previous state was Self Refresh or Power Down.
2. DESELECT and NOP are functionally interchangeable.
3. All states and sequences not shown are illegal or reserved.
4. This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for precharging.
5. The new Read or Write command could be Auto Precharge enabled or Auto Precharge disabled.
6. Current State Definitions:
   Idle: The bank has been precharged, and t_{RP} has been met.
   Row Active: A row in the bank has been activated, and t_{RCD} has been met. No data bursts / accesses and no register accesses are in progress.
   Read: A READ burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
   Write: a WRITE burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
7. The following states must not be interrupted by a command issued to the same bank. DESELECT or NOP commands or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and the part of Command to Bank n, according to the part of Command to Bank m.
   Precharging: starts with the registration of a PRECHARGE command and ends when t_{RP} is met. Once t_{RP} is met, the bank will be in the idle state.
   Row Activating: starts with registration of an ACTIVE command and ends when t_{RCD} is met. Once t_{RCD} is met, the bank will be in the 'row active' state.
   Read with AP Enabled: starts with the registration of the READ command with Auto Precharge enabled and ends when t_{RP} has been met. Once t_{RP} has been met, the bank will be in the idle state.
   Write with AP Enabled: starts with registration of a WRITE command with Auto Precharge enabled and ends when t_{RP} has been met. Once t_{RP} is met, the bank will be in the idle state.
8. The following states must not be interrupted by any executable command; DESELECT or NOP commands must be applied to each positive clock edge during these states.
   Refreshing: starts with registration of an AUTO REFRESH command and ends when t_{RFC} is met. Once t_{RFC} is met, the device will be in an 'all banks idle' state.
   Accessing Mode Register: starts with registration of a MODE REGISTER SET command and ends when t_{MRD} has been met. Once t_{MRD} is met, the device will be in an 'all banks idle' state.
   Precharging All: starts with registration of a PRECHARGE ALL command and ends when t_{RP} is met. Once t_{RP} is met, the bank will be in the idle state.
9. Not bank-specific; requires that all banks are idle and no bursts are in progress.
10. Not bank-specific. BURST TERMINATE affects the most recent read burst, regardless of bank.
11. Requires appropriate DM masking.
12. A WRITE command may be applied after the completion of data output, otherwise a BURST TERMINATE command must be issued to end the READ prior to asserting a WRITE command.
13. Read with AP enabled and Write with AP enabled: the Read with Auto Precharge enabled or Write with Auto Precharge enabled states can be broken into two parts: the access period and the precharge period. For Read with AP, the precharge period is defined as if the same burst was executed with Auto Precharge disabled and then followed with the earliest possible PRECHARGE command that still accesses all the data in the burst. For Write with AP, the precharge period begins when t_{WR} ends, with t_{WR} measured as if Auto Precharge was disabled. The access period starts with registration of the command and ends where the precharge period (or t_{RP}) begins. During the precharge period of the Read with AP enabled or Write with AP enabled states, ACTIVE, PRECHARGE, READ, and WRITE commands to the other bank may be applied; during the access period, only ACTIVE and PRECHARGE commands to the other banks may be applied. In either case, all other related limitations apply (e.g. contention between READ data and WRITE data must be avoided).
14. AUTO REFRESH, SELF REFRESH, and MODE REGISTER SET commands may only be issued when all bank are idle.
15. A BURST TERMINATE command cannot be issued to another bank; it applies to the bank represented by the current state only.
16. READs or WRITEs listed in the Command column include READs and WRITEs with Auto Precharge enabled and READs and WRITEs with Auto Precharge disabled.

Basic Timing (Setup, Hold and Access Time @ BL=4, CL=3)

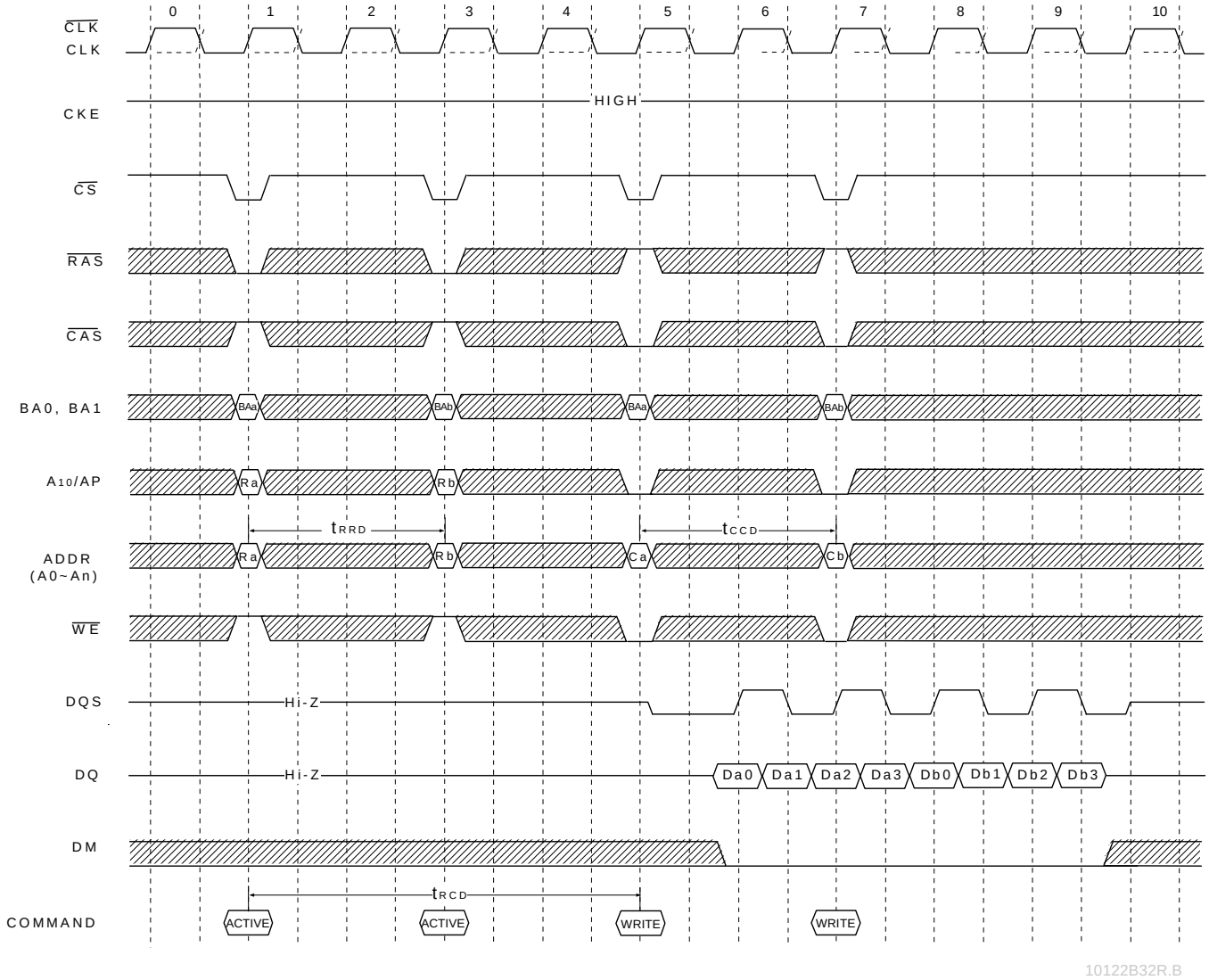


Note: t_{HP} is lesser of t_{CL} or t_{CH} clock transition collectively when a bank is active.

Multi Bank Interleaving READ (@BL=4, CL=3)



Multi Bank Interleaving WRITE (@BL=4)



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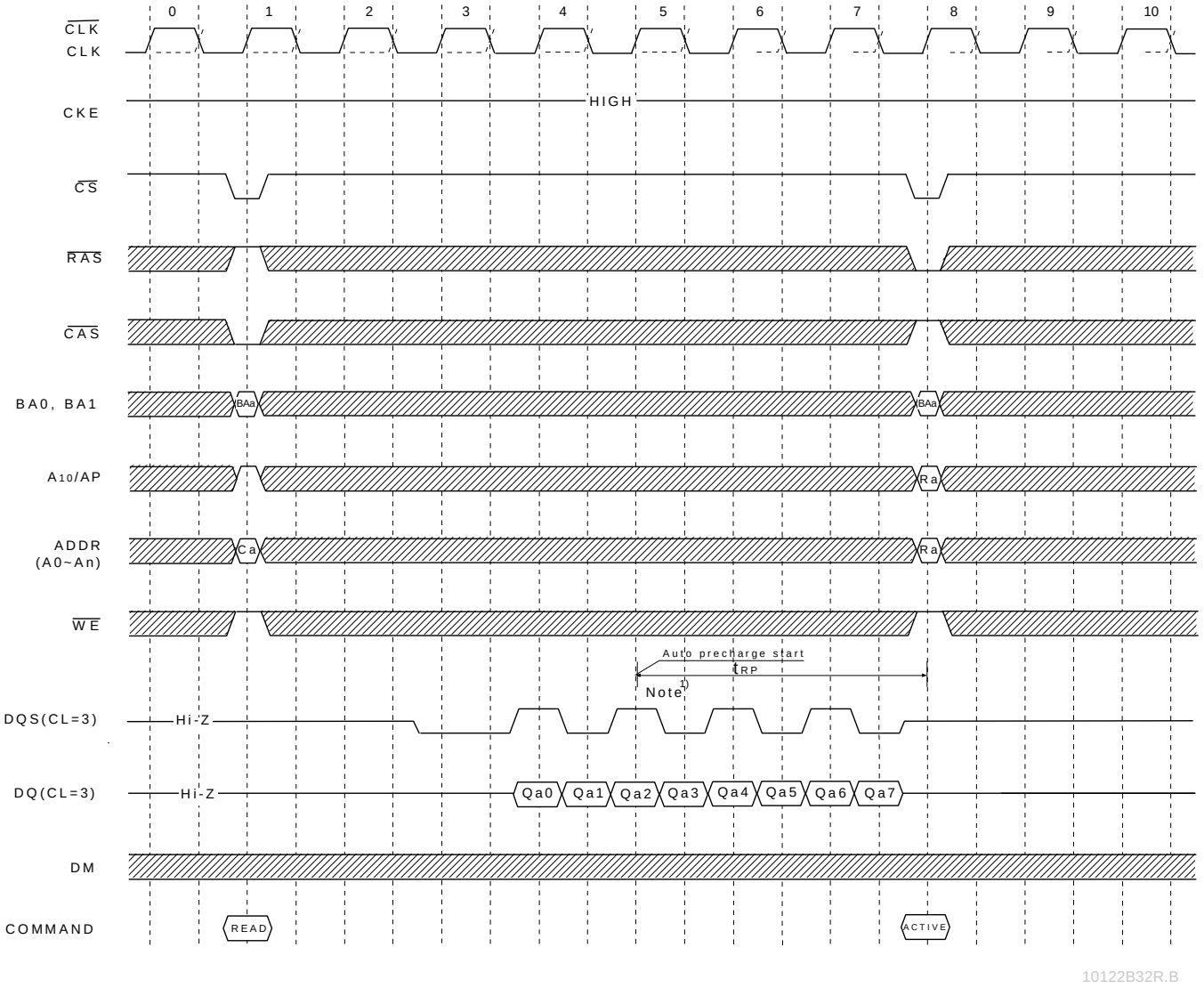
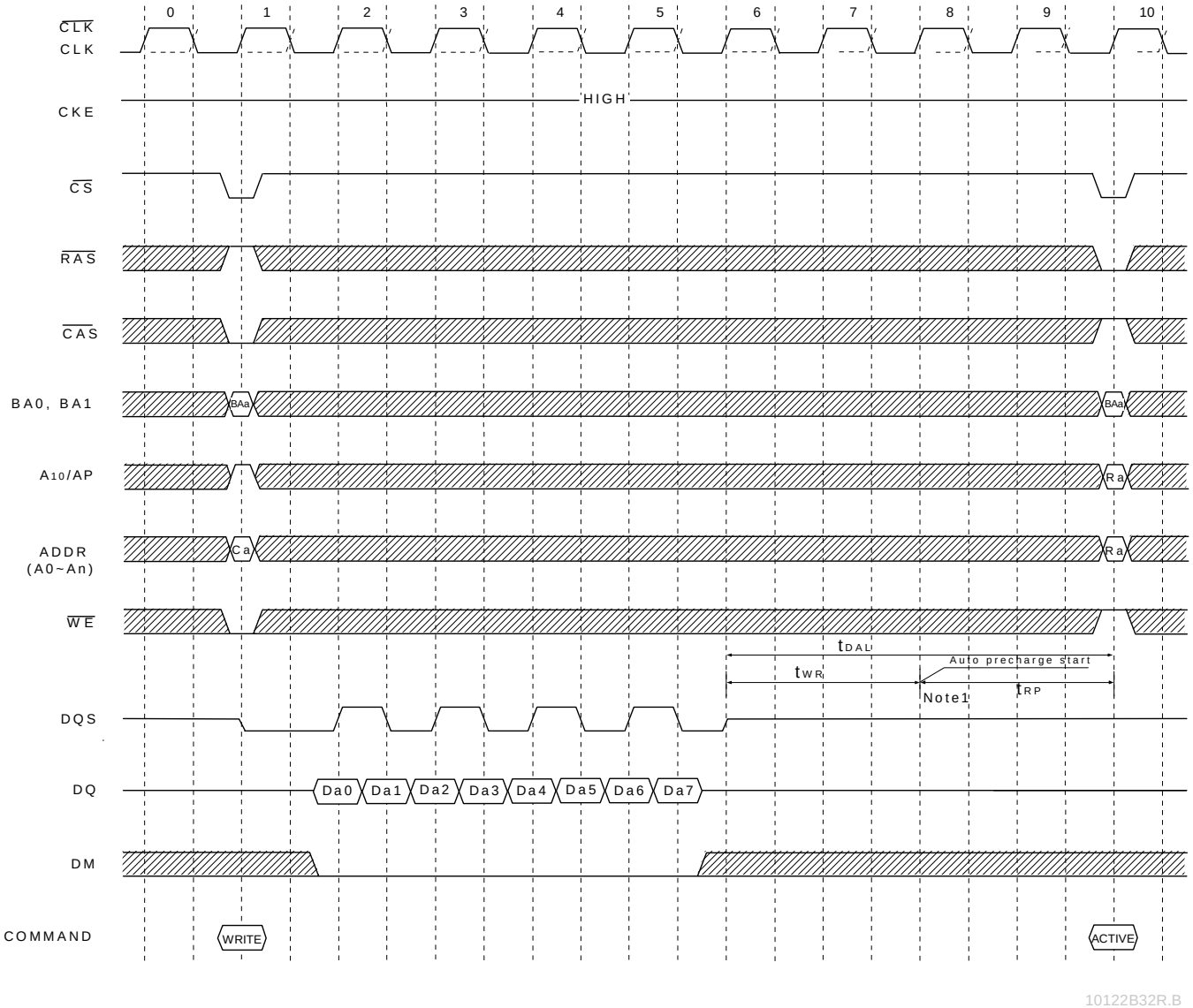
Read with Auto Precharge (@BL=8)



Note: The row active command of the precharge bank can be issued after t_{RP} from this point.

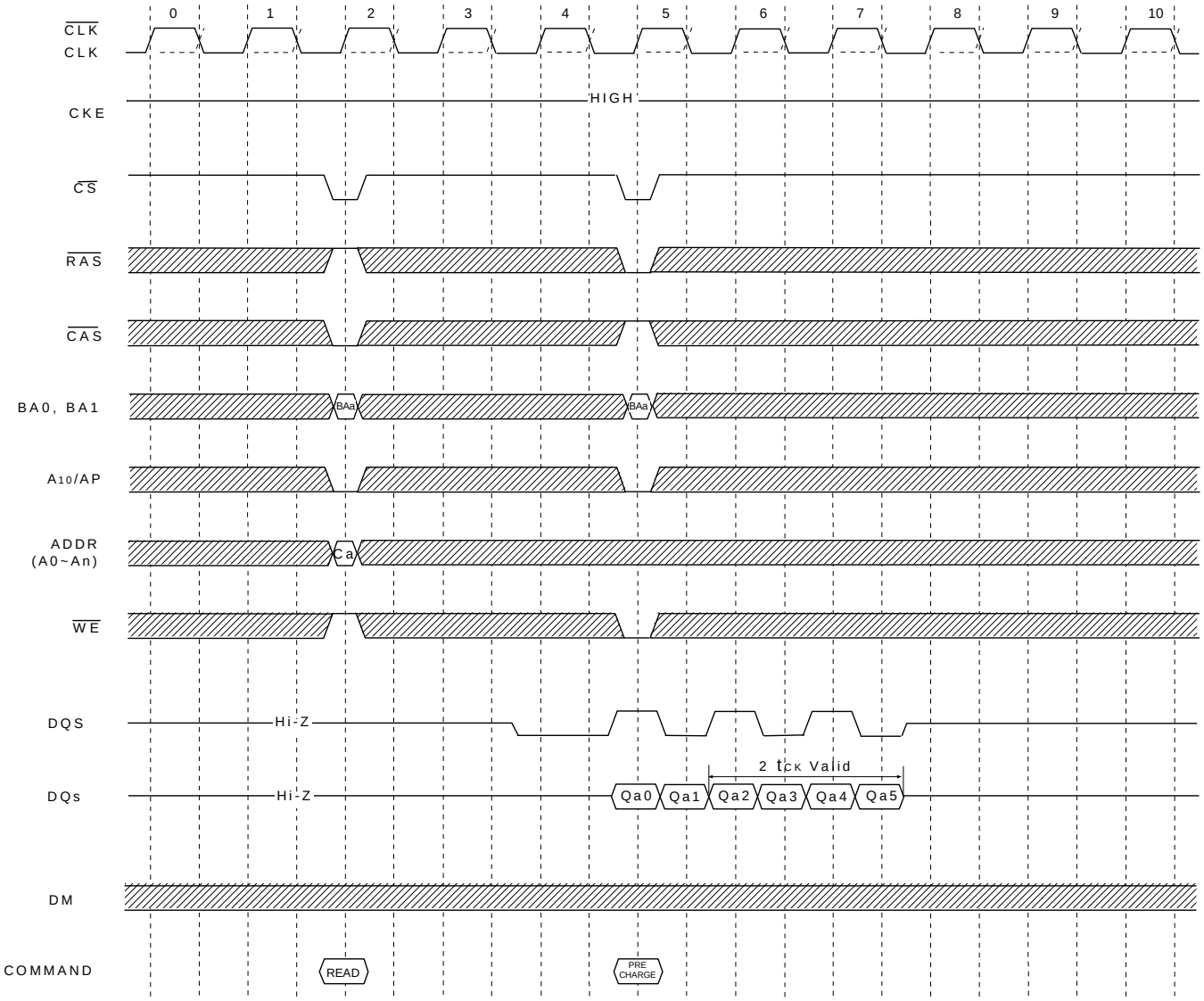
Write with Auto Precharge (@BL=8)



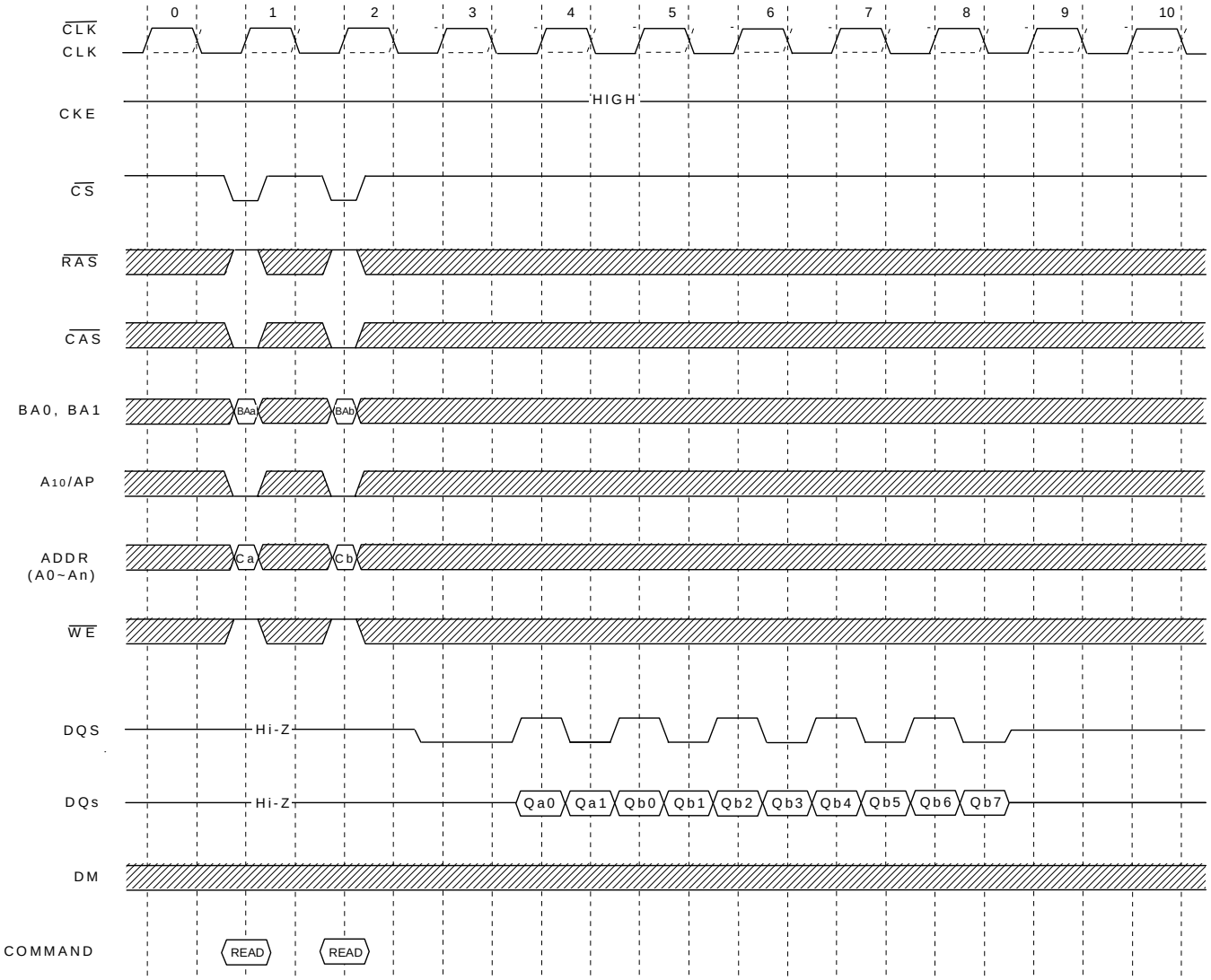
Note: The row active command of the precharge bank can be issued after t_{RP} from this point.

Read Interrupted by Precharge (@BL=8)

.



Read Interrupted by a Read (@BL=8, CL=3)



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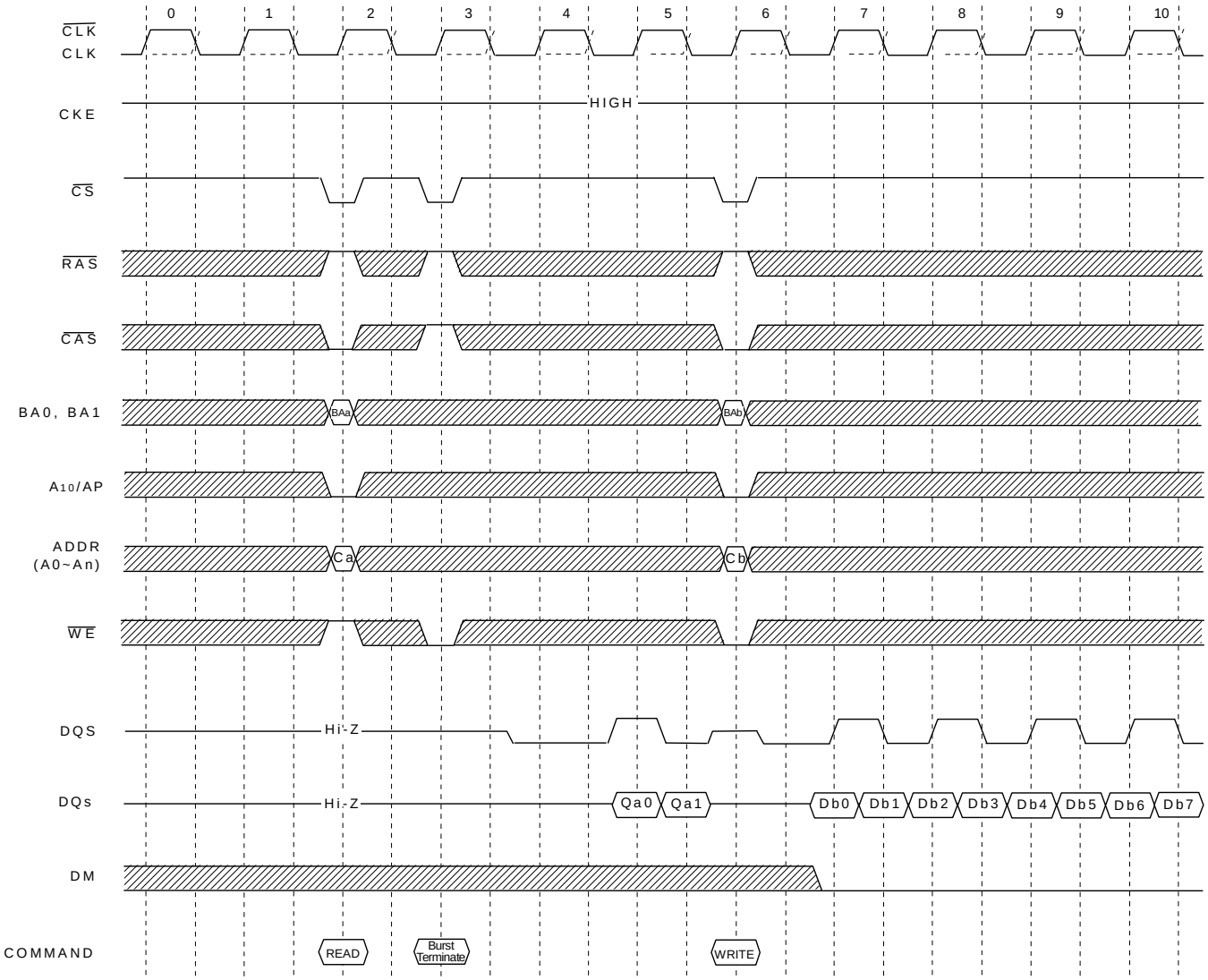
Read Interrupted by a Write & Burst Terminate (@BL=8, CL=3)



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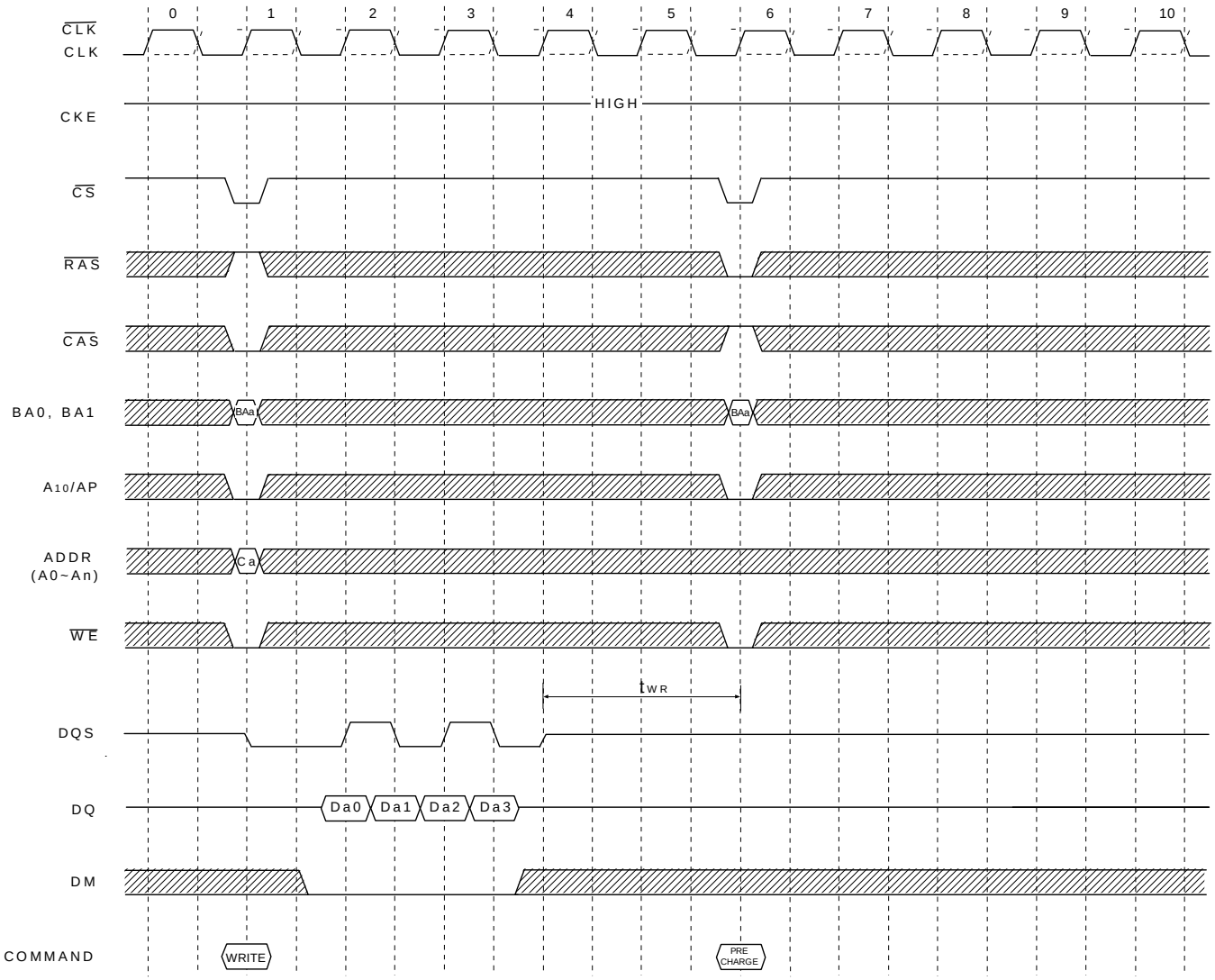
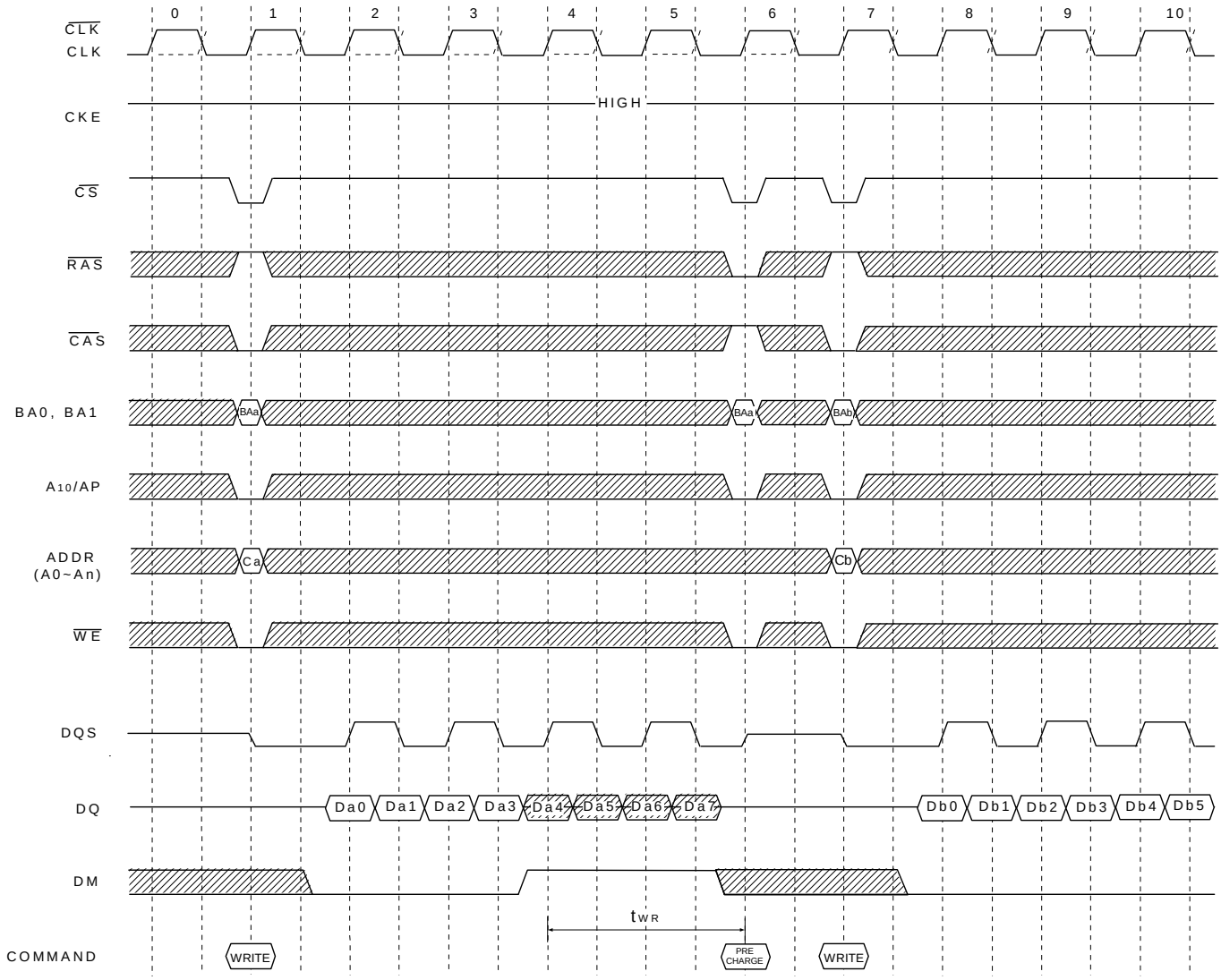
Write followed by Precharge (@BL=4)



Write Interrupted by Precharge & DM (@BL=8)



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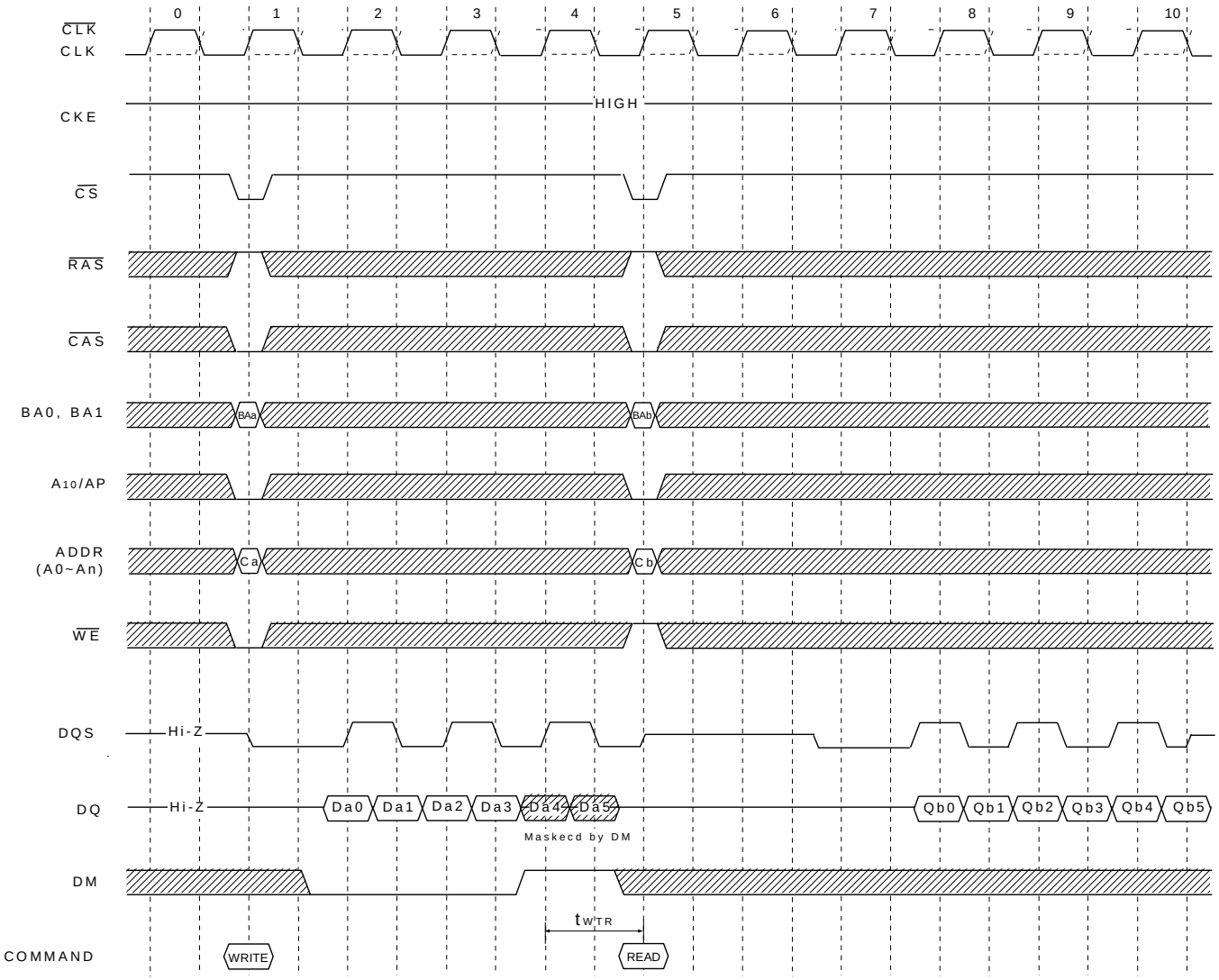
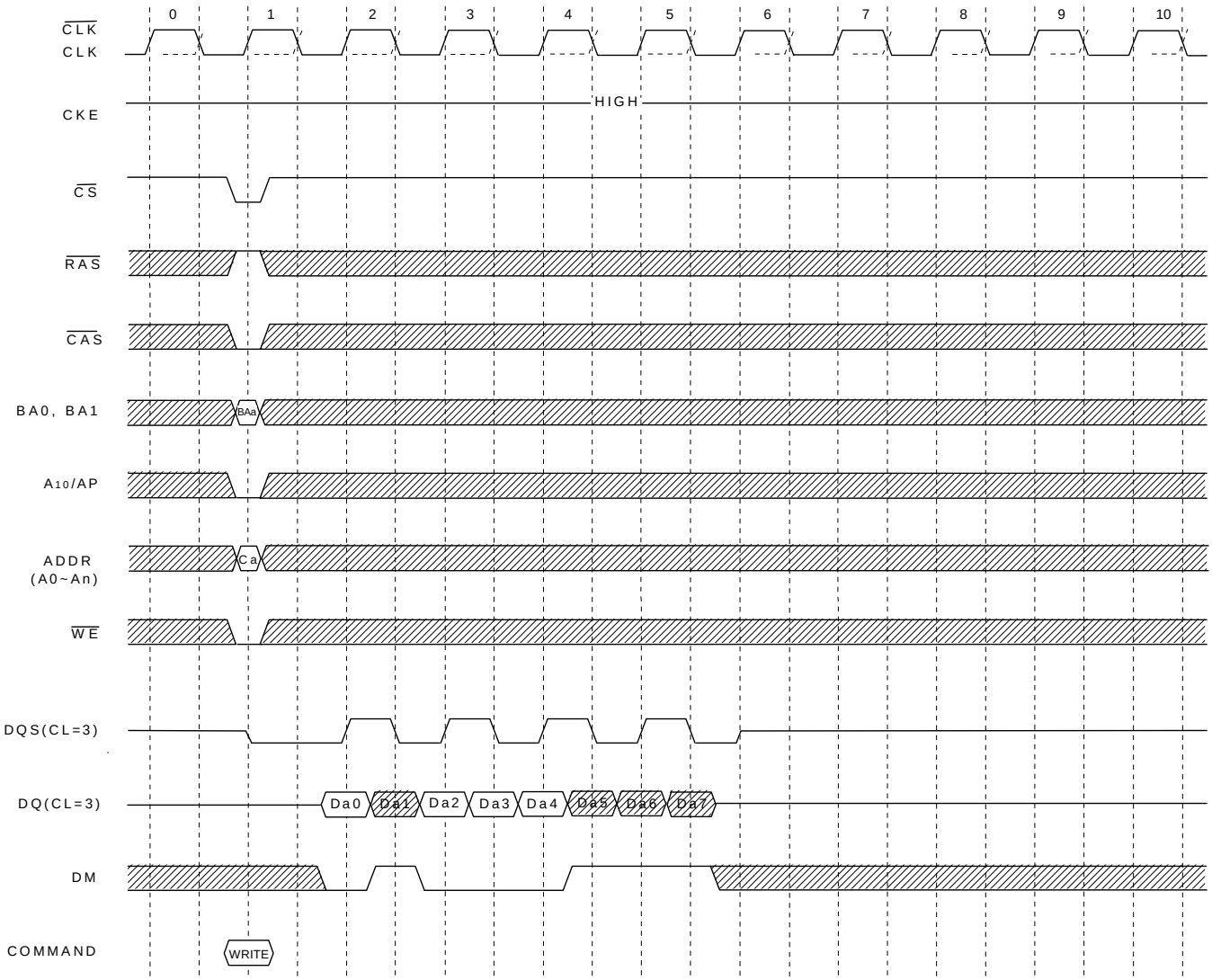
Write Interrupted by a Read (@BL=8, CL=3)



DM Function (@BL=8) only for write



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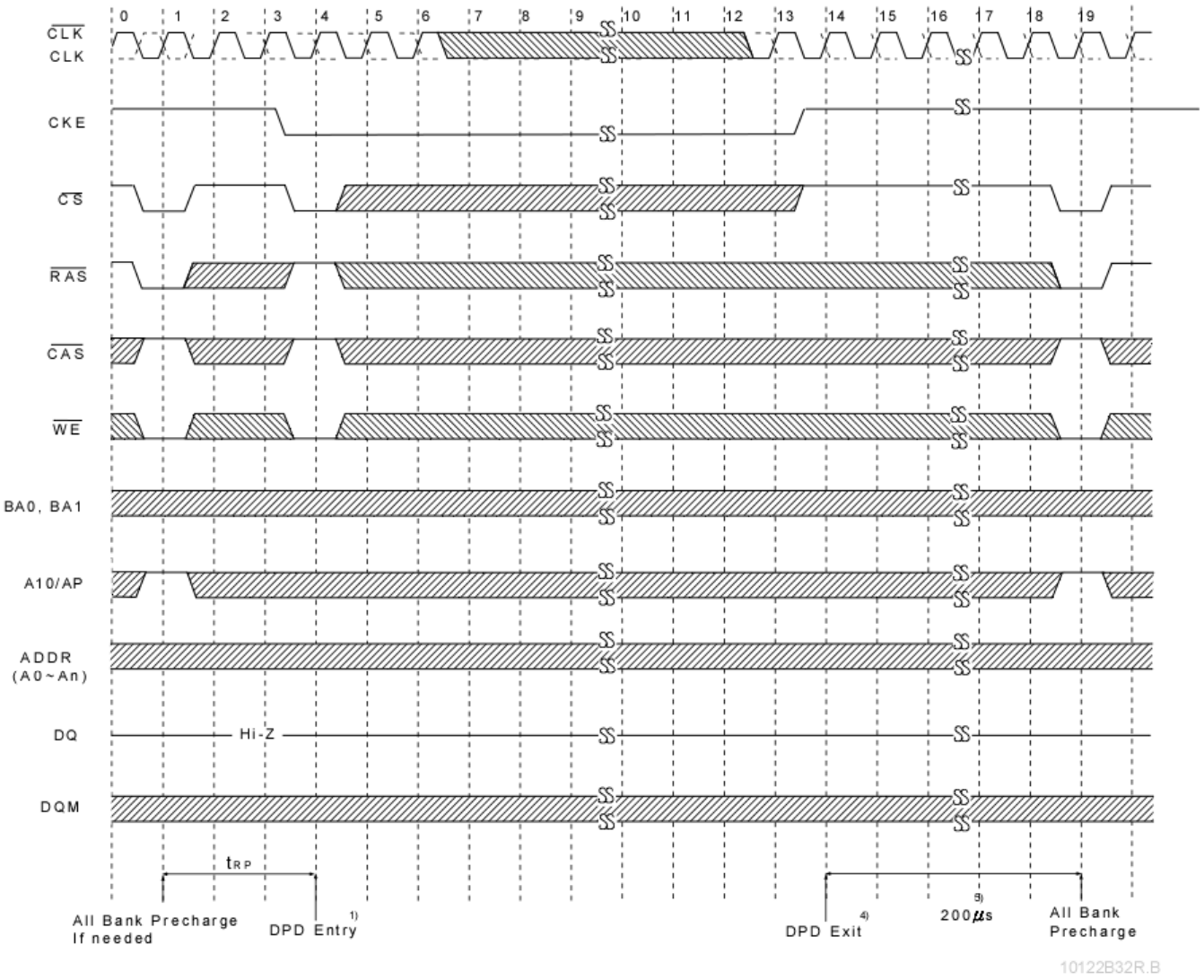
Deep Power Down Mode Entry & Exit Cycle



Note:

DEFINITION OF DEEP POWER MODE FOR LPDDR SDRAM:
Deep Power Down Mode is an operating mode to achieve maximum power reduction by cutting the power of the whole memory of the device. Once the device enters in Deep Power Down Mode, data will not be retained. Full initialization is required when the device exits from Deep Power Down Mode.

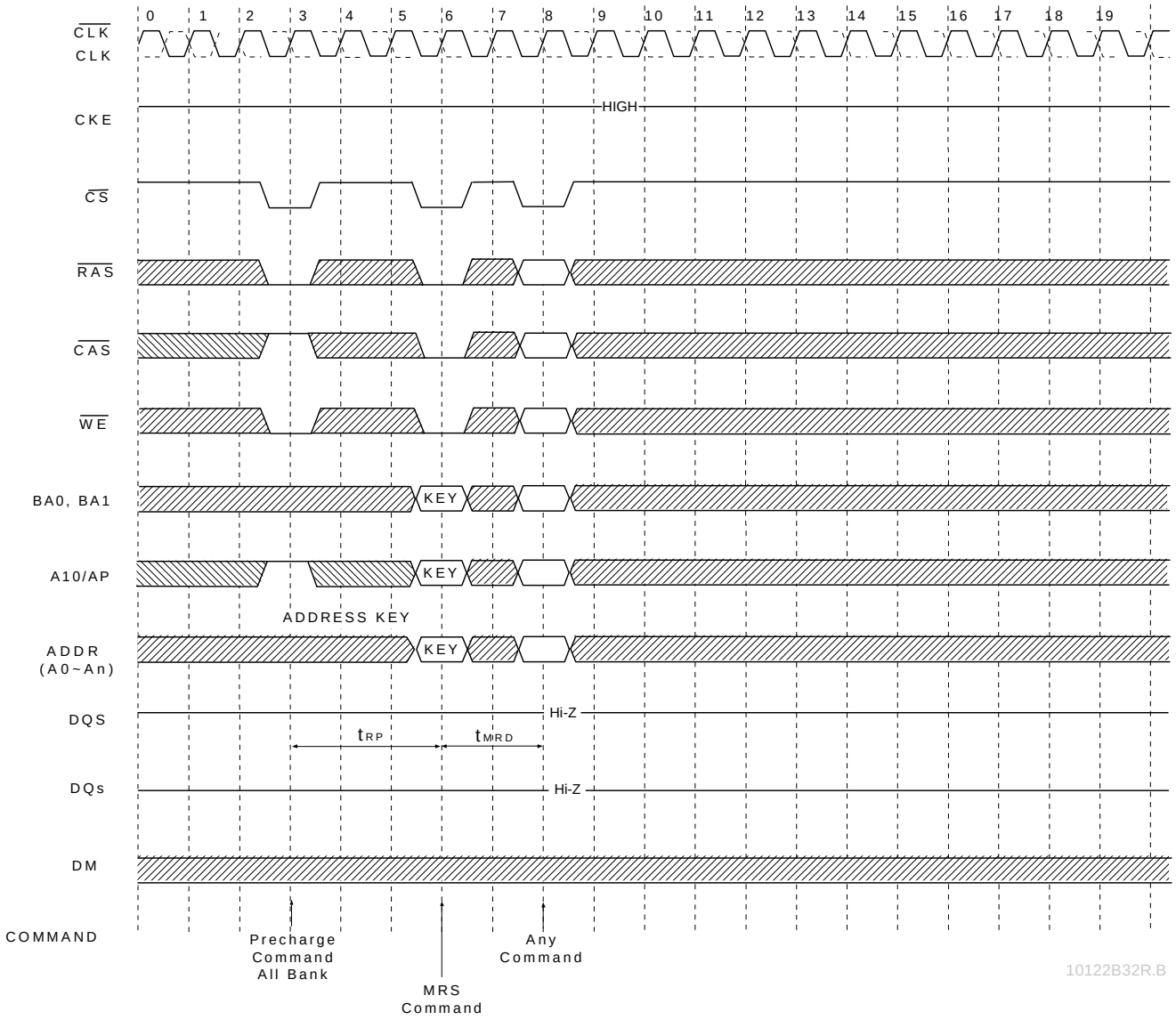
TO ENTER DEEP POWER DOWN MODE

1) The deep power down mode is entered by having $\overline{CS}$ and $\overline{WE}$ held low with $\overline{RAS}$ and $\overline{CAS}$ high at the rising edge of the clock. While CKE is low.
2) Clock must be stable before exited deep power down mode.
3) Device must be in the all banks idle state prior to entering Deep Power Down mode.

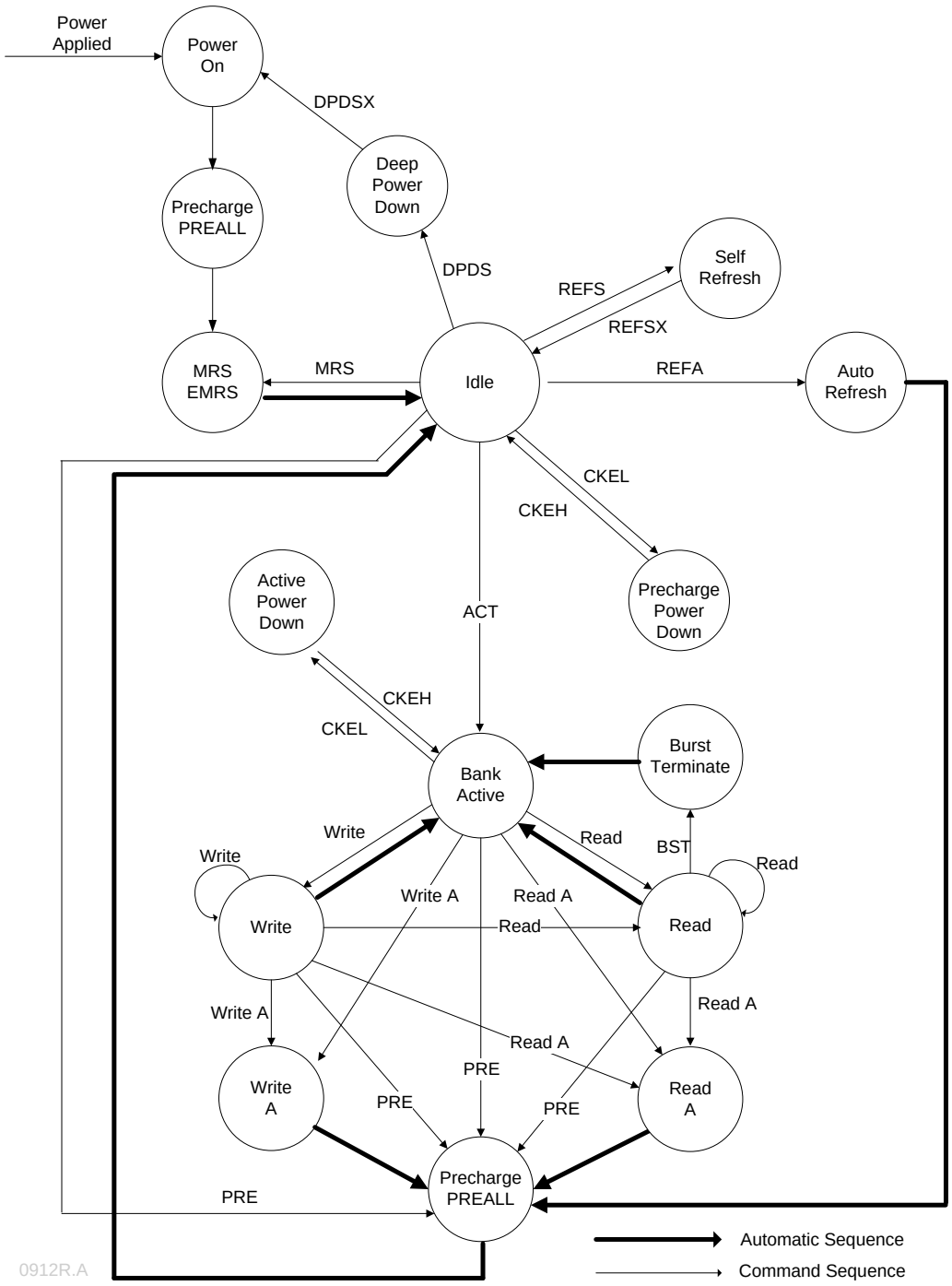
TO EXIT DEEP POWER DOWN MODE

4) The deep power down mode is exited by asserting CKE high.
5) 200μ s wait time is required to exit from Deep Power Down.
6) Upon exiting deep power down an all bank precharge command must be issued followed by two auto refresh commands and a load mode register sequence.

Mode Register Set



Simplified State Diagram

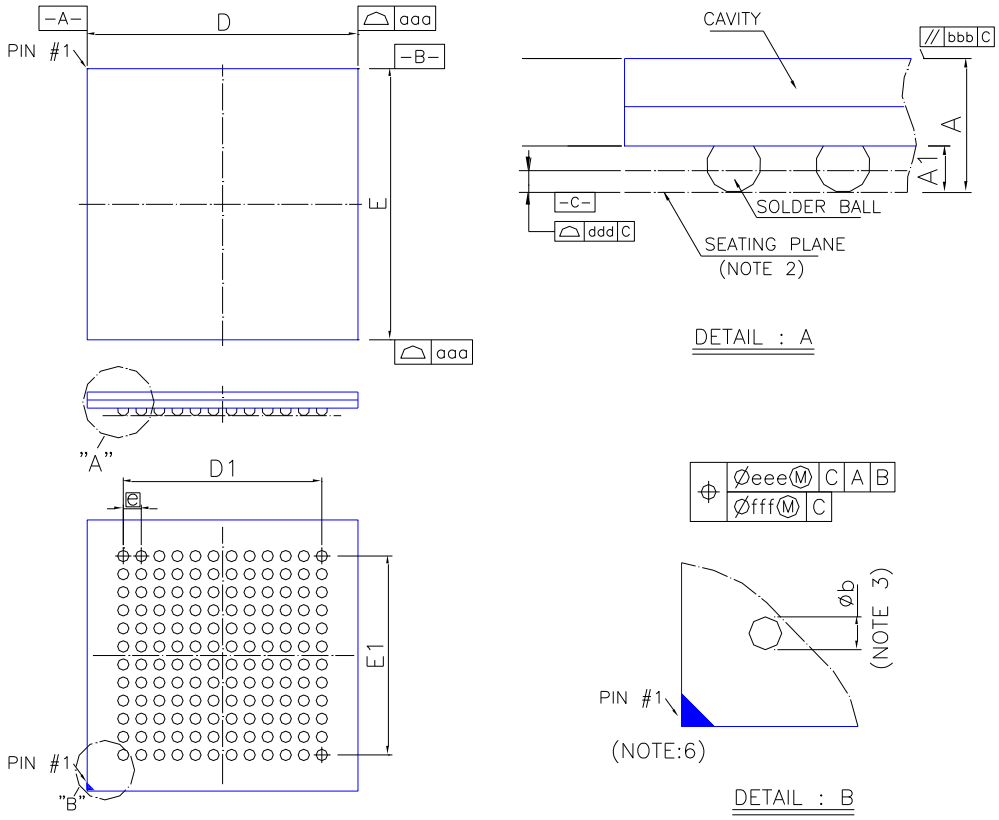


PREALL = Precharge All Banks
MRS = Mode Register Set
EMRS = Extended Mode Register Set
REFS = Enter Self Refresh
REFSX = Exit Self Refresh
REFA = Auto Refresh
CKEL = Enter Power Down
CKEH = Exit Power Down
ACT = Active

Write = Write w/o Auto Precharge
Write A = Write with Auto Precharge
Read = Read w/o Auto Precharge
Read A = Read with Auto Precharge
PRE = Precharge
BST = Burst Terminate
DPDS = Enter Deep Power-Down
DPDSX = Exit Deep Power-Down

PACKING DIMENSIONS

144-BALL FBGA DDR DRAM (12x12mm)



NOTE :

1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. THERE SHALL BE A MINIMUM CLEARANCE OF 0.25mm BETWEEN THE EDGE OF THE SOLDER BALL AND THE BODY EDGE.
5. REFERANCE DOCUMENT : JEDEC MO-205 .
6. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY .

Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max
A	1.14		1.40	0.049		0.055
A1	0.30	0.35	0.40	0.012	0.014	0.016
Φb	0.40	0.45	0.50	0.016	0.018	0.020
D	11.90	12.00	12.10	0.469	0.472	0.476
E	11.90	12.00	12.10	0.469	0.472	0.476
D1		8.80			0.346	
E1		8.80			0.346	
e		0.80			0.031	
aaa	0.10			0.004		
bbb	0.10			0.004		
ddd	0.12			0.005		
eee	0.15			0.004		
fff	0.08			0.006		
MD/ME	12/12			12/12		

Revision History

Revision	Date	Description
0.1	2013.11.26	Original
1.0	2015.03.19	1. Delete "Preliminary" 2.Modify speed grade 3.Modify the specification of IDD for speed grade -5 4. Delete 1.2V VDDQ
1.1	2016.01.18	1. Update Capacitance 2. Modify Mobile DDR to LPDDR 3. Modify the specification of tAC(3)/tDQSCK (3) for speed grade -4/-4.5

Important Notice

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