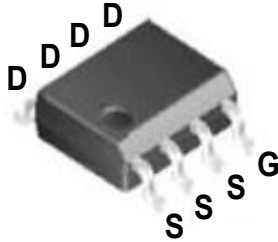
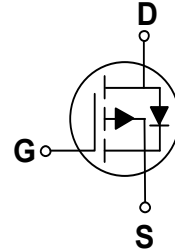


# P-Channel Enhancement Mode Field Effect Transistor



SOP-8



### Features

- $V_{DS} = -30V / I_D = -7A$
- $R_{DS(ON)} \leq 30m\Omega @ V_{GS} = -10V$
- Super high density cell design for extremely low  $R_{DS(ON)}$
- Suit for -4.5V Gate Drive Applications
- Fast switching
- SOP-8 package design

### Applications

- Notebook
- Battery Protection
- Load Switch
- Hand-held Instruments

### Ordering Information

| Part No. | Remark         | Package | Packing            |
|----------|----------------|---------|--------------------|
| ER3909   | RoHS Compliant | SOP-8   | 3000 / Tape & Reel |
| ER3909-H | Halogen Free   |         |                    |

### Maximum Ratings (TA=25°C unless otherwise noted)

| Parameter                              | Symbol         | Limits   | Unit |
|--|----------------|----------|------|
| Drain-Source Voltage                   | $V_{DS}$       | -30      | V    |
| Gate-Source Voltage                    | $V_{GS}$       | $\pm 20$ | V    |
| Continuous Drain Current               | $I_D$          | -7       | A    |
| Pulsed Drain Current                   | $I_{DM}$       | -30      | A    |
| Power Dissipation                      | $P_D$          | 2        | W    |
| Junction and Storage Temperature Range | $T_J, T_{STG}$ | -55~+150 | °C   |

### Thermal Characteristics

| Parameter           | Symbol          | Max | Unit |
|---------------------|-----------------|-----|------|
| Junction-to-Ambient | $R_{\theta JA}$ | 62  | °C/W |

**ER3909**

# P-Channel Enhancement Mode Field Effect Transistor

**Electrical Characteristics (TA=25°C unless otherwise noted)**

| Parameter   | Symbol   | Min.          | Typ. | Max. | Unit      |            |
|---|--|---------------|------|------|-----------|------------|
| <b>Static Parameters</b>                              |  |               |      |      |           |            |
| Drain-Source Breakdown Voltage                        | $I_D = -250\mu A, V_{GS} = 0V$                             | $V_{(BR)DSS}$ | -30  | -    | -         | V          |
| Gate Threshold Voltage                                | $V_{DS} = V_{GS}, I_D = -250\mu A$                         | $V_{GS(th)}$  | -1   | -    | -2.5      | V          |
| Gate-Body leakage current                             | $V_{DS} = 0V, V_{GS} = \pm 20V$                            | $I_{GSS}$     | -    | -    | $\pm 100$ | nA         |
| Zero Gate Voltage Drain Current                       | $V_{DS} = -24V, V_{GS} = 0V, T_J = 25^\circ C$             | $I_{DSS}$     | -    | -    | -1        | $\mu A$    |
| Forward Transconductance <sup>A</sup>                 | $V_{DS} = -5V, I_D = -7A$                                  | $g_{fs}$      | -    | 10   | -         | S          |
| Drain-Source On-State Resistance <sup>A</sup>         | $V_{GS} = -10V, I_D = -4A$                                 | $R_{DS(ON)}$  | -    | -    | 30        | m $\Omega$ |
|   | $V_{GS} = -4.5V, I_D = -2A$                                |               | -    | -    | 55        |            |
| <b>Dynamic Parameters</b>                             |  |               |      |      |           |            |
| Input Capacitance                                     | $V_{GS} = 0V, V_{DS} = -15V, f = 1MHz$                     | $C_{iss}$     | -    | 930  | -         | pF         |
| Output Capacitance                                    |  | $C_{oss}$     | -    | 148  | -         |            |
| Reverse Transfer Capacitance                          |  | $C_{rss}$     | -    | 115  | -         |            |
| Total Gate Charge <sup>B</sup>                        | $V_{GS} = -4.5V, V_{DS} = -20V, I_D = -7A$                 | $Q_g$         | -    | 9.8  | -         | nC         |
| Gate-Source Charge <sup>B</sup>                       |  | $Q_{gs}$      | -    | 2.2  | -         |            |
| Gate-Drain Charge <sup>B</sup>                        |  | $Q_{gd}$      | -    | 3.4  | -         |            |
| Turn-On Delay Time <sup>B</sup>                       | $V_{DS} = -24V, R_G = 3.3\Omega, V_{GS} = -10V, I_D = -1A$ | $t_{d(on)}$   | -    | 16.4 | -         | nS         |
| Turn-On Rise Time <sup>B</sup>                        |  | $t_r$         | -    | 20.2 | -         |            |
| Turn-Off Delay Time <sup>B</sup>                      |  | $t_{d(off)}$  | -    | 55   | -         |            |
| Turn-Off Fall Time <sup>B</sup>                       |  | $t_f$         | -    | 10   | -         |            |
| Gate resistance                                       | $V_{GS} = 0V, V_{DS} = 0V, f = 1MHz$                       | $R_g$         | -    | 15   | -         | $\Omega$   |
| <b>Source-Drain Diode Ratings And Characteristics</b> |  |               |      |      |           |            |
| Continuous Current                                    | $V_G = V_D = 0V, \text{ Force Current}$                    | $I_S$         | -    | -    | -7        | A          |
| Pulsed Current <sup>C</sup>                           |  | $I_{SM}$      | -    | -    | -14       | A          |
| Diode Forward Voltage <sup>A</sup>                    | $I_S = -2.3A, V_{GS} = 0V$                                 | $V_{SD}$      | -    | -    | -1.2      | V          |

NOTES :

A : Pulse test : Pulse width  $\leq 300 \mu sec$ , Duty Cycle  $\leq 2\%$ 

B : Independent of operating temperature

C : Pulse width limited by maximum junction temperature



# P-Channel Enhancement Mode Field Effect Transistor

## Typical Characteristics

Fig. 1 - Typical Output Characteristics

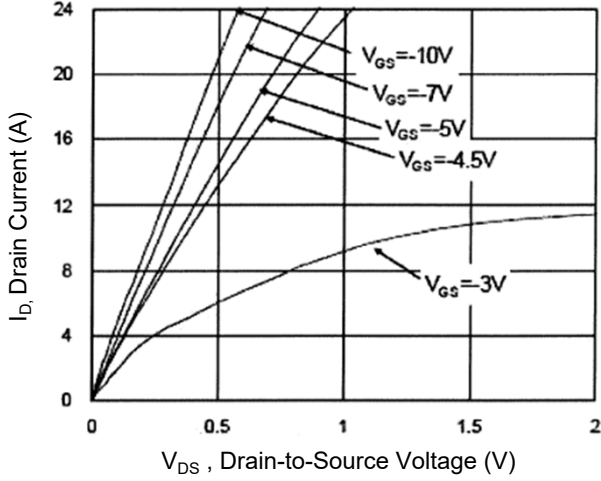


Fig. 2 - Typical Output Characteristics

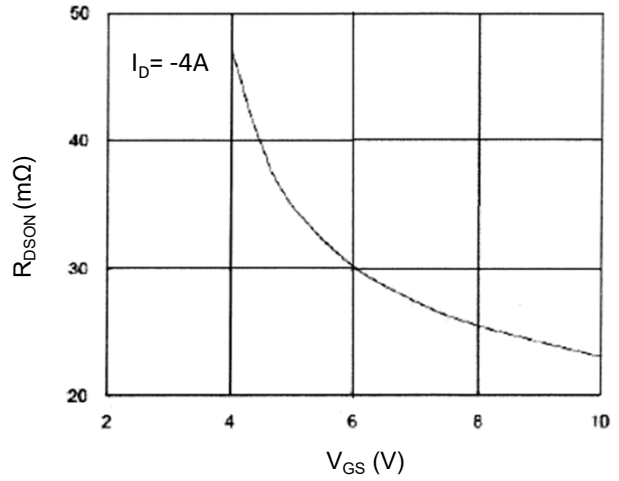


Fig. 3 - Forward Characteristics of Reverse

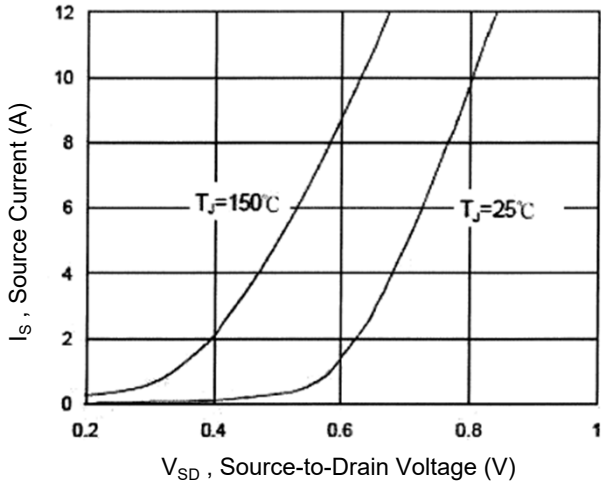


Fig. 4 - Gate-Charge Characteristics

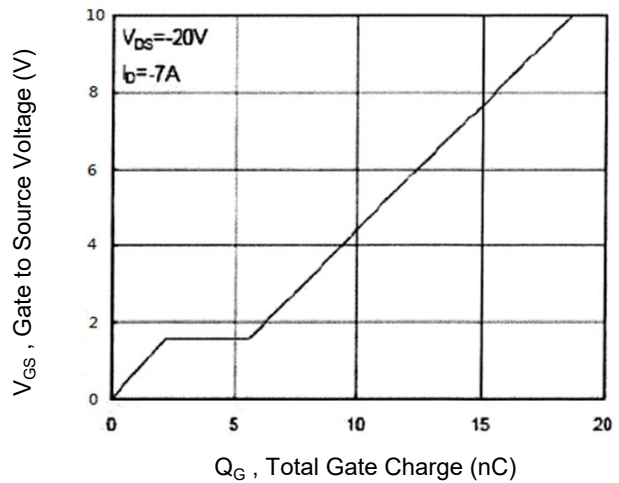


Fig. 5 - Normalized  $V_{GS(th)}$  v.s  $T_J$

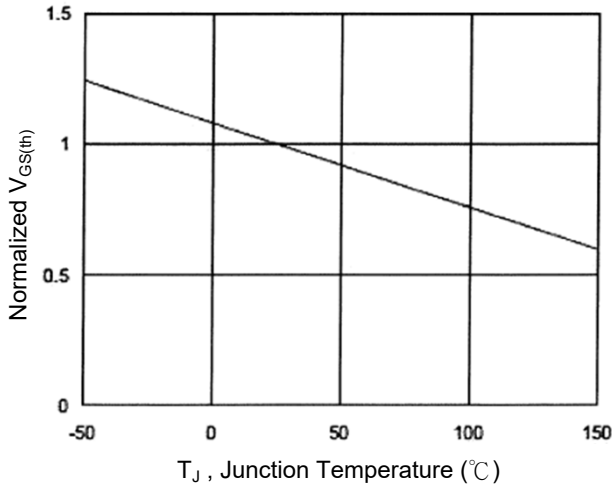
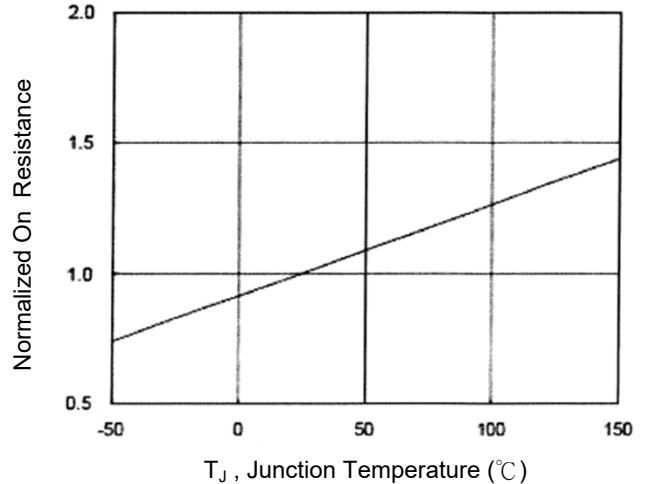


Fig. 6 - Normalized  $R_{DS(on)}$  v.s  $T_J$





# P-Channel Enhancement Mode Field Effect Transistor

## Typical Characteristics

Fig. 7 - Capacitance

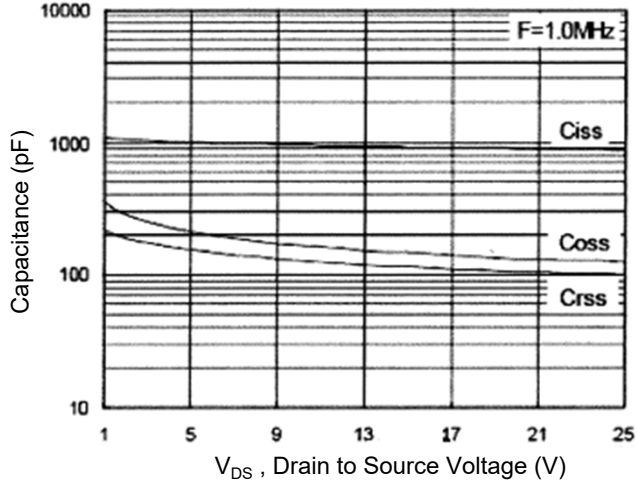


Fig. 8 - Safe Operating Area

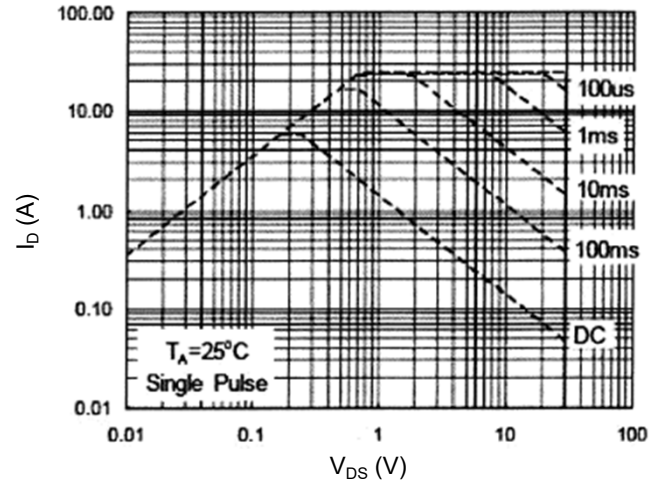


Fig. 9 - Normalized Maximum Transient Thermal Impedance

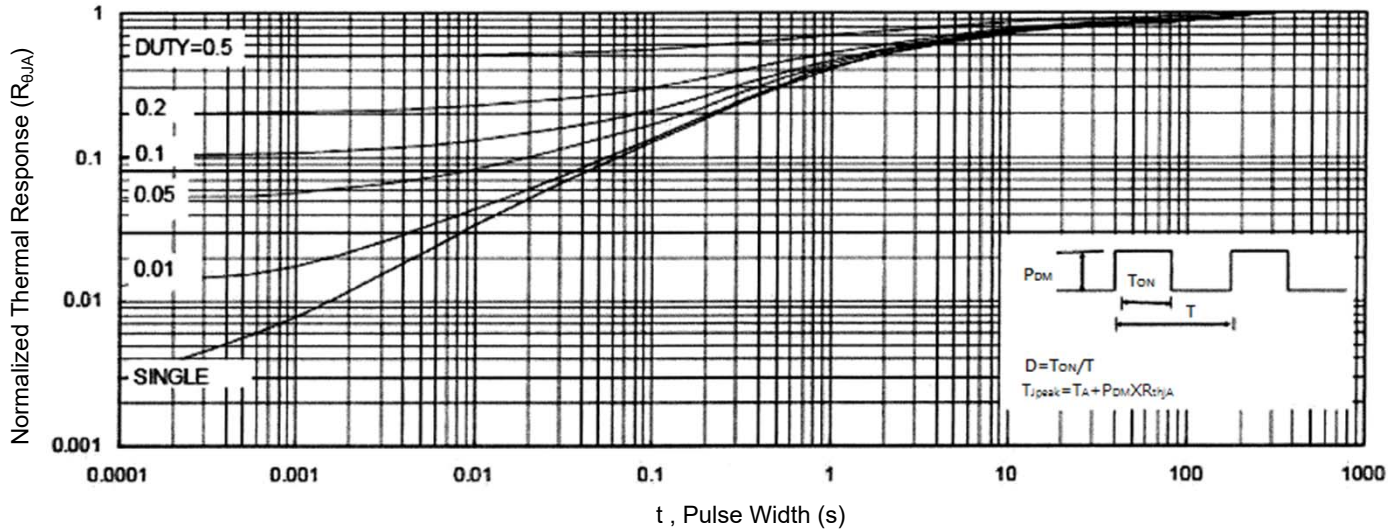
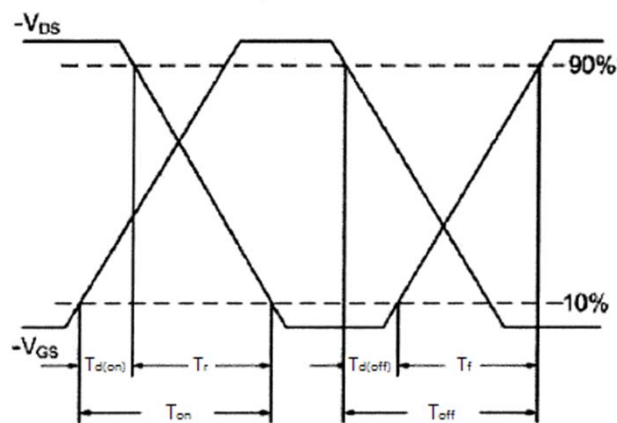


Fig. 10 - Switching Time Waveform



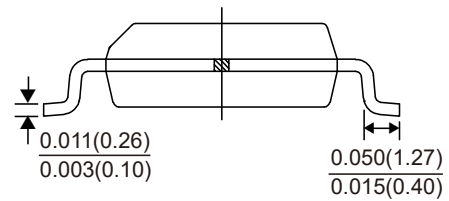
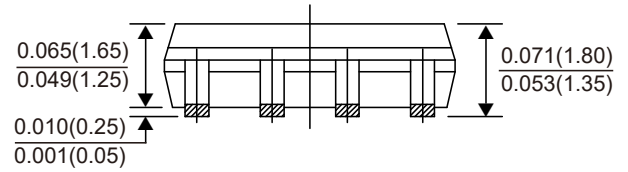
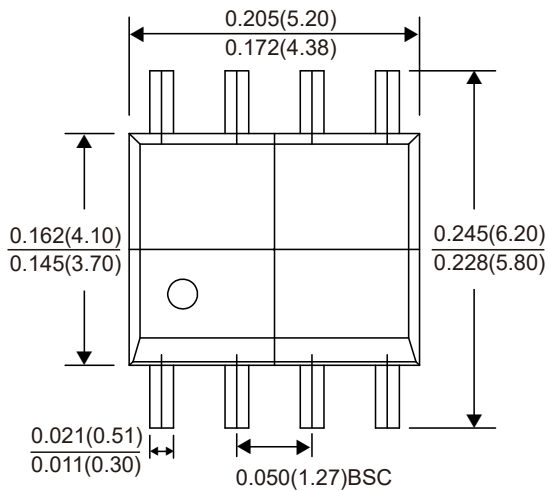


ER3909



# P-Channel Enhancement Mode Field Effect Transistor

## Package Outline Dimensions

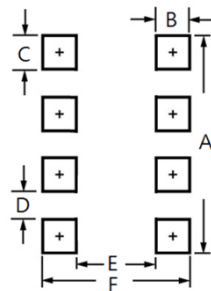


## SOP-8

Dimensions in inches and (millimeters)

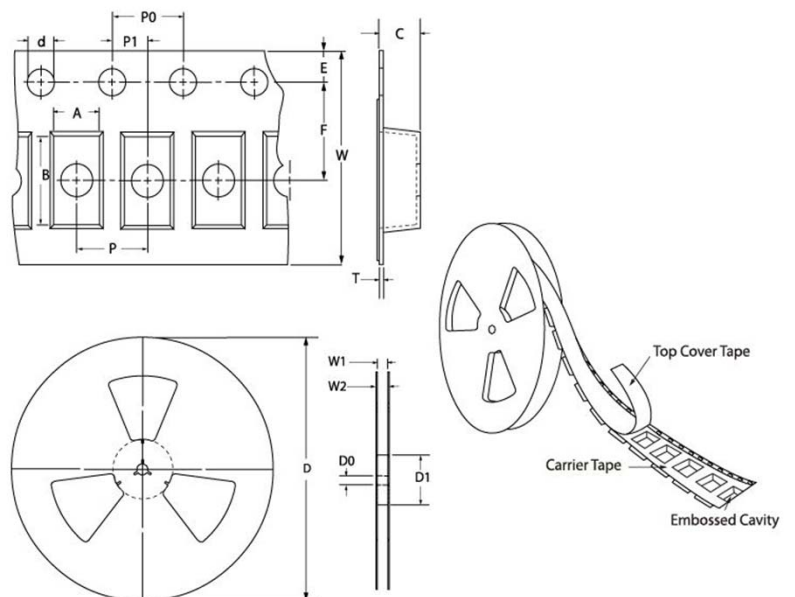
## Suggested Pad Layout

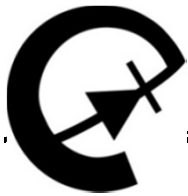
| Symbol | Outline | SOP-8 millimeters |
|--------|---------|-------------------|
| A      |         | 4.51              |
| B      |         | 1.00              |
| C      |         | 0.70              |
| D      |         | 0.57              |
| E      |         | 4.40              |
| F      |         | 6.40              |



## Tape & Reel Specification

| Item                   | Symbol | SOP-8 (mm)   |
|------------------------|--------|--------------|
| Carrier width          | A      | 6.4 ± 0.1    |
| Carrier length         | B      | 5.2 ± 0.1    |
| Carrier depth          | C      | 2.1 ± 0.1    |
| Sprocket hole          | d      | 1.5 ± 0.1    |
| Reel outside diameter  | D      | 330 ± 1      |
| Feed hole diameter     | D0     | 13.0 ± 0.3   |
| Reel inner diameter    | D1     | 100.0 ± 0.5  |
| Sprocket hole position | E      | 1.7 ± 0.15   |
| Punch hole position    | F      | 5.5 ± 0.1    |
| Sprocket hole pitch    | P      | 8 ± 0.1      |
| Sprocket hole pitch    | P0     | 4 ± 0.1      |
| Embossment center      | P1     | 2 ± 0.05     |
| Overall tape thickness | T      | 0.245 ± 0.15 |
| Tape width             | W      | 12.0 ± 0.15  |
| Reel width             | W2     | 18.6 (max)   |
| Reel width             | W1     | 14 (max)     |





---

**P-Channel Enhancement Mode  
Field Effect Transistor****LEGAL DISCLAIMER**

- The product is provided “AS IS” without any guarantees or warranty. In association with the product, Eris Technology Corporation, its affiliates, and their directors, officers, employees, agents, successors and assigns (collectively, the “Eris”) makes no warranties of any kind, either express or implied, including but not limited to warranties of merchantability, fitness for a particular purpose, of title, or of non-infringement of third party rights.
- The information in this document and any product described herein are subject to change without notice and should not be construed as a commitment by Eris. Eris assumes no responsibility for any errors that may appear in this document.
- Eris does not assume any liability arising out of the application or use of this document or any product described herein, any Customer or user of this document or products described herein in such applications shall assume all risks of such use and will agree to hold Eris and all the companies whose products are represented on Eris website, harmless against all damages.
- No license, express or implied, by estoppels or otherwise, to any intellectual property is granted by this document or by any conduct of Eris. Product name and markings notes herein may be trademarks of their respective owners.
- Eris does not warrant or accept any liability whatsoever in respect of any products purchased through unauthorized sales channel.
- Should Customers purchase or use Eris products for any unintended or unauthorized application, Customers shall indemnify and hold Eris and its representatives harmless against all claims, damages, expenses, and attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized application.
- The official text is written in English and the English version of this document is the only version endorsed by Eris. Any discrepancies or differences created in the translations are not binding and have no legal effect on Eris for compliance or enforcement purposes.