EN25QH256A (2RC)
256 Megabit 3V Serial Flash Memory with 4Kbyte Uniform Sector

FEATURES

- Single power supply operation
  - Full voltage range: 2.7-3.6 volt
- Serial Interface Architecture
  - SPI Compatible: Mode 0 and Mode 3
- 256 M-bit Serial Flash
  - 256 M-bit / 32,768 KByte / 131,072 pages
  - 256 bytes per programmable page
- Standard, Dual or Quad SPI
  - Standard SPI: CLK, CS#, DI, DO, WP#, HOLD#
  - Dual SPI: CLK, CS#, DQ_0, DQ_1, WP#, HOLD#
  - Quad SPI: CLK, CS#, DQ_0, DQ_1, DQ_2, DQ_3
  - Configurable dummy cycle number
- High performance
  - 104MHz clock rate for Standard SPI
  - 104MHz clock rate for two data bits
  - 104MHz clock rate for four data bits
- Low power consumption
  - 6 mA typical active current
  - 1 μA typical power down current
- Uniform Sector Architecture:
  - 8,192 sectors of 4-Kbyte
  - 1,024 blocks of 32-Kbyte
  - 512 blocks of 64-Kbyte
  - Any sector or block can be erased individually
- Software and Hardware Write Protection:
  - Write Protect all or portion of memory via software
  - Enable/Disable protection with WP# pin
- High performance program/erase speed
  - Page program time: 0.5ms typical
  - Sector erase time: 40ms typical
  - Half Block erase time 120ms typical
  - Block erase time 150ms typical
  - Chip erase time: 100 seconds typical
- 3byte address and 4byte address switch
- Volatile Status Register Bits
- Lockable 3x512 byte OTP security sector
- Support Serial Flash Discoverable Parameters (SFDP) signature
- Read Unique ID Number
- Minimum 100K endurance cycle
- Data retention time 20 years
- Package Options
  - 8 contact VDFN / WSON 8x6 mm
  - 16 pins SOP 300mil body width
  - All Pb-free packages are compliant RoHS, Halogen-Free and REACH.
- Industrial temperature Range

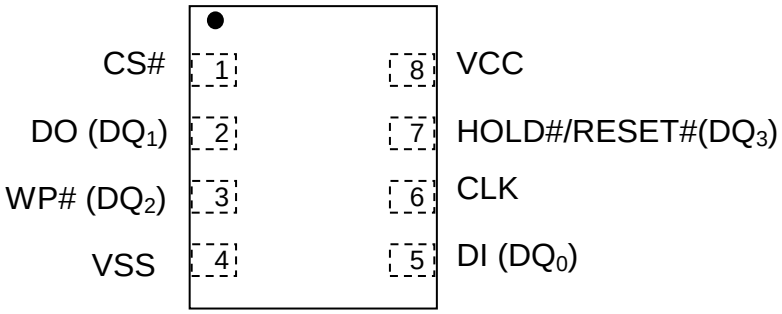
GENERAL DESCRIPTION

The device is a 256 Megabit (32,768K-byte) Serial Flash memory, with advanced write protection mechanisms. The device supports the single bit and four bits serial input and output commands via standard Serial Peripheral Interface (SPI) pins: Serial Clock, Chip Select, Serial DQ0 (DI) and DQ1(DO), DQ2(WP#) and DQ3(HOLD#/RESET#). The memory can be programmed 1 to 256 bytes at a time, using the Page Program instruction.

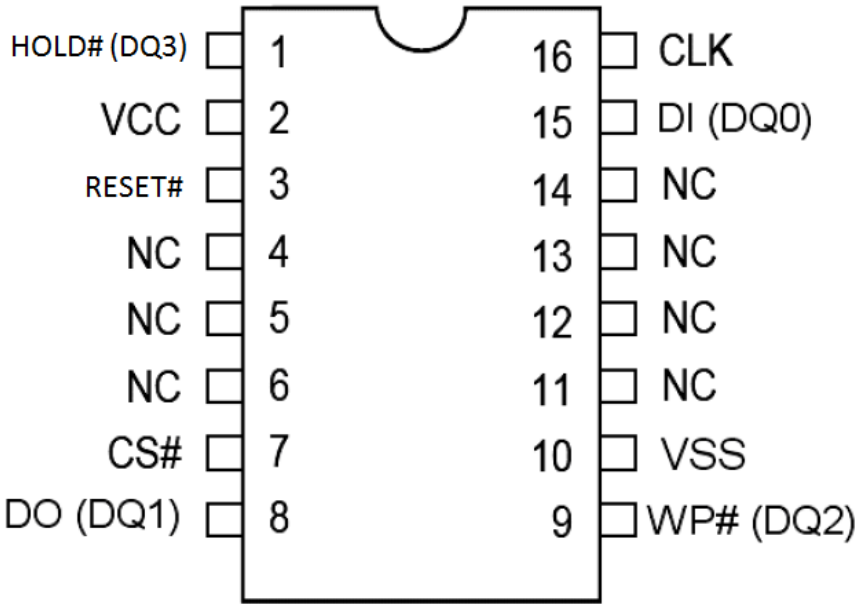
By providing the ability to protect and unprotect blocks, a system can unprotect blocks to modify their content while keeping the remaining blocks of the memory array securely protected. This is useful in applications where program code is patched or updated on a subroutine or module basis or in applications where data storage segments need to be modified without running the risk of errant modifications to the program code segments.

The device is designed to allow either single Sector/Block at a time or full chip erase operation. The device can be configured to protect part of the memory as the software protected mode. The device scans sustain a minimum of 100K program/erase cycles on each sector or block.

Figure.1 CONNECTION DIAGRAMS (TOP VIEW)



8 – LEAD VDFN / WSON



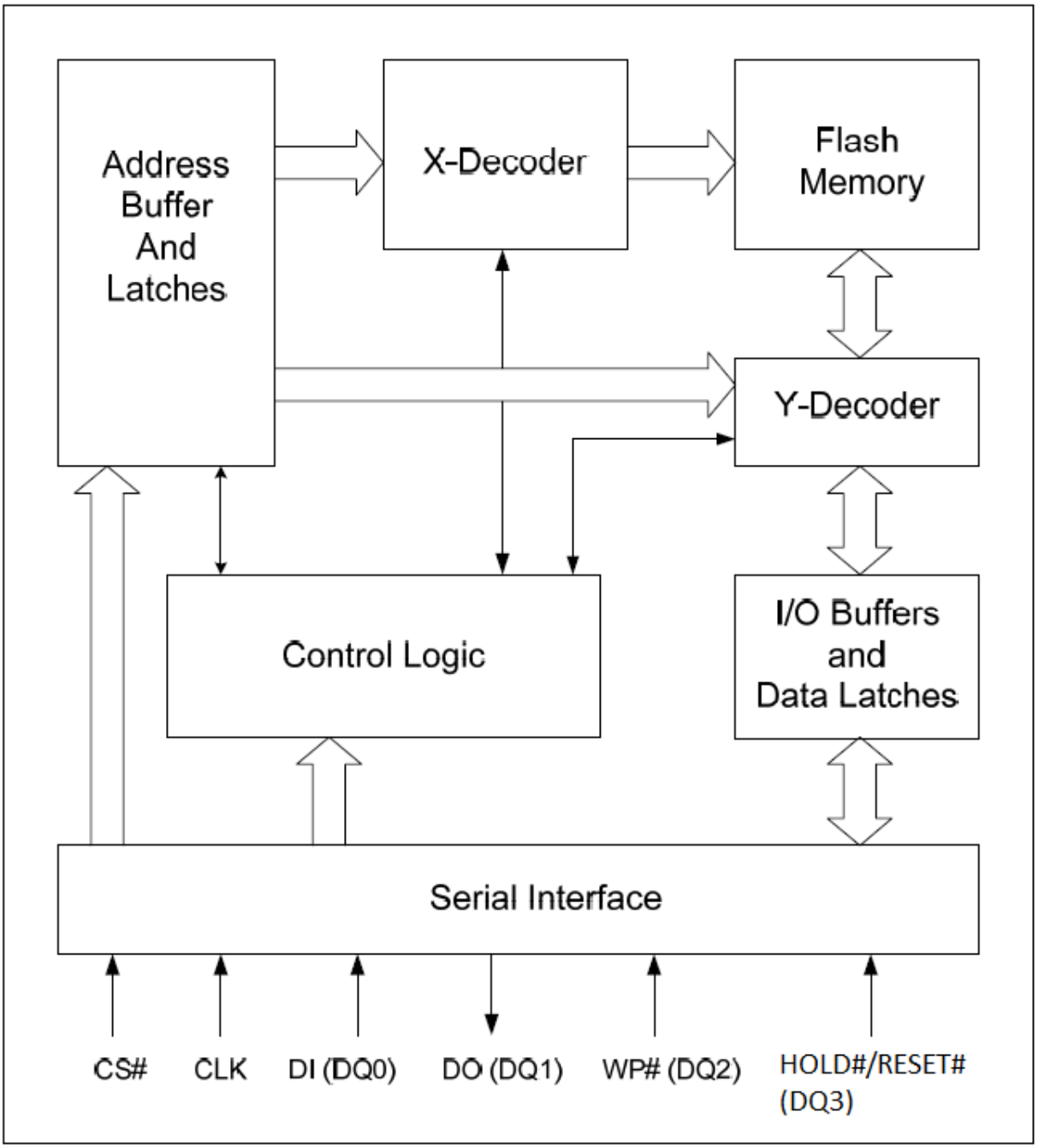
16 – LEAD SOP

Table 1. Pin Names

Symbol	Pin Name
CLK	Serial Clock Input
DI (DQ_0)	Serial Data Input (Data Input Output 0) *1
DO (DQ_1)	Serial Data Output (Data Input Output 1) *1
CS#	Chip Enable
WP# (DQ_2)	Write Protect (Data Input Output 2) *2
HOLD# /RESET#(DQ_3)	HOLD#/RESET# pin (Data Input Output 3) *2
HOLD#(DQ3)	HOLD# pin (Data Input Output 3) *2 (only SOP16)
RESET#	RESET# pin (only SOP16)
V_{CC}	Supply Voltage (2.7-3.6 V)
V_{SS}	Ground
NC	No Connect

Note:
1. DQ_0 and DQ_1 are used for Dual and Quad instructions.
2. DQ_0 ~ DQ_3 are used for Quad instructions.
   VDFN/ WSON package, WP# & HOLD#/RESET# functions are only available for Standard/Dual SPI.
   HOLD# and RESET# function is selected by HDDIS and RSEN bits.
3. For SOP16 package, RESET# is selected by RSEN.

Figure 2. BLOCK DIAGRAM



Note:

1. DQ_0 and DQ_1 are used for Dual instructions.
2. DQ_0 ~ DQ_3 are used for Quad instructions.
3. For the SOP16 package, HOLD# (DQ3) and RESET# are independent.

SIGNAL DESCRIPTION

Serial Data Input, Output and IOs (DI, DO and DQ_0, DQ_1, DQ_2, DQ_3)

The device support standard SPI, Dual SPI and Quad SPI operation. Standard SPI instructions use the unidirectional DI (input) pin to serially write instructions, addresses or data to the device on the rising edge of the Serial Clock (CLK) input pin. Standard SPI also uses the unidirectional DO (output) to read data or status from the device on the falling edge CLK.

Dual and Quad SPI instruction use the bidirectional IO pins to serially write instruction, addresses or data to the device on the rising edge of CLK and read data or status from the device on the falling edge of CLK.

Serial Clock (CLK)

The SPI Serial Clock Input (CLK) pin provides the timing for serial input and output operations. ("See SPI Mode")

Chip Select (CS#)

The SPI Chip Select (CS#) pin enables and disables device operation. When CS# is high the device is deselected and the Serial Data Output (DO, or DQ_0, DQ_1, DQ_2 and DQ_3) pins are at high impedance. When deselected, the device s power consumption will be at standby levels unless an internal erase, program or status register cycle is in progress. When CS# is brought low the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, CS# must transition from high to low before a new instruction will be accepted.

Write Protect (WP#)

The Write Protect (WP#) pin can be used to prevent the Status Register from being written. Used in conjunction with the Status Register's Block Protect (CMP, TB, BP2, BP1 and BP0) bits and Status Register Protect (SRP) bits, a portion or the entire memory array can be hardware protected. The WP# function is only available for standard SPI and Dual SPI operation, when during Quad SPI, this pin is the Serial Data IO (DQ_2) for Quad I/O operation.

HOLD (HOLD#)

The factory default of HOLD# disable bit (HDDIS) is 1 and Hold# could be enabled by setting the register bit to 0.The HOLD# pin allows the device to be paused while it is actively selected. When HOLD# is brought low, while CS# is low, the DO pin will be at high impedance and signals on the DI and CLK pins will be ignored (don't care). The hold function can be useful when multiple devices are sharing the same SPI signals. The HOLD# function is only available for standard SPI and Dual SPI operation, when during Quad SPI, this pin is the Serial Data IO (DQ3) for Quad I/O operation

For this device, there is HOLD# pin while shipping out from factory. User can enable it setting SR4.1 bit(HDDIS) in status register4.

RESET (RESET#)

The RESET# pin allows the device to be reset while it is actively selected. When RSEN bit is "0" (factory default), the RESET# pin is disabled. For VDFN8/ WSON8 package, the Hardware Reset function is only available for standard SPI and Dual SPI operation, when during Quad SPI, this pin is the Serial Data IO (DQ3) for Quad I/O operation or Quad Output operation. For SOP16 package, the RESET# pin is a dedicated hardware reset pin regardless of device settings or operation states. If the hardware reset function is not used, this pin can be left floating or connected to V_{CC} in the system.

Set RESET# to low for a minimum period 1us(tHRST) will interrupt any on-going instructions to have the device to initial state. The device can accept new instructions again in 28us(tHRSL) after RESET# back to high.

MEMORY ORGANIZATION

The memory is organized as:

- 33,554,432 bytes
- Uniform Sector Architecture
  512 blocks of 64-Kbyte
  1,024 sectors of 32-Kbyte
  8,192 sectors of 4-Kbyte
  131,072 pages (256 bytes each)

Each page can be individually programmed (bits are programmed from 1 to 0). The device is Sector, Block or Chip Erasable but not Page Erasable.

Table 2. Uniform Block Sector Architecture

64KB Block	32KB Block	Sector	Address range		64KB Block	32KB Block	Sector	Address range	
511	1023	8191	1FFF000h	1FFFFFFh	255	511	4095	0FFF000h	0FFFFFFh
	⋮	⋮	⋮	⋮		⋮	⋮	⋮	⋮
	1022	8176	1FF0000h	1FF0FFFh		510	4080	0FF0000h	0FF0FFFh
510	1021	8175	1FEF000h	1FEFFFFh	254	509	4079	0FEF000h	0FEFFFFh
	⋮	⋮	⋮	⋮		⋮	⋮	⋮	⋮
	1020	8160	1FE0000h	1FE0FFFh		508	4064	0FE0000h	0FE0FFFh
509	1019	8159	1FDF000h	1FDFFFFh	253	507	4063	0FDF000h	0FDFFFFh
	⋮	⋮	⋮	⋮		⋮	⋮	⋮	⋮
	1018	8144	1FD0000h	1FD0FFFh		506	4048	0FD0000h	0FD0FFFh
508	1017	8143	1FCF000h	1FCFFFFh	252	505	4047	0FCF000h	0FCFFFFh
	⋮	⋮	⋮	⋮		⋮	⋮	⋮	⋮
	1016	8128	1FC0000h	1FC0FFFh		504	4032	0FC0000h	0FC0FFFh
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
259	519	4159	103F000h	103FFFFh	3	7	63	003F000h	003FFFFh
	⋮	⋮	⋮	⋮		⋮	⋮	⋮	⋮
	518	4144	1030000h	1030FFFh		6	48	0030000h	0030FFFh
258	517	4143	102F000h	102FFFFh	2	5	47	002F000h	002FFFFh
	⋮	⋮	⋮	⋮		⋮	⋮	⋮	⋮
	516	4128	1020000h	1020FFFh		4	32	0020000h	0020FFFh
257	515	4127	101F000h	101FFFFh	1	3	31	001F000h	001FFFFh
	⋮	⋮	⋮	⋮		⋮	⋮	⋮	⋮
	514	4112	1010000h	1010FFFh		2	16	0010000h	0010FFFh
256	513	4111	100F000h	100FFFFh	0	1	15	000F000h	000FFFFh
	⋮	⋮	⋮	⋮		⋮	⋮	⋮	⋮
	512	4096	1000000h	1000FFFh		0	0	0000000h	0000FFFh

OPERATING FEATURES

Standard SPI Modes

The device is accessed through an SPI compatible bus consisting of four signals: Serial Clock (CLK), Chip Select (CS#), Serial Data Input (DI) and Serial Data Output (DO). Both SPI bus operation Modes 0 (0, 0) and 3 (1, 1) are supported. The primary difference between Mode 0 and Mode 3, as shown in Figure 3, concerns the normal state of the CLK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0 the CLK signal is normally low. For Mode 3 the CLK signal is normally high. In either case data input on the DI pin is sampled on the rising edge of the CLK. Data output on the DO pin is clocked out on the falling edge of CLK.

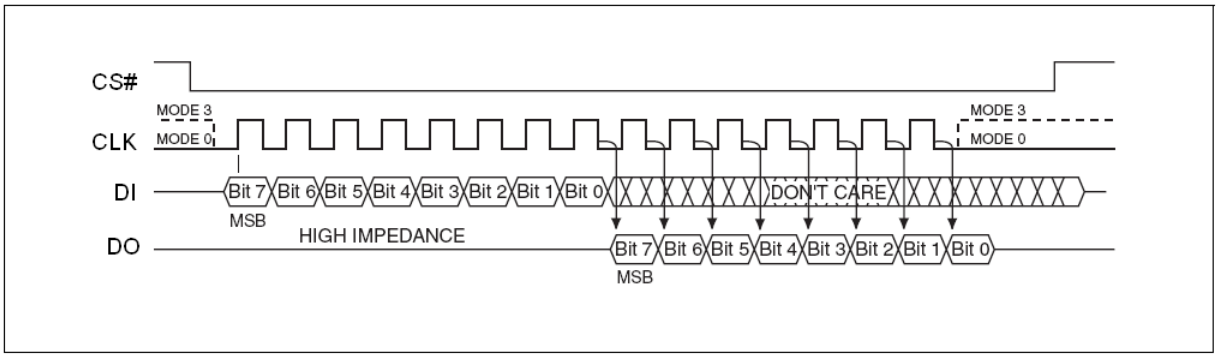


Figure 3. SPI Modes

Dual SPI Instruction

The device supports Dual SPI operation when using the “Dual Output Fast Read and Dual I/ O FAST_READ” (3Bh/3Ch and BBh/BCh) instructions. These instructions allow data to be transferred to or from the Serial Flash memory at two to three times the rate possible with the standard SPI. The Dual Read instructions are ideal for quickly downloading code from Flash to RAM upon power-up (code-shadowing) or for application that cache code-segments to RAM for execution. The Dual output feature simply allows the SPI input pin to also serve as an output during this instruction. When using Dual SPI instructions the DI and DO pins become bidirectional I/O pins; DQ_0 and DQ_1. All other operations use the standard SPI interface with single output signal.

Quad I/O SPI Instruction or Quad Output SPI Instruction

The device supports Quad output operation when using the Quad I/O Fast Read (EBh/ECh) or Quad Output Fast Read(6Bh/6Ch).This instruction allows data to be transferred to or from the Serial Flash memory at four to six times the rate possible with the standard SPI. The Quad Read instruction offer a significant improvement in continuous and random access transfer rates allowing fast code-shadowing to RAM or for application that cache code-segments to RAM for execution.

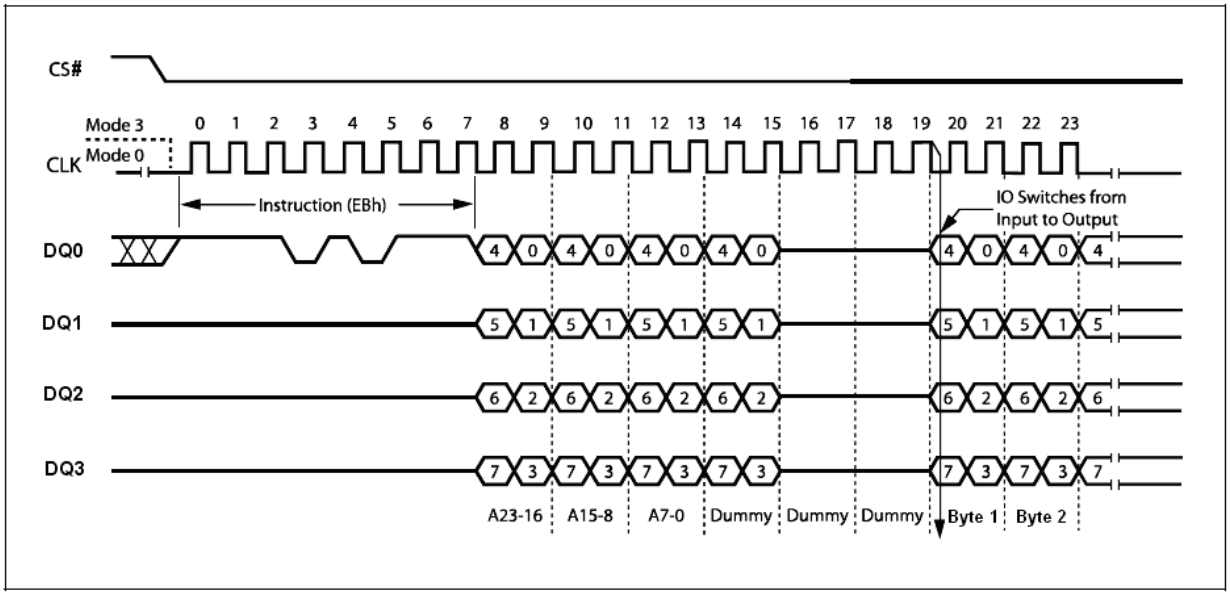


Figure 4. Quad I/O SPI Modes

Note: Please note the above address cycles are base on 3-byte address mode, for 4-byte address mode, the address cycles will be increased.

Full Quad SPI Modes (QPI)

The device also supports Full Quad SPI Mode (QPI) function while using the Enable Quad Peripheral Interface mode (EQPI) (38h). When using Quad SPI instruction the DI and DO pins become bidirectional I/O pins; DQ0 and DQ1, and the WP# and HOLD#/RESET# pins become DQ2 and DQ3 respectively.

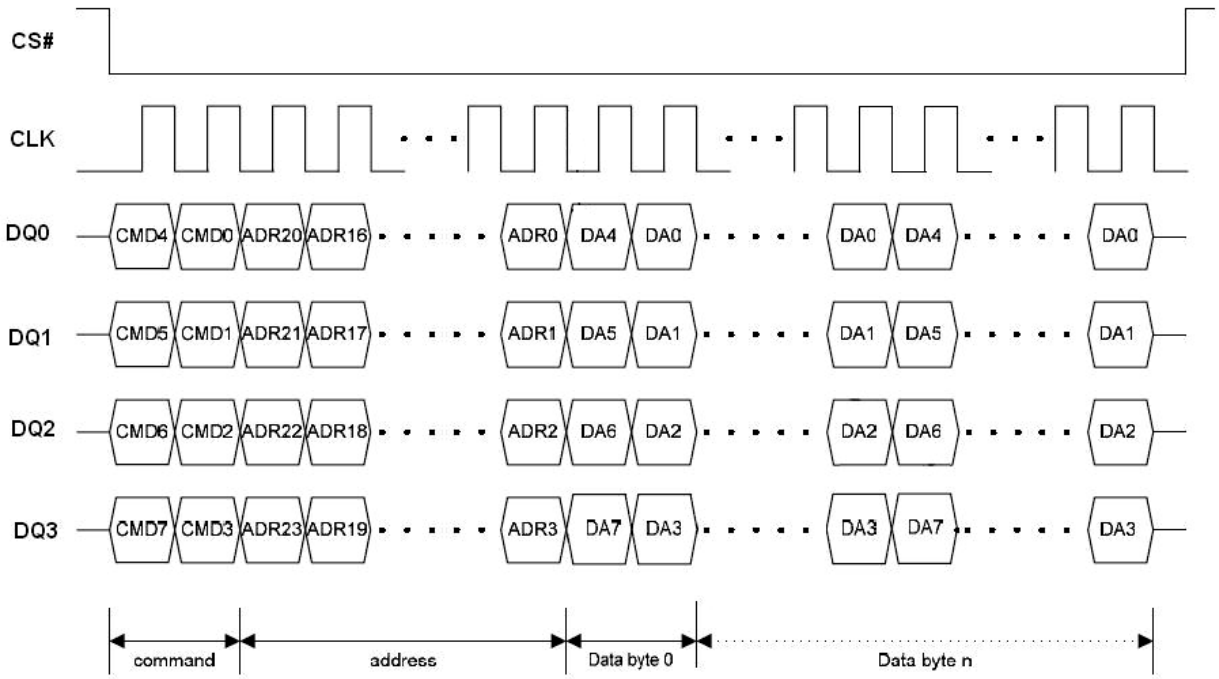


Figure 5. Full Quad SPI Modes

Note: Please note the above address cycles are base on 3-byte address mode, for 4-byte address mode, the address cycles will be increased.

Page Programming

To program one data byte, two instructions are required: Write Enable (WREN), which is one byte, and a Page Program (PP) or Quad Input Page Program (QPP) sequence, which consists of four bytes plus data. This is followed by the internal Program cycle (of duration t_{PP}).
To spread this overhead, the Page Program (PP) or Quad Input Page Program (QPP) instruction allows up to 256 bytes to be programmed at a time (changing bits from 1 to 0) provided that they lie in consecutive addresses on the same page of memory.

Sector Erase, Half Block Erase, Block Erase and Chip Erase

The Page Program (PP) or Quad Input Page Program (QPP) instruction allows bits to be reset from 1 to 0. Before this can be applied, the bytes of memory need to have been erased to all 1s (FFh). This can be achieved a sector at a time, using the Sector Erase (SE) instruction, half a block at a time using the Half Block Erase (HBE) instruction, a block at a time using the Block Erase (BE) instruction or throughout the entire memory, using the Chip Erase (CE) instruction. This starts an internal Erase cycle (of duration t_{SE}, t_{HBE}, t_{BE} or t_{CE}). The Erase instruction must be preceded by a Write Enable (WREN) instruction.

Polling During a Write, Program or Erase Cycle

A further improvement in the time to Write Status Register (WRSR, WRSR3, WRSR4), Program (PP, QPP) or Erase (SE, HBE, BE or CE) can be achieved by not waiting for the worst case delay (t_W, t_{PP}, t_{SE}, t_{HBE}, t_{BE} or t_{CE}). The Write In Progress (WIP) bit is provided in the Status Register so that the application program can monitor its value, polling it to establish when the previous Write cycle, Program cycle or Erase cycle is complete.

Active Power, Stand-by Power and Deep Power-Down Modes

When Chip Select (CS#) is Low, the device is enabled, and in the Active Power mode. When Chip Select (CS#) is High, the device is disabled, but could remain in the Active Power mode until all internal cycles have completed (Program, Erase, Write Status Register). The device then goes into the Stand-by Power mode. The device consumption drops to I_{CC1}.
The Deep Power-down mode is entered when the specific instruction (the Enter Deep Power-down Mode (DP) instruction) is executed. The device consumption drops further to I_{CC2}. The device remains in this mode until another specific instruction (the Release from Deep Power-down Mode and Read Device ID (RDI) instruction) is executed.
All other instructions are ignored while the device is in the Deep Power-down mode. This can be used as an extra software protection mechanism, when the device is not in active use, to protect the device from inadvertent Write, Program or Erase instructions.

Write Protection

Applications that use non-volatile memory must take into consideration the possibility of noise and other adverse system conditions that may compromise data integrity. To address this concern, the DEVICE provides the following data protection mechanisms:

- Power-On Reset and an internal timer (t_{PUW}) can provide protection against inadvertent changes while the power supply is outside the operating specification.
- Program, Erase and Write Status Register instructions are checked that they consist of a number of clock pulses that is a multiple of eight, before they are accepted for execution.
- All instructions that modify data must be preceded by a Write Enable (WREN) instruction to set the Write Enable Latch (WEL) bit. This bit is returned to its reset state by the following events:
  - Power-up
  - Write Disable (WRDI) instruction completion or Write Status Register (WRSR) instruction completion or Write Status Register 3/4 (WRSR3/WRSR4) instruction completion or Page Program (PP) or Quad Input Page Program (QPP) instruction completion or Sector Erase (SE) instruction completion or Half Block Erase (HBE) / Block Erase (BE) instruction completion or Chip Erase (CE) instruction completion
- The Block Protect (CMP, TB, BP3, BP2, BP1, BP0) bits allow part of the memory to be configured as read-only. This is the Software Protected Mode (SPM).
- The Write Protect (WP#) signal allows CMP, TB, BP3, BP2, BP1, BP0 bits and Status Register Protect (SRP) bit to be protected. This is the Hardware Protected Mode (HPM).
- In addition to the low power consumption feature, the Deep Power-down mode offers extra software protection from inadvertent Write, Program and Erase instructions, as all instructions are ignored except one particular instruction (the Release from Deep Power-down instruction).

Table 3. Protected Area Sizes Sector Organization

Status Register Content [1]						Memory Content [2]			
CMP	TB	BP3	BP2	BP1	BP0	Protect Areas	Addresses	Density	Portion
0	X	0	0	0	0	None	None	None	None
0	0	0	0	0	1	Block 511	1FF0000h-1FFFFFFh	64KB	Upper 1/512
0	0	0	0	1	0	Block 510 to 511	1FE0000h-1FFFFFFh	128KB	Upper 1/256
0	0	0	0	1	1	Block 508 to 511	1FC0000h-1FFFFFFh	256KB	Upper 1/128
0	0	0	1	0	0	Block 504 to 511	1F80000h-1FFFFFFh	512KB	Upper 1/64
0	0	0	1	0	1	Block 496 to 511	1F00000h-1FFFFFFh	1MB	Upper 1/32
0	0	0	1	1	0	Block 480 to 511	1E00000h-1FFFFFFh	2MB	Upper 1/16
0	0	0	1	1	1	Block 448 to 511	1C00000h-1FFFFFFh	4MB	Upper 1/8
0	0	1	0	0	0	Block 384 to 511	1800000h-1FFFFFFH	8MB	Upper 1/4
0	0	1	0	0	1	Block 256 to 511	1000000h-1FFFFFFh	16MB	Upper 1/2
0	1	0	0	0	1	Block 0	0000000h-000FFFFh	64KB	Lower 1/512
0	1	0	0	1	0	Block 0 to 1	0000000h-001FFFFh	128KB	Lower 1/256
0	1	0	0	1	1	Block 0 to 3	0000000h-003FFFFh	256KB	Lower 1/128
0	1	0	1	0	0	Block 0 to 7	0000000h-007FFFFh	512KB	Lower 1/64
0	1	0	1	0	1	Block 0 to 15	0000000h-007FFFFh	1MB	Lower 1/32
0	1	0	1	1	0	Block 0 to 31	0000000h-01FFFFFh	2MB	Lower 1/16
0	1	0	1	1	1	Block 0 to 63	0000000h-03FFFFFh	4MB	Lower 1/8
0	1	1	0	0	0	Block 0 to 127	0000000h-07FFFFFh	8MB	Lower 1/4
0	1	1	0	0	1	Block 0 to 255	0000000h-0FFFFFFh	16MB	Lower 1/2
0	x	1	1	0	x	Block 0 to 511	0000000h-1FFFFFFh	32MB	All
0	x	1	x	1	x	Block 0 to 511	0000000h-1FFFFFFh	32MB	All
1	X	0	0	0	0	Block 0 to 511	0000000h-1FFFFFFh	All	All
1	0	0	0	0	1	Block 0 to 510	0000000h-1FEFFFFh	32,704 KB	Lower 511/512
1	0	0	0	1	0	Block 0 to 509	0000000h-1FDFFFFh	32,640 KB	Lower 255/256
1	0	0	0	1	1	Block 0 to 507	0000000h-1FBFFFFh	32,512 KB	Lower 127/128
1	0	0	1	0	0	Block 0 to 503	0000000h-1F7FFFFh	32,256 KB	Lower 63/64
1	0	0	1	0	1	Block 0 to 495	0000000h-1EFFFFFh	31MB	Lower 31/32
1	0	0	1	1	0	Block 0 to 479	0000000h-1DFFFFFh	30MB	Lower 15/16
1	0	0	1	1	1	Block 0 to 447	0000000h-1BFFFFFh	28MB	Lower 7/8
1	0	1	0	0	0	Block 0 to 383	0000000h-17FFFFFh	24MB	Lower 3/4
1	0	1	0	0	1	Block 0 to 255	0000000h-0FFFFFFh	16MB	Lower 1/2
1	1	0	0	0	1	Block 1 to 511	0010000h-1FFFFFFh	32,704 KB	Upper 511/512
1	1	0	0	1	0	Block 2 to 511	0020000h-1FFFFFFh	32,640 KB	Upper 255/256
1	1	0	0	1	1	Block 4 to 511	0040000h-1FFFFFFh	32,512 KB	Upper 127/128
1	1	0	1	0	0	Block 8 to 511	0080000h-1FFFFFFh	32,256 KB	Upper 63/64
1	1	0	1	0	1	Block 16 to 511	0100000h-1FFFFFFh	31MB	Upper 31/32
1	1	0	1	1	0	Block 32 to 511	0200000h-1FFFFFFh	30MB	Upper 15/16
1	1	0	1	1	1	Block 64 to 511	0400000h-1FFFFFFh	28MB	Upper 7/8
1	1	1	0	0	0	Block 128 to 511	0800000h-1FFFFFFh	24MB	Upper 3/4
1	1	1	0	0	1	Block 256 to 511	1000000h-1FFFFFFh	16MB	Upper 1/2

1	x	1	1	0	x	None	None	None	None
1	x	1	x	1	x	None	None	None	None

Notes:
1. X = don't care
2. If any Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored.

INSTRUCTIONS

All instructions, addresses and data are shifted in and out of the device, most significant bit first. Serial Data Input (DI) is sampled on the first rising edge of Serial Clock (CLK) after Chip Select (CS#) is driven Low. Then, the one-byte instruction code must be shifted in to the device, most significant bit first, on Serial Data Input (DI), each bit being latched on the rising edges of Serial Clock (CLK).

The instruction set is listed in Table 4. Every instruction sequence starts with a one-byte instruction code. Depending on the instruction, it might be followed by address bytes, or data bytes, or both or none. Chip Select (CS#) must be driven High after the last bit of the instruction sequence has been shifted in. In the case of a Read Data Bytes (READ), Read Data Bytes at Higher Speed (Fast_Read), Dual Output Fast Read, Dual I/O Fast Read, Quad Output Fast Read, Quad Input/Output FAST_READ, Read Status Register (RDSR), Read Status Register 2 (RDSR2), Read Status Register 3 (RDSR3), Read Status Register 4 (RDSR4), Read Extended Register or Release from Deep Power-down, and Read Device ID (RDI) instruction, the shifted-in instruction sequence is followed by a data-out sequence. Chip Select (CS#) can be driven High after any bit of the data-out sequence is being shifted out.

In the case of a write instruction, Chip Select (CS#) must be driven High exactly at a byte boundary, otherwise the instruction is rejected, and is not executed. That is, Chip Select (CS#) must driven High when the number of clock pulses after Chip Select (CS#) being driven Low is an exact multiple of eight. For Page Program, if at any time the input byte is not a full byte, nothing will happen and WEL will not be reset.

In the case of multi-byte commands of Page Program (PP), Quad Input Page Program (QPP) and Release from Deep Power Down (RES) minimum number of bytes specified has to be given, without which, the command will be ignored.

In the case of Page Program, if the number of byte after the command is less than 4 (at least 1 data byte), it will be ignored too. In the case of SE and HBL/BE, exact 24-bit(or 32-bit, depends on mode state) address is a must, any less or more will cause the command to be ignored.

All attempts to access the memory array during a Write Status Register cycle, Program cycle or Erase cycle are ignored, and the internal Write Status Register cycle, Program cycle or Erase cycle continues unaffected.

Table 4A. Instruction Set

Instruction Name	Byte 1 Code	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	n-Bytes
RSTEN	66h						
RST(1)	99h						
EQPI	38h						
RSTQIO(2)	FFh						
Write Enable (WREN)	06h						
Volatile Status Register Write Enable (3)	50h						
Write Disable (WRDI)/ Exit OTP mode	04h						
Read Status Register (RDSR)	05h	(S7-S0)(4)					continuous(5)
Read Status Register 2 (RDSR2)	09h	(S7-S0)(4)					continuous(5)
Read Status Register 3 (RDSR3)	95h	(S7-S0)(4)					
Read Status Register 4 (RDSR4)	85h	(S7-S0)(4)					
Write Status Register (WRSR)	01h	S7-S0					
Write Status Register 3 (WRSR3)	C0h	S7-S0					
Write Status Register 4 (WRSR4)	C1h	S7-S0					
Deep Power-down	B9h						
Release from Deep Power-down, and read Device ID (RES)	ABh	dummy	dummy	dummy	(ID7-ID0)		(6)
Release from Deep Power-down (RDP)							
Manufacturer/ Device ID	90h	dummy	dummy	00h	(M7-M0)	(ID7-ID0)	(7)
				01h	(ID7-ID0)	(M7-M0)	
Read Identification (RDID)	9Fh	(M7-M0)	(ID15-ID8)	(ID7-ID0)	(8)		
Enter OTP mode	3Ah						
Read SFDP mode and Unique ID Number	5Ah	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(Next Byte) Continuous
Read Extended address Mode	C8h	(S7-S0)(4)					
Write Extended address Register	C5h	S7-S0					
Enter 4byte address mode	B7h						
Exit 4byte address mode	E9h						

Notes:

1. RST command only executed if RSTEN command is executed first. Any intervening command will disable Reset.
2. Release Full Quad SPI or Fast Read Enhanced mode. Device accepts eight-clocks command in Standard SPI mode, or two-clocks command in Full Quad SPI mode.
3. Volatile Status Register Write Enable command must precede WRSR command without any intervening commands to write data to Volatile Status Register.
4. Data bytes are shifted with Most Significant Bit first. Byte fields with data in parenthesis “( )” indicate data being read from the device on the DO pin.
5. The Status Register contents will repeat continuously until CS# terminates the instruction.
6. The Device ID will repeat continuously until CS# terminates the instruction.
7. The Manufacturer ID and Device ID bytes will repeat continuously until CS# terminates the instruction. 00h on Byte 4 starts with MID and alternate with DID, 01h on Byte 4 starts with DID and alternate with MID.
8. (M7-M0): Manufacturer, (ID15-ID8): Memory Type, (ID7-ID0): Memory Capacity.

Table 4B. Instruction Set (Read Instruction)

Instruction Name	OP Code	Address bits	Dummy bits / Clocks (Default)	Data Out	Remark
Read Data (1)	03h	24/32 bits	0	(D7-D0, …)	(Next Byte) continuous
Fast Read (1)	0Bh	24/32 bits	8 bits / 8 clocks	(D7-D0, …)	(Next Byte) continuous
Dual Output Fast Read (1)	3Bh	24/32 bits	8 bits / 8 clocks	(D7-D0, …)	(one byte Per 4 clocks, continuous)
Dual I/O Fast Read (1)	BBh	24/32 bits	8 bits / 4 clocks	(D7-D0, …)	(one byte Per 4 clocks, continuous)
Quad Output Fast Read (1)	6Bh	24/32 bits	8 bits / 8 clocks	(D7-D0, …)	(one byte per 2 clocks, continuous)
Quad I/O Fast Read (1)	EBh	24/32 bits	24 bits / 6 clocks	(D7-D0, …)	(one byte per 2 clocks, continuous)
Read Data with 4 bytes address	13h	32 bits	0	(D7-D0, …)	(Next Byte) continuous
Fast Read with 4 bytes address	0Ch	32 bits	8 bits / 8 clocks	(D7-D0, …)	(Next Byte) continuous
Dual Output Fast Read with 4 bytes address	3Ch	32 bits	8 bits / 8 clocks	(D7-D0, …)	(one byte Per 4 clocks, continuous)
Dual I/O Fast Read with 4 bytes address	BCh	32 bits	8 bits / 4 clocks	(D7-D0, …)	(one byte Per 4 clocks, continuous)
Quad Output Fast Read with 4 bytes address	6Ch	32 bits	8 bits / 8 clocks	(D7-D0, …)	(one byte per 2 clocks, continuous)
Quad I/O Fast Read with 4 bytes address	ECh	32 bits	24 bits / 6 clocks	(D7-D0, …)	(one byte per 2 clocks, continuous)

Notes:
1. The address cycles default is 3-byte address mode. If using 4byte address, please issue enter 4byte address mode first.

Table 4C. Instruction Set (Program Instruction)

Instruction Name	OP Code	Address bits	Dummy bits / Clocks (Default)	Data Out	Remark
Page Program (PP) (1)	02h	24/32 bits	0	(D7-D0, …)	(Next Byte) continuous
Quad Input Page Program (QPP) (1)	32h	24/32 bits	0	(D7-D0, …)	(one byte per 2 clocks, continuous)
Page Program (PP) with 4 bytes address	12h	32 bits	0	(D7-D0, …)	(Next Byte) continuous
Quad Input Page Program (QPP) with 4 bytes address	34h	32 bits	0	(D7-D0, …)	(one byte per 2 clocks, continuous)

Notes:
1. The address cycles default is 3-byte address mode. If using 4byte address, please issue enter 4byte address mode first.

Table 4D. Instruction Set (Erase Instruction)

Instruction Name	OP Code	Address bits	Dummy bits / Clocks (Default)	Data Out	Remark
Sector Erase (SE) (1)	20h	24/32 bits	0	-	
32K Half Block Erase (HBE) (1)	52h	24/32 bits	0	-	
64K Block Erase (BE) (1)	D8h	24/32 bits	0	-	
Chip Erase (CE)	C7h/ 60h	0	0	-	
Sector Erase (SE) with 4 bytes address	21h	32 bits	0	-	
32K Half Block Erase (HBE) with 4 bytes address	5Ch	32 bits	0	-	
64K Block Erase (BE) with 4 bytes address	DCh	32 bits	0	-	

Notes:
1. The address cycles default is 3-byte address mode. If using 4byte address, please issue enter 4byte address mode first.

Table 4E. Instruction Set (Read Instruction support mode and dummy cycle setting)

Instruction Name	OP Code	Start From SPI/QPI (1)		Dummy Cycle (2)	
		SPI	QPI	Start From SPI	Start From QPI
Read Data (1) (3)	03h	Yes	No	N/A	N/A
Fast Read (1) (3)	0Bh	Yes	Yes	8 clocks	By SR3.4~3.5
Dual Output Fast Read (1) (3)	3Bh	Yes	No	8 clocks	N/A
Dual I/O Fast Read (1) (3)	BBh	Yes	No	4 clocks	N/A
Quad Output Fast Read (1) (3)	6Bh	Yes	No	8 clocks	N/A
Quad I/O Fast Read (1) (3)	EBh	Yes	Yes	By SR3.4~3.5	By SR3.4~3.5
Read Data with 4byte address	13h	Yes	No	N/A	N/A
Fast Read with 4byte address	0Ch	Yes	Yes	8 clocks	By SR3.4~3.5
Dual Output Fast Read with 4byte address	3Ch	Yes	No	8 clocks	N/A
Dual I/O Fast Read with 4byte address	BCh	Yes	No	4 clocks	N/A
Quad Output Fast Read with 4byte address	6Ch	Yes	No	8 clocks	N/A
Quad I/O Fast Read with 4byte address	ECh	Yes	Yes	By SR3.4~3.5	By SR3.4~3.5

Note:
1. 'Start From SPI/QPI' means if this command is initiated from SPI or QPI mode.
2. The dummy byte settings please refer to table 9.
3. The address cycles default is 3-byte address mode. If using 4byte address, please issue enter 4byte address mode first.

Table 5. Manufacturer and Device Identification

OP Code	(M7-M0)	(ID15-ID0)	(ID7-ID0)
ABh			18h
90h	1Ch		18h
9Fh	1Ch	7019h	

Reset-Enable (RSTEN) (66h) and Reset (RST) (99h)

The Reset operation is used as a system (software) reset that puts the device in normal operating Ready mode. This operation consists of two commands: Reset-Enable (RSTEN) and Reset (RST).

To reset the device the host drives CS# low, sends the Reset-Enable command (66h), and drives CS# high. Next, the host drives CS# low again, sends the Reset command (99h), and drives CS# high.
The Reset operation requires the Reset-Enable command followed by the Reset command. Any command other than the Reset command after the Reset-Enable command will disable the Reset-Enable.

A successful command execution will reset the status register, see Figure 6 for SPI Mode and Figure 6.1 for Quad Mode. A device reset during an active Program or Erase operation aborts the operation, which can cause the data of the targeted address range to be corrupted or lost. Depending on the prior operation, the reset timing may vary. Recovery from a Write operation requires more software latency time (t_{SR}) than recovery from other operations.

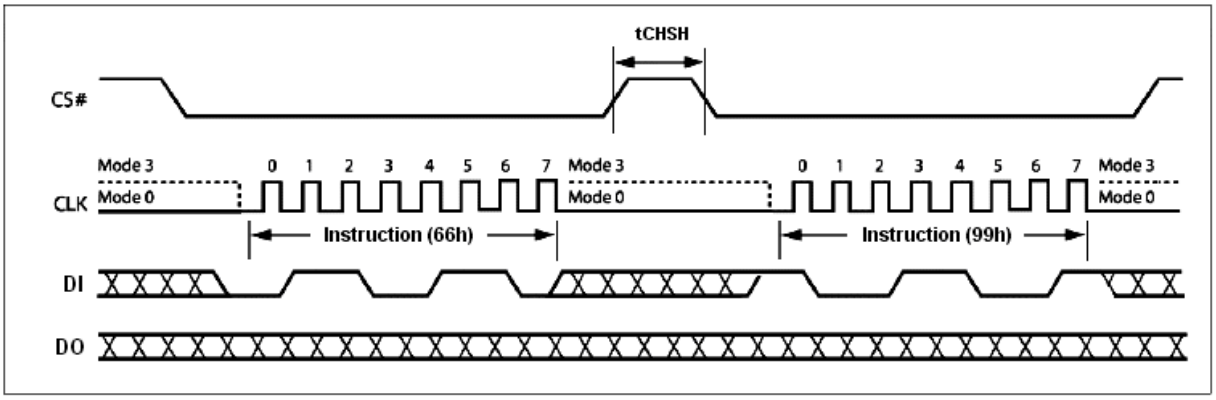


Figure 6. Reset-Enable and Reset Sequence Diagram

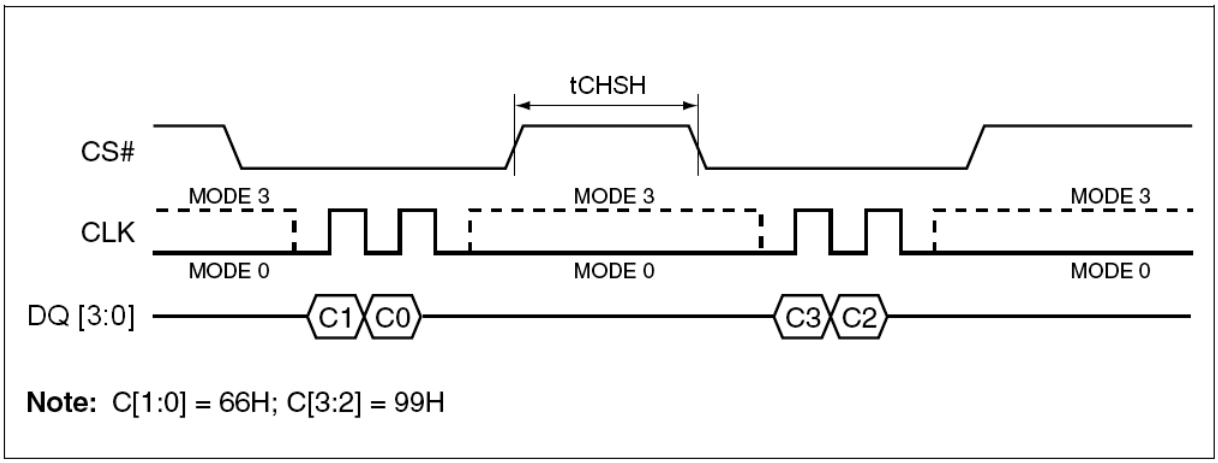
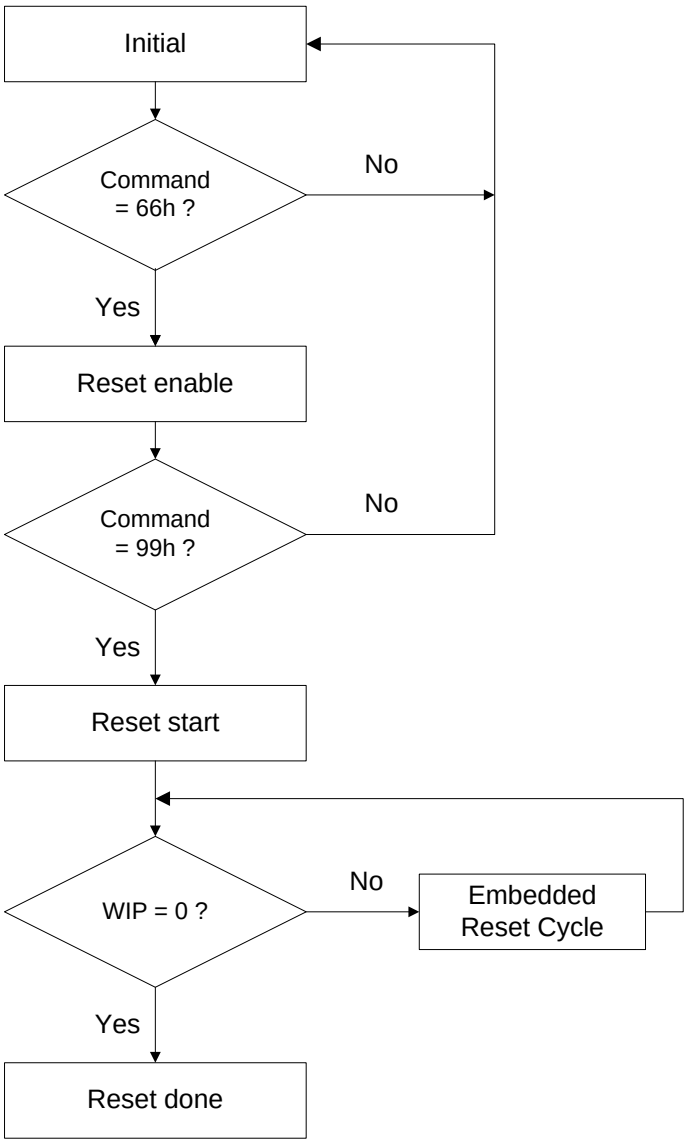


Figure 6.1 Reset-Enable and Reset Sequence Diagram under QPI Mode

Software Reset Flow



Note:

1. Reset-Enable (RSTEN) (66h) and Reset (RST) (99h) commands need to match standard SPI or QPI (quad) mode.
2. Continue (Enhance) EB mode need to use quad Reset-Enable (RSTEN) (66h) and quad Reset (RST) (99h) commands.
3. If user is not sure it is in SPI or Quad mode, we suggest to execute sequence as follows:

   Quad Reset-Enable (RSTEN) (66h) -> Quad Reset (RST) (99h) -> SPI Reset-Enable (RSTEN) (66h) -> SPI Reset (RST) (99h) to reset.
4. The reset command could be executed during embedded program and erase process, QPI mode, Continue EB mode to back to SPI mode.
5. This flow can not release the device from Deep power down mode.
6. The Status Register Bits and Status Register 2/3/4 Bits will reset to default value after reset done.
7. If user reset device during erase, the embedded reset cycle software reset latency will take about 28us in worst case.
8. User can't do software reset command while doing 4K/32K erase operation.

Enable Quad Peripheral Interface mode (EQPI) (38h)

The Enable Quad Peripheral Interface mode (EQPI) instruction will enable the flash device for Quad SPI bus operation. Upon completion of the instruction, all instructions thereafter will be 4-bit multiplexed input/output until a power cycle or “Reset Quad I/O instruction” instruction, as shown in Figure 7. The device did not support the Read Data Bytes (READ) (03h/13h)**,** Dual Output Fast Read (3Bh/3Ch), Dual Input/Output FAST_READ (BBh/BCh), Quad Output Fast Read (6Bh/6Ch) and Quad Input Page Program(32h/34h) modes while the Enable Quad Peripheral Interface mode (EQPI) (38h) turns on.

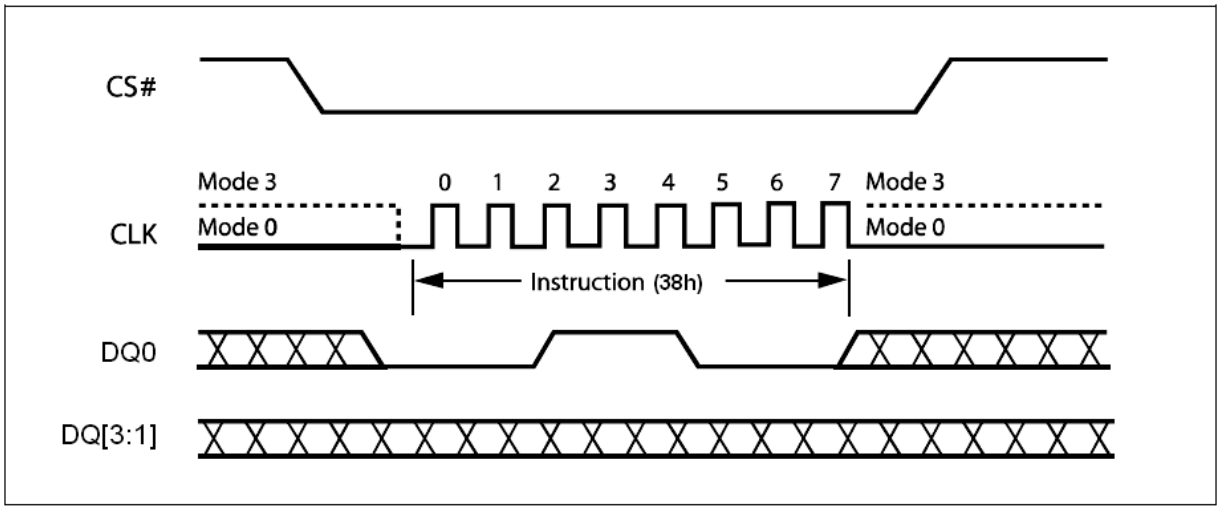


Figure 7. Enable Quad Peripheral Interface mode Sequence Diagram

Reset Quad I/O (RSTQIO) or Release Quad I/O Fast Read Enhancement Mode (FFh)

The Reset Quad I/O instruction resets the device to 1-bit Standard SPI operation. To execute a Reset Quad I/O operation, the host drives CS# low, sends the Reset Quad I/O command cycle (FFh) then, drives CS# high. This command can’t be used in Standard SPI mode.

User also can use the FFh command to release the Quad I/O Fast Read Enhancement Mode. The detail description, please see the Quad I/O Fast Read Enhancement Mode section.

Note:

If the system is in the Quad I/O Fast Read Enhance Mode in QPI Mode, it is necessary to execute FFh command by two times. The first FFh command is to release Quad I/O Fast Read Enhance Mode, and the second FFh command is to release EQPI Mode.

Write Enable (WREN) (06h)

The Write Enable (WREN) instruction (Figure 8) sets the Write Enable Latch (WEL) bit. The Write Enable Latch (WEL) bit must be set prior to every Page Program (PP), Quad Input Page Program (QPP), Sector Erase (SE), Block Erase (HBE/BE), Chip Erase (CE) and Write Status Register (WRSR/ WRSR3/WRSR4) instruction.
The Write Enable (WREN) instruction is entered by driving Chip Select (CS#) Low, sending the instruction code, and then driving Chip Select (CS#) High.

The instruction sequence is shown in Figure 10.1 while using the Enable Quad Peripheral Interface mode (EQPI) (38h) command.

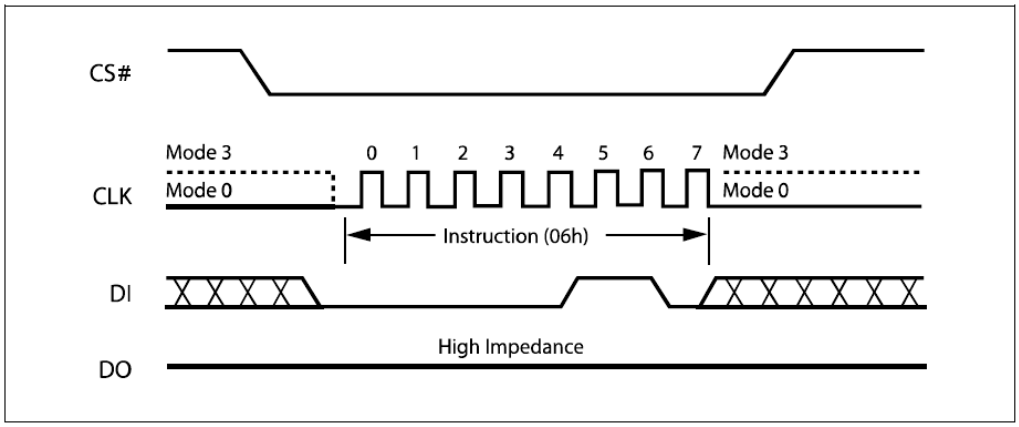


Figure 8. Write Enable Instruction Sequence Diagram

Volatile Status Register Write Enable (50h)

This feature enable user to change memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. The Volatile Status Register Write Enable (50h) command won't set the Write Enable Latch (WEL) bit, it is only valid for 'Write Status Register' (01h) command to change the Volatile Status Register bit values.
To write to Volatile Status Register, issue the Volatile Status Register Write Enable (50h) command prior issuing WRSR (01h). The Status Register bits will be refresh to Volatile Status Register (SR[7:2]) within t_{SHSL2} (50ns). Upon power off or the execution of a Software/Hardware Reset, the volatile Status Register bit values will be lost, and the non-volatile Status Register bit values will be restored. The instruction sequence is shown in Figure 9.

The instruction sequence is shown in Figure 10.1 while using the Enable Quad Peripheral Interface mode (EQPI) (38h) command.

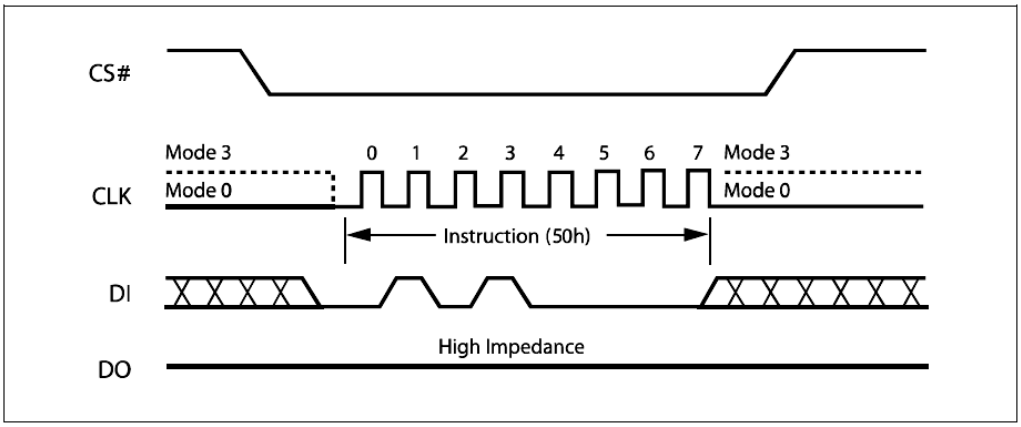


Figure 9. Volatile Status Register Write Enable Instruction Sequence Diagram

Write Disable (WRDI) (04h)

The Write Disable instruction (Figure 10) resets the Write Enable Latch (WEL) bit in the Status Register to a 0 or exit from OTP mode to normal mode. The Write Disable instruction is entered by driving Chip Select (CS#) low, shifting the instruction code “04h” into the DI pin and then driving Chip Select (CS#) high. Note that the WEL bit is automatically reset after Power-up and upon completion of the Write Status Register, Page Program, Sector Erase, Block Erase (HBE/BE) and Chip Erase instructions.

The instruction sequence is shown in Figure 10.1 while using the Enable Quad Peripheral Interface mode (EQPI) (38h) command.

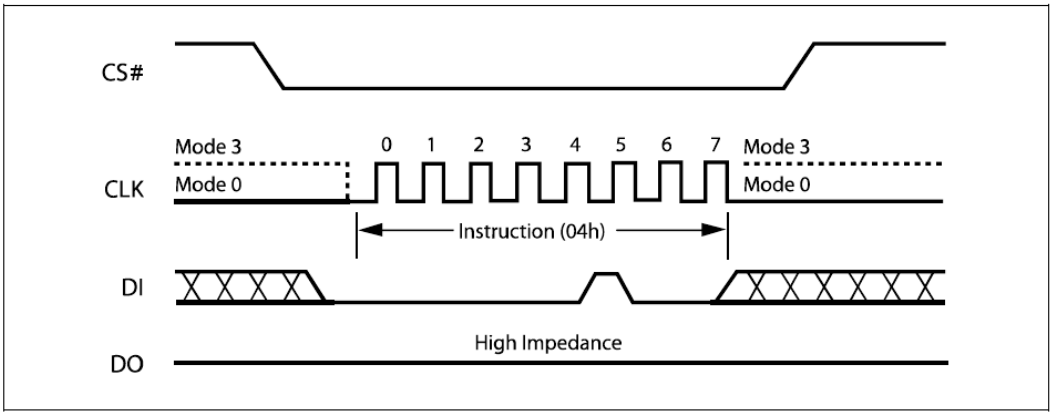


Figure 10. Write Disable Instruction Sequence Diagram

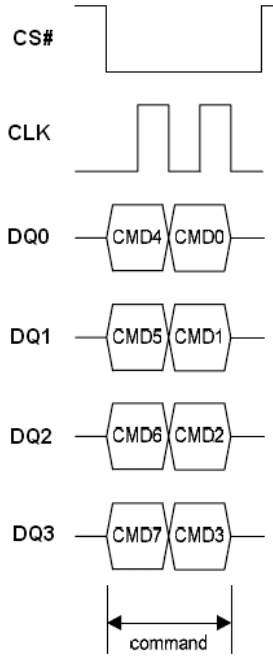


Figure 10.1 Write Enable/Disable Instruction Sequence under QPI Mode

Read Status Register (RDSR) (05h)

The Read Status Register (RDSR) instruction allows the Status Register to be read. The Status Register may be read at any time, even while a Program, Erase or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write In Progress (WIP) bit before sending a new instruction to the device. It is also possible to read the Status Register continuously, as shown in Figure 11.

The instruction sequence is shown in Figure 11.1 while using the Enable Quad Peripheral Interface mode (EQPI) (38h) command.

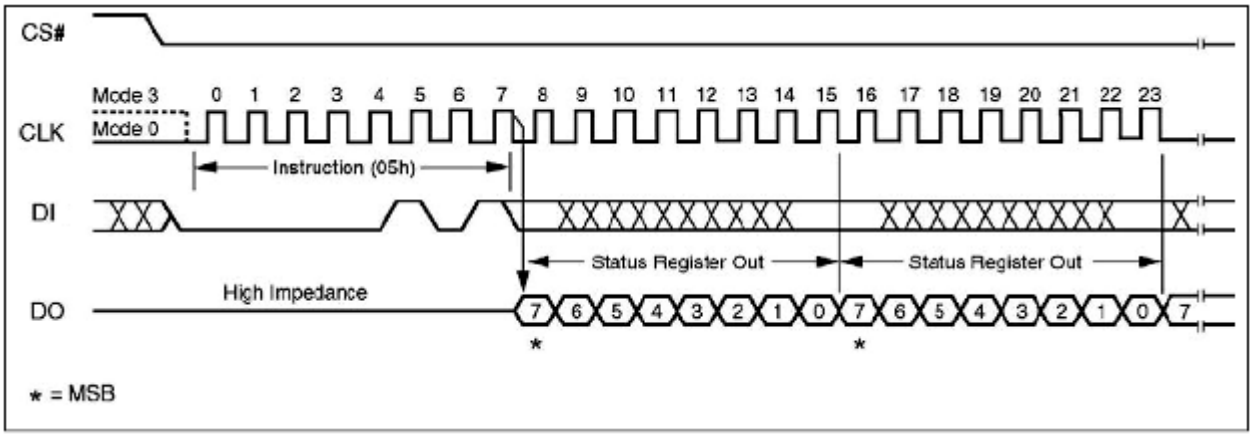


Figure 11. Read Status Register Instruction Sequence Diagram

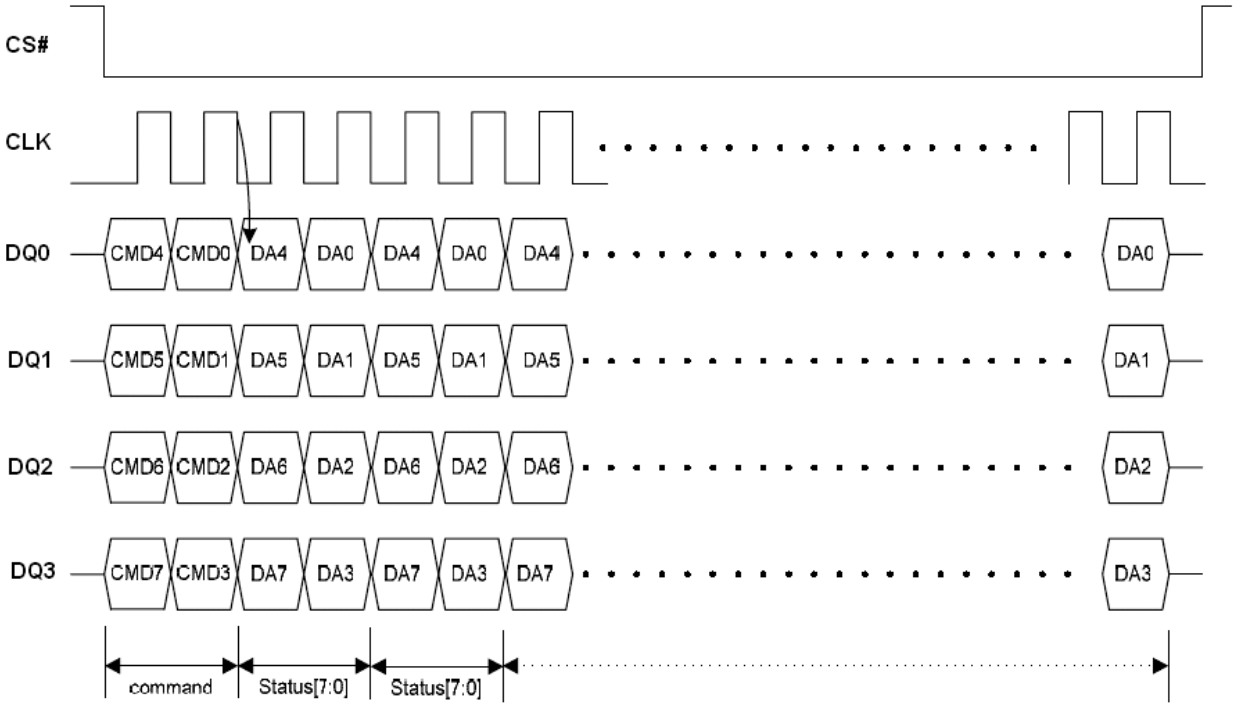


Figure 11.1 Read Status Register Instruction Sequence under QPI Mode

Table 6. Status Register Bit Locations

SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
SRP	**TB**	**BP3**	**BP2**	**BP1**	**BP0**	**WEL**	**WIP**
SPL0	Reversed	Reversed	Reversed	Reversed	**SPL1**	**SPL2**	**WIP**

Table 6.1 Status Register Bit Locations (In Normal mode)

SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
SRP (Status Register Protect)	**TB** (Top / Bottom Protect)	**BP3** (Block Protected)	**BP2** (Block Protected)	**BP1** (Block Protected)	**BP0** (Block Protected)	**WEL** (Write Enable Latch)	**WIP** (Write In Progress)
1 = status register write disable	1 = Bottom 0 = Top (default 0)	(note 2)	(note 2)	(note 2)	(note 2)	1 = write enable 0 = not write enable	1 = write operation 0 = not in write operation
Volatile bit / Non-volatile bit	Volatile bit / Non-volatile bit	Volatile bit / Non-volatile bit	Volatile bit / Non-volatile bit	Volatile bit / Non-volatile bit	Volatile bit / Non-volatile bit	Read only bit	Read only bit

Table 6.2 Status Register Bit Locations (In OTP mode)

SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
SPL0	Reversed bit	Reserved bit	Reserved bit	Reserved bit	**SPL1**	**SPL2**	**WIP** (Write In Progress bit)
1 = security sector 0 is protected					1 = security sector 1 is protected	1 = security sector 2 is protected	1 = write operation 0 = not in write operation
OTP bit					OTP bit	OTP bit	Read only bit

Note:
1. In OTP mode, SR7 bit is served as SPL0 bit; SR2 bit is served as SPL1 bit ; SR1 bit is served as SPL2 bit and SR0 bit is served as WIP bit.
2. See the table 3 “Protected Area Sizes Sector Organization”.

The status and control bits of the Status Register are as follows:

WIP bit. The Write In Progress (WIP) bit indicates whether the memory is busy with a Write Status Register, Program or Erase cycle. When set to 1, such a cycle is in progress, when reset to 0 no such cycle is in progress.

WEL bit. The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write Status Register, Program or Erase instruction is accepted.

BP3, BP2, BP1, BP0 bits. The Block Protect (BP3, BP2, BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase instructions. These bits are written with the Write Status Register (WRSR) instruction. When one or both of the Block Protect (BP3, BP2, BP1, BP0) bits is set to 1, the relevant memory area (as defined in Table 3.) becomes protected against Page Program (PP), Quad Input Page Program (QPP), Sector Erase (SE) and Block Erase (HBE/BE) instructions. The Block Protect (BP3, BP2, BP1, BP0) bits can be written and provided that the Hardware Protected mode has not been set. The Chip Erase (CE) instruction is executed if all memory regions aren’t protected by the Block Protect (CMP, TB, BP3, BP2, BP1, BP0) bits.

TB bit. The Top/Bottom Protect Bit (TB) controls if the Block Protect Bits (BP3, BP2, BP1, BP0) protect from the Top (TB = 0) or the Bottom (TB = 1) of the array as shown in the Protected Area Sizes Sector Organization table.

SRP bit. The Status Register Protect (SRP) bit is operated in conjunction with the Write Protect (WP#) signal. The Status Register Write Protect (SRP) bit and Write Protect (WP#) signal allow the device to be put in the Hardware Protected mode (when the Status Register Protect (SRP) bit is set to 1, and Write Protect (WP#) is driven Low). In this mode, the bits of the Status Register (TB, BP3, BP2, BP1, BP0 and CMP) become read-only bits and the Write Status Register (WRSR) instruction is no longer accepted for execution.

In OTP mode, SR7,SR2~SR0 bits are served as SPL0 bit, SPL1 bit, SPL2 bit and WIP bit.

SPL2 bit. The SPL2 bit is non-volatile One Time Program (OTP) bit in status register that provide the write protect control and status to the security sector 2. User can read/program/erase security sector 2 as normal sector while SPL2 value is equal 0, after SPL2 is programmed with 1 by WRSR command, the security sector 2 is protected from program and erase operation. The SPL2 bit can only be programmed once.

SPL1 bit. The SPL1 bit is non-volatile One Time Program (OTP) bit in status register that provide the write protect control and status to the security sector 1. User can read/program/erase security sector 1 as normal sector while SPL1 value is equal 0, after SPL1 is programmed with 1 by WRSR command, the security sector 1 is protected from program and erase operation. The SPL1 bit can only be programmed once.

SPL0 bit. The SPL0 bit is non-volatile One Time Program (OTP) bit in status register that provide the write protect control and status to the security sector 0. User can read/program/erase security sector 0 as normal sector while SPL0 value is equal 0, after SPL0 is programmed with 1 by WRSR command, the security sector 0 is protected from program and erase operation. The SPL0 bit can only be programmed once.

Reserved bits. Status Register bit locations SR3, SR4, SR5 and SR6 in OTP mode is reserved for future use.

Read Status Register 2 (RDSR2) (09h)

The Read Status Register 2 (RDSR2) instruction allows the Status Register 2 to be read. The Status Register 2 may be read at any time, even while a program/erase cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write In Progress (WIP) bit before sending a new instruction to the device. It is also possible to read the Status Register 2 continuously, as shown in Figure 12.

The instruction sequence is shown in Figure 12.1 while using the Enable Quad Peripheral Interface mode (EQPI) (38h) command.

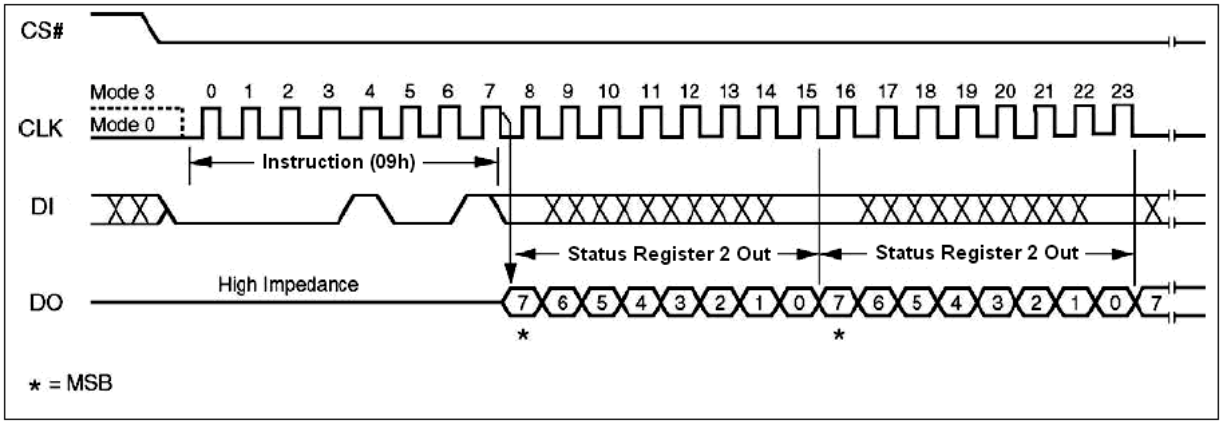


Figure 12. Read Status Register 2 Instruction Sequence Diagram

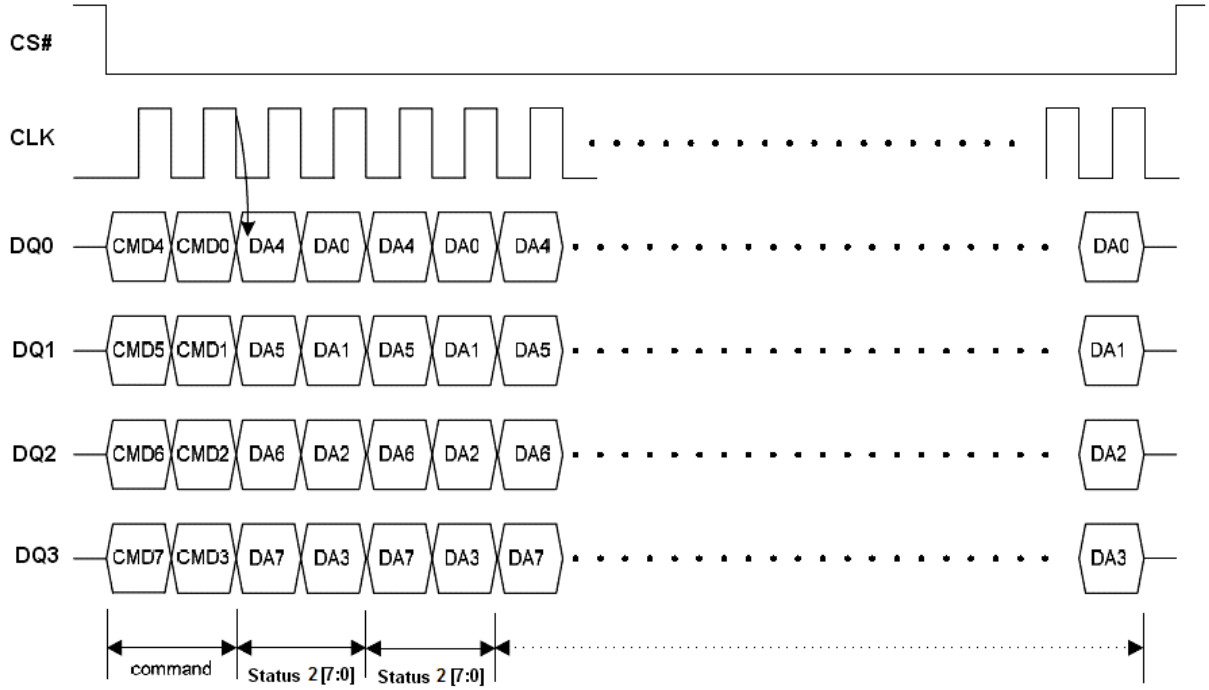


Figure 12.1 Read Status Register 2 Instruction Sequence under QPI Mode

Table 7. Status Register 2 Bit Locations

SR2.7	SR2.6	SR2.5	SR2.4	SR2.3	SR2.2	SR2.1	SR2.0
Reserved bit	Erase Fail Flag	Program Fail Flag	**4byte** (Byte of Address flag)	Reserved bit	Reserved bit	**WEL** (Write Enable Latch)	**WIP** (Write In Progress bit) (Note 1)
	1= indicate Erase failed 0=normal Erase succeed (default=0)	1= indicate Program failed 0=normal Program succeed (default=0)	1 = 4 byte address 0 = 3 byte address			1 = write enable 0 = not write enable	1 = write operation 0 = not in write operation
	volatile bit	volatile bit	volatile bit			Volatile bit	volatile bit
	Read Only	Read Only	Read Only			Read Only	Read Only

Note:
1. The default of each volatile bit is “0” at Power-up or after reset.
2. When executed the (RDSR2) (09h) command, the WIP (SR2.0) value is the same as WIP (SR0) in table 6.

The status and control bits of the Suspend Status Register 2 are as follows:

WIP bit. The Write In Progress (WIP) bit indicates whether the memory is busy with a Write Status Register, Program or Erase cycle.
WEL bit. The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write Status Register, Program or Erase instruction is accepted.

4byte bit. The 4byte flag bit indicates bit is a read only bit in the Status Register 2 that indicates which address mode the device is currently operating in. When 4byte=0, the device is in the 3-Byte Address Mode, when 4byte=1, the device is in the 4-Byte Address Mode.

Program Fail Flag bit. While a program failure happened, the Program Fail Flag bit would be set. This bit will also be set when the user attempts to program a protected main memory region or a locked OTP region. This bit can indicated whether one or more of program operations fail, and can be reset by Program (PP), Quad Input Page Program (QPP) or Erase (SE, HBE/BE or CE) instructions.

Erase Fail Flag bit. While an erase failure happened, the Erase Fail Flag bit would be set. This bit will also be set when the user attempts to erase a protected main memory region or a locked OTP region. This bit can indicate whether one or more of erase operations fail, and can be reset by Program (PP), Quad Input Page Program (QPP) or Erase (SE, HBE/BE or CE) instructions.

Reserved bit. Status Register 2 bit locations SR2.2, SR2.3 and SR2.7 are reserved for future use. Current devices will read 0 for these bit locations. It is recommended to mask out the reserved bits when testing the Status Register 2. Doing this will ensure compatibility with future devices.

Read Status Register 3 (RDSR3) (95h)

The Read Status Register 3 (RDSR3) instruction allows the Status Register 3 to be read. The Status Register 3 may be read at any time, even while a program/erase cycle is in progress. When one of these bytes is in progress, it is recommended to check the Write In Progress (WIP) bit before sending a new instruction to the device. It is also possible to read the Read Status Register 3 continuously, as shown in Figure 13.

The instruction sequence is shown in Figure 13.1 while using the Enable Quad Peripheral Interface mode (EQPI) (38h) command.

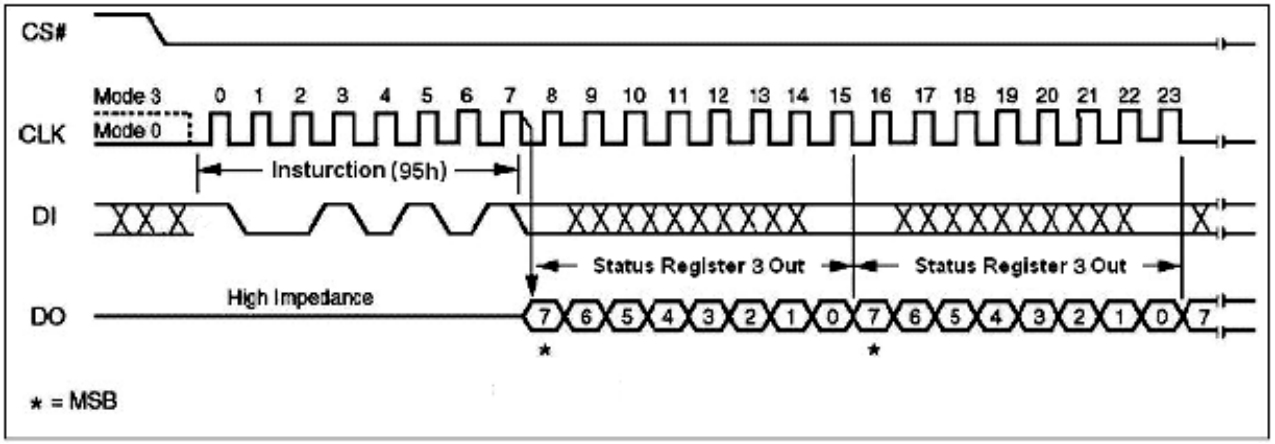


Figure 13. Read Status Register 3 Instruction Sequence Diagram

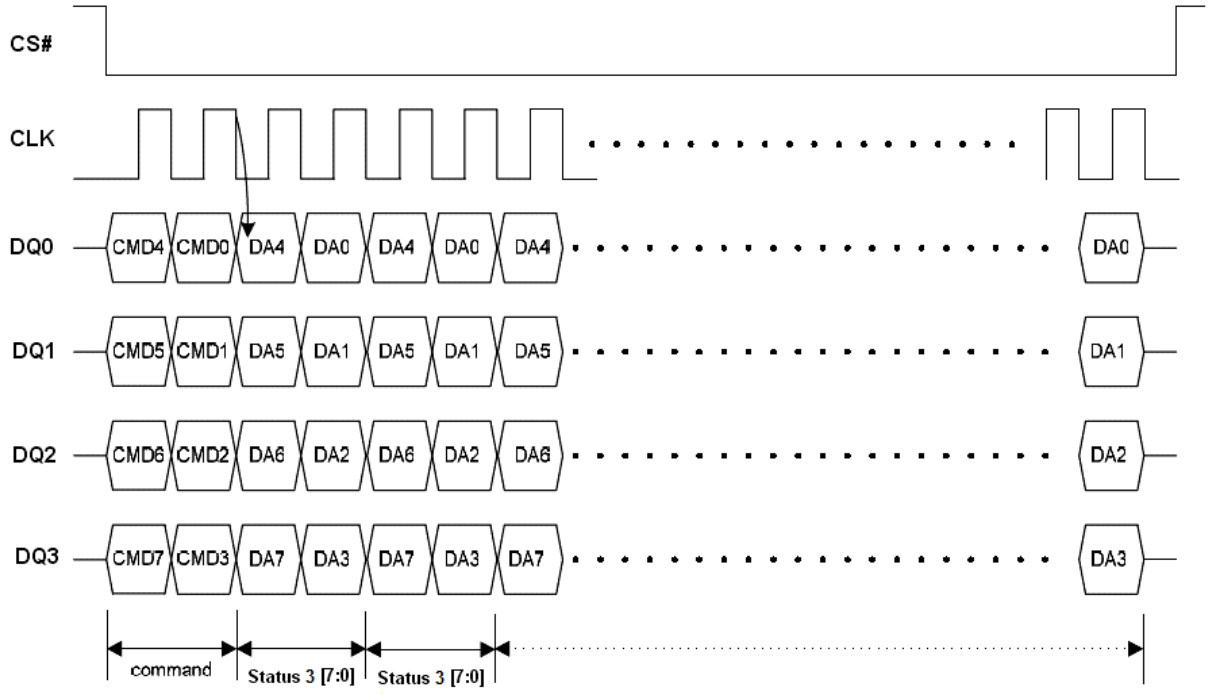


Figure 13.1 Read Status Register 3 Instruction Sequence in QPI Mode

Table 8. Status Register 3 Bit Locations

SR3.7	SR3.6	SR3.5	SR3.4	SR3.3	SR3.2	SR3.1	SR3.0
Reserved bit	Reserved bit	**Dummy Byte** (1)		**Output Drive Strength**		Reserved bit	Reserved bit
		00 = 3 Bytes 01 = 2 Bytes 10 = 4 Bytes 11 = 5 Bytes (default = 00)		00 = 67% (2/3) Drive (default) 01 = Full Drive 10 = 50% (1/2) Drive 11 = 33% (1/3) Drive			
		volatile bit		volatile bit			

Note:
1. 2 Bytes (4 clocks in Quad mode), 3 Bytes (6 clocks in Quad mode), 4 Bytes (8 clocks in Quad mode), 5 Bytes (10 clocks in Quad mode)

The status and control bits of the Status Register 3 are as follows:

Output Drive Strength bit. The Output Drive Strength (SR3.3 and SR3.2) bits indicate the status of output Drive Strength in I/O pins.

Dummy Byte bit. The Dummy Byte (SR3.5 and SR3.4) bits indicate the status of the number of dummy byte in high performance read.

Reserved bit. SR3.7, SR3.6, SR3.1 and SR3.0 are reserved for future use.

Table 9. SR3.4 and SR3.5 Status (for Dummy Bytes)

Instruction Name	Op Code	Start Address (1)	Dummy Byte settings
			<=104MHz(2.7v-3.6v)
Fast Read	**0Bh**	Byte	00 (3)
		Word	01 (2)
		Dword	01 (2)
Quad IO Fast Read	**EBh**	Byte	00 (3)
		Word	01 (2)
		Dword	01 (2)

Note:
1. “Dword” means the start address is 4-byte aligned (i.e. Start Address is 0, 4, 8...), “Word” means the start address is 2-byte aligned (i.e. Start Address is 0, 2, 4, 8...) and “Byte” means the start address can be anywhere without 2-byte or 4-byte aligned.

Read Status Register4 (RDSR4) (85h)

The Read Status Register4 (RDSR4) instruction allows the Status Register4 to be read. The Status Register may be read at any time, even while a Program, Erase or Write Status Register4 cycle is in progress. It is also possible to read the Status Register continuously, as shown in Figure 14.

The instruction sequence is shown in Figure 14.1 while using the Enable Quad Peripheral Interface mode (EQPI) (38h) command.

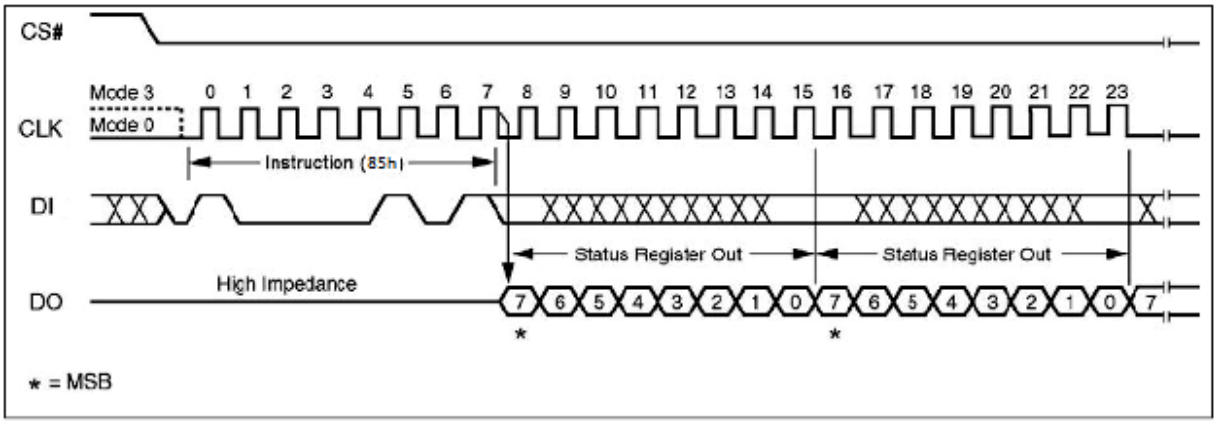


Figure 14. Read Status Register4 Instruction Sequence Diagram

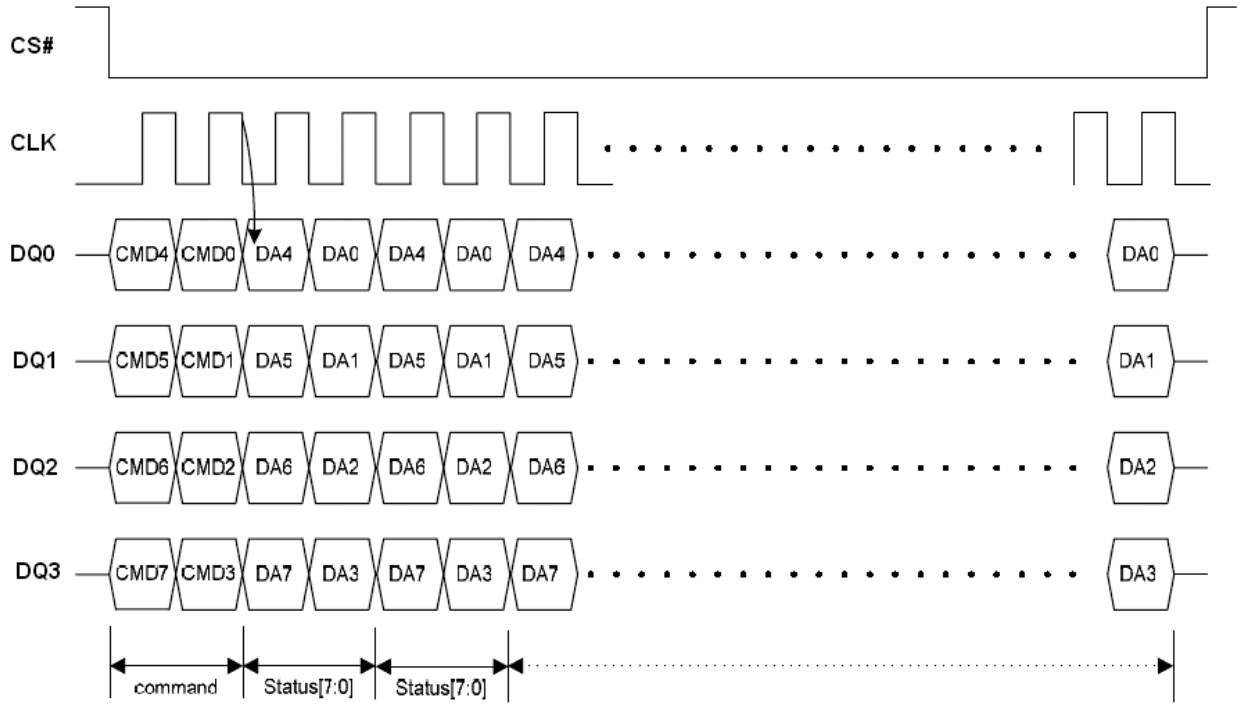


Figure 14.1 Read Status Register Instruction Sequence under QPI Mode

Table 11. Status Register4 Bit Locations

SR4.7	SR4.6	SR4.5	SR4.4	SR4.3	SR4.2	SR4.1	SR4.0
Reserved bit	**CMP** (Complement Portect)	Reserved bit	**4byteP** (address mode select)	**RSEN** (RESET# enabled)	**WPDIS** (WP# disabled)	**HDDIS** (HOLD# disabled)	**WIP** (Write In Progress)
	(note 1)		1 = 4byte address mode 0= 3byte address mode (default 0)	1 = RESET# enable 0= RESET# disable (default 0)	1 = WP# disable 0= WP# enable (default 0)	1 = HOLD# disable 0 = HOLD# enable (default ~~0~~ 1)	1 = write operation 0 = not in write operation
	Volatile bit / Non-volatile bit		Non-volatile bit	Volatile bit / Non-volatile bit	Volatile bit / Non-volatile bit	Volatile bit / Non-volatile bit	Read only bit

Note:

1. For VDFN8/WSON package, HDDIS has higher priority than RSEN.

The status and control bits of the Status Register4 are as follows:

WIP bit. The Write In Progress (WIP) bit indicates whether the memory is busy with a Write Status Register, Program or Erase cycle. When set to 1, such a cycle is in progress, when reset to 0 no such cycle is in progress.

CMP bit. The Complement Protect bit(CMP) is a non-volatile bit in Status Register 4. It is used in conjunction with TB, BP3, BP2, BP1, BP0 bits to provide mode flexibility for the array protection. The default setting is CMP=0.

4byteP bit. The 4byteP bit is a non-volatile bit that determines the initial address mode when the device is powered on or reset. This bit is only used during the power on or device reset initialization period, and it is only writable by the non-volatile Write Status sequence (06h + C1h). When 4byteP=0 (factory default), the device will power up into 3-Byte Address Mode, the Extended Address Register must be used to access memory regions beyond 128Mb. When 4byteP=1, the device will power up into 4-Byte Address Mode directly. Those commands which support 32bit address only are not related to data of 4byteP.

RSEN bit. The RESET# disable bit(RSEN), non-volatile bit, it indicates the RESET# is disabled or not. When it is “0”(factory default), the RESET# is disabled. On the other hand, while RSEN bit is “1”, the RESET# is enabled. This bit works with HDDIS bit to enable or disable HOLD#/RESET#/DQ3 at WSON/VDFN, and enable/disable RESET# for SOP16.

WPDIS bit. The Write Protect disable(WPDIS) bit, non-volatile bit, when it is reset to “0”(factory default) to enable WP# function or is set to “1” to disable WP# function. No matter WPDIS is “0” or “1”, the system can executes Quad I/O Fast Read(EBh) or EQPI(38h) command directly. User can use Flash Programmer to set WPDIS as “1” and then the host system can let WP# keep floating in SPI mode.

HDDIS bit. The HOLD# disable bit(HDDIS), non-volatile bit, it indicates the HOLD# is disabled or not. When is it “1”(factory default), the HOLD# is disabled. On the other hand, while HDDIS bit is “0”, the HOLD# is enabled. If the system executes Quad mode commands, this HDDIS bit becomes no affection since HOLD# function will be disabled by Quad mode commands.

Reserved bits. In Status Register4, SR4.5 and SR4.7 are reserved for future use. It is recommended to mask out the reserved bit when testing the Status Register4. Doing this will ensure compatibility with future devices.

Write Status Register (WRSR) (01h)

The Write Status Register (WRSR) instruction allows new values to be written to the Status Register. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded and executed, the device sets the Write Enable Latch (WEL).

The Write Status Register (WRSR) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code and the data byte on Serial Data Input (DI).

The instruction sequence is shown in Figure 15. The Write Status Register (WRSR) instruction has no effect on S1 and S0 of the Status Register. Chip Select (CS#) must be driven High after the eighth bit of the data byte has been latched in. If not, the Write Status Register (WRSR) instruction is not executed. As soon as Chip Select (CS#) is driven High, the self-timed Write Status Register cycle (whose duration is t_W) is initiated. While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Write Status Register cycle, and is 0 when it is completed. When the cycle is completed, the Write Enable Latch (WEL) is reset.

The Write Status Register (WRSR) instruction allows the user to change the values of the SRP bit, TB bit and Block Protect (BP3, BP2, BP1, BP0) bits, to define the size of the area that is to be treated as read-only, as defined in Table 3. The Write Status Register (WRSR) instruction also allows the user to set or reset the Status Register Protect (SRP) bit in accordance with the Write Protect (WP#) signal. The Status Register Protect (SRP) bit and Write Protect (WP#) signal allow the device to be put in the Hardware Protected Mode (HPM). The Write Status Register (WRSR) instruction is not executed once the Hardware Protected Mode (HPM) is entered.

The instruction sequence is shown in Figure 15.1 while using the Enable Quad Peripheral Interface mode (EQPI) (38h) command.

NOTE:

In the OTP mode without enabling Volatile Status Register function (50h), WRSR command is used to program SPL0 bit, SPL1 bit and SPL2 bit to '1', but these bits can only be programmed once.

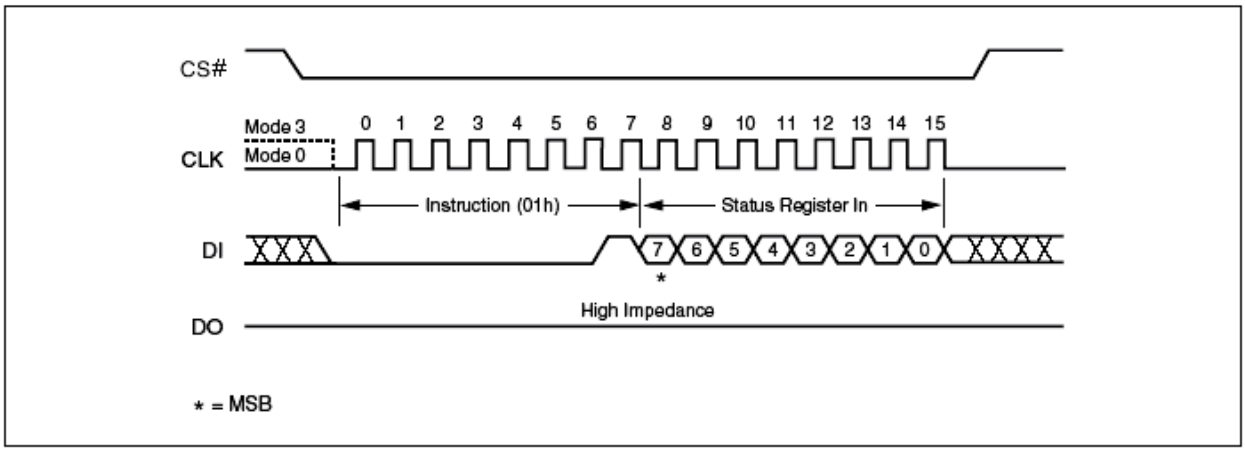


Figure 15. Write Status Register Instruction Sequence Diagram

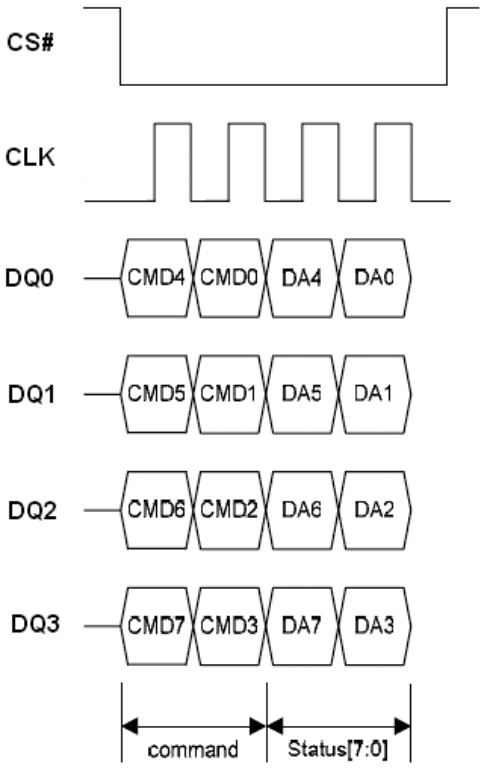


Figure 15.1 Write Status Register Instruction Sequence in QPI Mode

Read Data Bytes (READ) (03h)

The device is first selected by driving Chip Select (CS#) Low. The instruction code for the Read Data Bytes (READ) instruction is followed by a 3-byte address (A23-A0) or 4-byte address (A31-A0) (depending on mode state), each bit being latched-in during the rising edge of Serial Clock (CLK). Then the memory contents, at that address, is shifted out on Serial Data Output (DO), each bit being shifted out, at a maximum frequency f_R, during the falling edge of Serial Clock (CLK).

The instruction sequence is shown in Figure 16. The first byte addressed can be at any location. To access higher address (larger than 128Mb) in 3 byte address mode, user can issue Write Extended Register(C5h) operation before Read Data Bytes(03h). The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes (READ) instruction. When the highest address is reached, the address counter rolls over to 000000h, allowing the read sequence to be continued indefinitely.

The Read Data Bytes (READ) instruction is terminated by driving Chip Select (CS#) High. Chip Select (CS#) can be driven High at any time during data output. Any Read Data Bytes (READ) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

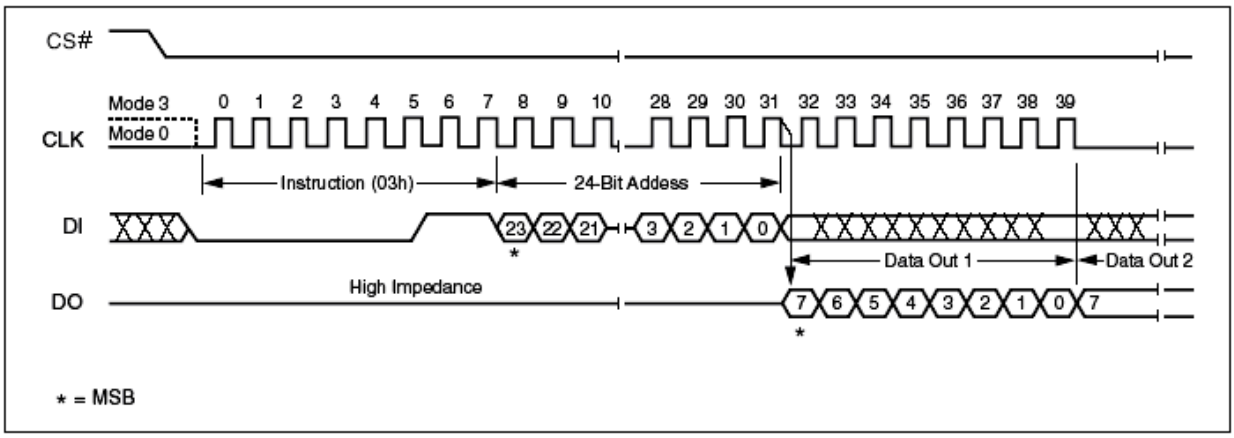


Figure 16. Read Data Instruction Sequence Diagram

Note: The above address cycles are base on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.

Read Data Bytes with 4byte address (READ4A) (13h)

The device is first selected by driving Chip Select (CS#) Low. The instruction code for the Read Data Bytes with 4bytes address (READ4A) instruction is followed by a 4-byte address (A31-A0), each bit being latched-in during the rising edge of Serial Clock (CLK). Then the memory contents, at that address, is shifted out on Serial Data Output (DO), each bit being shifted out, at a maximum frequency f_R, during the falling edge of Serial Clock (CLK).

The instruction sequence is shown in Figure 17. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes with 4byte address (READ4A) instruction. When the highest address is reached, the address counter rolls over to 000000h, allowing the read sequence to be continued indefinitely.

The Read Data Bytes with 4 byte address(READ4A) instruction is terminated by driving Chip Select (CS#) High. Chip Select (CS#) can be driven High at any time during data output. Any Read Data Bytes with 4byte address(READ4A) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

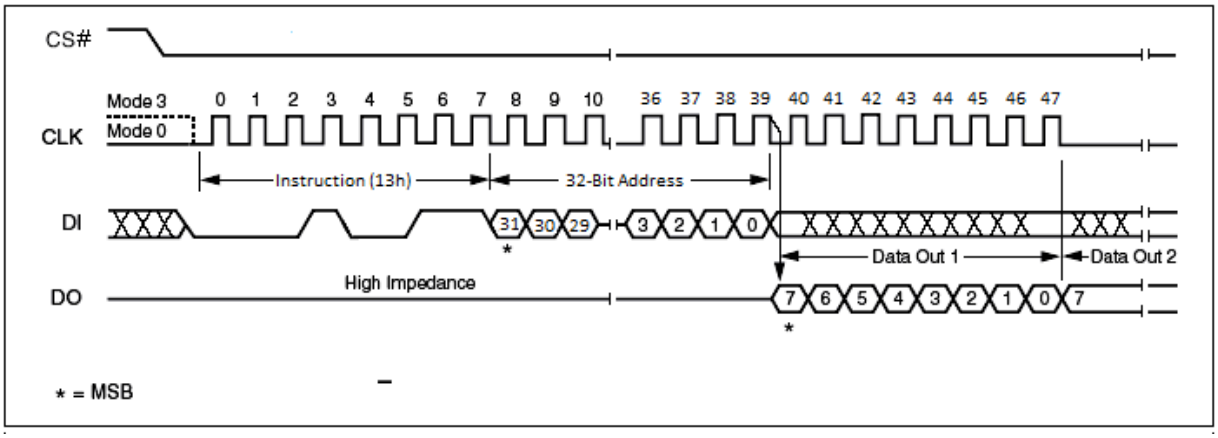


Figure 17. Read Data with 4byte address Instruction Sequence Diagram

Note: This instruction is workable while in 4byte address mode.

Read Data Bytes at Higher Speed (FAST_READ) (0Bh)

The device is first selected by driving Chip Select (CS#) Low. The instruction code for the Read Data Bytes at Higher Speed (FAST_READ) instruction is followed by a 3-byte address (A23-A0) or 4-byte address (A31-A0) (depending on mode state) and a dummy byte, each bit being latched-in during the rising edge of Serial Clock (CLK). Then the memory contents, at that address, is shifted out on Serial Data Output (DO), each bit being shifted out, at a maximum frequency F_R, during the falling edge of Serial Clock (CLK).

The instruction sequence is shown in Figure 18. The first byte addressed can be at any location. To access higher address (larger than 128Mb) in 3 byte address mode, user can issue Write Extended Register(C5h) operation before Read Data Bytes at Higher Speed(0Bh). The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes at Higher Speed (FAST_READ) instruction. When the highest address is reached, the address counter rolls over to 000000h, allowing the read sequence to be continued indefinitely.

The Read Data Bytes at Higher Speed (FAST_READ) instruction is terminated by driving Chip Select (CS#) High. Chip Select (CS#) can be driven High at any time during data output. Any Read Data Bytes at Higher Speed (FAST_READ) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

The instruction sequence is shown in Figure 18.1 while using the Enable Quad Peripheral Interface mode (EQPI) (38h) command.

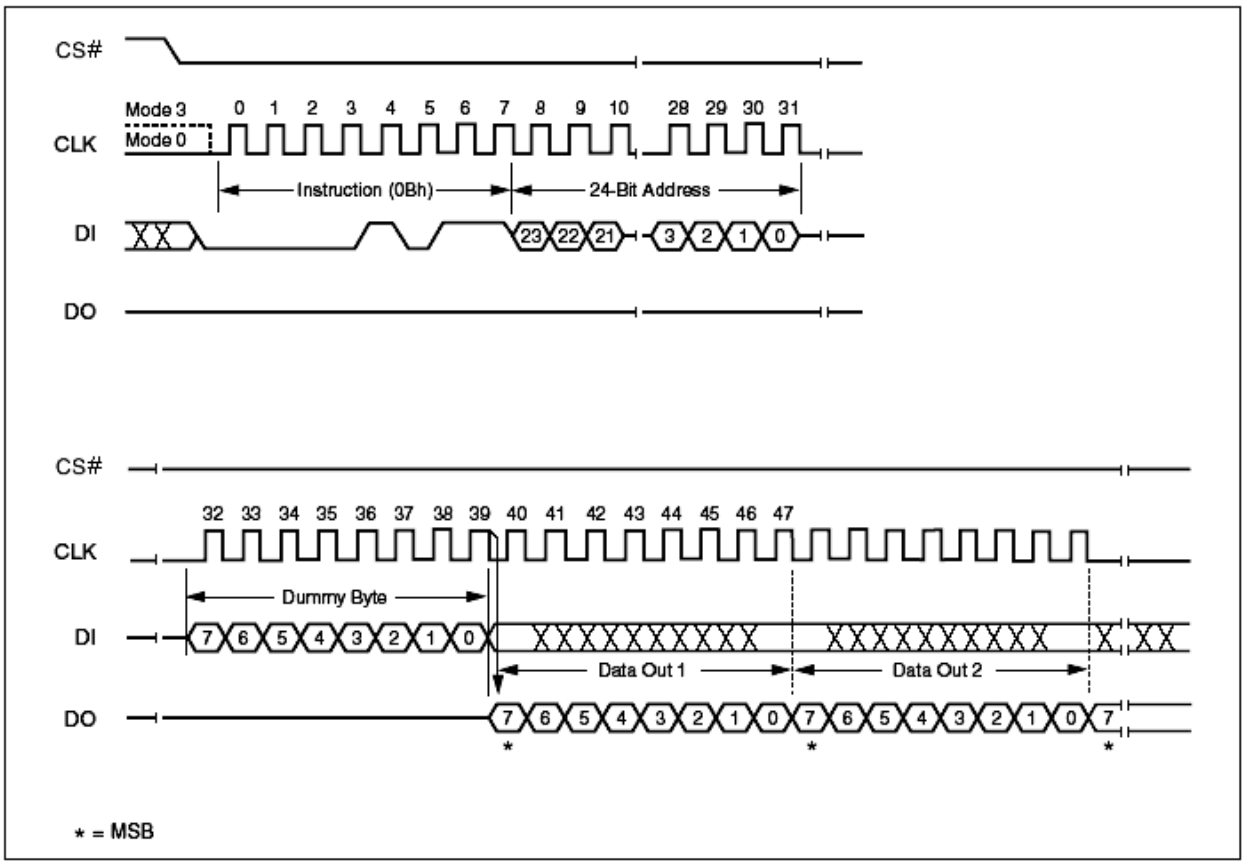


Figure 18. Fast Read Instruction Sequence Diagram

Note: The above address cycles are base on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.

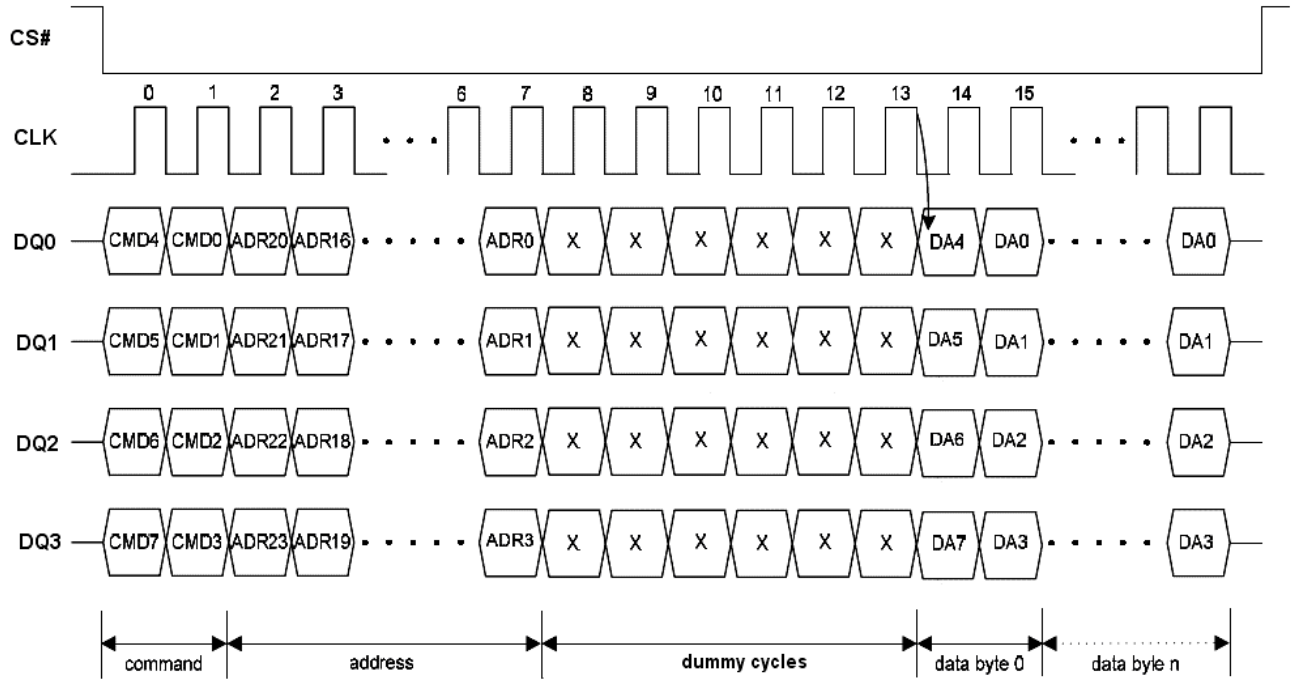


Figure 18.1 Fast Read Instruction Sequence in QPI Mode

Note: The above address cycles are base on 3-byte address mode, for 4-byte address mode, the address cycles will be increased.

Read Data Bytes at Higher Speed with 4byte address (FAST_READ4A) (0Ch)

The device is first selected by driving Chip Select (CS#) Low. The instruction code for the Read Data Bytes at Higher Speed with 4byte address (FAST_READ4A) instruction is followed by a 4-byte address (A31-A0) and a dummy byte, each bit being latched-in during the rising edge of Serial Clock (CLK). Then the memory contents, at that address, is shifted out on Serial Data Output (DO), each bit being shifted out, at a maximum frequency F_R, during the falling edge of Serial Clock (CLK).

The instruction sequence is shown in Figure 19. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes at Higher Speed with 4byte address (FAST_READ4A) instruction. When the highest address is reached, the address counter rolls over to 000000h, allowing the read sequence to be continued indefinitely.

The Read Data Bytes at Higher Speed with 4byte address (FAST_READ4A) instruction is terminated by driving Chip Select (CS#) High. Chip Select (CS#) can be driven High at any time during data output. Any Read Data Bytes at Higher Speed with 4byte address (FAST_READ4A) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

The instruction sequence is shown in Figure 19.1 while using the Enable Quad Peripheral Interface mode (EQPI) (38h) command.

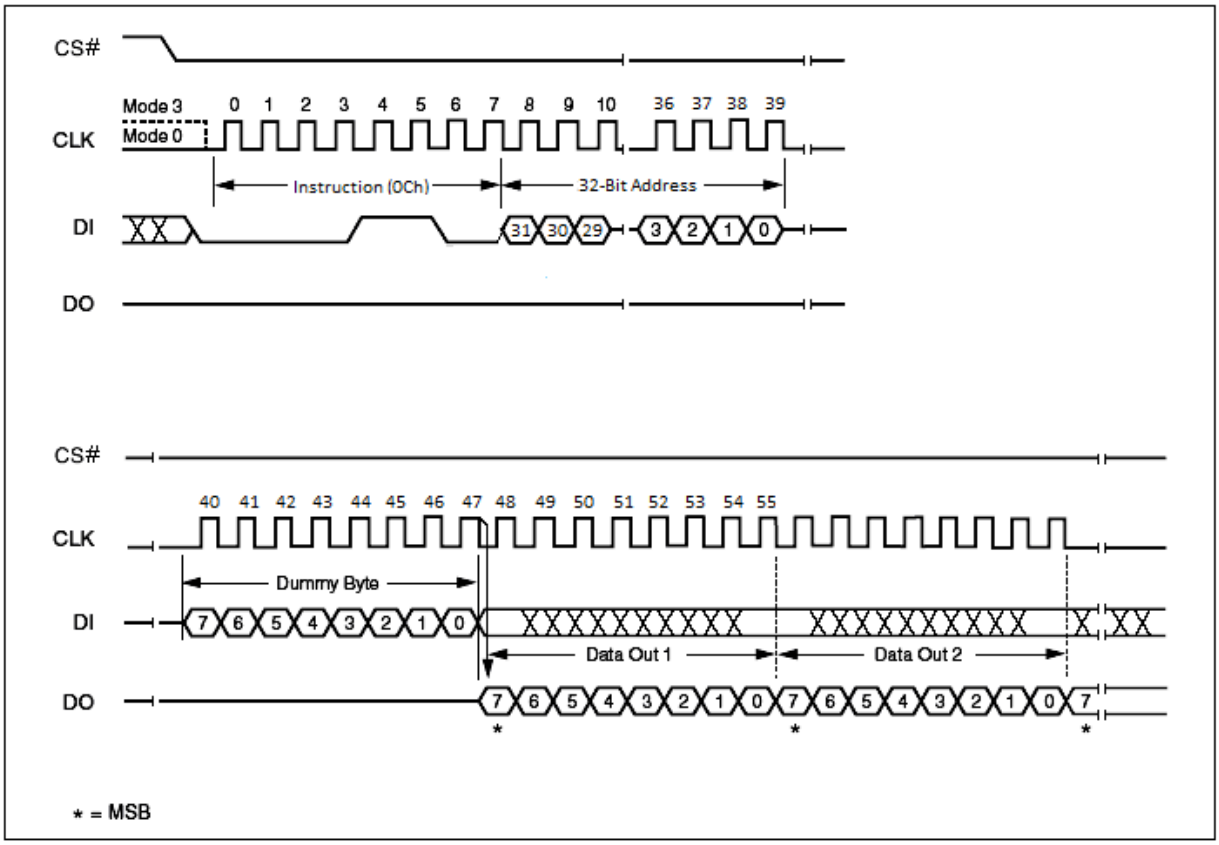


Figure 19. Fast Read with 4byte address Instruction Sequence Diagram

Note: This instruction is workable while in 4byte address mode.

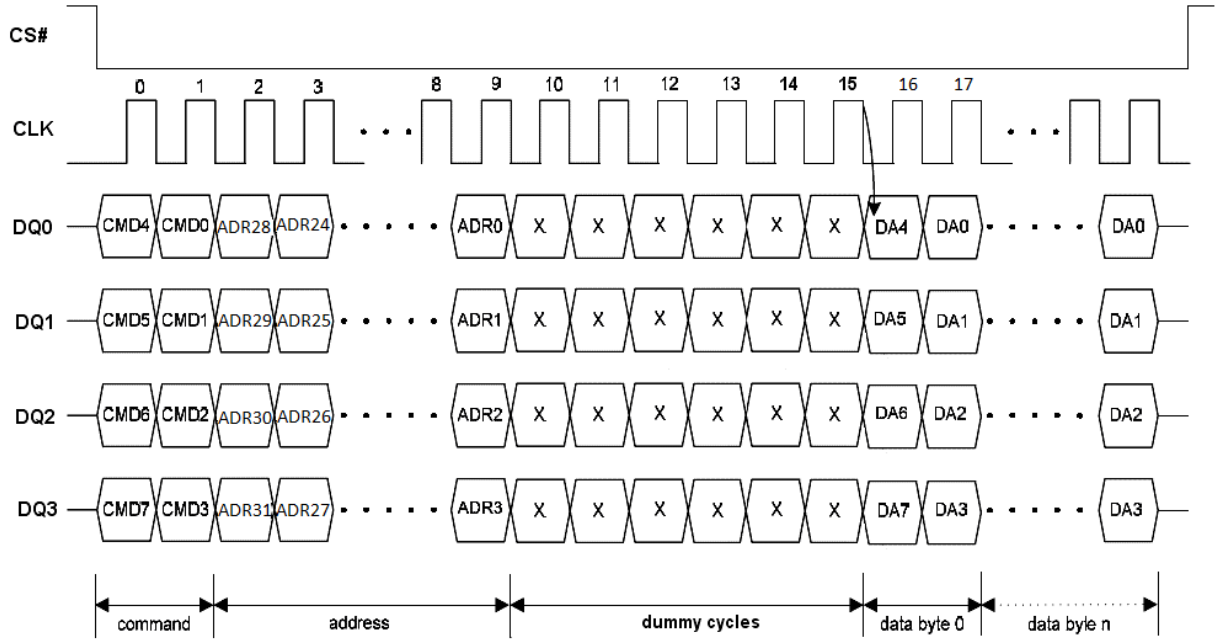


Figure 19.1 Fast Read with 4byte address Instruction Sequence in QPI Mode

Note: This instruction is workable while in 4byte address mode.

Dual Output Fast Read (3Bh)

The Dual Output Fast Read (3Bh) is similar to the standard Fast Read (0Bh) instruction except that data is output on two pins, DQ_0 and DQ_1, instead of just DQ_1. This allows data to be transferred from the device at twice the rate of standard SPI device s. The Dual Output Fast Read instruction is ideal for quickly downloading code from to RAM upon power-up or for applications that cache code-segments to RAM for execution.

Similar to the Fast Read instruction, the Dual Output Fast Read instructions can operation at the highest possible frequency of FR (see AC Electrical Characteristics). This is accomplished by adding eight "dummy clocks after the 24-bit address or 32-bit address(depend on mode state) as shown in Figure 20. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clock is "don't care". However, the DI pin should be high-impedance prior to the falling edge of the first data out clock.

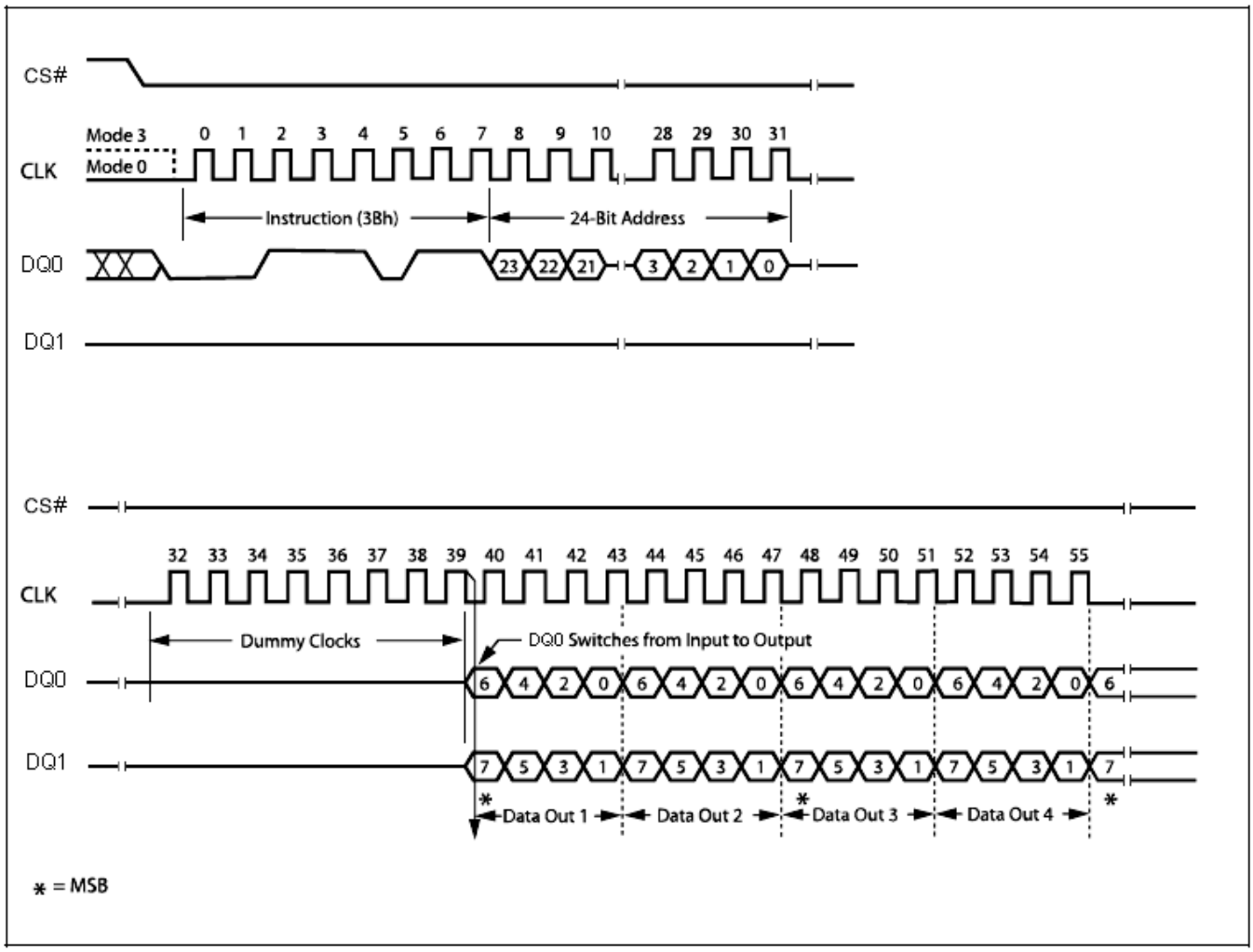


Figure 20. Dual Output Fast Read Instruction Sequence Diagram

Note: The above address cycles are base on 3-byte address mode, for 4-byte address mode, the address cycles will be increased.

Dual Output Fast Read with 4byte address(3Ch)

The Dual Output Fast Read with 4byte address(3Ch) is similar to the standard Fast Read with 4byte address (0Ch) instruction except that data is output on two pins, DQ_0 and DQ_1, instead of just DQ_1. This allows data to be transferred from the device at twice the rate of standard SPI device's. The Dual Output Fast Read with 4byte address instruction is ideal for quickly downloading code from to RAM upon power-up or for applications that cache code-segments to RAM for execution.

Similar to the Fast Read with 4byte address instruction, the Dual Output Fast Read with 4byte address instruction can operation at the highest possible frequency of FR (see AC Electrical Characteristics). This is accomplished by adding eight dummy clocks after the 32-bit address as shown in Figure 21. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clock is "don't care". However, the DI pin should be high-impedance prior to the falling edge of the first data out clock.

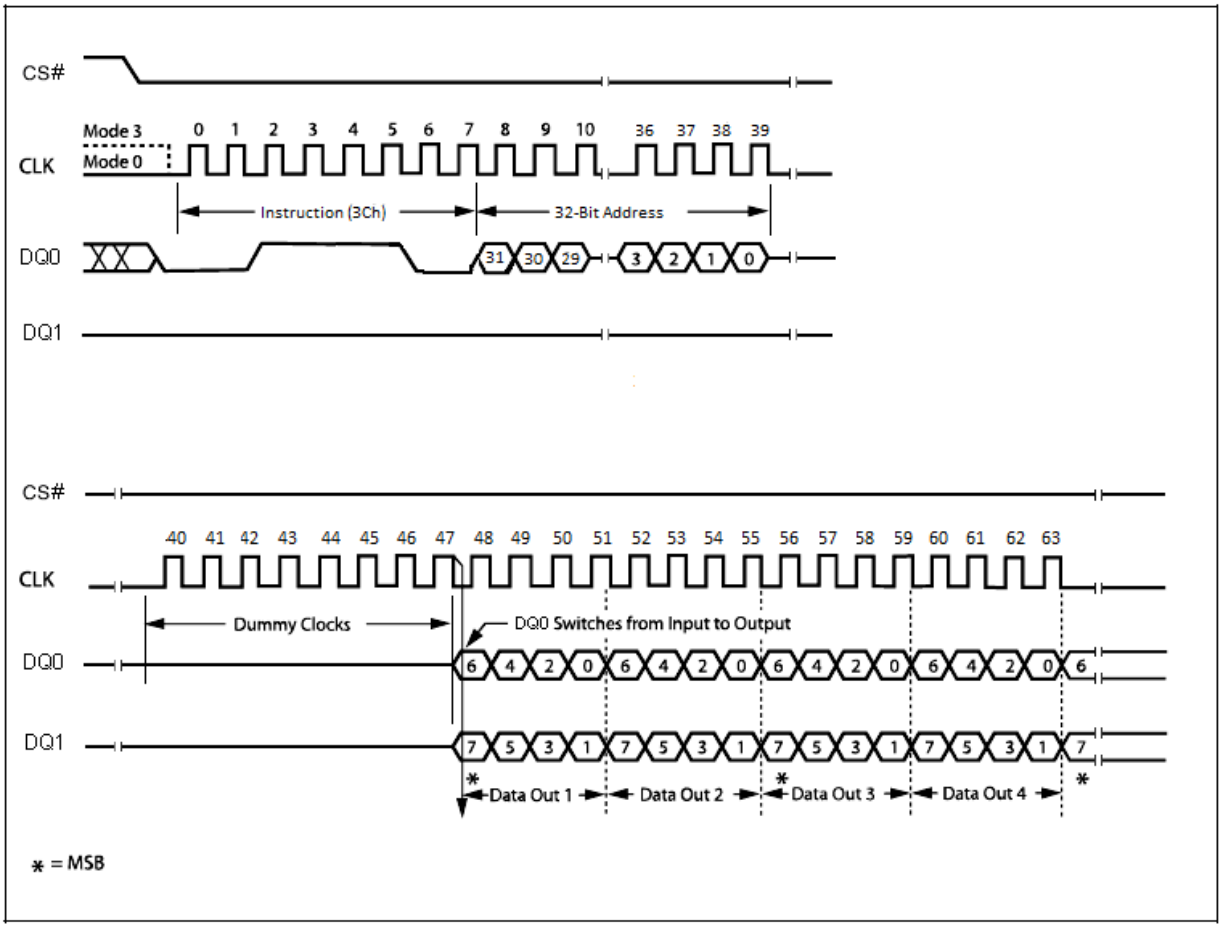


Figure 21. Dual Output Fast Read with 4byte address Instruction Sequence Diagram

Note: This instruction is workable while in 4byte address mode.

Dual Input / Output FAST_READ (BBh)

The Dual I/O Fast Read (BBh) instruction allows for improved random access while maintaining two IO pins, DQ_0 and DQ_1. It is similar to the Dual Output Fast Read (3Bh) instruction but with the capability to input the Address bits (A23-0 or A31-0, depends on mode state) two bits per clock. This reduced instruction overhead may allow for code execution (XIP) directly from the Dual SPI in some applications.

The Dual I/O Fast Read instruction enable double throughput of Serial Flash in read mode. The address is latched on rising edge of CLK, and data of every two bits (interleave 2 I/O pins) shift out on the falling edge of CLK at a maximum frequency. The first address can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single Dual I/O Fast Read instruction. To access higher address (larger than 128Mb) in 3 byte address mode, user can issue Write Extended Register(C5h) operation before Dual Input / Output FAST_READ(BBh). The address counter rolls over to 0 when the highest address has been reached. Once writing Dual I/O Fast Read instruction, the following address/dummy/data out will perform as 2-bit instead of previous 1-bit, as shown in Figure 22.

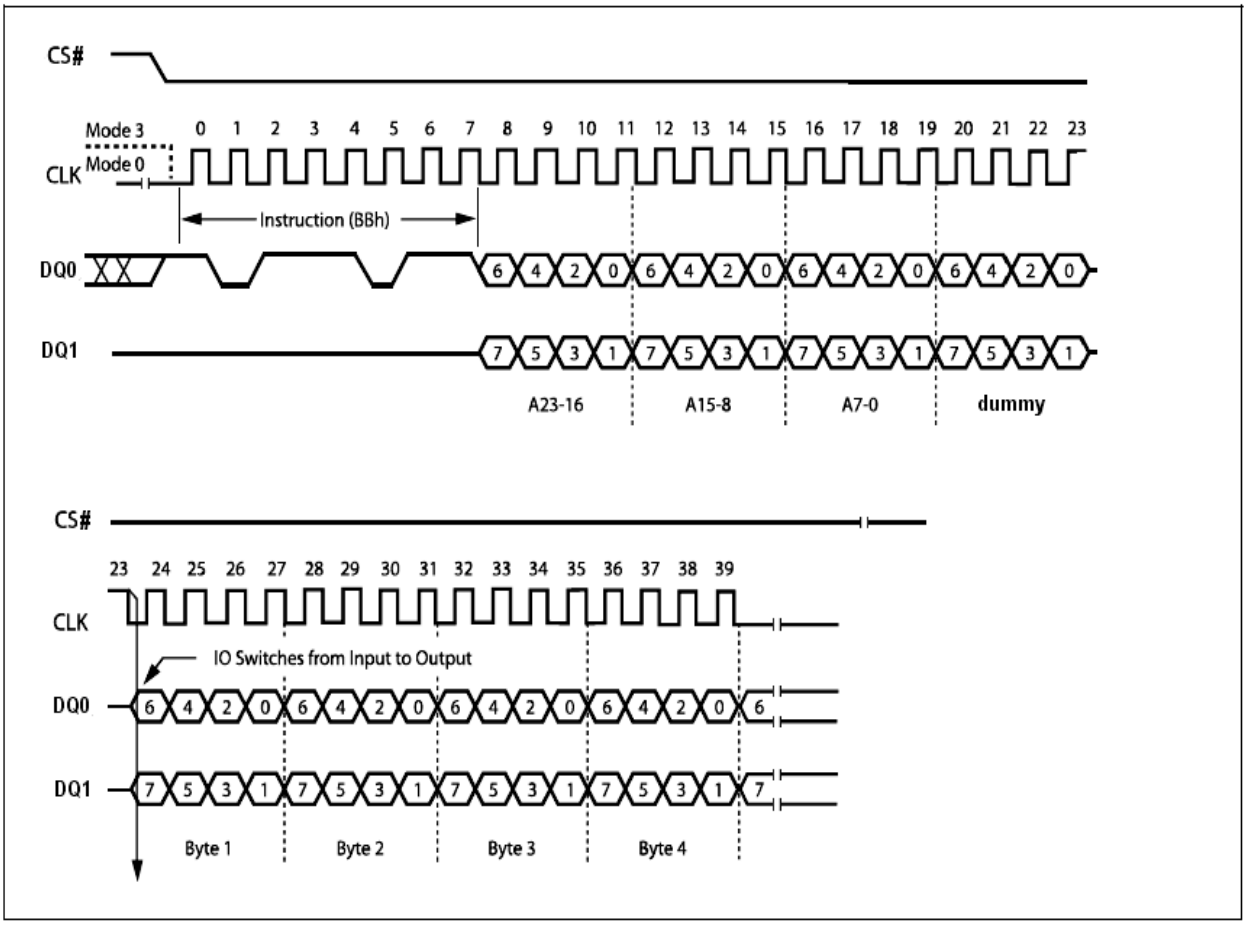


Figure 22. Dual Input / Output Fast Read Instruction Sequence Diagram

Note: The above address cycles are base on 3-byte address mode, for 4-byte address mode, the address cycles will be increased.

Dual Input / Output FAST_READ with 4byte address(BCh)

The Dual I/O Fast Read with 4byte address(BCh) instruction allows for improved random access while maintaining two IO pins, DQ_0 and DQ_1. It is similar to the Dual Output Fast Read with 4byte address(3Ch) instruction but with the capability to input the Address bits (A31-0) two bits per clock. This reduced instruction overhead may allow for code execution (XIP) directly from the Dual SPI in some applications.

The Dual I/O Fast Read with 4byte address instruction enable double throughput of Serial Flash in read mode. The address is latched on rising edge of CLK, and data of every two bits (interleave 2 I/O pins) shift out on the falling edge of CLK at a maximum frequency. The first address can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single Dual I/O Fast Read with 4byte address instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing Dual I/O Fast Read with 4byte address instruction, the following address/dummy/data out will perform as 2-bit instead of previous 1-bit, as shown in Figure 23.

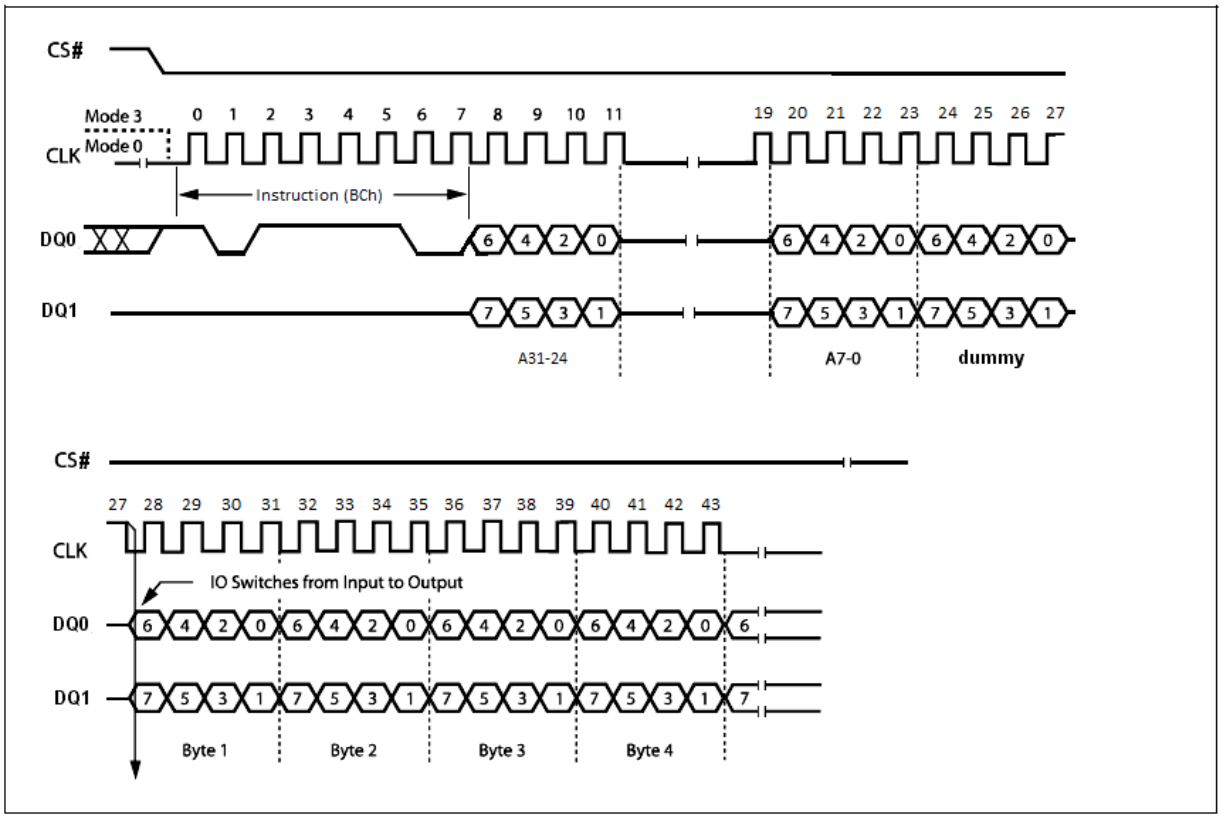


Figure 23. Dual Input / Output Fast Read with 4byte address Instruction Sequence Diagram

Note: This instruction is workable while in 4byte address mode.

Quad Output Fast Read (6Bh)

The Quad Output Fast Read (6Bh) instruction is similar to the Dual Output Fast Read (3Bh) instruction except that data is output through four pins, DQ0, DQ1, DQ2 and DQ3 and eight dummy clocks are required prior to the data output. The Quad Output dramatically reduces instruction overhead allowing faster random access for code execution (XIP) directly from the Quad SPI.

The Quad Output Fast Read (6Bh) address is latching on rising edge of CLK, and data of every four bits (interleave on 4 I/O pins) shift out on the falling edge of CLK at a maximum frequency FR. The first address can be any location. To access higher address (larger than 128Mb) in 3 byte address mode, user can issue Write Extended Register(C5h) operation before Quad Output FAST_READ(6Bh). The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single Quad Output Fast Read instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence of issuing Quad Output Fast Read (6Bh) instruction is: CS# goes low -> sending Quad Output Fast Read (6Bh) instruction -> 24-bit/32-bit address on DQ0 (depend on mode state) -> 8 dummy clocks -> data out interleave on DQ3, DQ2, DQ1 and DQ0 -> to end Quad Output Fast Read (6Bh) operation can use CS# to high at any time during data out, as shown in Figure 24. The WP# (DQ2) and HOLD#/RESET# (DQ3) need to drive high before address input if WP#, HOLD# or RESET# is enable.

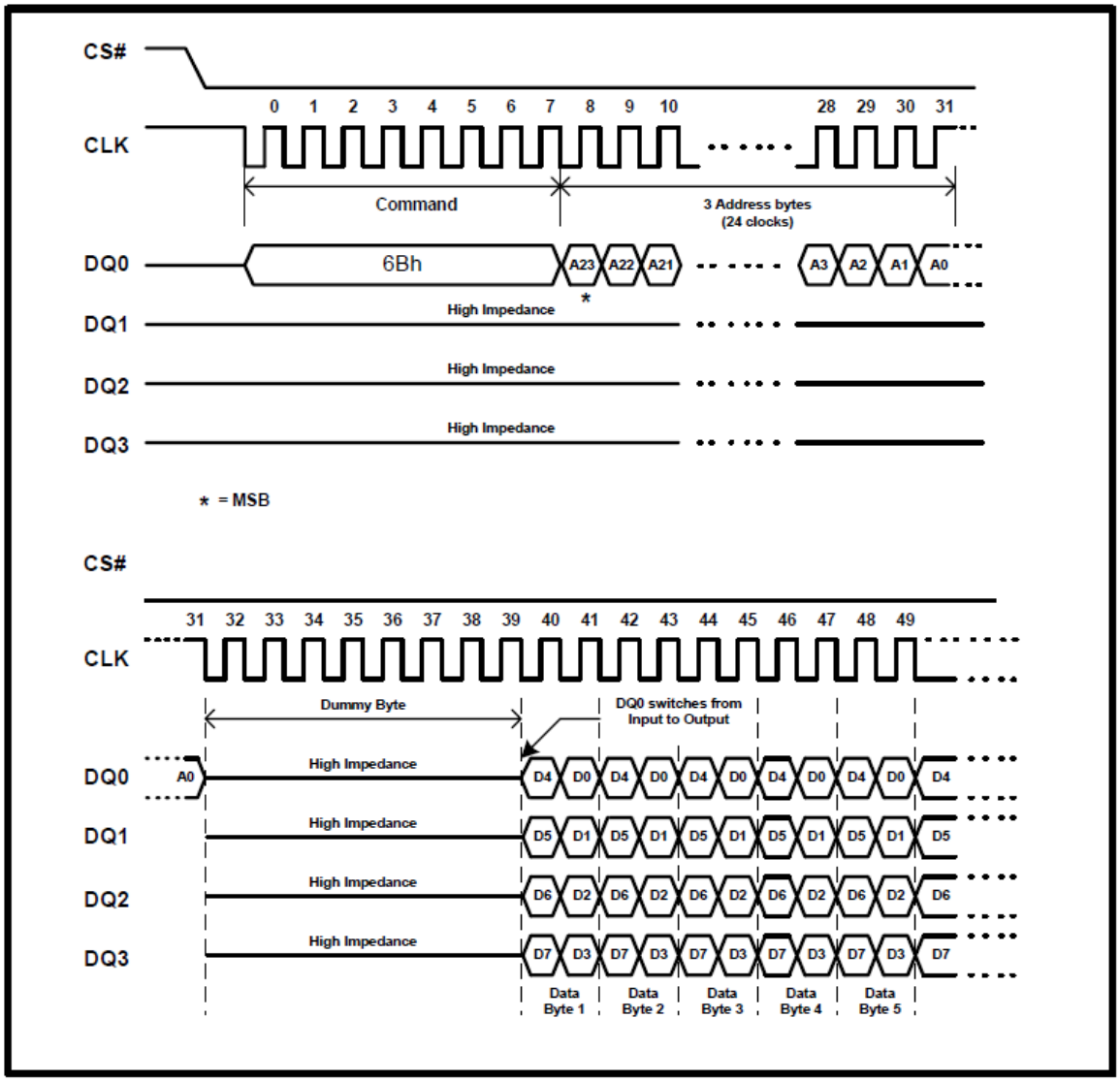


Figure 24. Quad Output Fast Read Instruction Sequence Diagram

Note: The above address cycles are base on 3-byte address mode, for 4-byte address mode, the address cycles will be increased.

Quad Output Fast Read with 4byte address (6Ch)

The Quad Output Fast Read with 4byte address (6Ch) instruction is similar to the Dual Output Fast Read with 4byte address(3Ch) instruction except that data is output through four pins, DQ0, DQ1, DQ2 and DQ3 and eight dummy clocks are required prior to the data output. The Quad Output dramatically reduces instruction overhead allowing faster random access for code execution (XIP) directly from the Quad SPI.

The Quad Output Fast Read with 4byte address(6Ch) address is latching on rising edge of CLK, and data of every four bits (interleave on 4 I/O pins) shift out on the falling edge of CLK at a maximum frequency FR. The first address can be any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single Quad Output Fast Read with 4byte address instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence of issuing Quad Output Fast Read with 4byte address (6Ch) instruction is: CS# goes low -> sending Quad Output Fast Read with 4byte addrses (6Ch) instruction -> 32-bit address on DQ0 -> 8 dummy clocks -> data out interleave on DQ3, DQ2, DQ1 and DQ0 -> to end Quad Output Fast Read with 4byte address(6Ch) operation can use CS# to high at any time during data out, as shown in Figure 25. The WP# (DQ2) and HOLD#/RESET# (DQ3) need to drive high before address input if WP#, HOLD# or RESET# is enable.

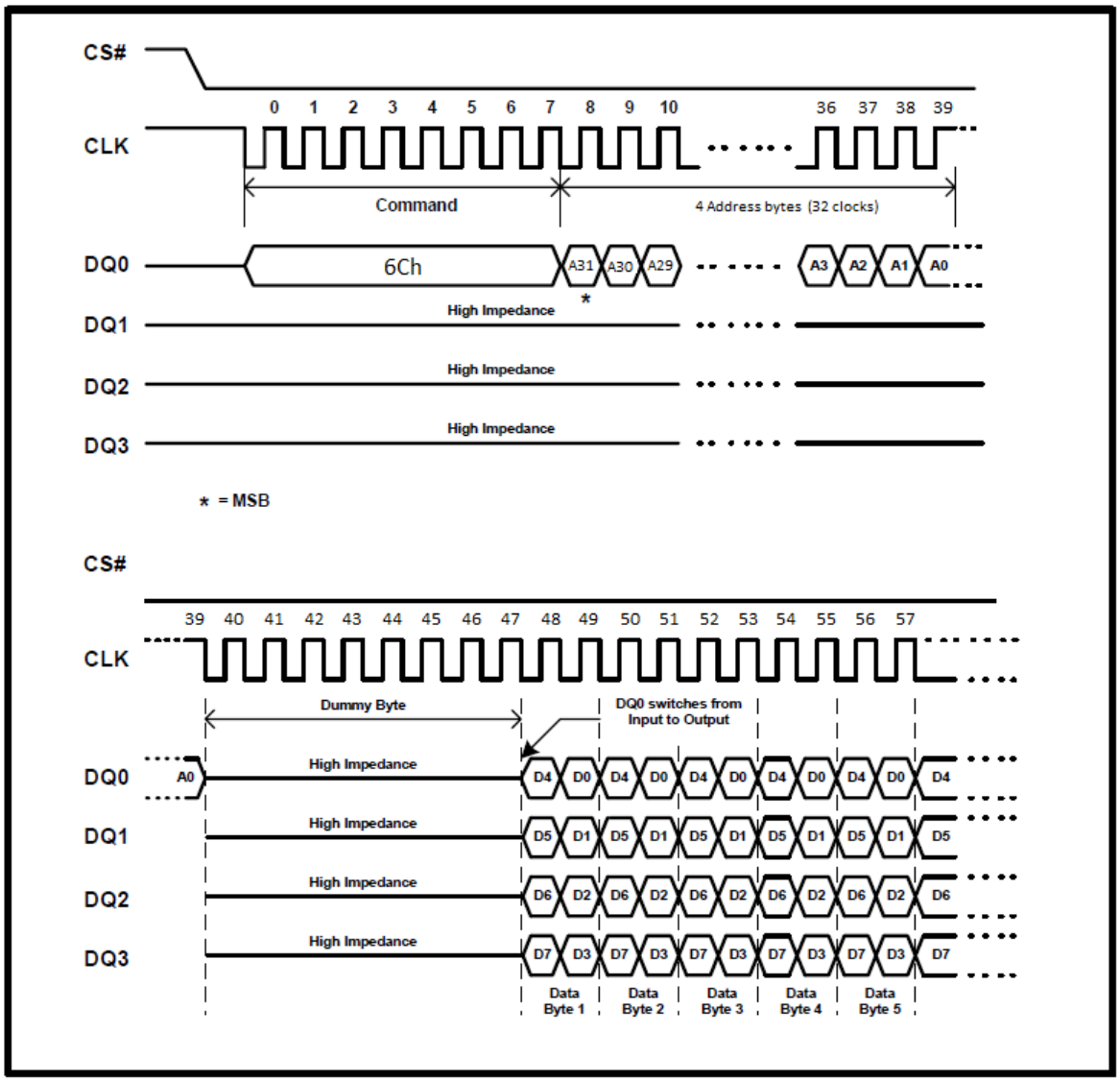


Figure 25. Quad Output Fast Read with 4byte address Instruction Sequence Diagram

Note: This instruction is workable while in 4byte address mode.

Quad Input / Output FAST_READ (EBh)

The Quad Input/Output FAST_READ (EBh) instruction is similar to the Dual I/O Fast Read (BBh) instruction except that address and data bits are input and output through four pins, DQ_0, DQ_1, DQ_2 and DQ_3 and six dummy clocks are required prior to the data output. The Quad I/O dramatically reduces instruction overhead allowing faster random access for code execution (XIP) directly from the Quad SPI.

The Quad Input/Output FAST_READ (EBh) instruction enable quad throughput of Serial Flash in read mode. The address is latching on rising edge of CLK, and data of every four bits (interleave on 4 I/O pins) shift out on the falling edge of CLK at a maximum frequency F_R. The first address can be any location. To access higher address (larger than 128Mb) in 3 byte address mode, user can issue Write Extended Register(C5h) operation before Quad Input/Output FAST_READ(EBh).The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single Quad Input/Output FAST_READ instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing Quad Input/Output FAST_READ instruction, the following address/dummy/data out will perform as 4-bit instead of previous 1-bit.

The sequence of issuing Quad Input/Output FAST_READ (EBh) instruction is: CS# goes low -> sending Quad Input/Output FAST_READ (EBh) instruction -> 24-bit(or 32-bit, depends on mode state) address interleave on DQ_3, DQ_2, DQ_1 and DQ_0 -> 6 dummy clocks -> data out interleave on DQ_3, DQ_2, DQ_1 and DQ_0 -> to end Quad Input/Output FAST_READ (EBh) operation can use CS# to high at any time during data out, as shown in Figure 26.

The instruction sequence is shown in Figure 26.1 while using the Enable Quad Peripheral Interface mode (EQPI) (38h) command.

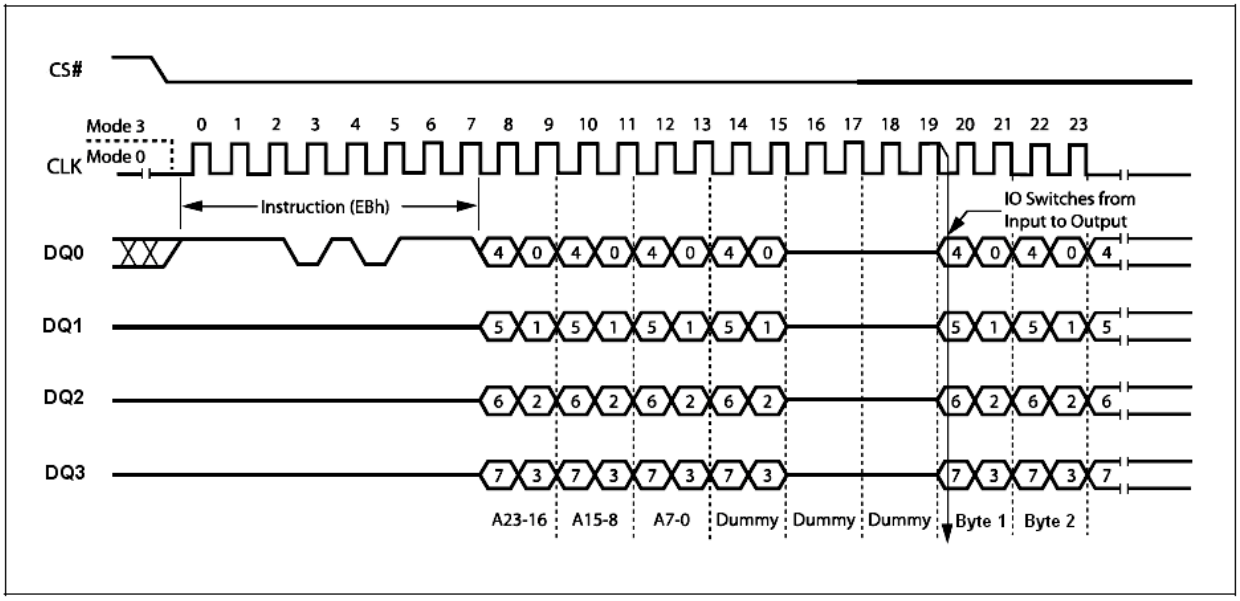


Figure 26. Quad Input / Output Fast Read Instruction Sequence Diagram

Note: The above address cycles are base on 3-byte address mode, for 4-byte address mode, the address cycles will be increased.

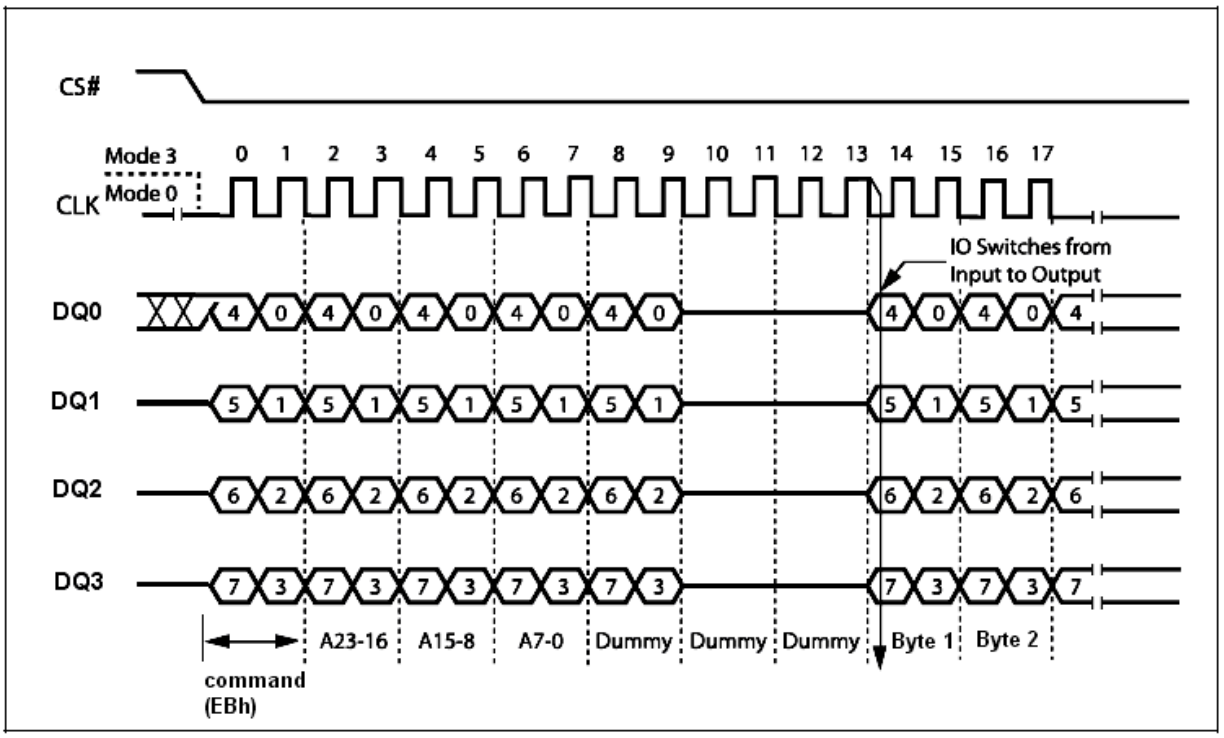


Figure 26.1 Quad Input / Output Fast Read Instruction Sequence in QPI Mode

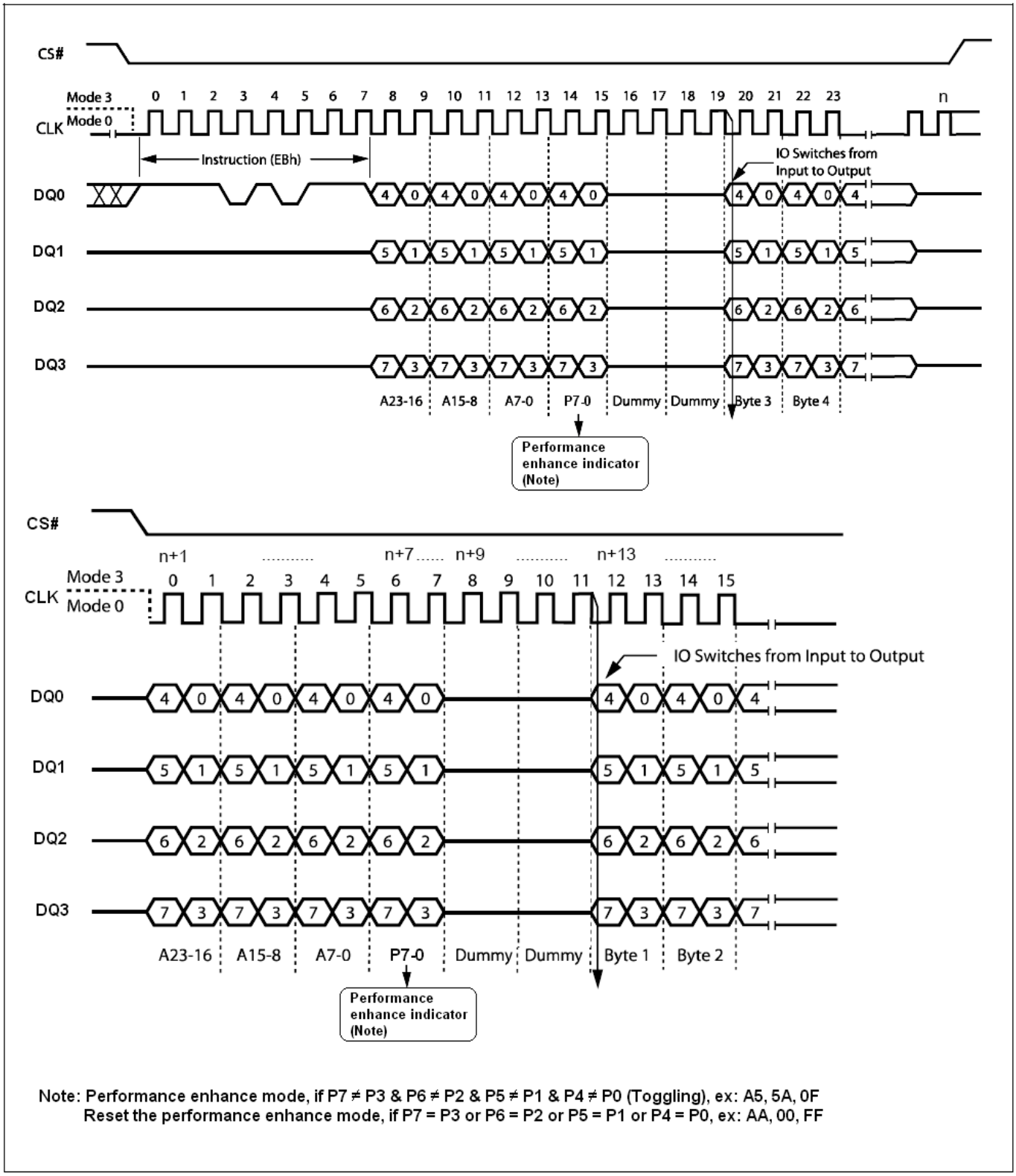
Note: The above address cycles are base on 3-byte address mode, for 4-byte address mode, the address cycles will be increased.

Another sequence of issuing Quad Input/Output FAST_READ (EBh) instruction especially useful in random access is : CS# goes low -> sending Quad Input/Output FAST_READ (EBh) instruction -> 24-bit(or 32-bit, depends on mode state) address interleave on DQ_3, DQ_2, DQ_1 and DQ_0 -> performance enhance toggling bit P[7:0] -> 4 dummy clocks -> data out interleave on DQ_3, DQ_2, DQ_1 and DQ_0 till CS# goes high -> CS# goes low (reduce Quad Input/Output FAST_READ (EBh) instruction) -> 24-bit (or 32-bit, depends on mode state) random access address, as shown in Figure 27.

In the performance – enhancing mode, P[7:4] must be toggling with P[3:0] ; likewise P[7:0] = A5h, 5Ah, F0h or 0Fh can make this mode continue and reduce the next Quad Input/Output FAST_READ (EBh) instruction. Once P[7:4] is no longer toggling with P[3:0] ; likewise P[7:0] = FFh, 00h, AAh or 55h. These commands will reset the performance enhance mode. And afterwards CS# is raised or issuing FFh command (CS# goes high -> CS# goes low -> sending FFh -> CS# goes high) instead of no toggling, the system then will escape from performance enhance mode and return to normal operation.

While Program/ Erase/ Write Status Register is in progress, Quad Input/Output FAST_READ (EBh) instruction is rejected without impact on the Program/ Erase/ Write Status Register current cycle.

The instruction sequence is shown in Figure 27.1 while using the Enable Quad Peripheral Interface mode (EQPI) (38h) command.



Note: Performance enhance mode, if P7 ≠ P3 & P6 ≠ P2 & P5 ≠ P1 & P4 ≠ P0 (Toggling), ex: A5, 5A, 0F
Reset the performance enhance mode, if P7 = P3 or P6 = P2 or P5 = P1 or P4 = P0, ex: AA, 00, FF

Figure 27. Quad Input/Output Fast Read Enhance Performance Mode Sequence Diagram

Note: The above address cycles are base on 3-byte address mode, for 4-byte address mode, the address cycles will be increased.

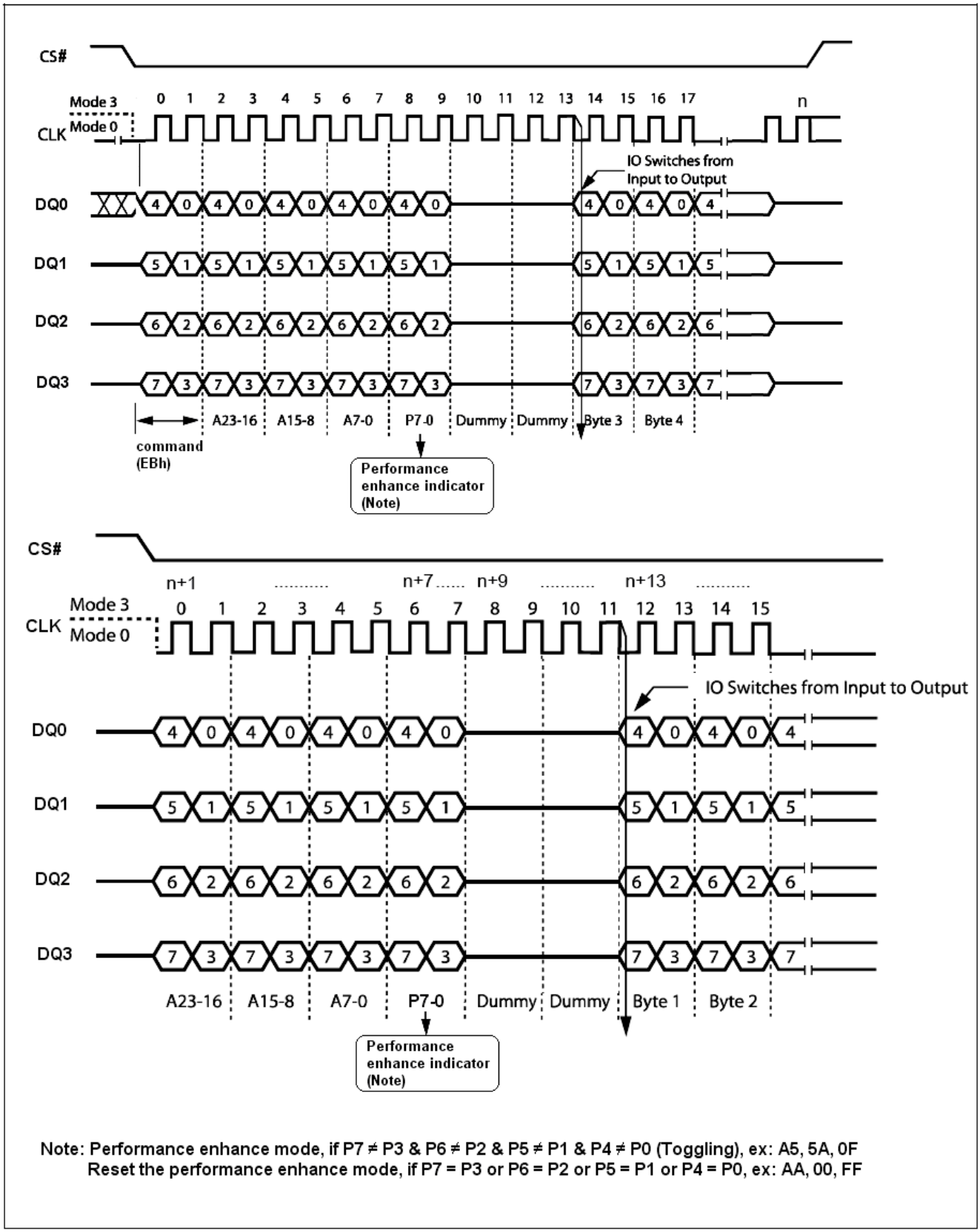


Figure 27.1 Quad Input/Output Fast Read Enhance Performance Mode Sequence in QPI Mode

Note: The above address cycles are base on 3-byte address mode, for 4-byte address mode, the address cycles will be increased.

Quad Input / Output FAST_READ with 4byte address (ECh)

The Quad Input/Output FAST_READ with 4byte address(ECh) instruction is similar to the Dual I/O Fast Read with 4byte address(BCh) instruction except that address and data bits are input and output through four pins, DQ_0, DQ_1, DQ_2 and DQ_3 and six dummy clocks are required prior to the data output. The Quad I/O dramatically reduces instruction overhead allowing faster random access for code execution (XIP) directly from the Quad SPI.

The Quad Input/Output FAST_READ with 4byte address(ECh) instruction enable quad throughput of Serial Flash in read mode. The address is latching on rising edge of CLK, and data of every four bits (interleave on 4 I/O pins) shift out on the falling edge of CLK at a maximum frequency F_R. The first address can be any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single Quad Input/Output FAST_READ with 4byte address instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing Quad Input / Output FAST_READ with 4byte address instruction, the following address/dummy/data out will perform as 4-bit instead of previous 1-bit.

The sequence of issuing Quad Input/Output FAST_READ with 4byte address (ECh) instruction is: CS# goes low -> sending Quad Input/Output FAST_READ (EBh) instruction -> 32-bit address interleave on DQ_3, DQ_2, DQ_1 and DQ_0 -> 6 dummy clocks -> data out interleave on DQ_3, DQ_2, DQ_1 and DQ_0 -> to end Quad Input/Output FAST_READ with 4byte address(ECh) operation can use CS# to high at any time during data out, as shown in Figure 28.

The instruction sequence is shown in Figure 28.1 while using the Enable Quad Peripheral Interface mode (EQPI) (38h) command.

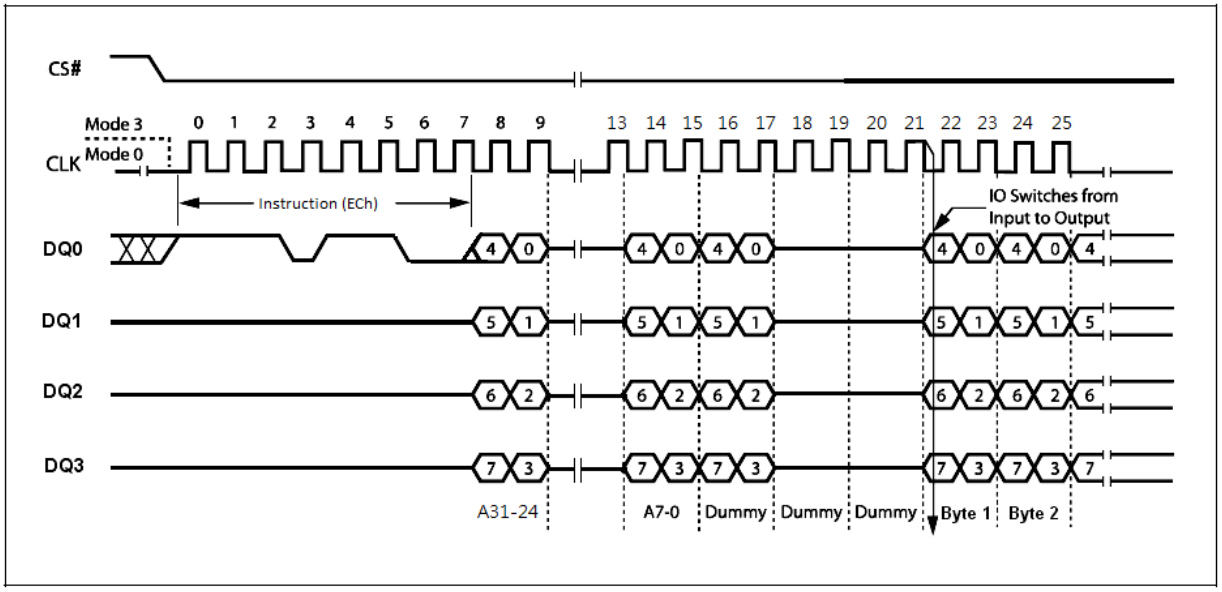


Figure 28. Quad Input / Output Fast Read with 4byte address Instruction Sequence Diagram

Note: This instruction is workable while in 4byte address mode.

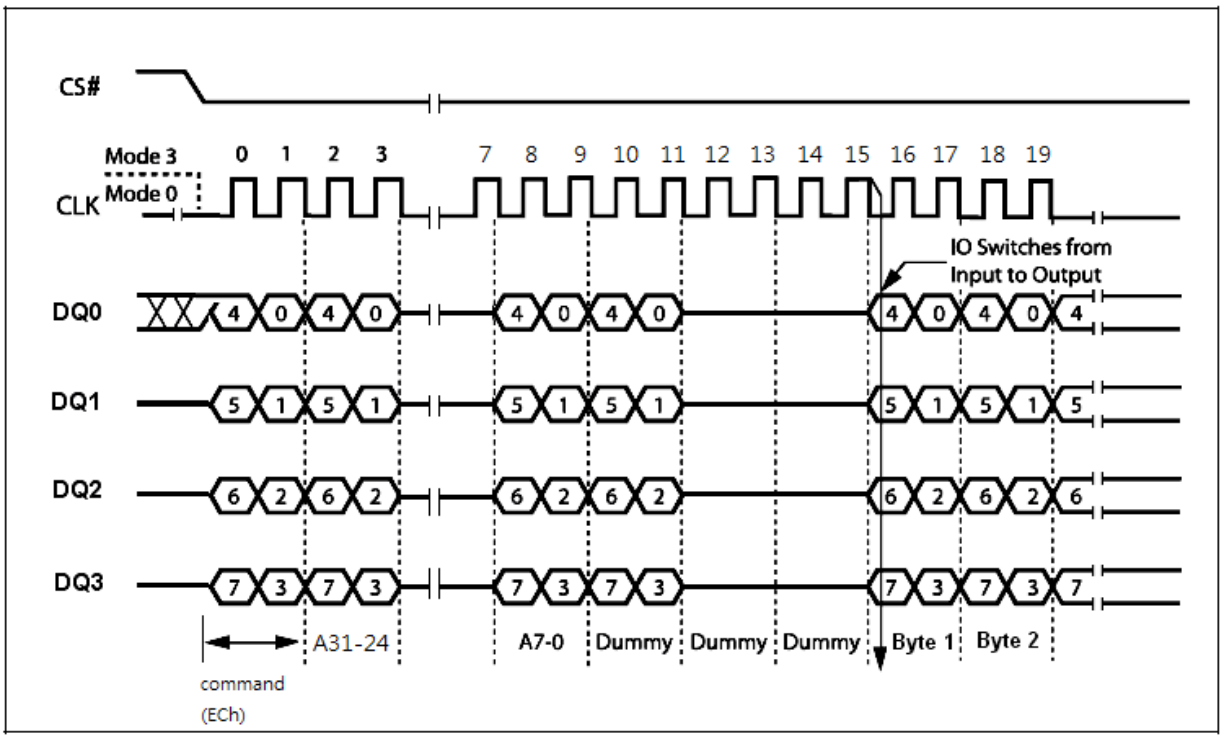


Figure 28.1 Quad Input / Output Fast Read with 4byte address Instruction Sequence in QPI Mode

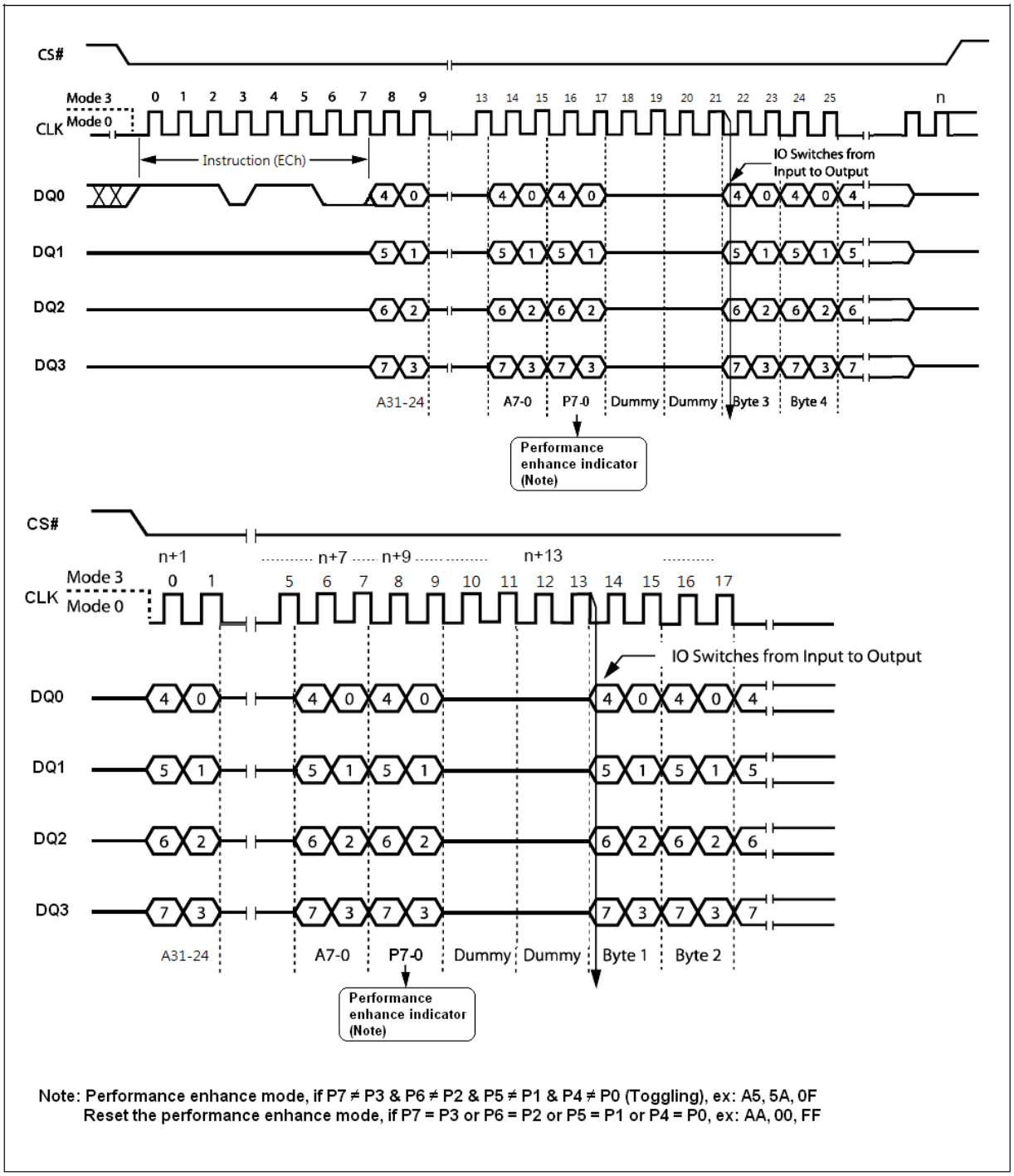
Note: This instruction is workable while in 4byte address mode.

Another sequence of issuing Quad Input/Output FAST_READ with 4byte address(ECh) instruction especially useful in random access is : CS# goes low -> sending Quad Input/Output FAST_READ with 4byte address(ECh) instruction -> 32-bit address interleave on DQ_3, DQ_2, DQ_1 and DQ_0 -> performance enhance toggling bit P[7:0] -> 4 dummy clocks -> data out interleave on DQ_3, DQ_2, DQ_1 and DQ_0 till CS# goes high -> CS# goes low (reduce Quad Input/ Output FAST_READ with 4byte address(ECh) instruction) -> 32-bit random access address, as shown in Figure 29.

In the performance – enhancing mode, P[7:4] must be toggling with P[3:0] ; likewise P[7:0] = A5h, 5Ah, F0h or 0Fh can make this mode continue and reduce the next Quad Input/ Output FAST_READ with 4byte address(ECh) instruction. Once P[7:4] is no longer toggling with P[3:0] ; likewise P[7:0] = FFh, 00h, AAh or 55h. These commands will reset the performance enhance mode. And afterwards CS# is raised or issuing FFh command (CS# goes high -> CS# goes low -> sending FFh -> CS# goes high) instead of no toggling, the system then will escape from performance enhance mode and return to normal operation.

While Program/ Erase/ Write Status Register is in progress, Quad Input/Output FAST_READ with 4byte address (ECh) instruction is rejected without impact on the Program/ Erase/ Write Status Register current cycle.

The instruction sequence is shown in Figure 29.1 while using the Enable Quad Peripheral Interface mode (EQPI) (38h) command.



Note: Performance enhance mode, if P7 ≠ P3 & P6 ≠ P2 & P5 ≠ P1 & P4 ≠ P0 (Toggling), ex: A5, 5A, 0F
Reset the performance enhance mode, if P7 = P3 or P6 = P2 or P5 = P1 or P4 = P0, ex: AA, 00, FF

Figure 29. Quad Input/Output Fast Read Enhance Performance Mode with 4byte address Sequence Diagram

Note: This instruction is workable while in 4byte address mode.

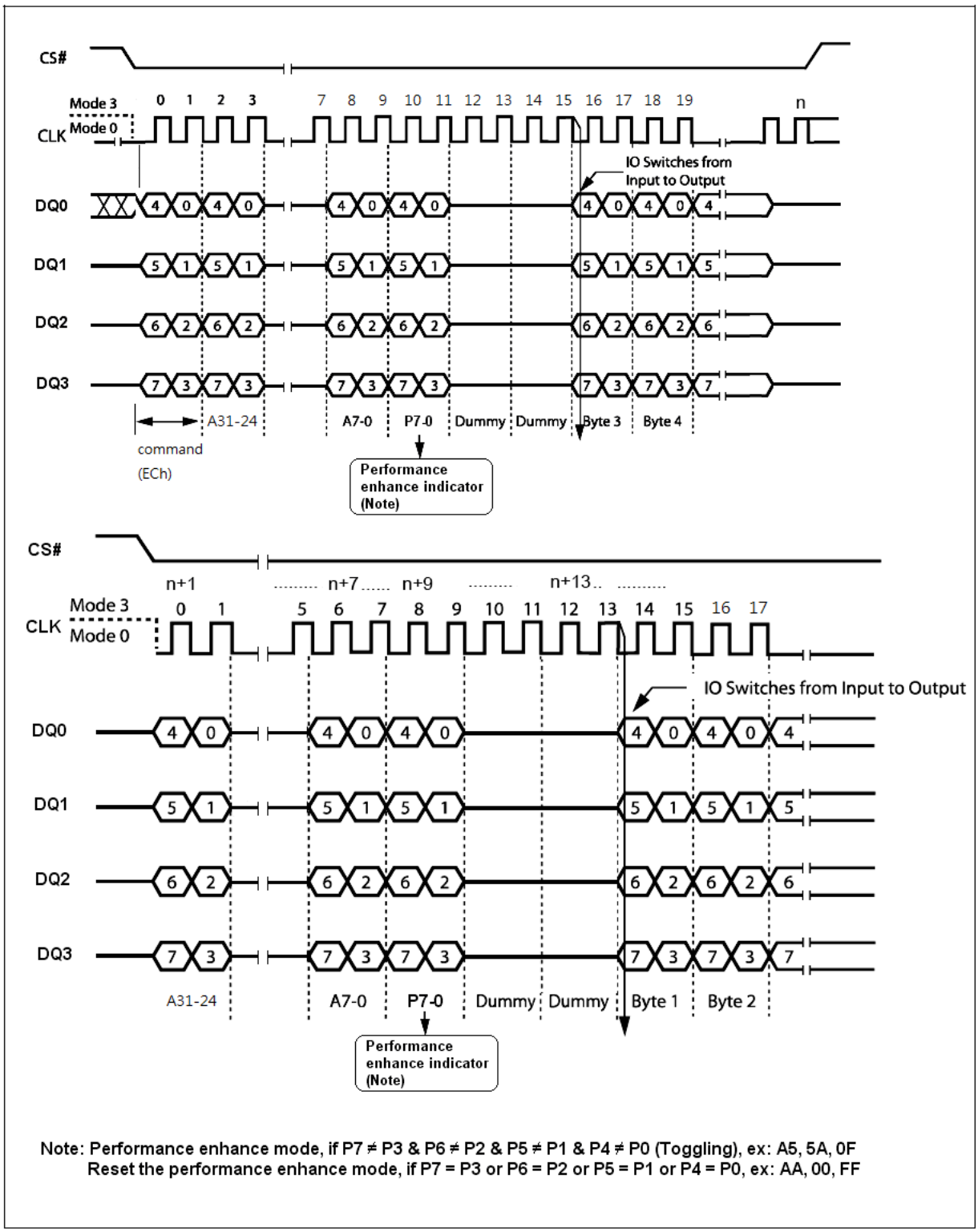


Figure 29.1 Quad Input/Output Fast Read Enhance Performance Mode Sequence with 4byte address in QPI Mode

Note: This instruction is workable while in 4byte address mode.

Write Status Register 3 (C0h)

The Write Status Register 3 (C0h) command can be used to set output drive strength in I/O pins and the number of dummy byte in high performance read. To set output I/O driver strength and dummy byte, the host driver CS# low, sends the Write Status Register 3 (C0h) and one data byte, then drivers CS# high. After power-up or reset, the output drive strength is set to 67% drive (00b) and the dummy byte is set to 3 bytes (00b), please refer to Table 8 for Status Register 3 data and Figure 30 for the sequence.

In QPI mode, a cycle is two nibbles, or two clocks, long, most significant nibble first. The instruction sequence is shown in Figure 30.1 while using the Enable Quad Peripheral Interface mode (EQPI) (38h) command.

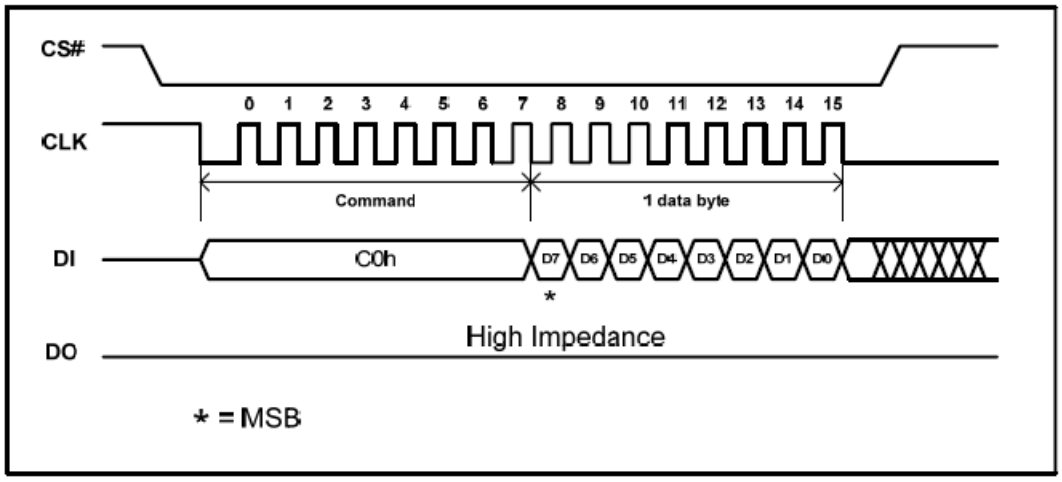
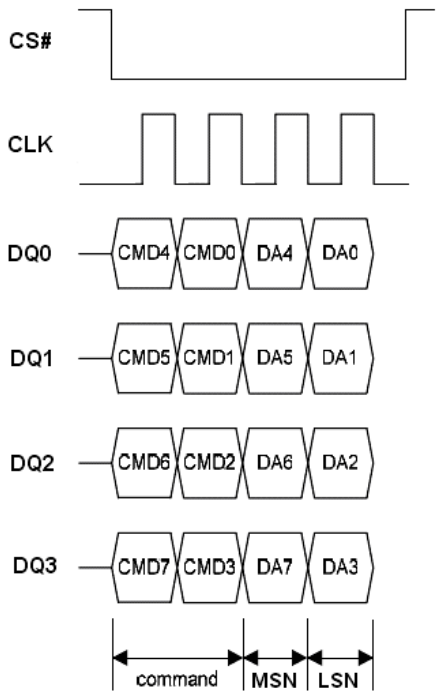


Figure 30. Write Status Register 3 Instruction Sequence Diagram



Note: MSN = Most Significant Nibble,
LSN = Least Significant Nibble

Figure 30.1 Write Status Register 3 Instruction Sequence Diagram in QPI mode

Write Status Register 4 (C1h)

The Write Status Register 4 (C1h) command can be used to enable or disable HOLD#, WP# and RESET# pin by using HDDIS, WPDIS and RSEN bit, set CMP bit to protect array data and 4byteP for 3byte or 4byte address mode. This register also can driver CS# low, sends the Write Status Register4(C1h) and one data byte, then drivers CS# high, please refer to Table 10 for Status Register 4 data and Figure 31 for the sequence. In QPI mode, a cycle is two nibbles, or two clocks, most significant nibble first.
The Write Status Register 4(WRSR4) instruction also allows the user to set or reset the Status Register Protect(SRP) bit in accordance with the Write Protect(WP#) signal. The Status Register Protect(SRP) bit and Write Protect(WP#) signal allow the device to be put in the Hardware Protected Mode(HPM). The Write Status Register 4(WRSR4) instruction is not executed once the Hardware Protected Mode(HPM) is entered.

The instruction sequence is shown in Figure 31.1 while using the Enable Quad Peripheral Interface mode (EQPI) (38h) command.

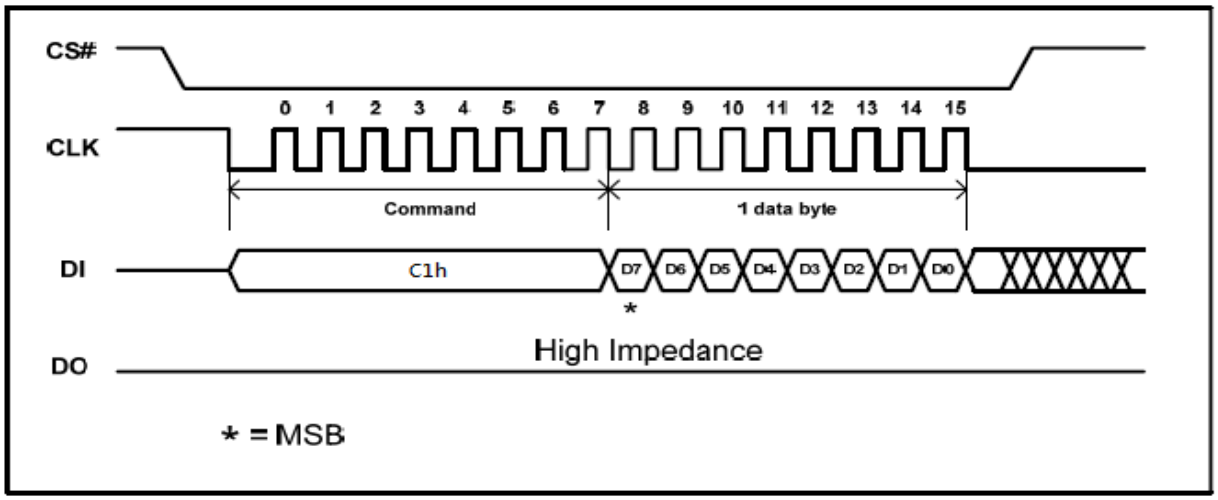
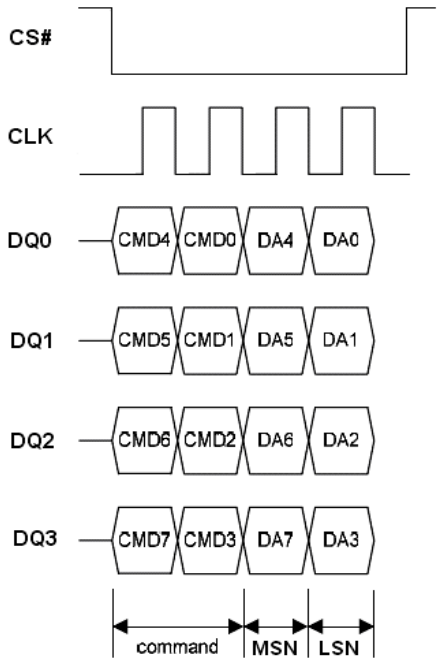


Figure 31. Write Status Register 4 Instruction Sequence Diagram



Note: MSN = Most Significant Nibble,
LSN = Least Significant Nibble

Figure 31.1 Write Status Register 4 Instruction Sequence Diagram in QPI mode

Page Program (PP) (02h)

The Page Program (PP) instruction allows bytes to be programmed in the memory. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Page Program (PP) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code, three (or four, depends on mode state) address bytes and at least one data byte on Serial Data Input (DI). If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). Chip Select (CS#) must be driven Low for the entire duration of the sequence.
The instruction sequence is shown in Figure 32. If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 Data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page.
To access higher address (larger than 128Mb) in 3 byte address mode, user can issue Write Extended Register(C5h) operation before Page Program(02h).

Chip Select (CS#) must be driven High after the eighth bit of the last data byte has been latched in, otherwise the Page Program (PP) instruction is not executed.

As soon as Chip Select (CS#) is driven high, the self-timed Page Program cycle (whose duration is t_{PP}) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Page Program (PP) instruction applied to a page which is protected by the Block Protect (CMP, TB, BP3, BP2, BP1, BP0) bits (see Table 3) is not executed.

The instruction sequence is shown in Figure 32.1 while using the Enable Quad Peripheral Interface mode (EQPI) (38h) command.

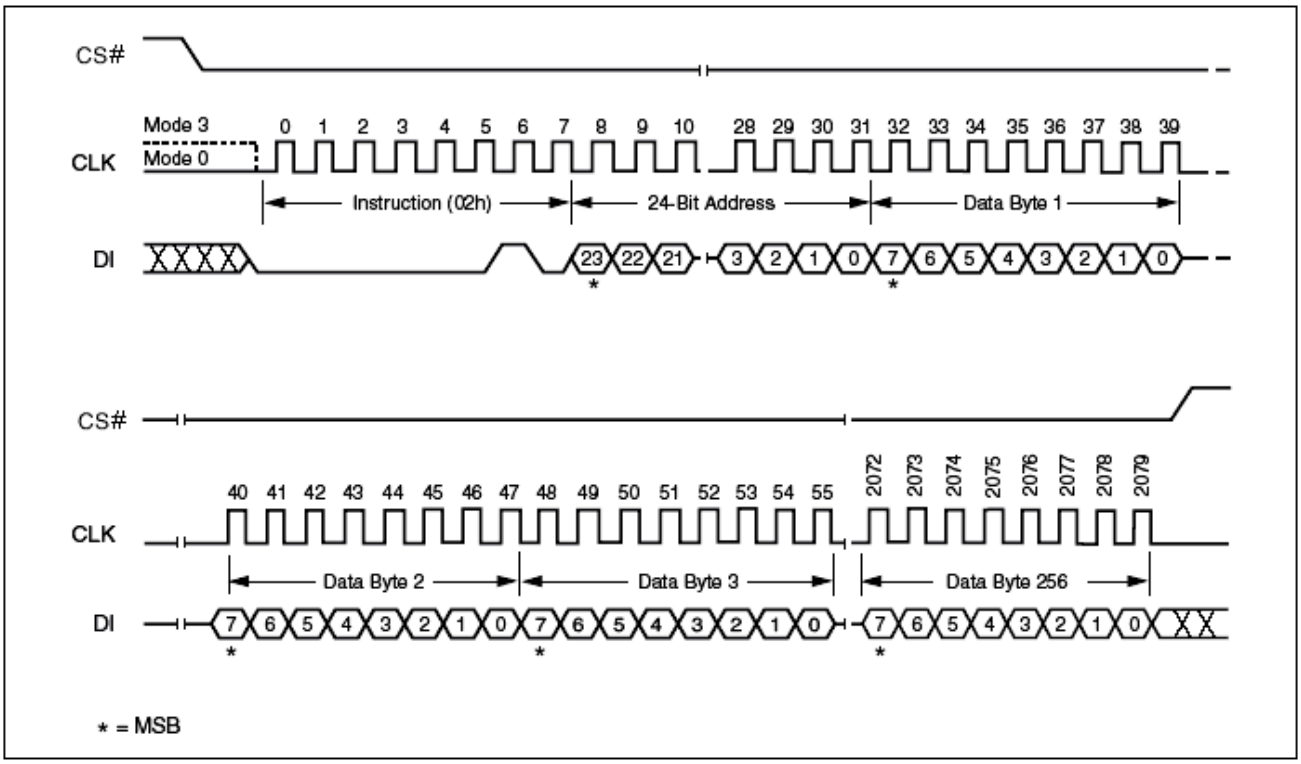


Figure 32. Page Program Instruction Sequence Diagram

Note: The above address cycles are base on 3-byte address mode, for 4-byte address mode, the address cycles will be increased.

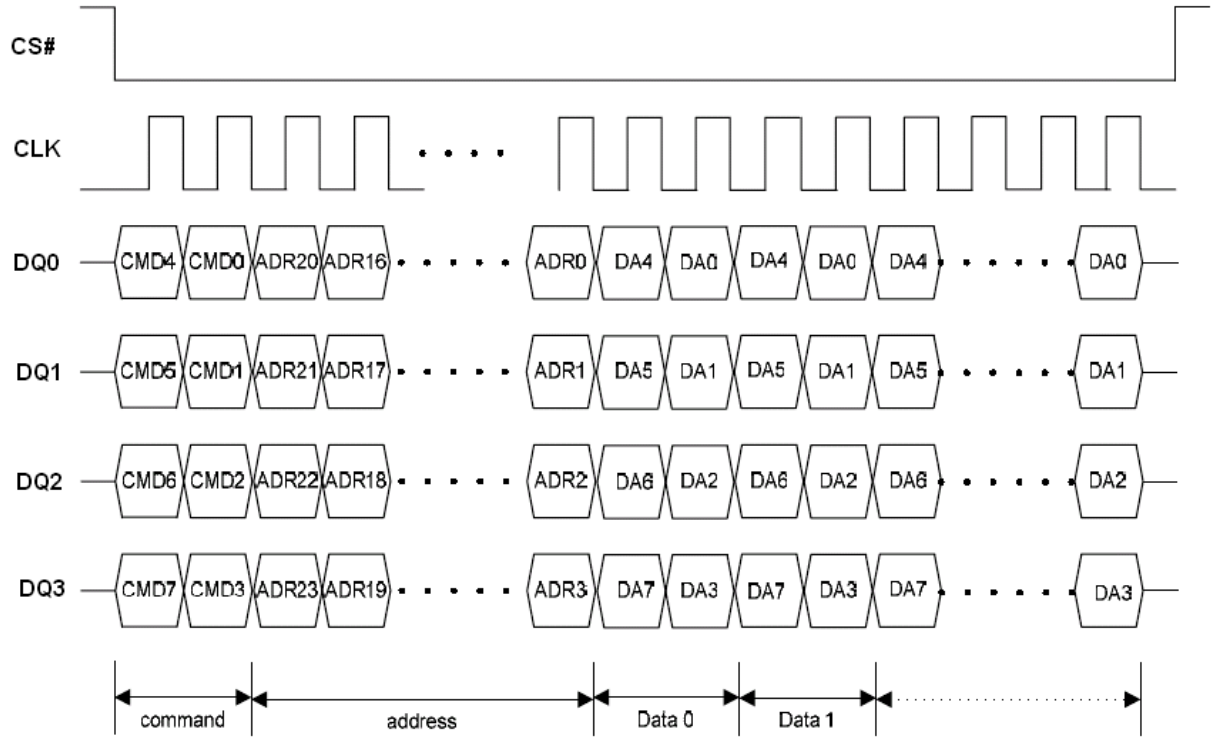


Figure 32.1 Program Instruction Sequence in QPI Mode

Note: The above address cycles are base on 3-byte address mode, for 4-byte address mode, the address cycles will be increased.

Page Program with 4byte address (12h)

The Page Program with 4byte address instruction allows bytes to be programmed in the memory. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Page Program with 4byte address instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code, **four** address bytes and at least one data byte on Serial Data Input (DI). If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). Chip Select (CS#) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in Figure 33. If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 Data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page.

Chip Select (CS#) must be driven High after the eighth bit of the last data byte has been latched in, otherwise the Page Program with 4byte address instruction is not executed.

As soon as Chip Select (CS#) is driven high, the self-timed Page Program with 4byte address cycle (whose duration is t_{PP}) is initiated. While the Page Program with 4byte address cycle is in progress, the

Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Page Program with 4byte address cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Page Program with 4byte address instruction applied to a page which is protected by the Block Protect (CMP, TB, BP3, BP2, BP1, BP0) bits (see Table 3) is not executed.

The instruction sequence is shown in Figure 33.1 while using the Enable Quad Peripheral Interface mode (EQPI) (38h) command.

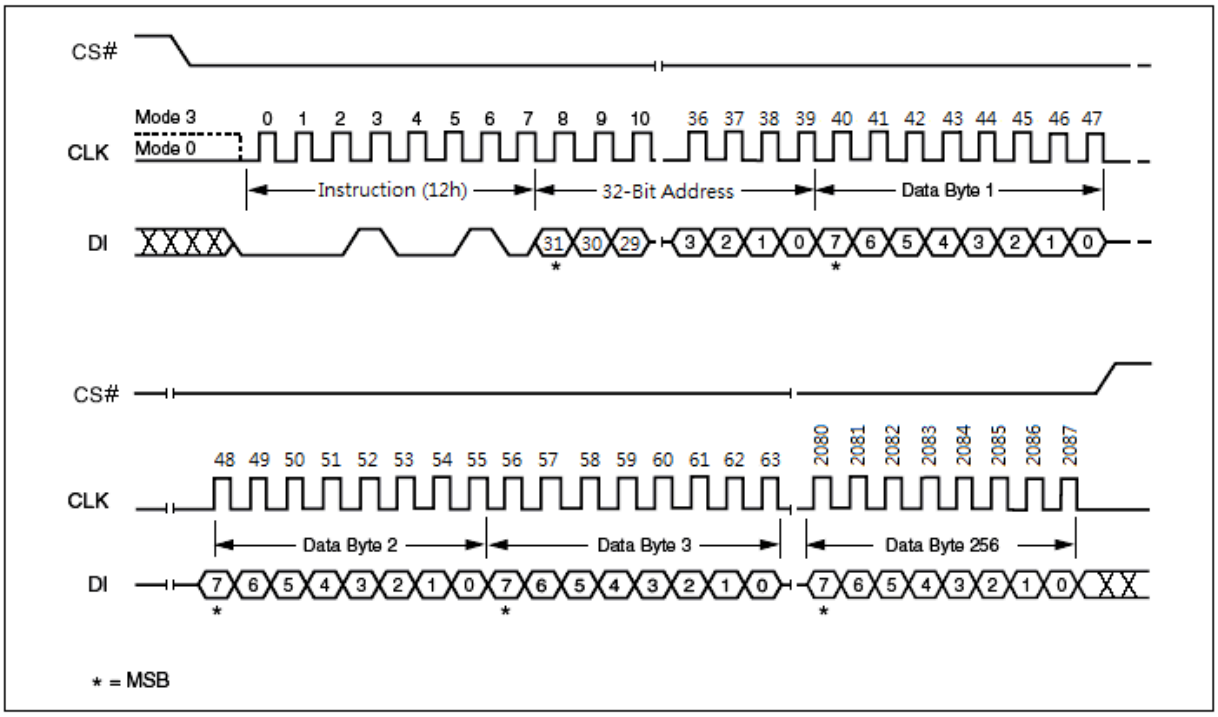


Figure 33. Page Program with 4byte address Instruction Sequence Diagram

Note: This instruction is workable while in 4byte address mode.

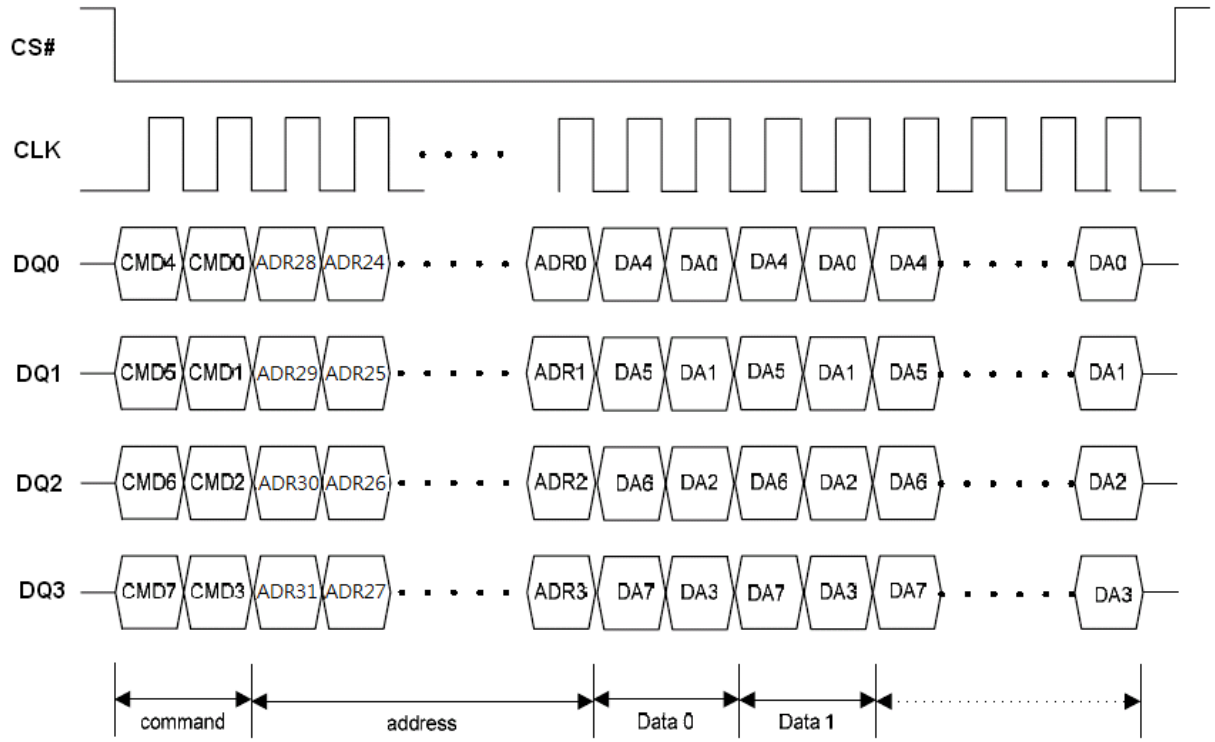


Figure 33.1 Program with 4byte address Instruction Sequence in QPI Mode

Note: This instruction is workable while in 4byte address mode.

Quad Input Page Program (QPP) (32h)

The Quad Page Program (QPP) instruction allows up to 256 bytes of data to be programmed at previously erased (FFh) memory locations using four pins: DQ0, DQ1, DQ2 and DQ3. The Quad Page Program can improve performance for PROM Programmer and applications that have slow clock speeds < 5MHz. Systems with faster clock speed will not realize much benefit for the Quad Page Program instruction since the inherent page program time is much greater than the time it take to clock-in the data. To access higher address (larger than 128Mb) in 3 byte address mode, user can issue Write Extended Register(C5h) operation before Quad Input Page Program(32h).

To use Quad Page Program (QPP) the WP#, HOLD#, RESET# Disable (WPDIS, HDDIS, RSEN) bits in Status Register4 must be set to 1, 1, 0. A Write Enable instruction must be executed before the device will accept the Quad Page Program (QPP) instruction (SR.1, WEL=1). The instruction is initiated by driving the CS# pin low then shifting the instruction code “32h” followed by a 24-bit address (A23-A0) or 32-bit address (A31-0) and at least one data byte, into the IO pins. The CS# pin must be held low for the entire length of the instruction while data is being sent to the device. All other functions of Quad Page Program (QPP) are identical to standard Page Program. The Quad Page Program (QPP) instruction sequence is shown in Figure 34.

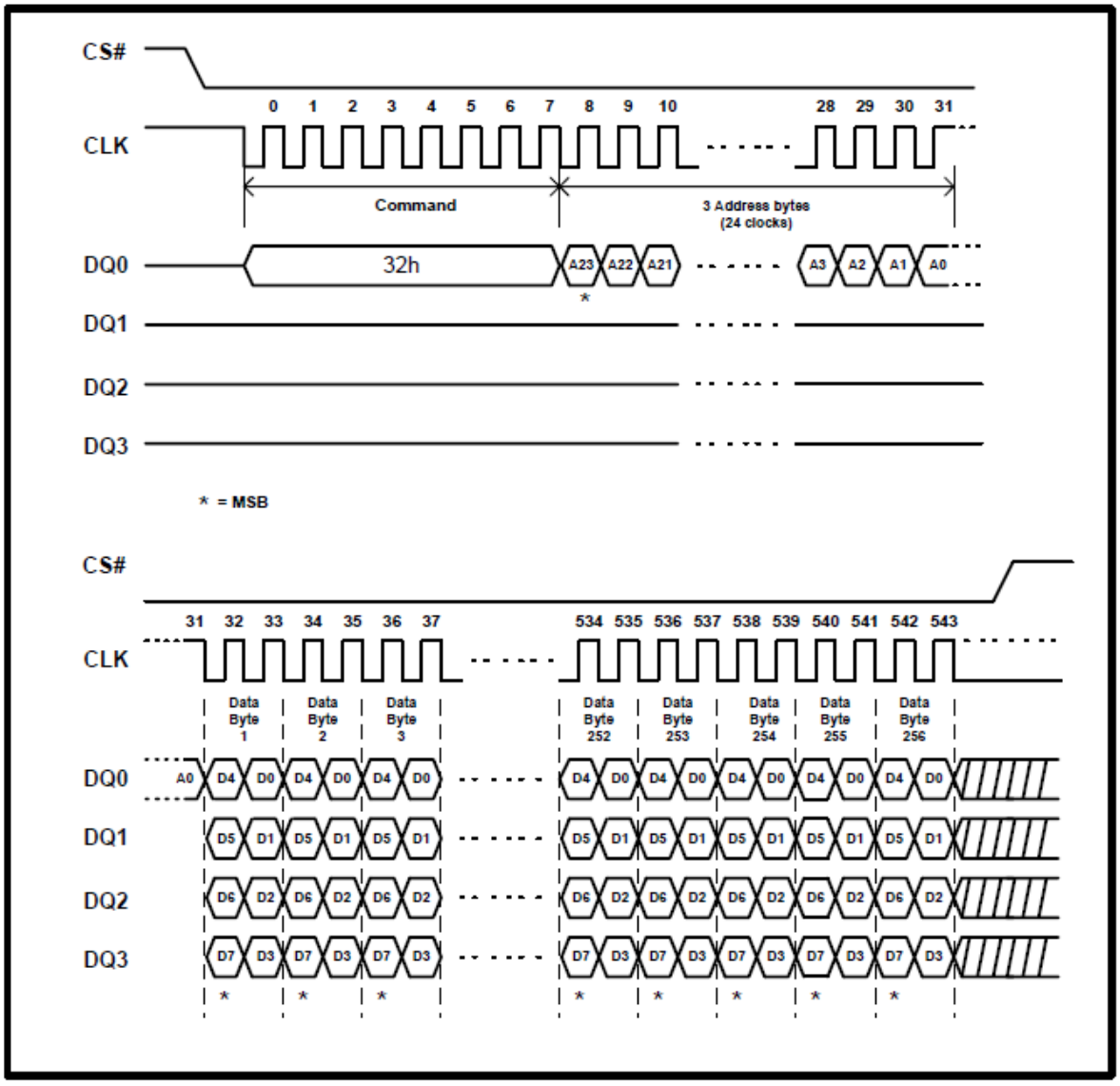


Figure 34. Quad Input Page Program Instruction Sequence Diagram (SPI Mode only)
Note: The above address cycles are base on 3-byte address mode, for 4-byte address mode, the address cycles will be increased.

Quad Input Page Program with 4byte address (34h)

The Quad Page Program with 4byte address instruction allows up to 256 bytes of data to be programmed at previously erased (FFh) memory locations using four pins: DQ0, DQ1, DQ2 and DQ3. The Quad Page Program with 4byte address can improve performance for PROM Programmer and applications that have slow clock speeds < 5MHz. Systems with faster clock speed will not realize much benefit for the Quad Page Program with 4byte address instruction since the inherent page program time is much greater than the time it take to clock- in the data.

To use Quad Page Program with 4byte address the WP#, HOLD# and RESET# Disable (WPDIS, HDDIS, RSEN) bits in Status Register4 must be set to 1, 1, 0. A Write Enable instruction must be executed before the device will accept the Quad Page Program with 4byte address instruction (SR.1, WEL=1). The instruction is initiated by driving the CS# pin low then shifting the instruction code “34h” followed by a 32-bit address (A31-A0) and at least one data byte, into the IO pins. The CS# pin must be held low for the entire length of the instruction while data is being sent to the device. All other functions of Quad Page Program with 4byte address are identical to standard Page Program with 4byte address. The Quad Page Program with 4byte address instruction sequence is shown in Figure 35.

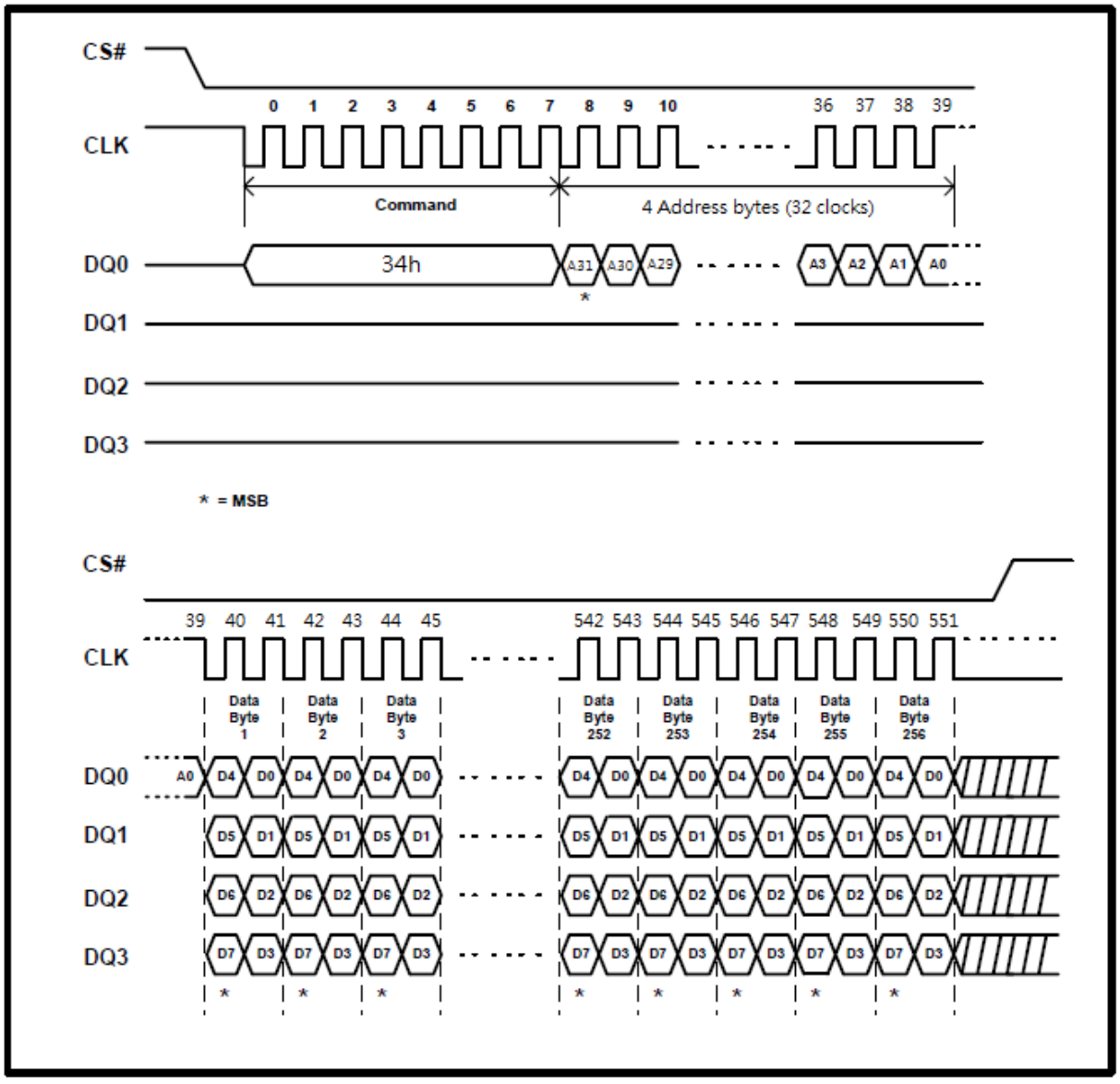


Figure 35. Quad Input Page Program with 4byte address Instruction Sequence Diagram (SPI Mode only)

Note: This instruction is workable while in 4byte address mode.

Sector Erase (SE) (20h)

The Sector Erase (SE) instruction sets to 1 (FFh) all bits inside the chosen sector. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Sector Erase (SE) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code, and three(or four, depends on modes state) address bytes on Serial Data Input (DI). Any address inside the Sector (see Table 2) is a valid address for the Sector Erase (SE) instruction. Chip Select (CS#) must be driven Low for the entire duration of the sequence. To access higher address (larger than 128Mb) in 3 byte address mode, user can issue Write Extended Register(C5h) operation before Sector Erase(20h).
The instruction sequence is shown in Figure 36. Chip Select (CS#) must be driven High after the eighth bit of the last address byte has been latched in, otherwise the Sector Erase (SE) instruction is not executed. As soon as Chip Select (CS#) is driven High, the self-timed Sector Erase cycle (whose duration is t_{SE}) is initiated. While the Sector Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Sector Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.
A Sector Erase (SE) instruction applied to a sector which is protected by the Block Protect (CMP, TB, BP3, BP2, BP1, BP0) bits (see Table 3) or Boot Lock feature will be ignored.

The instruction sequence is shown in Figure 38.1 while using the Enable Quad Peripheral Interface mode (EQPI) (38h) command.

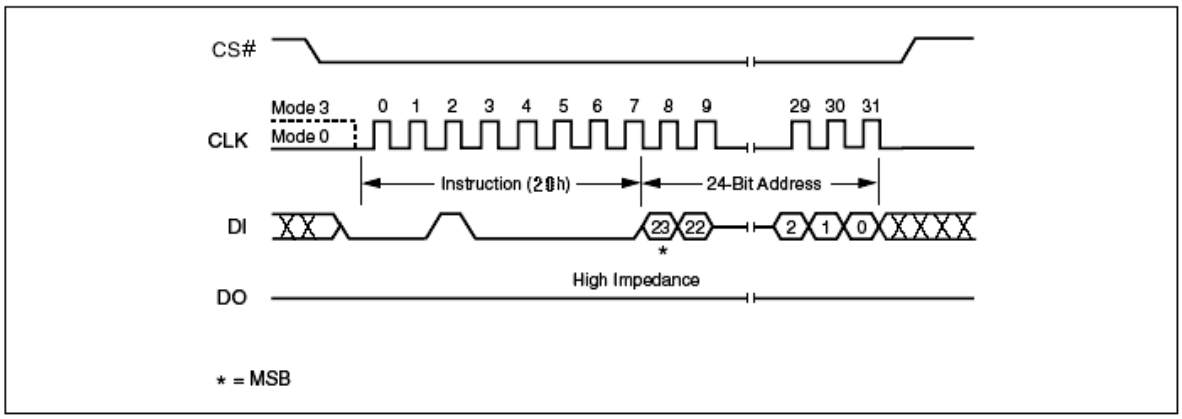


Figure 36. Sector Erase Instruction Sequence Diagram

Note: The above address cycles are base on 3-byte address mode, for 4-byte address mode, the address cycles will be increased.

32KB Half Block Erase (HBE) (52h)

The Half Block Erase (HBE) instruction sets to 1 (FFh) all bits inside the chosen block. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Half Block Erase (HBE) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code, and three(or four, depends on mode state) address bytes on Serial Data Input (DI). Any address inside the Block (see Table 2) is a valid address for the Half Block Erase (HBE) instruction. Chip Select (CS#) must be driven Low for the entire duration of the sequence. To access higher address (larger than 128Mb) in 3 byte address mode, user can issue Write Extended Register(C5h) operation before 32KB Half Block Erase(52h).

The instruction sequence is shown in Figure 37. Chip Select (CS#) must be driven High after the eighth bit of the last address byte has been latched in, otherwise the Half Block Erase (HBE) instruction is not executed. As soon as Chip Select (CS#) is driven High, the self-timed Block Erase cycle (whose duration is t_{HBE}) is initiated. While the Half Block Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Half Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Half Block Erase (HBE) instruction applied to a block which is protected by the Block Protect (CMP, TB, BP3, BP2, BP1, BP0) bits (see Table 3) or Boot Lock feature will be ignored.

The instruction sequence is shown in Figure 38.1 while using the Enable Quad Peripheral Interface mode (EQPI) (38h) command.

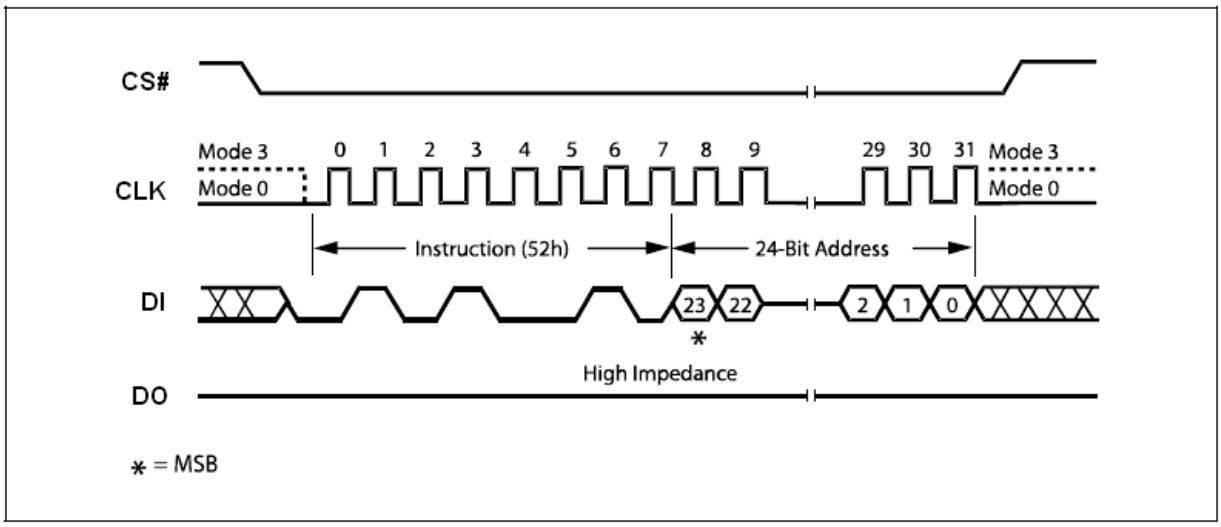


Figure 37. 32KB Half Block Erase Instruction Sequence Diagram

Note: The above address cycles are base on 3-byte address mode, for 4-byte address mode, the address cycles will be increased.

64KB Block Erase (BE) (D8h)

The Block Erase (BE) instruction sets to 1 (FFh) all bits inside the chosen block. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Block Erase (BE) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code, and three (or four, depends on mode state) address bytes on Serial Data Input (DI). Any address inside the Block (see Table 2) is a valid address for the Block Erase (BE) instruction. Chip Select (CS#) must be driven Low for the entire duration of the sequence. To access higher address (larger than 128Mb) in 3 byte address mode, user can issue Write Extended Register(C5h) operation before 64KB Block Erase(D8h).
The instruction sequence is shown in Figure 38. Chip Select (CS#) must be driven High after the eighth bit of the last address byte has been latched in, otherwise the Block Erase (BE) instruction is not executed. As soon as Chip Select (CS#) is driven High, the self-timed Block Erase cycle (whose duration is t_{BE}) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Block Erase (BE) instruction applied to a block which is protected by the Block Protect (CMP, TB, BP3, BP2, BP1, BP0) bits (see Table 3) or Boot Lock feature is not executed.

The instruction sequence is shown in Figure 38.1 while using the Enable Quad Peripheral Interface mode (EQPI) (38h) command.

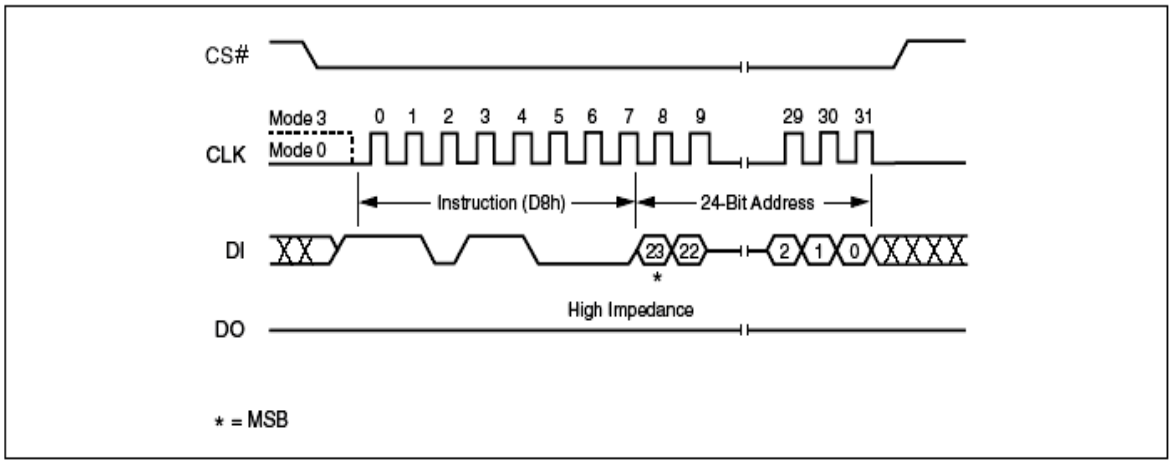


Figure 38. 64KB Block Erase Instruction Sequence Diagram

Note: The above address cycles are base on 3-byte address mode, for 4-byte address mode, the address cycles will be increased.

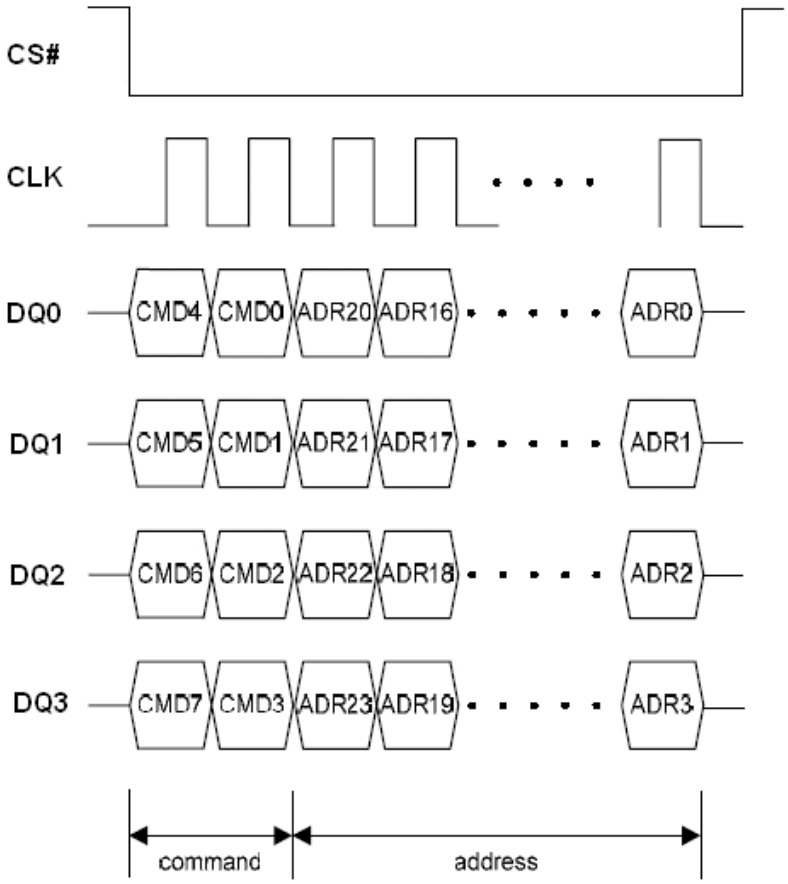


Figure 38.1 Block/Sector Erase Instruction Sequence in QPI Mode

Note: The above address cycles are base on 3-byte address mode, for 4-byte address mode, the address cycles will be increased.

Chip Erase (CE) (C7h/60h)

The Chip Erase (CE) instruction sets all bits to 1 (FFh). Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Chip Erase (CE) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code on Serial Data Input (DI). Chip Select (CS#) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in Figure 39. Chip Select (CS#) must be driven High after the eighth bit of the instruction code has been latched in, otherwise the Chip Erase instruction is not executed. As soon as Chip Select (CS#) is driven High, the self-timed Chip Erase cycle (whose duration is t_{CE}) is initiated. While the Chip Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Chip Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

The Chip Erase (CE) instruction is ignored if one or more blocks are protected.

The instruction sequence is shown in Figure 39.1 while using the Enable Quad Peripheral Interface mode (EQPI) (38h) command.

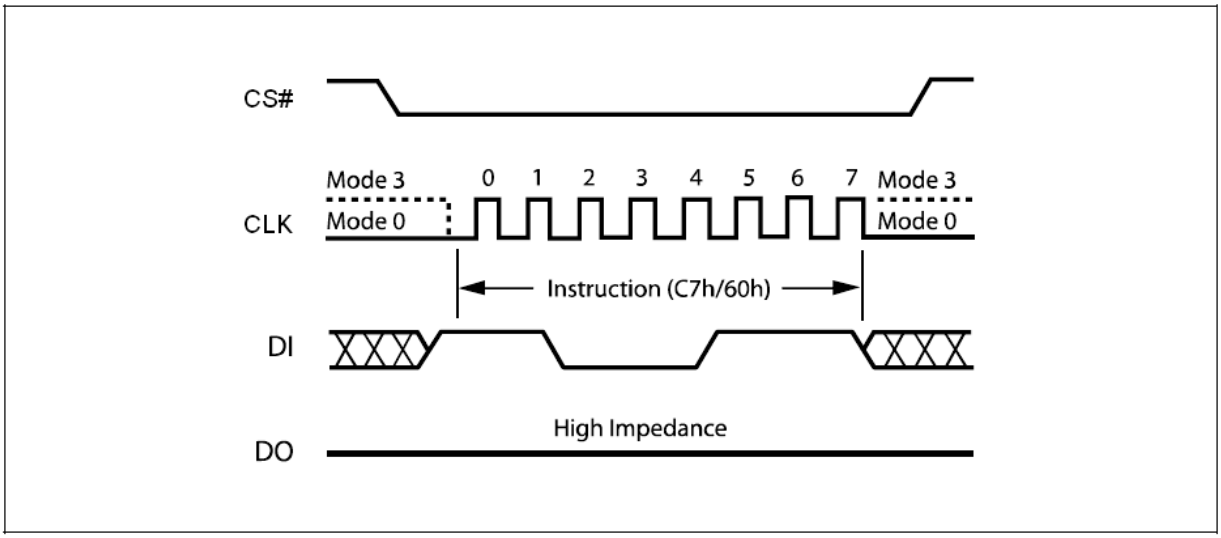


Figure 39. Chip Erase Instruction Sequence Diagram

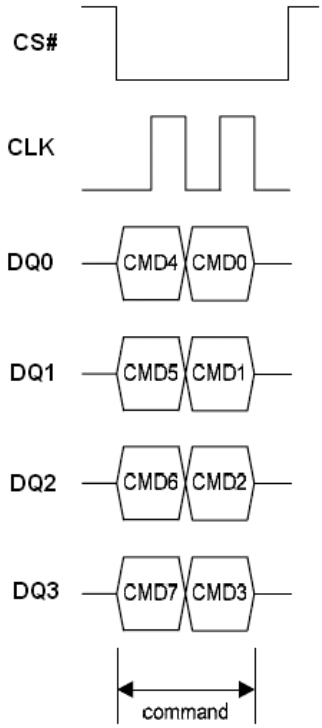


Figure 39.1 Chip Erase Sequence under EQPI Mode

Enter 4-Byte Address Modes (B7h)

The enter 4byte address mode instruction enables accessing the address length of 32-bit for the memory area of higher density (larger than 128Mb). The device default is in 24-bit address mode; after sending out the enter 4byte address mode instruction, the 4byte bit of Status Register 2 will be automatically set to "1" to indicate the 4-byte address mode has been enabled. Once the 4-byte address mode is enabled, the address length becomes 32-bit instead of the default 24-bit. There is a method to exit the 4-byte mode: writing exit 4-byte mode instruction. All instructions are accepted normally, and just the address bit is changed from 24-bit to 32-bit.

The sequence of issuing enter 4byte address mode instruction is: CS# goes low → sending enter 4byte address mode instruction to enter 4-byte mode(automatically set 4byte bit as "1") → CS# goes high. (Figure 40 for SPI mode, and Figure 40.1 for EQPI mode)

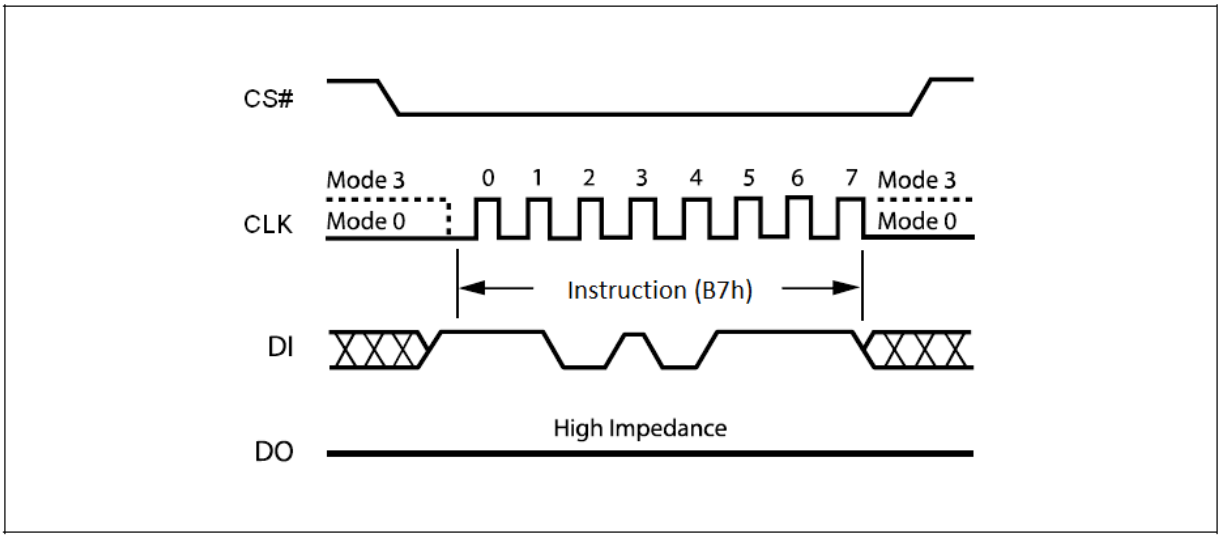


Figure 40. Enter 4byte address mode Instruction Sequence Diagram

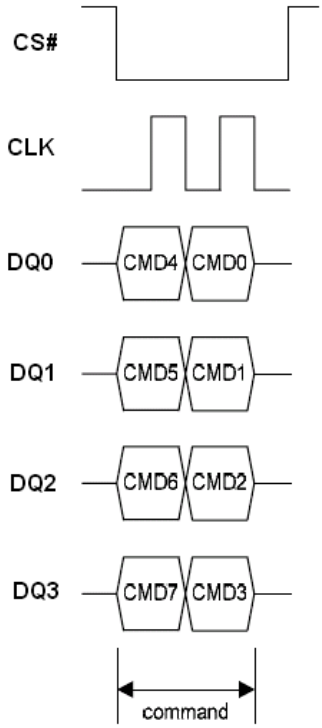


Figure 40.1 Enter 4byte address mode Sequence under EQPI Mode

Exit 4-Byte Address Modes (E9h)

The Exit 4byte address mode instruction is executed to exit the 4-byte address mode and return to the default 3-bytes address mode. After sending out the exit 4byte address mode instruction, the 4byte bit of Status Register 2 will be cleared to be "0" to indicate the exit of the 4-byte address mode. Once exiting the 4-byte address mode, the address length will return to 24-bit.

The sequence of issuing Exit 4-Byte Address Modes instruction is: CS# goes low → sending exit 4byte address mode instruction to exit 4-byte mode (automatically clear the 4BYTE bit to be "0") → CS# goes high. (Figure 41 for SPI mode, and Figure 41.1 for EQPI mode)

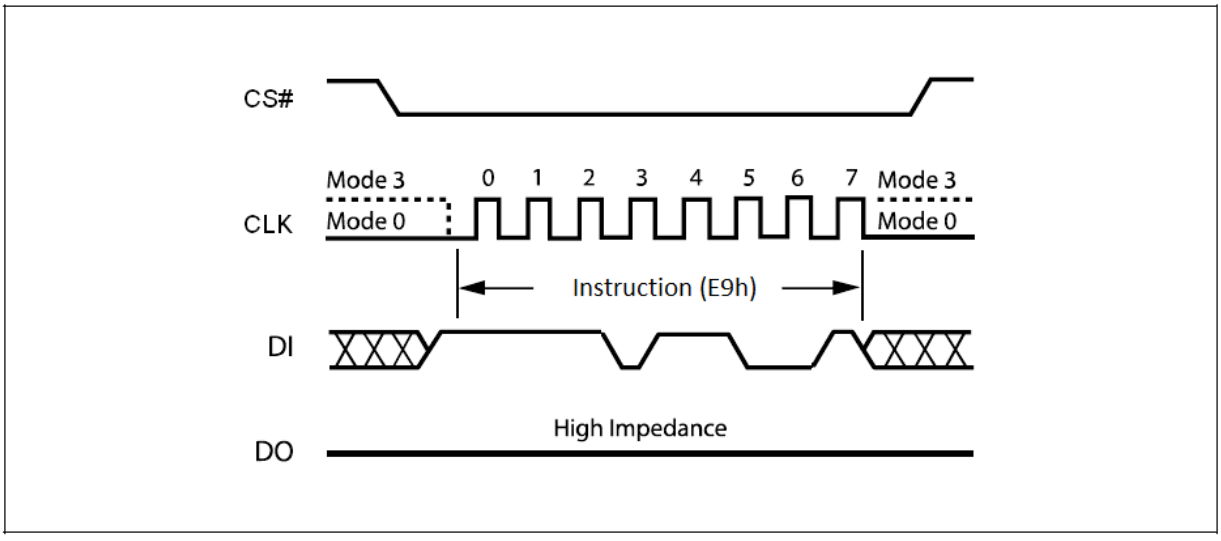


Figure 41. Exit 4byte address mode Instruction Sequence Diagram

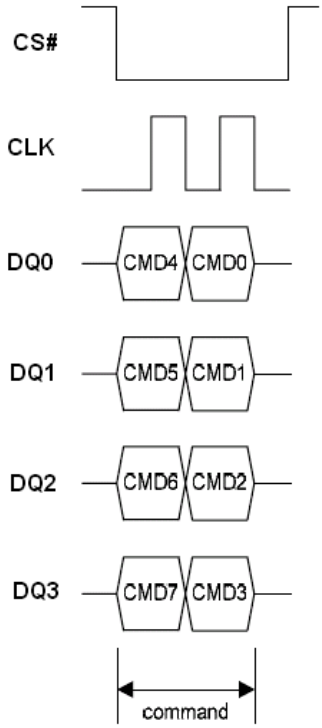


Figure 41.1 Exit 4byte address mode Sequence under EQPI Mode

Read Extended Address Register (C8h)

When the device is in the 3-Byte Address Mode, the Extended Address Register is used as the 4th address byte A[31:24] to access memory regions beyond 128Mb. The Read Extended Address Register instruction is entered by driving CS# low and shifting the instruction code "C8h" into the DI pin on the rising edge of CLK. The Extended Address Register bits are then shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first as shown in Figure 42.

When the device is in the 4byte address Mode, the Extended Address Register is not used.

Table 10. 1 Extended Register Bit Locations

ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0
A31	A30	A29	A28	A27	A26	A25	A24
Volatile bit	Volatile bit	Volatile bit	Volatile bit	Volatile bit	Volatile bit	Volatile bit	Volatile bit

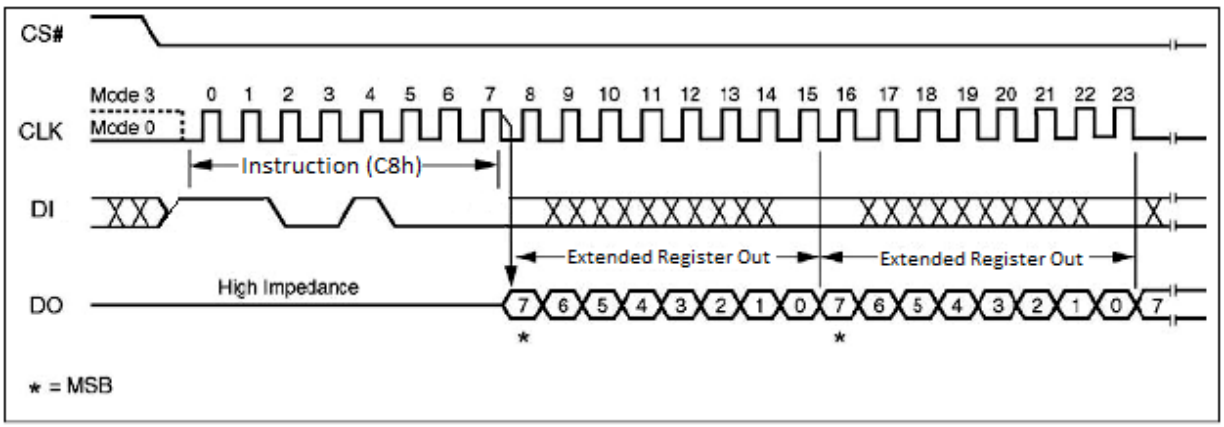


Figure 42. Read Extended Address Register Instruction Sequence Diagram

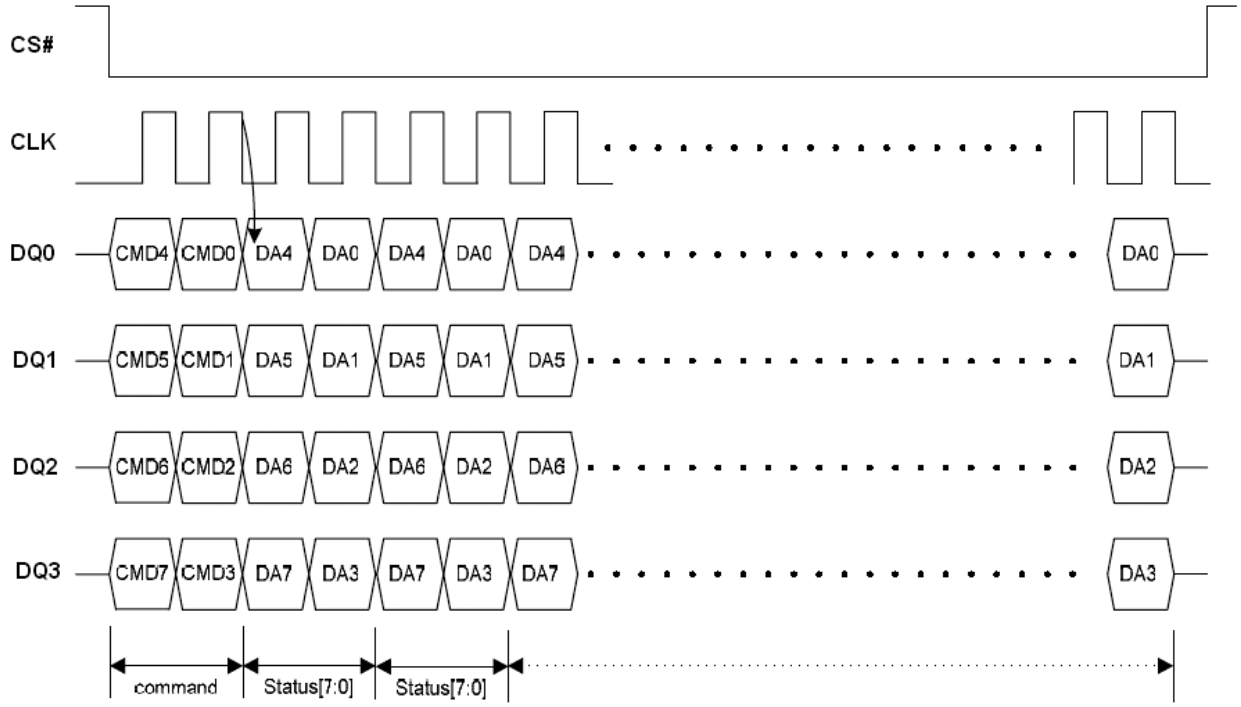


Figure 42.1 Read Extended Address Register Instruction Sequence under QPI Mode

Write Extended Address Register (C5h)

The Extended Address Register is a volatile register that stores the 4th byte address (A31-A24) when the device is operating in the 3-Byte Address Mode. To write the Extended Address Register bits, a Write Enable (06h) instruction must previously have been executed for the device to accept the Write Extended Address Register instruction (Status Register bit WEL must equal 1). Once write enabled, the instruction is entered by driving CS# low, sending the instruction code "C5h", and then writing the Extended Address Register data byte as illustrated in Figure 43 and Figure 43.1.

Upon power up or the execution of a Software or Hardware Reset, the Extended Address Register bit values will be cleared to 0.

The Extended Address Register is only effective when the device is in the 3-Byte Address Mode. When the device operates in the 4byte address mode, any command with address input of A31-A24 will replace the Extended Address Register values. It is recommended to check and update the Extended Address Register if necessary when the device is switched from 4byte to 3byte address mode.

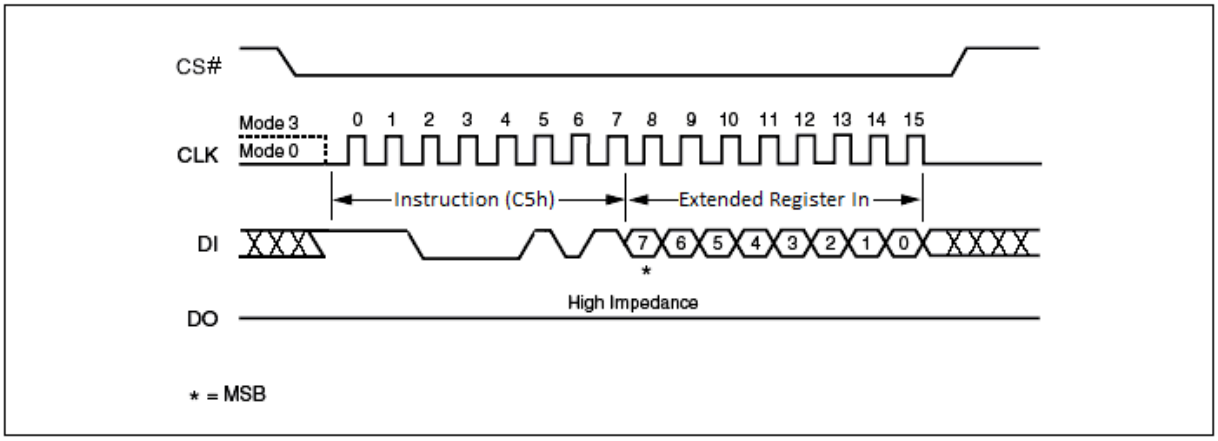


Figure 43. Write Extended Register Instruction Sequence Diagram

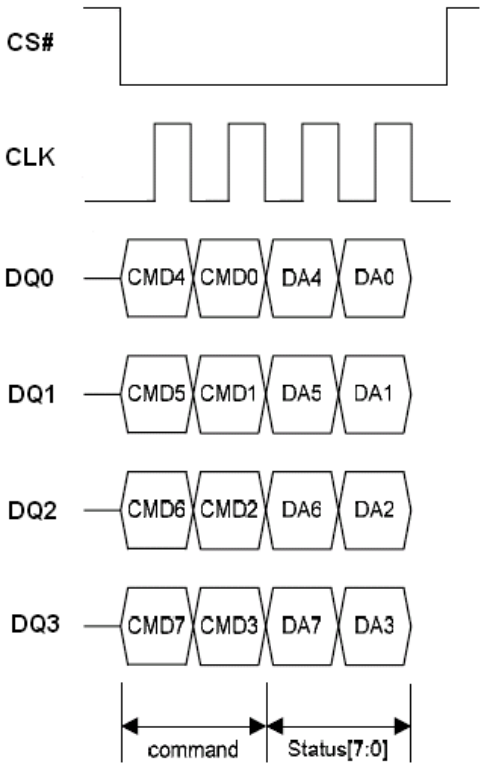


Figure 43.1 Write Extended Register Instruction Sequence in QPI Mode

Deep Power-down (DP) (B9h)

Executing the Deep Power-down (DP) instruction is the only way to put the device in the lowest consumption mode (the Deep Power-down mode). It can also be used as an extra software protection mechanism, while the device is not in active use, since in this mode, the device ignores all Write, Program and Erase instructions.

Driving Chip Select (CS#) High deselects the device, and puts the device in the Standby mode (if there is no internal cycle currently in progress). But this mode is not the Deep Power-down mode. The Deep Power-down mode can only be entered by executing the Deep Power-down (DP) instruction, to reduce the standby current (from I_{CC1} to I_{CC2}, as specified in Table 16.)

Once the device has entered the Deep Power-down mode, all instructions are ignored except the Release from Deep Power-down, Read Device ID (RDI) and Software Reset instruction which release the device from this mode. The Release from Deep Power-down and Read Device ID (RDI) instruction also allows the Device ID of the device to be output on Serial Data Output (DO).

The Deep Power-down mode automatically stops at Power-down, and the device always Powers-up in the Standby mode. The Deep Power-down (DP) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code on Serial Data Input (DI). Chip Select (CS#) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in Figure 44. Chip Select (CS#) must be driven High after the eighth bit of the instruction code has been latched in, otherwise the Deep Power-down (DP) instruction is not executed. As soon as Chip Select (CS#) is driven High, it requires a delay of t_{DP} before the supply current is reduced to I_{CC2} and the Deep Power-down mode is entered.

Any Deep Power-down (DP) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

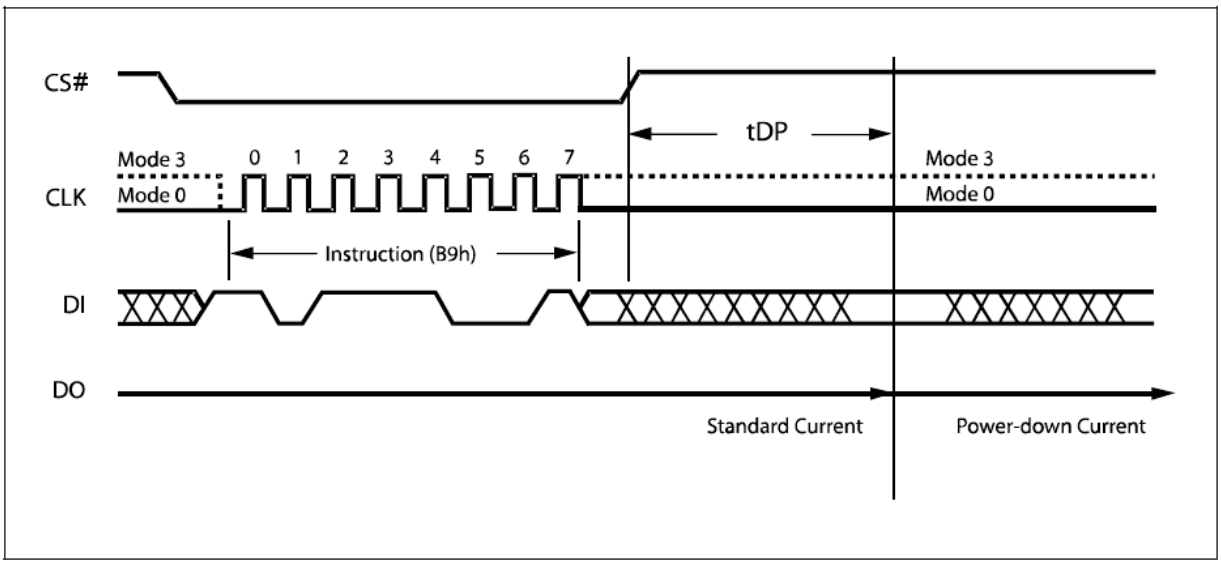


Figure 44. Deep Power-down Instruction Sequence Diagram

Release from Deep Power-down and Read Device ID (RDI)

Once the device has entered the Deep Power-down mode, all instructions are ignored except the Release from Deep Power-down and Read Device ID (RDI) instruction. Executing this instruction takes the device out of the Deep Power-down mode.

Please note that this is not the same as, or even a subset of, the JEDEC 16-bit Electronic Signature that is read by the Read Identifier (RDID) instruction. The old-style Electronic Signature is supported for reasons of backward compatibility, only, and should not be used for new designs. New designs should, instead, make use of the JEDEC 16-bit Electronic Signature, and the Read Identifier (RDID) instruction.

When used only to release the device from the power-down state, the instruction is issued by driving the CS# pin low, shifting the instruction code "ABh" and driving CS# high as shown in Figure 45. After the time duration of t_{RES1} (See AC Characteristics) the device will resume normal operation and other instructions will be accepted. The CS# pin must remain high during the t_{RES1} time duration.

When used only to obtain the Device ID while not in the power-down state, the instruction is initiated by driving the CS# pin low and shifting the instruction code "ABh" followed by 3-dummy bytes. The Device ID bits are then shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 46. The Device ID value for the DEVICE is listed in Table 5. The Device ID can be read continuously. The instruction is completed by driving CS# high.

When Chip Select (CS#) is driven High, the device is put in the Stand-by Power mode. If the device was not previously in the Deep Power-down mode, the transition to the Stand-by Power mode is immediate. If the device was previously in the Deep Power-down mode, though, the transition to the Standby Power mode is delayed by t_{RES2}, and Chip Select (CS#) must remain High for at least t_{RES2} (max), as specified in Table 18. Once in the Stand-by Power mode, the device waits to be selected, so that it can receive, decode and execute instructions.

Except while an Erase, Program or Write Status Register cycle is in progress, the Release from Deep Power-down and Read Device ID (RDI) instruction always provides access to the 8bit Device ID of the device , and can be applied even if the Deep Power-down mode has not been entered.

Any Release from Deep Power-down and Read Device ID (RDI) instruction while an Erase, Program or Write Status Register cycle is in progress, is not decoded, and has no effect on the cycle that is in progress.

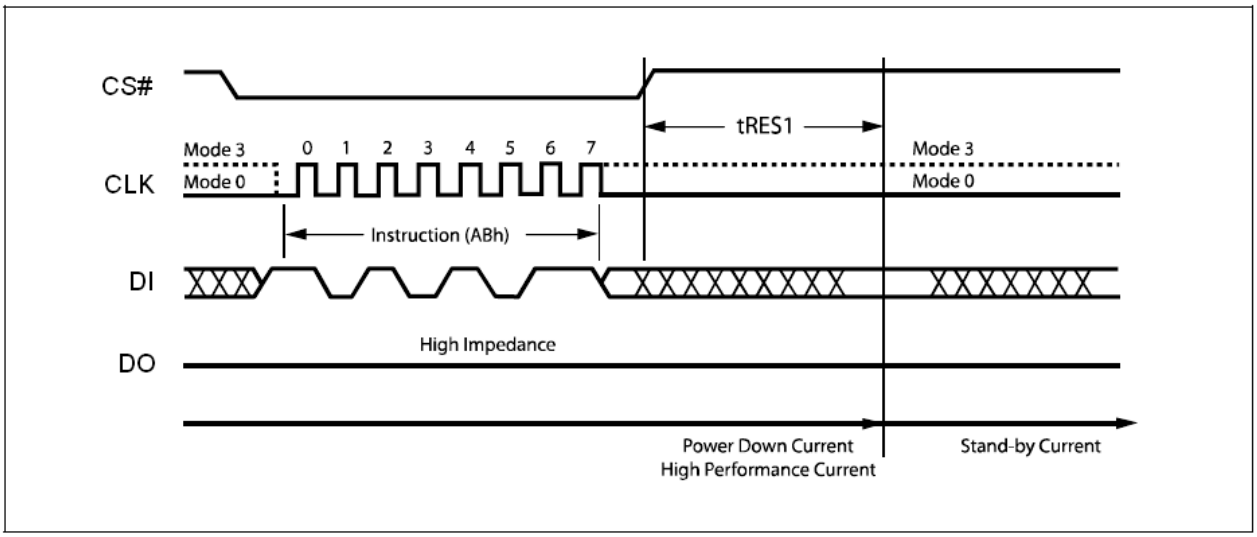


Figure 45. Release Power-down Instruction Sequence Diagram

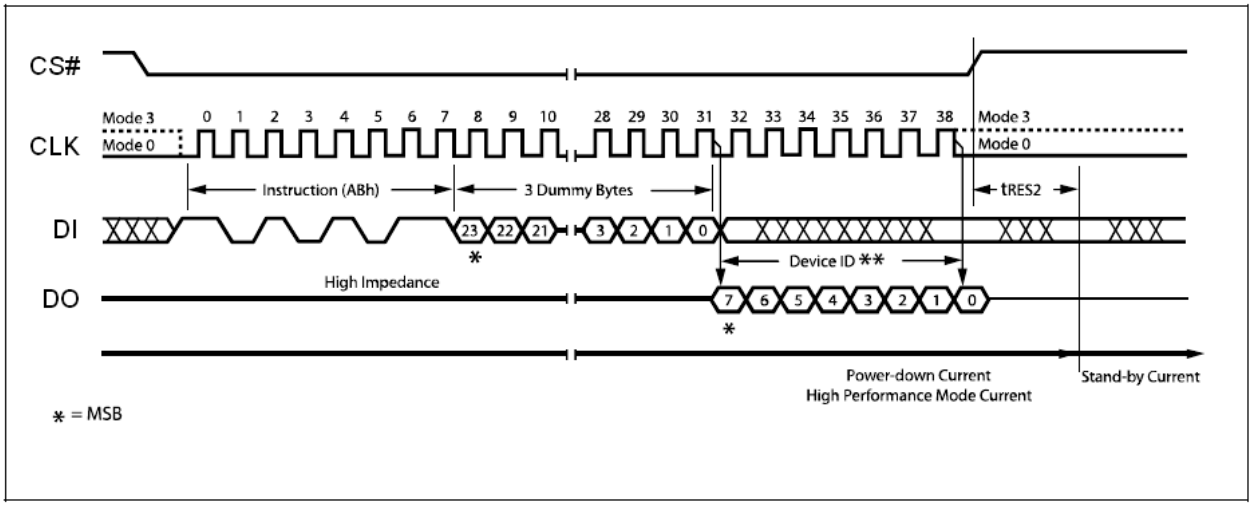


Figure 46. Release Power-down / Device ID Instruction Sequence Diagram

Read Manufacturer / Device ID (90h)

The Read Manufacturer/Device ID instruction is an alternative to the Release from Power-down / Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID.
The Read Manufacturer/Device ID instruction is very similar to the Release from Power-down / Device ID instruction. The instruction is initiated by driving the CS# pin low and shifting the instruction code "90h" followed by a 24-bit address (A23-A0) of 000000h. After which, the Manufacturer ID for Eon (1Ch) and the Device ID are shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 47. The Device ID values for the DEVICE are listed in Table 5. If the 24-bit address is initially set to 000001h the Device ID will be read first

The instruction sequence is shown in Figure 47.1 while using the Enable Quad Peripheral Interface mode (EQPI) (38h) command.

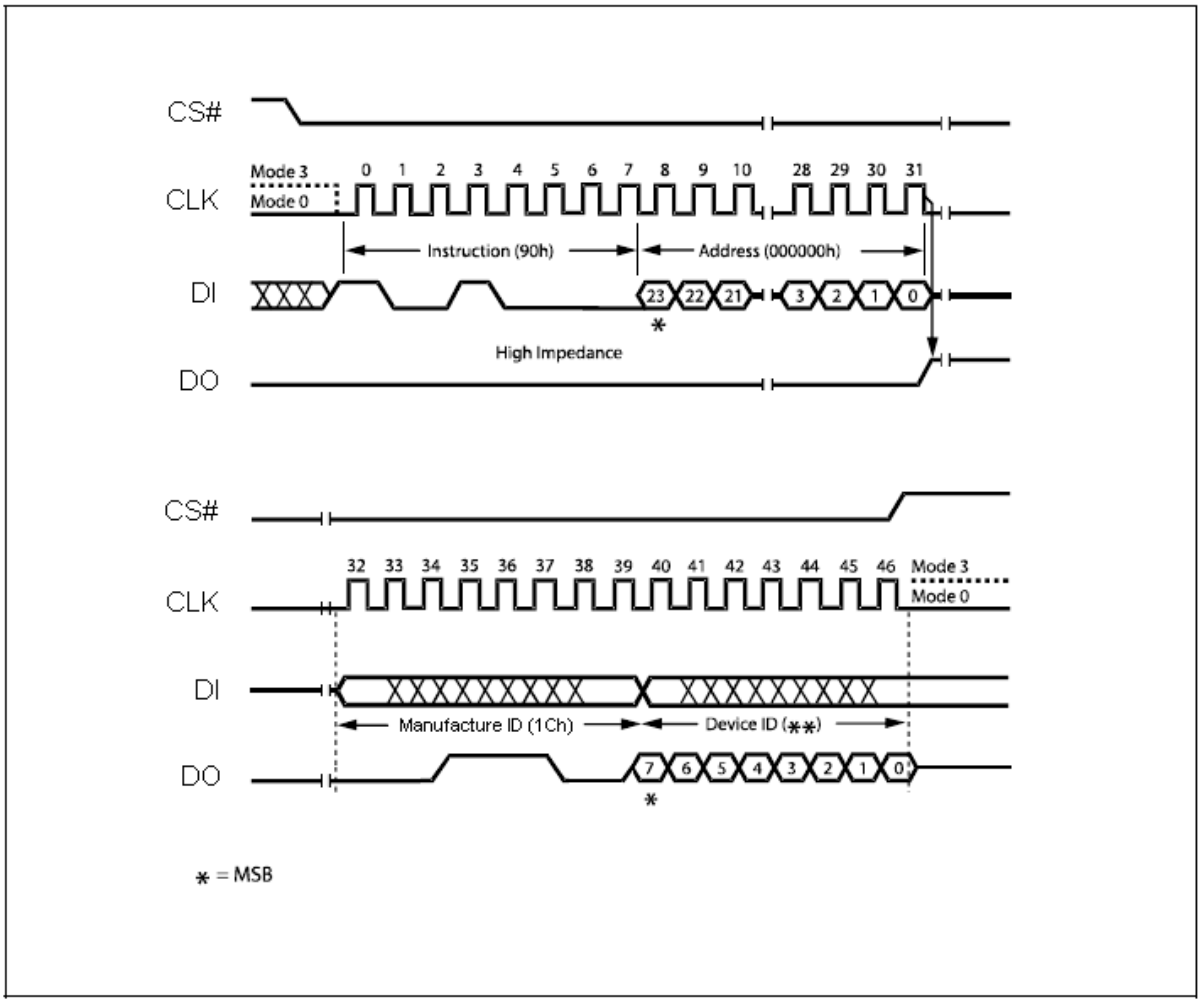


Figure 47. Read Manufacturer / Device ID Diagram

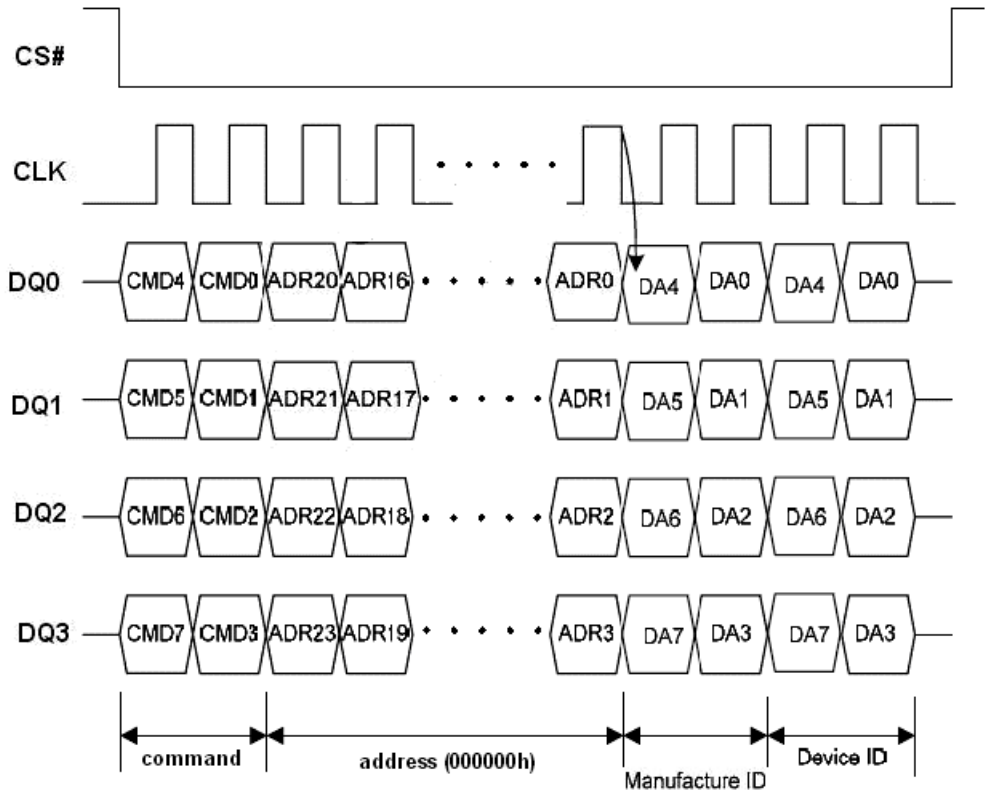


Figure 47.1 Read Manufacturer / Device ID Diagram in QPI Mode

Read Identification (RDID) (9Fh)

The Read Identification (RDID) instruction allows the 8-bit manufacturer identification to be read, followed by two bytes of device identification. The device identification indicates the memory type in the first byte, and the memory capacity of the device in the second byte.

Any Read Identification (RDID) instruction while an Erase or Program cycle is in progress, is not decoded, and has no effect on the cycle that is in progress. The Read Identification (RDID) instruction should not be issued while the device is in Deep Power down mode.

The device is first selected by driving Chip Select Low. Then, the 8-bit instruction code for the instruction is shifted in. This is followed by the 24-bit device identification, stored in the memory, being shifted out on Serial Data Output, each bit being shifted out during the falling edge of Serial Clock. The instruction sequence is shown in Figure 48. The Read Identification (RDID) instruction is terminated by driving Chip Select High at any time during data output.
When Chip Select is driven High, the device is put in the Standby Power mode. Once in the Standby Power mode, the device waits to be selected, so that it can receive, decode and execute instructions.

The instruction sequence is shown in Figure 48.1 while using the Enable Quad Peripheral Interface mode (EQPI) (38h) command.

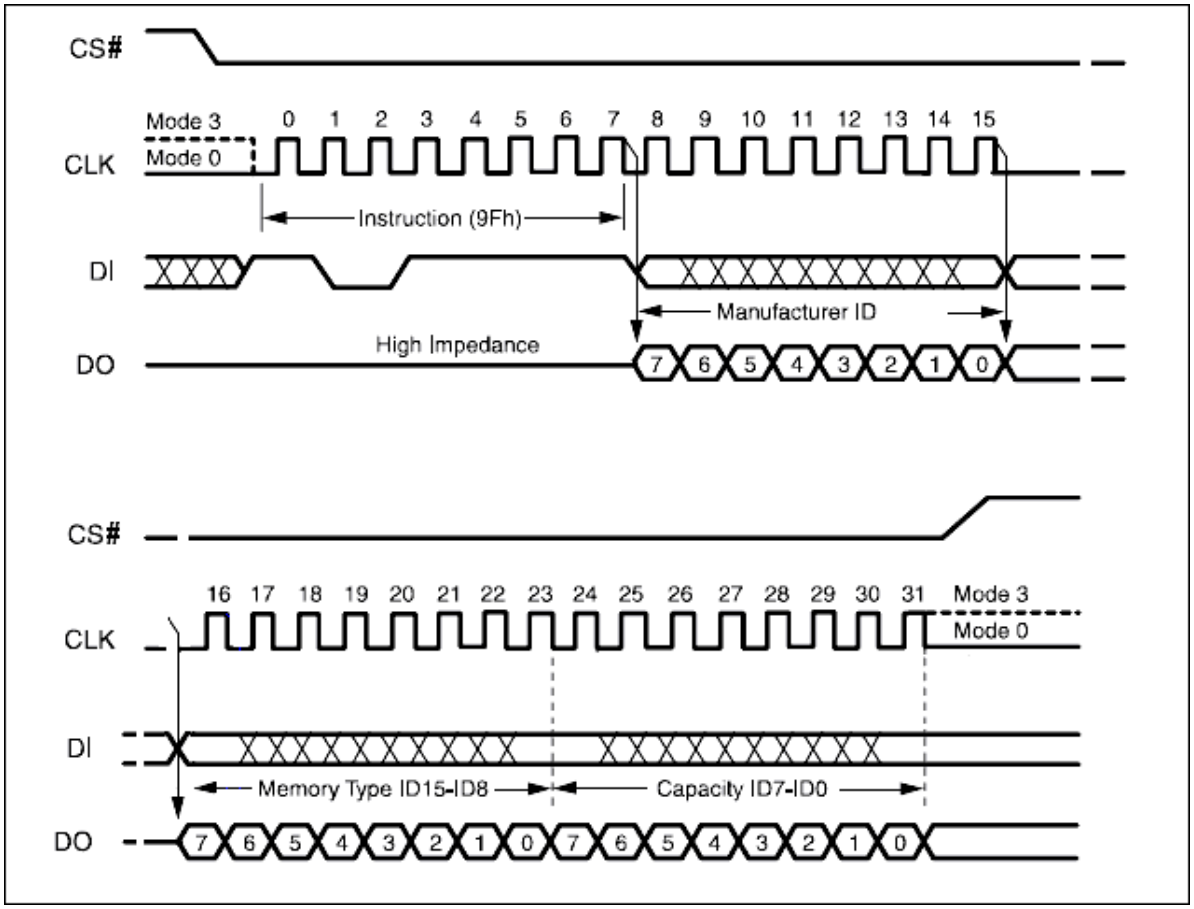


Figure 48. Read Identification (RDID)

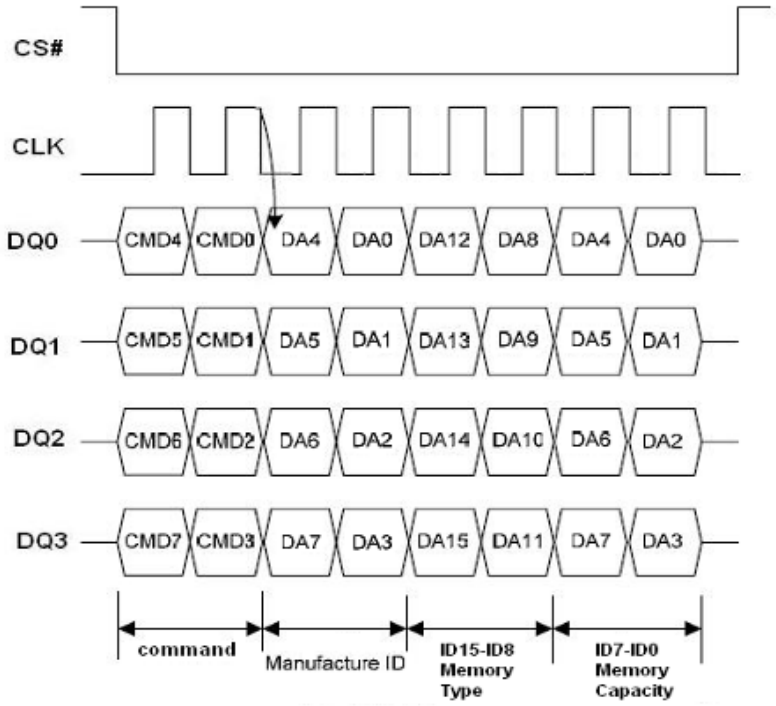


Figure 48.1 Read Identification (RDID) in QPI Mode

Enter OTP Mode (3Ah)

This Flash support OTP mode to enhance the data protection, user can use the Enter OTP mode (3Ah) command for entering this mode. In OTP mode, the Status Register SR7 bit is served as SPL0 bit, SR2 bit is served as SPL1 bit, SR1 bit is served as SPL2 bit and SR0 bit is served as WIP bit. They can be read by RDSR command.

This Flash has 3 x 512 bytes OTP sector, user must issue ENTER OTP MODE command to read, program or erase OTP sector. After entering OTP mode, the OTP sector is mapping to sector 8191~8189, **SRP bit** becomes SPL0 bit, **BP0 bit** becomes SPL1 bit and **WEL bit** becomes SPL2 bit,. The Chip Erase, Block Erase and Half Block Erase commands are also disabled.

In OTP mode, user can read other sectors, but program / Sector Erase (20h) other sectors only allowed when they are not protected by Block Protect (CMP, TB, BP3, BP2, BP1, BP0) bits and Block Lock feature. The OTP sector can ***only*** be erased by Sector Erase (20h/21h) command. The Chip Erase (C7h/ 60h), 64K Block Erase (D8h/DCh) and 32K Half Block Erase (52h/5Ch) commands are disable in OTP mode.

Table 12. OTP Sector Address

Lock bit	Sector	Sector Size	Address Range
SPL0	8191	512 byte	1FFF000h –1FFF1FFh
SPL1	8190	512 byte	1FFE000h – 1FFE1FFh
SPL2	8189	512 byte	1FFD000h – 1FFD1FFh

Note: The OTP sector is mapping to sector 8189~8191.

WRSR command is used to program SPL0 bit, SPL1 bit and SPL2 bit to '1', but these bits only can be programmed once. User can use WRDI (04h) command to exit OTP mode.

The instruction sequence is shown in Figure 49.1 while using the Enable Quad Peripheral Interface mode (EQPI) (38h) command.

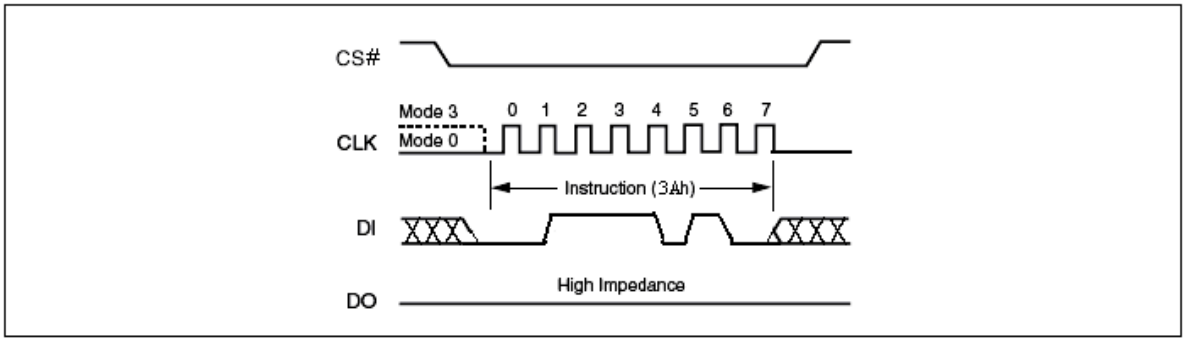


Figure 49. Enter OTP Mode

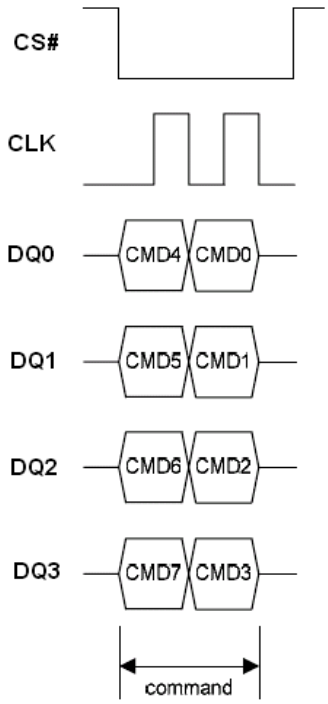


Figure 49.1 Enter OTP Mode Sequence in QPI Mode

Read SFDP Mode and Unique ID Number (5Ah)

Read SFDP mode

DEVICE features Serial Flash Discoverable Parameters (SFDP) mode. Host system can retrieve the operating characteristics, structure and vendor specified information such as identifying information, memory size, operating voltage and timing information of this device by SFDP mode.
The device is first selected by driving Chip Select (CS#) Low. The instruction code for the Read SFDP Mode is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of Serial Clock (CLK). Then the memory contents, at that address, is shifted out on Serial Data Output (DO), each bit being shifted out, at a maximum frequency F_R, during the falling edge of Serial Clock (CLK).
The instruction sequence is shown in Figure 50. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Serial Flash Discoverable Parameters (SFDP) instruction. When the highest address is reached, the address counter rolls over to 0x00h, allowing the read sequence to be continued indefinitely. The Serial Flash Discoverable Parameters (SFDP) instruction is terminated by driving Chip Select (CS#) High. Chip Select (CS#) can be driven High at any time during data output. Any Read Data Bytes at Serial Flash Discoverable Parameters (SFDP) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

The SFDP version is 216B

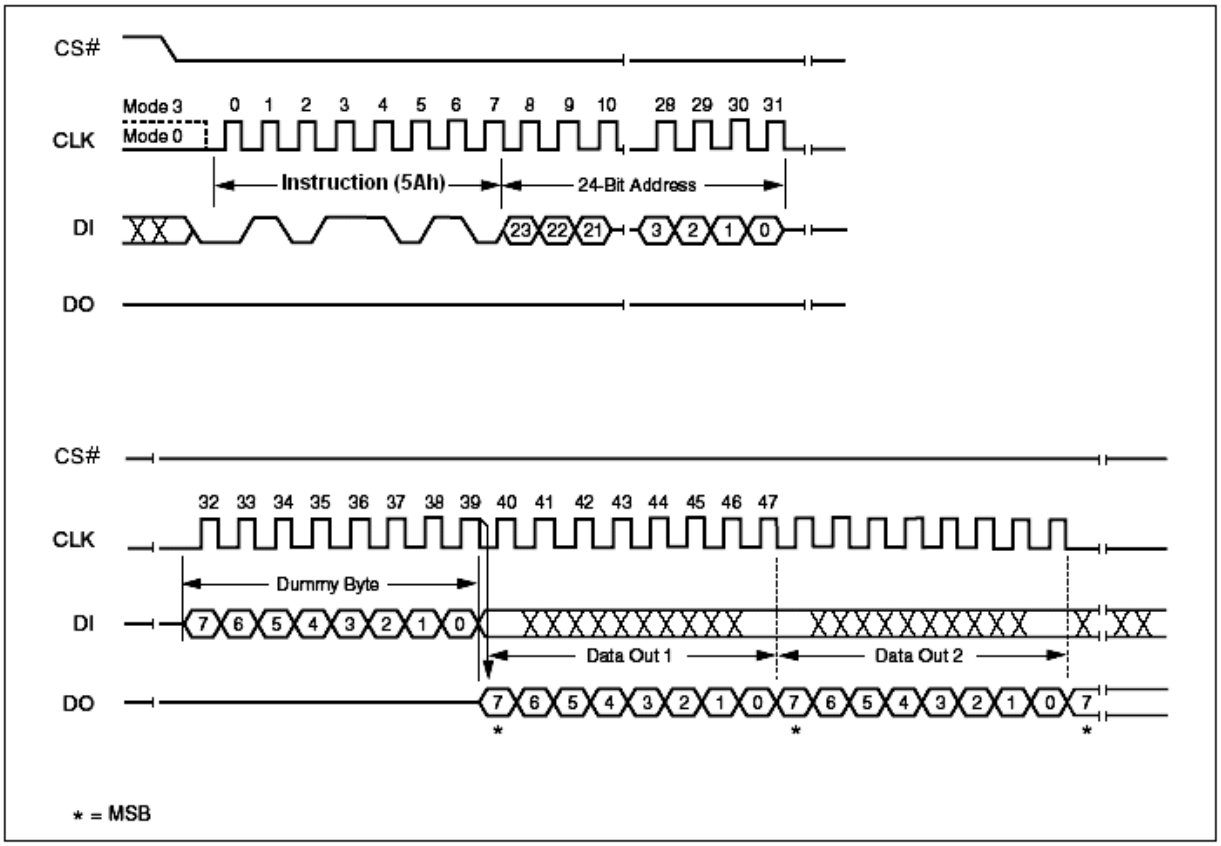


Figure 50. Read SFDP Mode and Unique ID Number Instruction Sequence Diagram

Table 13. Serial Flash Discoverable Parameters (SFDP) Signature and Parameter Identification Data Value (Advanced Information)

Description	Address (h) (Byte Mode)	Address (Bit)	Data	Comment
SFDP Signature	00h	07 : 00	53h	Signature [31:0]: Hex: 50444653
	01h	15 : 08	46h	
	02h	23 : 16	44h	
	03h	31 : 24	50h	
SFDP Minor Revision Number	04h	07 : 00	06h	Star from 0x06
SFDP Major Revision Number	05h	15 : 08	01h	Star from 0x01
Number of Parameter Headers (NPH)	06h	23 : 16	02h	2 parameter header
Unused	07h	31 : 24	FFh	Reserved
ID Number	08h	07 : 00	00h	JEDEC ID
Parameter Table Minor Revision Number	09h	15 : 08	06h	Star from 0x06
Parameter Table Major Revision Number	0Ah	23 : 16	01h	Star from 0x01
Parameter Table Length (in DW)	0Bh	31 : 24	10h	16 DWORDs
Parameter Table Pointer (PTP)	0Ch	07 : 00	30h	000030h
	0Dh	15 : 08	00h	
	0Eh	23 : 16	00h	
Unused	0Fh	31 : 24	FFh	Reserved

Table 13. Serial Flash Discoverable Parameters (SFDP) Signature and Parameter Identification Data Value (Advanced Information)

Description	Address (h) (Byte Mode)	Address (Bit)	Data(h/b)	Comment
ID Number(Vender ID)	10h	07:00	1Ch	
Parameter Table Minor revision Number	11h	15:08	00h	Start from 00h
Parameter Table Major Revision Number	12h	23:16	01h	Start from 01h
Parameter Table Length(in fdouble word)	13h	31:24	04h	
Parameter Table Pointer (PTP)	14h	07:00	10h	
	15h	15:08	01h	
	16h	23:16	00h	
Unused	17h	31:24	FFh	
ID Number(4byte address)	18h	07:00	84h	
Parameter Table Minor revision Number	19h	15:08	00h	
Parameter Table Major Revision Number	1Ah	23:16	01h	
Parameter Table Length(in fdouble word)	1Bh	31:24	02h	
Parameter Table Pointer (PTP)	1Ch	07:00	C0h	
	1Dh	15:08	00h	
	1Eh	23:16	00h	
Unused	1Fh	31:24	FFh	

Table 13. Parameter ID (0) (Advanced Information) 1/17

Description	Address (h) (Byte Mode)	Address (Bit)	Data	Comment
Block / Sector Erase sizes Identifies the erase granularity for all Flash Components	30h	00	01b	00 = reserved 01 = 4KB erase 10 = reserved 11 = 64KB erase
		01		
Write Granularity		02	1b	0 = No, 1 = Yes
Volatile Status Register Block Protect bits		03	0b	0: Block Protect bits in device's status register are solely non-volatile or may be programmed either as volatile using the 50h instruction for write enable or non-volatile using the 06h instruction for write enable.
Write Enable Opcode Select for Writing to Volatile Status Register		04	0b	0: 50h 1: 06h
Unused		07:05	111b	Reserved
4 Kilo-Byte Erase Opcode	31h	15:08	20h	4 KB Erase Support (FFh = not supported)
Supports (1-1-2) Fast Read Device supports single input opcode & address and dual output data Fast Read	32h	16	1b	0 = not supported 1 = supported
Address Byte Number of bytes used in addressing for flash array read, write and erase.		17	01b	00 = 3-Byte 01 = 3- or 4-Byte (e.g. defaults to 3-Byte mode; enters 4-Byte mode on command) 10 = 4-Byte 11 = reserved
		18		
Supports Double Data Rate (DDR) Clocking Indicates the device supports some type of double transfer rate clocking.		19	0b	0 = not supported 1 = supported
Supports (1-2-2) Fast Read Device supports single input opcode, dual input address, and dual output data Fast Read		20	1b	0 = not supported 1 = supported
Supports (1-4-4) Fast Read Device supports single input opcode, quad input address, and quad output data Fast Read		21	1b	0 = not supported 1 = supported
Supports (1-1-4) Fast Read Device supports single input opcode & address and quad output data Fast Read		22	1b	0 = not supported 1 = supported
Unused		23	1b	Reserved
Unused	33h	31:24	FFh	Reserved

Table 13. Parameter ID (0) (Advanced Information) 2/17

Description	Address (h) (Byte Mode)	Address (Bit)	Data	Comment
Flash Memory Density	37h : 34h	31 : 00	0FFFFFFFh	256 Mbits

Table 13. Parameter ID (0) (Advanced Information) 3/17

Description	Address (h) (Byte Mode)	Address (Bit)	Data(b/h)	Data(h)	Comment
(1-4-4) Fast Read Number of Wait states (dummy clocks) needed before valid output	38h	04:00	00100b	44h	4 dummy clocks
Quad Input Address Quad Output (1-4-4) Fast Read Number of Mode Bits		07:05	010b		8 mode bits
(1-4-4) Fast Read Opcode Opcode for single input opcode, quad input address, and quad output data Fast Read.	39h	15:08	EBh	EBh	
(1-1-4) Fast Read Number of Wait states (dummy clocks) needed before valid output	3Ah	20:16	01000b	08h	8 dummy clocks
(1-1-4) Fast Read Number of Mode Bits		23:21	000b		Not Supported
(1-1-4) Fast Read Opcode Opcode for single input opcode & address and quad output data Fast Read.	3Bh	31 : 24	6Bh	6Bh	

Table 13. Parameter ID (0) (Advanced Information) 4/17

Description	Address (h) (Byte Mode)	Address (Bit)	Data(b/h)	Data(h)	Comment
(1-1-2) Fast Read Number of Wait states (dummy clocks) needed before valid output	3Ch	04:00	01000b	08h	8 dummy clocks
(1-1-2) Fast Read Number of Mode Bits		07:05	000b		Not Supported
(1-1-2) Fast Read Opcode Opcode for single input opcode & address and dual output data Fast Read.	3Dh	15 : 08	3Bh	3Bh	
(1-2-2) Fast Read Number of Wait states (dummy clocks) needed before valid output	3Eh	20:16	00100b	04h	4 dummy clocks
(1-2-2) Fast Read Number of Mode Bits		23:21	000b		Not Supported
(1-2-2) Fast Read Opcode Opcode for single input opcode, dual input address, and dual output data Fast Read.	3Fh	31 : 24	BBh	BBh	

Table 13. Parameter ID (0) (Advanced Information) 5/17

Description	Address(h) (Byte mode)	Address (Bit)	Data(b/h)	Data(h)	Comment
Supports (2-2-2) Fast Read Device supports dual input opcode & address and dual output data Fast Read.	40h	00	0b	FEh	0 = not supported 1 = supported
Reserved. These bits default to all 1's		03:01	111b		Reserved
Supports (4-4-4) Fast Read Device supports Quad input opcode & address and quad output data Fast Read.		04	1b		0 = not supported 1 = supported (EQPI Mode)
Reserved. These bits default to all 1's		07:05	111b		Reserved
Reserved. These bits default to all 1's	43h : 41h	31 : 08	FFh	FFh	Reserved

Table 13. Parameter ID (0) (Advanced Information) 6/17

Description	Address (h) (Byte Mode)	Address (Bit)	Data(b/h)	Data(h)	Comment
Reserved. These bits default to all 1's	45h : 44h	15 : 00	FFh	FFh	Reserved
(2-2-2) Fast Read Number of Wait states (dummy clocks) needed before valid output	46h	20:16	00000b	00h	Not Supported
(2-2-2) Fast Read Number of Mode Bits		23:21	000b		Not Supported
(2-2-2) Fast Read Opcode Opcode for dual input opcode & address and dual output data Fast Read.	47h	31 : 24	FFh	FFh	Not Supported

Table 13. Parameter ID (0) (Advanced Information) 7/17

Description	Address (h) (Byte Mode)	Address (Bit)	Data(b/h)	Data(h)	Comment
Reserved. These bits default to all 1's	49h : 48h	15 : 00	FFh	FFh	Reserved
(4-4-4) Fast Read Number of Wait states (dummy clocks) needed before valid output	4Ah	20:16	00100b	44h	4 dummy clocks
(4-4-4) Fast Read Number of Mode Bits		23:21	010b		8 mode bits
(4-4-4) Fast Read Opcode Opcode for quad input opcode/address, quad output data Fast Read.	4Bh	31 : 24	EBh	EBh	Must Enter EQPI Mode Firstly

Table 13. Parameter ID (0) (Advanced Information) 8/17

Description	Address (h) (Byte Mode)	Address (Bit)	Data	Comment
Sector Type 1 Size	4Ch	07 : 00	0Ch	4 KB
Sector Type 1 Opcode	4Dh	15 : 08	20h	
Sector Type 2 Size	4Eh	23 : 16	0Fh	32KB
Sector Type 2 Opcode	4Fh	31 : 24	52h	

Table 13. Parameter ID (0) (Advanced Information) 9/17

Description	Address (h) (Byte Mode)	Address (Bit)	Data	Comment
Sector Type 3 Size	50h	07 : 00	10h	64 KB
Sector Type 3 Opcode	51h	15 : 08	D8h	
Sector Type 4 Size	52h	23 : 16	00h	Not Supported
Sector Type 4 Opcode	53h	31 : 24	FFh	Not Supported

Table 13. Parameter ID (0) (Advanced Information) 10/17

Description	Address (h) (Byte Mode)	Address (Bit)	Data(b/h)	Data(h)	Comment
Multiplier form typical erase time to maximum erase time (max time = 2*(count+1)*erase typical time)	54h	03:00	0101b	35h	count
Erase type 1 Erase, typical time (typical time = (count + 1)*units)		07:04	00011b		count
	55h	08		3Ah	
		10:09	01b		units : 00b: 1 ms, 01b: 16 ms, 10b: 128 ms, 11b: 1 s
Erase type 2 Erase, typical time (typical time = (count + 1)*units)		15:11	00111b		count
	56h	17:16	01b	A5h	units : 00b: 1 ms, 01b: 16 ms, 10b: 128 ms, 11b: 1 s
Erase type 3 Erase, typical time (typical time = (count + 1)*units)		22:18	01001b		count
		23	01b		Units: 00b: 1 ms, 01b: 16 ms, 10b: 128 ms, 11b: 1 s
Erase type 4 Erase, typical time (typical time = (count + 1)*units)	57h	24		00h	
		29:25	00000b		count
		31:30	00b		Units : 00b: 1 ms, 01b: 16 ms, 10b: 128 ms, 11b: 1 s

Table 13. Parameter ID (0) (Advanced Information) 11/17

Description	Address (h) (Byte Mode)	Address (Bit)	Data(b/h)	Data(h)	Comment
Multiplier from typical time to max time for Page or byte program (maximum time = 2 * (count + 1)*typical time)	58h	03:00	0010b	82h	count
Page Size		07:04	1000b		Page
Page Program typical time (typical page program time = (count+1)*units)	59h	12:08	01010b	EAh	count
		13	1b		Units : 0:8us, 1:64us
Byte Program typical time, first byte (first byte typical time = (count+1)*units)		15:14	0011b		count
	5Ah	17:16		14h	
		18	1b		Units : 0:1us, 1:8us
Byte Program typical time, additional byte (additional byte time = (count+1)*units)		22:19	0010b		count
		23	0b		Units: 0:1us, 1:8us
Chip Erase, typical time	5Bh	28:24	10011b	D3h	count
		30:29	10b		Units : 00b:16ms, 01b:256ms, 10b:4s, 11b:64s
Reserved		31	1b		Reserved

Table 13. Parameter ID (0) (Advanced Information) 12/17

Description	Address (h) (Byte Mode)	Address (Bit)	Data(b/h)	Data(h)	Comment
Prohibited Operations During Program suspend	5Ch	03:00	1100b	4Ch	xxx0b: May not initiate a new erase anywhere (erase nesting not permitted) xx0xb: May not initiate a new page program anywhere (program nesting not permitted) x1xxb: May not initiate a read in the program suspended page size 1xxxb: The erase and program restrictions in bits 1:0 are sufficient
Prohibited Operations During Erase suspend		07:04	0100b		xxx0b: May not initiate a new erase anywhere (erase nesting not permitted) xx0xb: May not initiate a page program anywhere x0xxb: Refer to vendor datasheet for read restrictions 0xxxb: Additional erase or program restrictions apply
Reserved	5Dh	08	1b	6Fh	reserved
Program Resume to Suspend interval		12:09	0111b		Count of fixed units of 64us
Suspend in-progress program max latency (max latency=(count+1)*untis		15:13	10011b		count
	5Eh	17:16		76h	
		19:18	01b		Units : 00b:128ns, 01b:1us, 10b;8us, 11b:64us
Erase resume to Suspend interval (latency=(count+1)*64us)		23:20	0111b		Count of fixed units of 64us
Suspend in-progress erase max latency	5Fh	28:24	10011b	B3h	count
		30:29	01b		Units : 00b: 128ns, 01b:1us, 10b:8us, 11b:64us
Suspend/Resume supported		31	1b		0:supported 1:not supported

Table 13. Parameter ID (0) (Advanced Information) 13/17

Description	Address (h) (Byte Mode)	Address (Bit)	Data	Comment
Program Resume Instruction	60h	07:00	FFh	
Program Suspend Instruction	61h	15:08	FFh	
Resume Instruction	62h	23:16	FFh	
Suspend Instruction	63h	31:24	FFh	

Table 13. Parameter ID (0) (Advanced Information) 14/17

Description	Address (h) (Byte Mode)	Address (Bit)	Data(b/h)	Data(h)	Comment
Reserved	64h	01:00	11b	F7h	Reserved
Status Register Polling Device Busy		07:02	111101b		Bit 2: Read WIP bit [0] by 05h Read instruction Bit 3: Read bit 7 of Status Register by 70h Read instruction (0=not supported 1=support) Bit 07:04, Reserved: 1111b
Exit Deep Power down to next operation delay (delay=(count+1)*units)	65h	12:08	11101b	BDh	count
		14:13	01b		Units : 00b:128ns, 01b:1us, 10b:8us, 11b:64us
Exit Deep Power down Instruction	66h	15	10101011b (ABh)	D5h	
		22:16			
Enter Deep Power down Instruction	67h	23	10111001b (B9h)	5Ch	
		30:24			
Deep Power down Supported		31	0b		0:suppored 1:not supported

Table 13. Parameter ID (0) (Advanced Information) 15/17

Description	Address (h) (Byte Mode)	Address (Bit)	Data(b/h)	Data(h)	Comment
4-4-4 mode disable sequences	68h	03:00	1001b	29h	xxx1b: issue FFh instruction 1xxxb: issue the Soft Reset 66/99 sequence
4-4-4 mode enable sequences		07:04	00010b		x_xx1xb: issue instruction 38h
	69h	08		96h	
0-4-4 mode supported		09	1b		0: not supported 1:supported
0-4-4 mode Exit Method		15:10	100101b		xx_xxx1b: Mode Bits[7:0] = 00h will terminate this mode at the end of the current read operation. xx_xx1xb: If 3-Byte address active, input Fh on DQ0-DQ3 for 8 clocks. If 4-Byte address active, input Fh on DQ0-DQ3 for 10 clocks. xx_x1xxb: Reserved xx_1xxxb: Input Fh (mode bit reset) on DQ0-DQ3 for 8 clocks. x1_xxxxb: Mode Bit[7:0] ≠ Axh 1x_xxxxb: Reserved
0-4-4 Mode entry Method	6Ah	19:16	1001b	89h	xxx1b: Mode Bits[7:0] = A5h Note: QE must be set prior to using this mode x1xxb: Mode Bit[7:0]=Axh 1xxxb: Reserved
Quad Enable Requirements		22:20	000b		000b: No QE bit. Detects 1-1-4/1-4-4 reads based on instruction 010b: QE is bit 6 of Status Register. where 1=Quad Enable or 0=not Quad Enable 111b: Not Supported
HOLD or RESET Disable		23	1b		0:not supported
Reserved	6Bh	31:24	FFh	FFh	Reserved

Table 13. Parameter ID (0) (Advanced Information) 16/17

Description	Address (h) (Byte Mode)	Address (Bit)	Data(b/h)	Data(h)	Comment
Volatile or Non-Volatile Register and Write Enable Instruction for Status Register 1	6Ch	06:00	1101000b	E8h	xxx_1xxxb: Non-Volatile/Volatile status register 1 powers-up to last written value in the nonvolatile status register, use instruction 06h to enable write to non-volatile status register. Volatile status register may be activated after power-up to override the non-volatile status register, use instruction 50h to enable write and activate the volatile status register. x1x_xxxxb: Reserved 1xx_xxxxb: Reserved NOTE If the status register is read-only then this field will contain all zeros in bits 4:0.
Reserved		07	1b		reserved
Soft Reset and Rescue Sequence Support	6Dh	13:08 09 10 11 12 13	010000b	50h	x1_xxxxb: issue reset enable instruction 66h, then issue reset instruction 99h. The reset enable, reset sequence may be issued on 1, 2, or 4 wires depending on the device operating mode.
Exit 4-byte Address	6Eh	15:14 18:16 23:19	00001b 11000b	C0h	xx_xxxx_xxx1b: issue instruction E9h to exit 4-Byte address mode (write enable instruction 06h is not required) x1_xxxx_xxxxb: Reserved 1x_xxxx_xxxxb: Reserved
Enter 4-Byte Address	6Fh	31:24	10000001b	81h	xxxx_xxx1b: issue instruction B7h (preceding write enable not required)

Table 13. Parameter ID (1) (Advanced Information-4byte address instruction)

Description (4byte address instruction)	Address (h) (Byte Mode)	Address (Bit)	Data(b/h)	Data(h)	Comment
Support for 1-1-1 Read Command, Instruction=13h	C0h	00	1b	FFh	0:not supported 1:supported
Support for 1-1-1 Fast Read Command, Instruction=0Ch		01	1b		0:not supported 1:supported
Support for 1-1-2 Fast Read Command, Instruction=3Ch		02	1b		0:not supported 1:supported
Support for 1-2-2 Fast Read Command, Instruction=BCh		03	1b		0:not supported 1:supported
Support for 1-1-4 Fast Read Command, Instruction=ECh		04	1b		0:not supported 1:supported
Support for 1-4-4 Fast Read Command, Instruction=ECh		05	1b		0:not supported 1:supported
Support for 1-1-1 Page Program Command, Instruction=12h		06	1b		0:not supported 1:supported
Support for 1-1-4 Page Program Command, Instruction=34h		07	1b		0:not supported 1:supported
Support for 1-4-4 Page Program Command, Instruction=3Eh	C1h	08	0b	0Eh	0:not supported 1:supported
Support for Erase Command-Type 1 size, instruction looup in next Dword		09	1b		0:not supported 1:supported
Support for Erase Command-Type 2 size, instruction lookup in next Dword		10	1b		0:not supported 1:supported
Support for Erase Command-Type 3 size, instruction lookup in next Dword		11	1b		0:not supported 1:supported
Support for Erase Command-Type 4 size, instruction lookup in next Dword		12	0b		0:not supported 1:supported
Support for 1-1-1 DTR Read Command, Instruction=0Eh		13	0b		0:not supported 1:supported
Support for 1-2-2 DTR Read Command, Instruction=BEh		14	0b		0:not supported 1:supported
Support for 1-4-4 DTR Read Command, Instruction=EEh		15	0b		0:not supported 1:supported
Support for volatile individual sector lock Read command, Instruction=E0h	C2h	16	0b	F0h	
Support for volatile individual sector lock Write command, Instruction=E1h		17	0b		
Support for non-volatile individual sector lock read command, Instruction=E2h		18	0b		
Support for non-volatile indivdual sector lock write command, Instrucion=E3h		19	0b		

Reserved		23:20	1111b		
Reserved	C3h	31:24	FFh	FFh	
Instruction for Erase Type 1	C4h	07:00	21h	21h	
Instruction for Erase Type 2	C5h	15:08	5Ch	5Ch	
Instruction for Erase Type 3	C6h	23:16	DCh	DCh	
Instruction for Erase Type 4	C7h	31:24	FFh	FFh	

Table 13. Parameter ID (2) (Advanced Information-ESMT flash parameter)

Description (ESMT Flash Parameter Tables)	Address (h) (Byte Mode)	Address (Bit)	Data(h/b)	Data(h)	Comment
Vcc Supply Max Voltage	111h:110h	07:00 15:08	00h 36h	00h 36h	
Vcc Supply Min Voltage	113h:112h	23:16 31:24	00h 27h	00h 27h	
HW RESET# pin	115h:114h	00	1b	9Fh	**0:not support 1:supported**
HW HOLD# pin		01	1b		**0:not support 1:supported**
Deep Power down Supported		02	1b		**0:not support 1:supported**
SW Reset		03	1b		**0:not support 1:supported**
SW Reset Instruction		07:04 11:08	99h		
Program Suspend/Resume		12	0b	49h	**0:not support 1:supported**
Erase Suspend/Resume		13	0b		**0:not support 1:supported**
Unused		14	1b		
Wrap Read Mode		15	0b		**0:not support 1:supported**
Wrap Read Instruction	116h	23:16	FFh	FFh	
Wrap Read data length	117h	31:24	FFh	FFh	
Individual block lock	11Bh:118h	00	0b	FCh	**0:not support 1:supported**
Individual block lock bit		01	0b		**0:volatile 1:nonvolatile**
Individual block lock Instruction		07:02 09:08	FFh		
Individual block lock Volatile protect bit default protect status		10	0b	EBh	**0:protecct 1:unprotect**
Secured OTP		11	1b		**0:not support 1:supported**
Read Lock		12	0b		**0:not support 1:supported**
Permanent Lock		13	1b		**0:not support 1:supported**
Unused		15:14	11b		
Unused		31:16	FFh	FFh	
Unused	11F:11Ch		FFh	FFh	

Read Unique ID Number

The Read Unique ID Number instruction accesses a factory-set read-only 96-bit number that is unique to each device. The ID number can be used in conjunction with user software methods to help prevent copying or cloning of a system. The Read Unique ID instruction is initiated by driving the CS# pin low and shifting the instruction code “5Ah” followed by a three bytes of addresses, **0x1E0h**, and one byte of dummy clocks. After which, the 96-bit ID is shifted out on the falling edge of CLK.

Table 14. Unique ID Number

Description	Address (h) (Byte Mode)	Address (Bit)	Data	Comment
Unique ID Number	**1E0h : 1EBh**	95 : 00	By die	

Power-up Timing

All functionalities and DC specifications are specified for a V_{CC} ramp rate of greater than 1V per 100 ms (0V to 2.7V in less than 270 ms). See Table 15 and Figure 51 for more information.

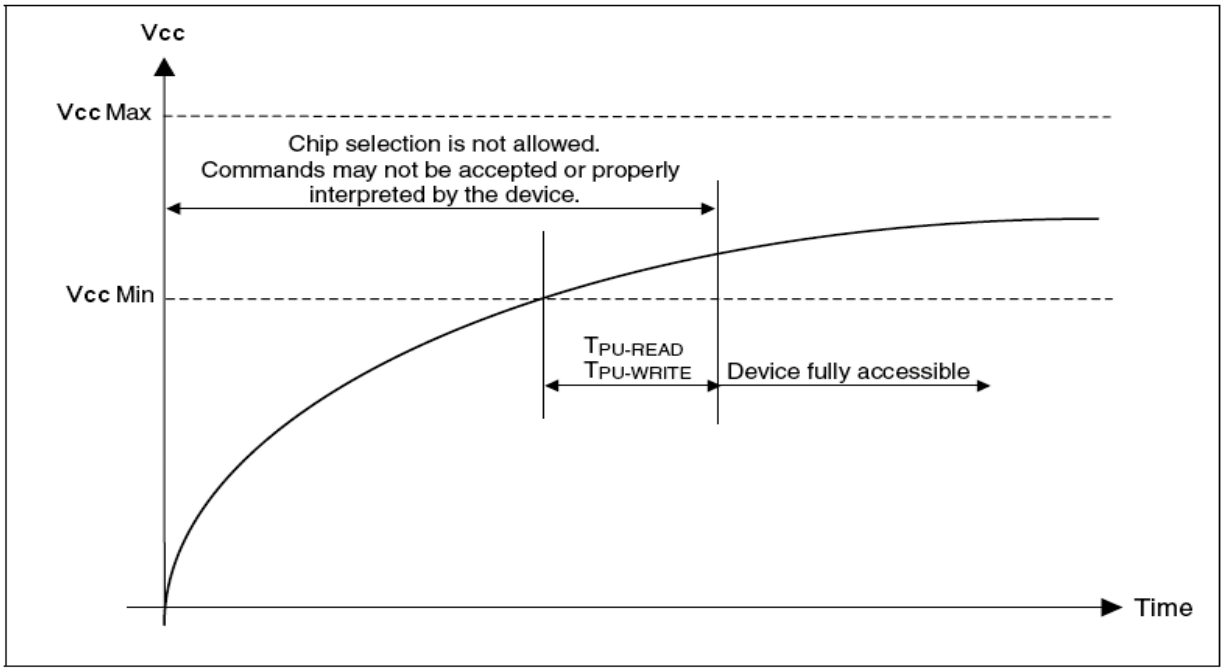


Figure 51. Power-up Timing

Table 15. Power-Up Timing

Symbol	Parameter	Min.	Unit
$T_{PU-READ}$ (1)	V_{CC} Min to Read Operation	100	µs
$T_{PU-WRITE}$ (1)	V_{CC} Min to Write Operation	100	µs

Note:
1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

INITIAL DELIVERY STATE

The device is delivered with the memory array erased: all bits are set to 1 (each byte contains FFh). The Status Register contains 00h (all Status Register bits are 0).

Table 16. DC Characteristics

(T_A = - 40°C to 85°C; V_{CC} = 2.7-3.6V)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{LI}	Input Leakage Current			1	± 2	µA
I_{LO}	Output Leakage Current			1	± 2	µA
I_{CC1}	Standby Current	CS# = V_{CC}, V_{IN} = V_{SS} or V_{CC}		1	20	µA
I_{CC2}	Deep Power-down Current	CS# = V_{CC}, V_{IN} = V_{SS} or V_{CC}		1	20	µA
I_{CC3}	Operating Current (READ)	CLK = 0.1 V_{CC} / 0.9 V_{CC} at 104MHz, DQ = open		6	15	mA
		CLK = 0.1 V_{CC} / 0.9 V_{CC} at 104MHz for Quad Output Read, DQ = open		8.5	20	mA
I_{CC4}	Operating Current (PP)	CS# = V_{CC}		15	30	mA
I_{CC5}	Operating Current (WRSR/WRSR3)	CS# = V_{CC}		20	25	mA
I_{CC6}	Operating Current (SE)	CS# = V_{CC}		20	25	mA
I_{CC7}	Operating Current (HBE/BE)	CS# = V_{CC}		20	25	mA
V_{IL}	Input Low Voltage		– 0.5		0.3 V_{CC}	V
V_{IH}	Input High Voltage		0.7V_{CC}		V_{CC}+0.4	V
V_{OL}	Output Low Voltage	I_{OL} = 100 µA, V_{CC}=V_{CC} Min.			0.3	V
V_{OH}	Output High Voltage	I_{OH} = –100 µA , V_{CC}=V_{CC} Min.	V_{CC}-0.2			V

Note:
1. Erase current measure on all cells=”0” states.

Table 17. AC Measurement Conditions

Symbol	Parameter	Min.	Max.	Unit
C_L	Load Capacitance	30		pF
	Input Rise and Fall Times		5	ns
	Input Pulse Voltages	0.2V_{CC} to 0.8V_{CC}		V
	Input Timing Reference Voltages	0.3V_{CC} to 0.7V_{CC}		V
	Output Timing Reference Voltages	V_{CC} / 2		V

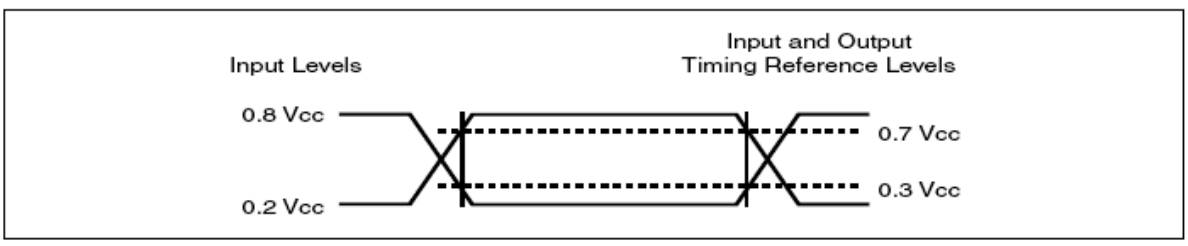


Figure 52. AC Measurement I/O Waveform

Table 18. AC Characteristics

(T_A = - 40°C to 85°C; V_{CC} = 2.7-3.6V)

Symbol	Alt	Parameter	Min	Typ	Max	Unit
F_R	f_C	Serial SDR Clock Frequency for: PP, QPP, SE, HBE, BE, CE, DP, RES, RDP, WREN, WRDI, WRSR, WRSR3, WRSR4, RDSR, RDSR2, RDSR3,RDSR4, RDID, Fast Read, Dual Output Fast Read, Dual I/O Fast Read, Quad Output Fast Read, Quad I/O Fast Read	D.C.		104	MHz
f_R		Serial Clock Frequency for READ	D.C.		50	MHz
t_{CH}[1]		Serial Clock High Time	3.5			ns
t_{CL}[1]		Serial Clock Low Time	3.5			ns
t_{CLCH}[2]		Serial Clock Rise Time (Slew Rate)	0.1			V / ns
t_{CHCL}[2]		Serial Clock Fall Time (Slew Rate)	0.1			V / ns
t_{SLCH}	t_{CSS}	CS# Active Setup Time	5			ns
t_{CHSH}		CS# Active Hold Time	5			ns
t_{SHCH}		CS# Not Active Setup Time	5			ns
t_{CHSL}		CS# Not Active Hold Time	5			ns
t_{SHSL}	t_{CSH}	CS# High Time	30			ns
t_{SHSL}[2]	t_{CSH}	Volatile Register Write Time	50			ns
t_{SHQZ}[2]	t_{DIS}	Output Disable Time			6	ns
t_{CLQX}	t_{HO}	Output Hold Time	0			ns
t_{DVCH}	t_{DSU}	Data In Setup Time	2			ns
t_{CHDX}	t_{DH}	Data In Hold Time	5			ns
t_{HLCH}		HOLD# Low Setup Time (relative to CLK)	5			ns
t_{HHCH}		HOLD# High Setup Time (relative to CLK)	5			ns
t_{CHHH}		HOLD# Low Hold Time (relative to CLK)	5			ns
t_{CHHL}		HOLD# High Hold Time (relative to CLK)	5			ns
t_{HLQZ}[2]	t_{HZ}	HOLD# to Output High-Z			6	ns
t_{HHQX}[2]	t_{LZ}	HOLD# to Output Low-Z			6	ns
t_{CLQV}	t_V	Output Valid from CLK for 30 pF			8	ns
		Output Valid from CLK for 15 pF			6	ns
t_{WHSL}[3]		Write Protect Setup Time before CS# Low	20			ns
t_{SHWL}[3]		Write Protect Hold Time after CS# High	100			ns
t_{DP}[2]		CS# High to Deep Power-down Mode			3	µs
t_{RES1}[2]		CS# High to Standby Mode without Electronic Signature read			3	µs
t_{RES2}[2]		CS# High to Standby Mode with Electronic Signature read			1.8	µs

Table 18. AC Characteristics-Continued

Symbol	Alt	Parameter		Min	Typ	Max	Unit
t_W		Write Status Register Cycle Time			4	30	ms
t_{PP}		Page Programming Time			0.5	3	ms
t_{SE}		Sector Erase Time			0.04	0.3	s
t_{HBE}		Half Block Erase Time			0.12	1	s
t_{BE}		Block Erase Time			0.15	2	s
t_{CE}		Chip Erase Time			100	400	s
	t_{SR}	Software Reset Latency	WIP = write operation		10	28	µs
			WIP = not in write operation			0	µs

Note:

1. $t_{CH} + t_{CL}$ must be greater than or equal to $1/ f_C$.
2. Value guaranteed by characterization, not 100% tested in production.
3. Only applicable as a constraint for a Write status Register instruction when Status Register Protect Bit is set at 1.

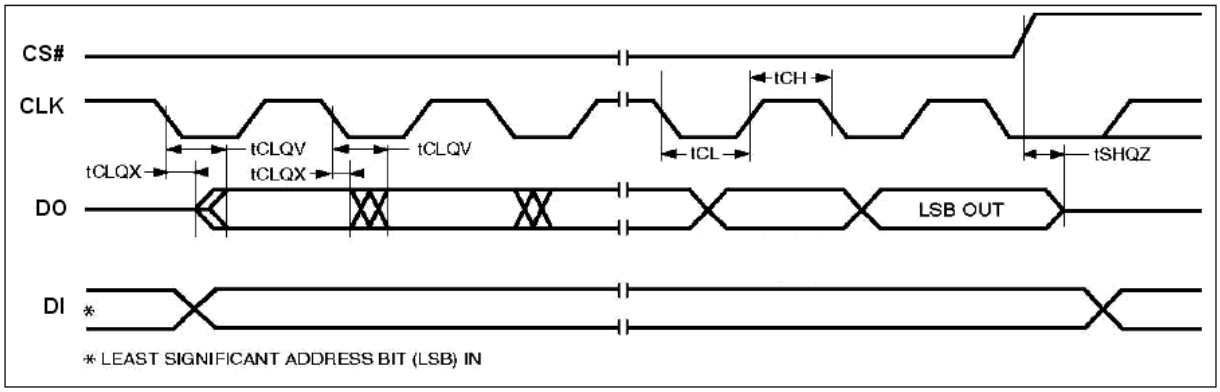


Figure 53. Serial Output Timing

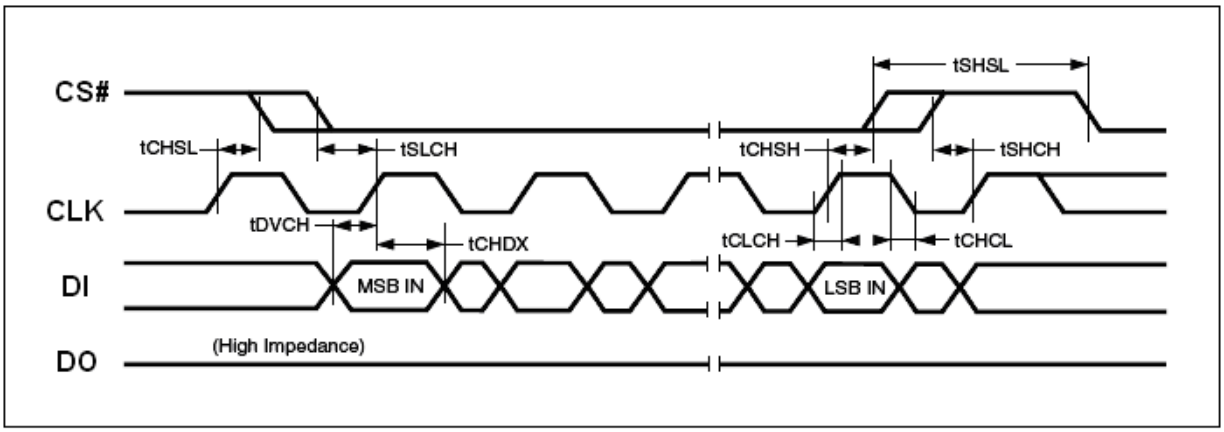


Figure 54. Input Timing

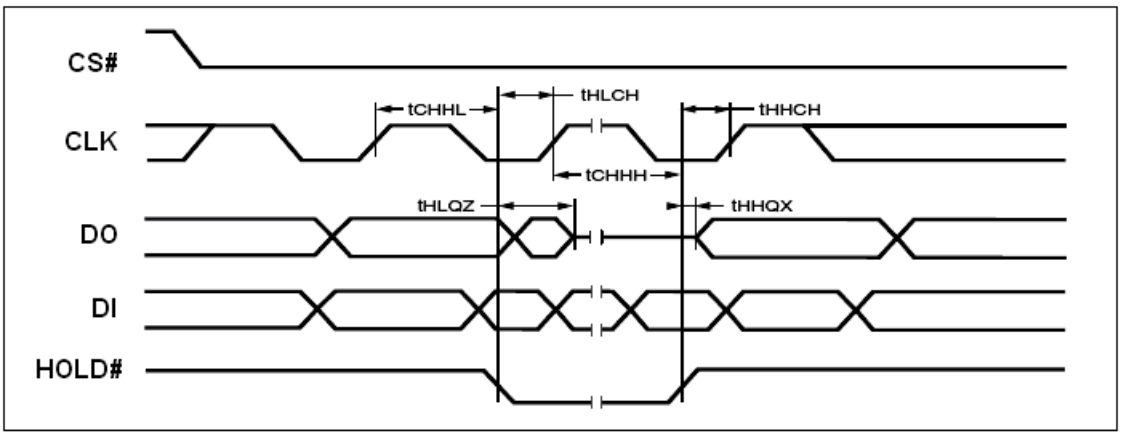


Figure 55. Hold Timing

ABSOLUTE MAXIMUM RATINGS

Stresses above the values so mentioned above may cause permanent damage to the device. These values are for a stress rating only and do not imply that the device should be operated at conditions up to or above these values. Exposure of the device to the maximum rating values for extended periods of time may adversely affect the device reliability.

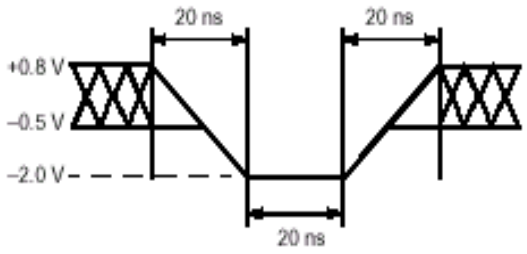
Parameter	Value	Unit
Storage Temperature	-65 to +150	°C
Output Short Circuit Current[1]	200	mA
Input and Output Voltage (with respect to ground) [2]	-0.5 to V_{CC}+0.5	V
V_{CC}	-0.5 to V_{CC}+0.5	V

Notes:
1. No more than one output shorted at a time. Duration of the short circuit should not be greater than one second.
2. Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, inputs may undershoot V_{SS} to –1.0V for periods of up to 50ns and to –2.0 V for periods of up to 20ns. See figure below. Maximum DC voltage on output and I/O pins is V_{CC} + 0.5 V. During voltage transitions, outputs may overshoot to V_{CC} + 2.0 V for periods up to 20ns. See figure below.

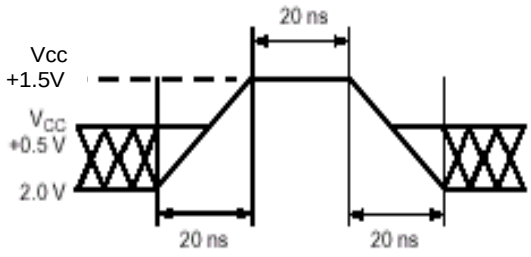
RECOMMENDED OPERATING RANGES [1]

Parameter	Value	Unit
Ambient Operating Temperature Industrial Devices	-40 to 85	°C
Operating Supply Voltage V_{CC}	Full: 2.7 to 3.6	V

Notes:
1. Recommended Operating Ranges define those limits between which the functionality of the device is guaranteed.



Maximum Negative Overshoot Waveform



Maximum Positive Overshoot Waveform

Table 19. CAPACITANCE

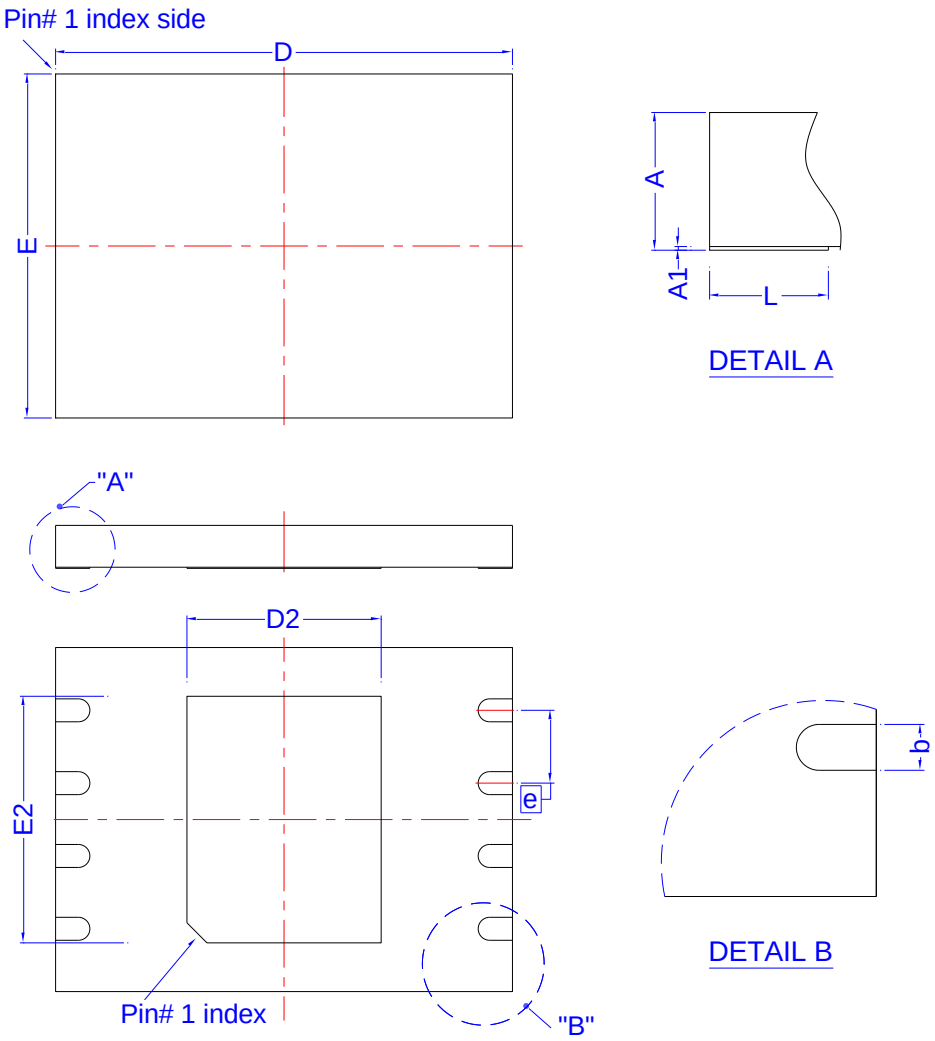
(V_{CC} = 2.7-3.6V)

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0		8	pF

Note: Sampled only, not 100% tested, at T_A = 25°C and a frequency of 20MHz.

PACKAGE MECHANICAL

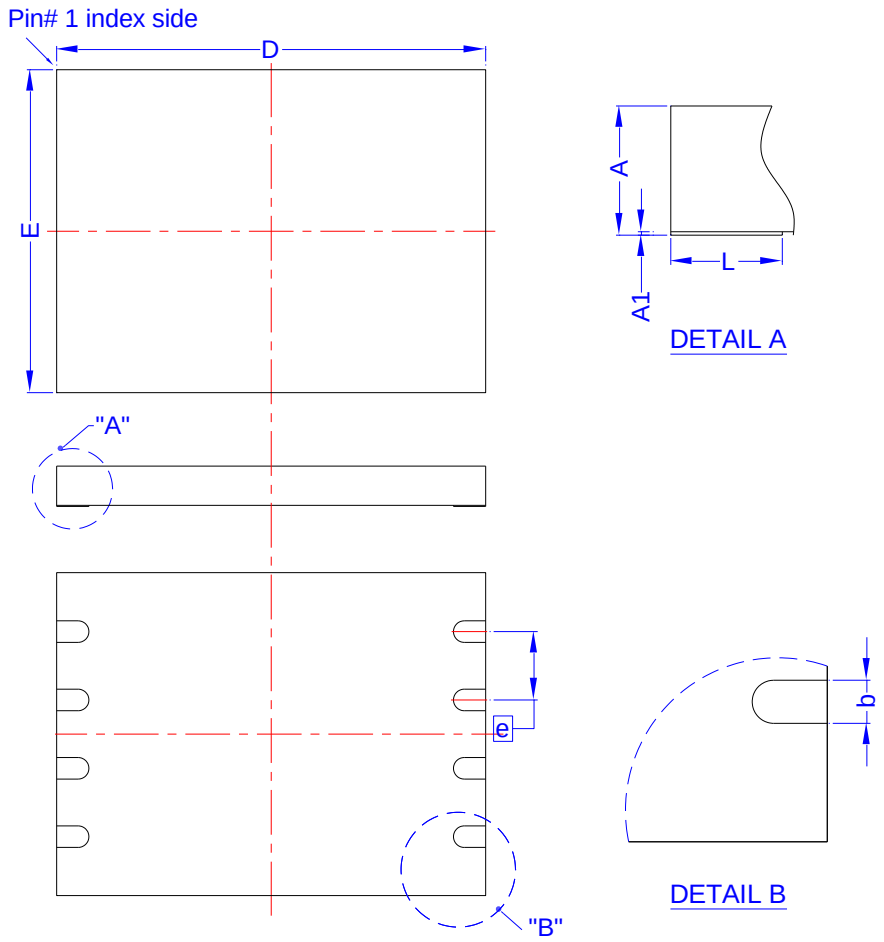
Figure 56. VDFN / WSON 8 (8x6 mm)



Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.35	0.40	0.45	0.014	0.016	0.018
D		8.00 BSC			0.315 BSC	
D2	3.30	3.40	3.50	0.130	0.134	0.138
E		6.00 BSC			0.236 BSC	
E2	4.20	4.30	4.40	0.165	0.169	0.173
e		1.27 BSC			0.050 BSC	
L	0.45	0.50	0.55	0.018	0.020	0.022

Controlling dimension : millimeter
(Revision date : Sep 07 2021)

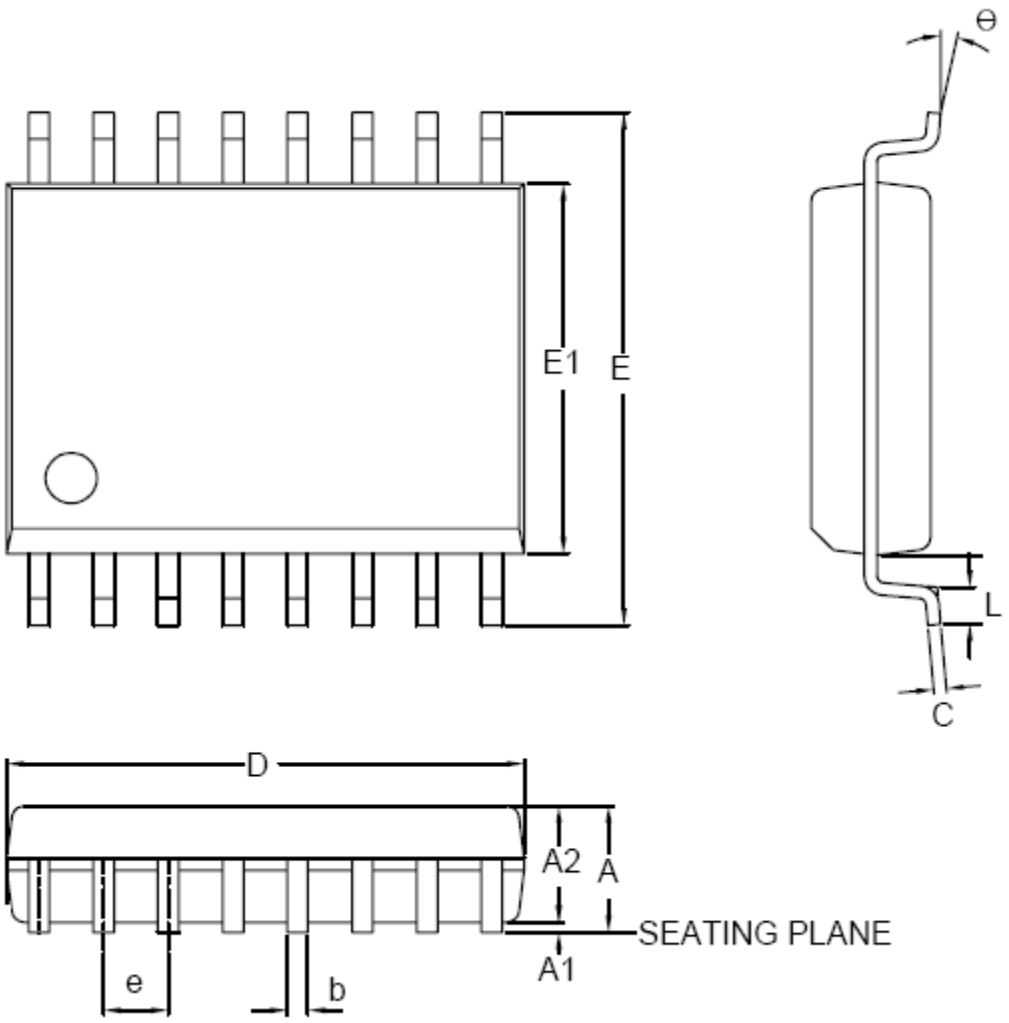
Figure 57. VDFN / WSON 8 (8x6mm) without Expose metal pad



Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.35	0.40	0.45	0.014	0.016	0.018
D	7.90	8.00	8.10	0.311	0.315	0.319
E	5.90	6.00	6.10	0.232	0.236	0.240
e	1.27 BSC			0.050 BSC		
L	0.40	0.50	0.60	0.016	0.020	0.024

Controlling dimension : millimeter
(Revision date : Apr 25 2018)

Figure 58. 16 LEAD SOP 300 mil



SYMBOL	DIMENSION IN MM		
	MIN.	NOR	MAX
A	- - -	- - -	2.65
A1	0.10	0.20	0.30
A2	2.25	- - -	2.40
C	0.20	0.25	0.30
D	10.10	10.30	10.50
E	10.00	- - -	10.65
E1	7.40	7.50	7.60
e	- - -	1.27	- - -
b	0.31	- - -	0.51
L	0.4	- - -	1.27
θ	0^0	5^0	8^0

Note : 1. Coplanarity: 0.1 mm

ORDERING INFORMATION

EN25QH256A - 104 F I P 2RC

DIFFERENTIATION CODE
2RCE = USON/WSON package without Expose metal pad

PACKAGING CONTENT
P = RoHS, Halogen-Free and REACH compliant

TEMPERATURE RANGE
I = Industrial (-40°C to +85°C)

PACKAGE
F = 16-pin 300mil SOP
Y = 8-pin VDFN / WSON (8x6 mm)

SPEED
104 = 104MHz

BASE PART NUMBER
EN = Eon Silicon Solution Inc.
25QH = 3V Serial Flash with 4KB Uniform-Sector
256 = 256 Megabit (1024K x 16)
A = version identifier

Revisions List

Revision No	Description	Date
1.0	Initial Release	2019/05/27
1.1	Add WSON package without exposed metal pad	2019/07/03
1.2	Correct typo	2020/02/13
1.3	Delete Plastic Packages Temperature	2020/10/15
1.4	1. Add the description of 4byteP bit. 2. Add Important Notice	2021/06/01
1.5	1. Modify Instruction Set (Erase Instruction) table 2. Modify DFN8 8x6x0.75mm packing dimension	2021/09/14

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