EN25E10A (2AQ)
1 Megabit Serial Flash Memory with 4Kbyte Uniform Sector

FEATURES

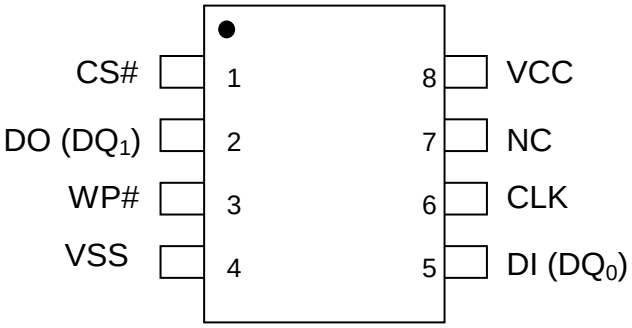
- Single power supply operation
  - Full voltage range: 2.3-3.6 volt
- Serial Interface Architecture
  - SPI Compatible: Mode 0 and Mode 3
- 1 M-bit Serial Flash
  - 1 M-bit/128 K-byte/512 pages
  - 256 bytes per programmable page
- Standard, Dual SPI
  - Standard SPI: CLK, CS#, DI, DO, WP#
  - Dual SPI: CLK, CS#, DQ_0, DQ_1, WP#
- High performance
  - 104MHz clock rate for Standard SPI
  - 104MHz clock rate for two data bits
- Low power consumption
  - 5 mA typical active current
  - 1 μA typical power down current
- Uniform Sector Architecture:
  - 32 sectors of 4-Kbyte
  - 4 blocks of 32-Kbyte
  - 2 blocks of 64-Kbyte
  - Any sector or block can be erased individually
- Software and Hardware Write Protection:
  - Write Protect all or portion of memory via software
  - Enable/Disable protection with WP# pin
- High performance program/erase speed
  - Page program time: 0.6ms typical
  - Sector erase time: 50ms typical
  - 32KB Block erase time: 150ms typical
  - 64KB Block erase time: 300ms typical
  - Chip erase time: 0.7 seconds typical
- Minimum 100K endurance cycle
- Data retention time 20years
- Package Options
  - 8 pins SOP 150mil body width
  - 8 contact USON 2x3x0.45 mm
  - All Pb-free packages are compliant RoHS, Halogen-Free and REACH.
- Industrial temperature Range

GENERAL DESCRIPTION

The device is a 1 Megabit (128 K-byte) Serial Flash memory, with enhanced write protection mechanisms. The device supports the standard Serial Peripheral Interface (SPI) and a high performance Dual output. SPI clock frequencies of up to 104MHz are supported allowing equivalent clock rates of 208MHz (104MHz x 2) for Dual Output. The memory can be programmed 1 to 256 bytes at a time, using the Page Program instruction.

The device is designed to allow either single Sector/Block at a time or full chip erase operation. The device can be configured to protect part of the memory as the software protected mode. The device can sustain a minimum of 100K program/erase cycles on each sector or block.

Figure.1 CONNECTION DIAGRAMS (TOP VIEW)



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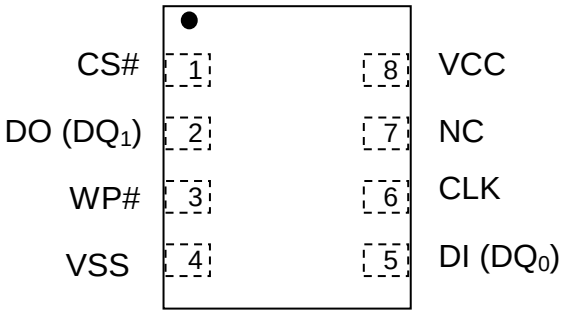

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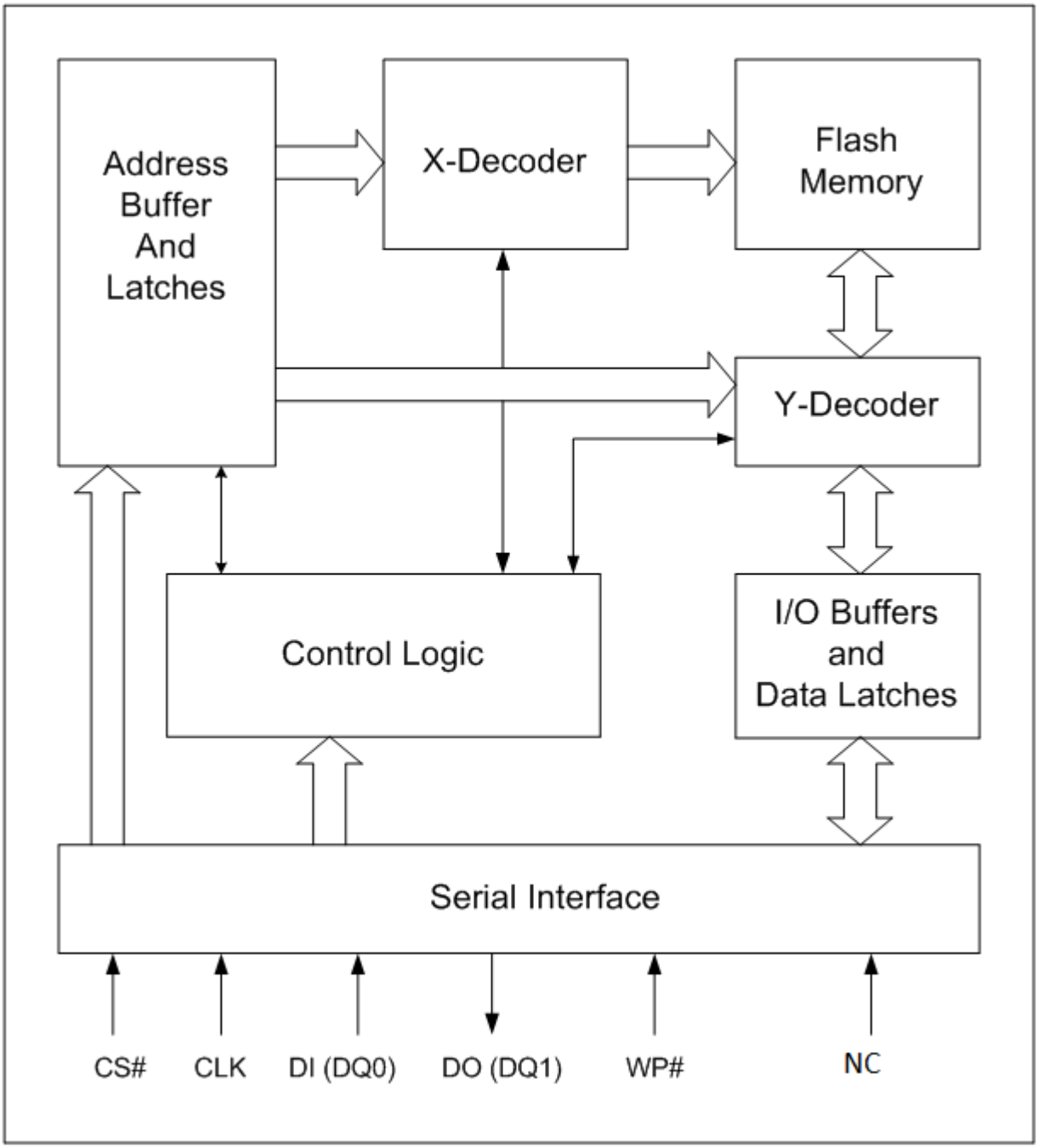
Figure 2. BLOCK DIAGRAM



Note:
1. DQ_0 and DQ_1 are used for Dual instructions.

Table 1. Pin Names

Symbol	Pin Name
CLK	Serial Clock Input
DI (DQ_0)	Serial Data Input (Data Input Output 0) *1
DO (DQ_1)	Serial Data Output (Data Output 1) *1
CS#	Chip Select
WP#	Write Protect
NC	NC pin
Vcc	Supply Voltage (2.3-3.6V)
Vss	Ground
NC	No Connect

Note:
1. DQ_0 and DQ_1 are used for Dual instructions.

SIGNAL DESCRIPTION

Serial Data Input, Output and IOs (DI, DO and DQ_0, DQ_1)

The device support standard SPI, Dual SPI operation. Standard SPI instructions use the unidirectional DI (input) pin to serially write instructions, addresses or data to the device on the rising edge of the Serial Clock (CLK) input pin. Standard SPI also uses the unidirectional DO (output) to read data or status from the device on the falling edge CLK.

Dual SPI instruction use the bidirectional IO pins to serially write instruction, addresses or data to the device on the rising edge of CLK and read data or status from the device on the falling edge of CLK.

Serial Clock (CLK)

The SPI Serial Clock Input (CLK) pin provides the timing for serial input and output operations. ("See SPI Mode")

Chip Select (CS#)

The SPI Chip Select (CS#) pin enables and disables device operation. When CS# is high the device is deselected and the Serial Data Output (DO, or DQ_0, DQ_1) pins are at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program or status register cycle is in progress. When CS# is brought low the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, CS# must transition from high to low before a new instruction will be accepted.

Write Protect (WP#)

The Write Protect (WP#) pin can be used to prevent the Status Register from being written. Used in conjunction with the Status Register's Block Protect (BP0, BP1, BP2) bits and Status Register Protect (SRP) bits, a portion or the entire memory array can be hardware protected. WP# default is enabled, user can disable it by set WPDIS=1 in status register.

MEMORY ORGANIZATION

The memory is organized as:

- 131,072 bytes
- Uniform Sector Architecture
  4 blocks of 32-Kbyte
  2 blocks of 64-Kbyte
  32 sectors of 4-Kbyte
- 512 pages (256 bytes each)

Each page can be individually programmed (bits are programmed from 1 to 0). The device is Sector, Block or Chip Erasable but not Page Erasable.

Table 2. Uniform Block Sector Architecture

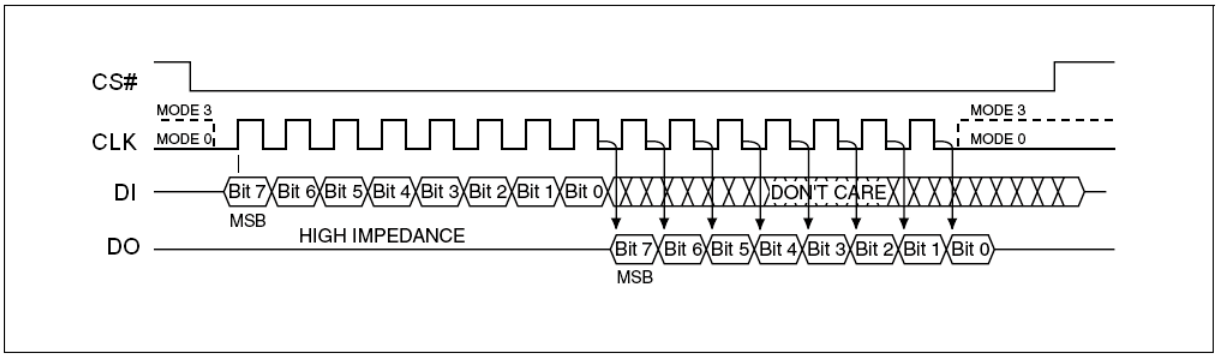
64KB Block	32KB Block	Sector	Address range	
1	3	31	01F000h	01FFFFh
		⋮	⋮	⋮
	2	16	010000h	010FFFh
0	1	15	00F000h	00FFFFh
		⋮	⋮	⋮
	0	0	000000h	000FFFh

OPERATING FEATURES

Standard SPI Modes

The device is accessed through a SPI compatible bus consisting of four signals: Serial Clock (CLK), Chip Select (CS#), Serial Data Input (DI) and Serial Data Output (DO). Both SPI bus operation Modes 0 (0,0) and 3 (1,1) are supported. The primary difference between Mode 0 and Mode 3, as shown in Figure 3, concerns the normal state of the CLK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0 the CLK signal is normally low. For Mode 3 the CLK signal is normally high. In either case data input on the DI pin is sampled on the rising edge of the CLK. Data output on the DO pin is clocked out on the falling edge of CLK.

Figure 3. SPI Modes



Dual SPI Instruction

The device supports Dual SPI operation when using the “Dual Output Fast Read“ (3Bh) instructions. These instructions allow data to be transferred to or from the Serial Flash memory at two times the rate possible with the standard SPI. The Dual Read instructions are ideal for quickly downloading code from Flash to RAM upon power-up (code-shadowing) or for application that cache code-segments to RAM for execution. The Dual output feature simply allows the SPI input pin to also serve as an output during this instruction. When using Dual SPI instructions the DI and DO pins become bidirectional I/O pins; DQ_0 and DQ_1. All other operations use the standard SPI interface with single output signal.

Page Programming

To program one data byte, two instructions are required: Write Enable (WREN), which is one byte, and a Page Program (PP) sequence, which consists of four bytes plus data. This is followed by the internal Program cycle (of duration t_{PP}).
To spread this overhead, the Page Program (PP) instruction allows up to 256 bytes to be programmed at a time (changing bits from 1 to 0) provided that they lie in consecutive addresses on the same page of memory.

Sector Erase, Half Block Erase, Block Erase and Chip Erase

The Page Program (PP) instruction allows bits to be reset from 1 to 0. Before this can be applied, the bytes of memory need to have been erased to all 1s (FFh). This can be achieved a sector at a time, using the Sector Erase (SE) instruction, half a block at a time using the Half Block Erase (HBE) instruction, a block at a time using the Block Erase (BE) instruction or throughout the entire memory, using the Chip Erase (CE) instruction. This starts an internal Erase cycle (of duration t_{SE}, t_{HBE}, t_{BE} or t_{CE}). The Erase instruction must be preceded by a Write Enable (WREN) instruction.

Polling During a Write, Program or Erase Cycle

A further improvement in the time to Write Status Register (WRSR), Program (PP) or Erase (SE, HBE, BE or CE) can be achieved by not waiting for the worst case delay (t_W, t_{PP}, t_{SE}, t_{HBE}, t_{BE} or t_{CE}). The Write In Progress (WIP) bit is provided in the Status Register so that the application program can monitor its value, polling it to establish when the previous Write cycle, Program cycle or Erase cycle is complete.

Active Power, Stand-by Power and Deep Power-Down Modes

When Chip Select (CS#) is Low, the device is enabled, and in the Active Power mode. When Chip Select (CS#) is High, the device is disabled, but could remain in the Active Power mode until all internal cycles have completed (Program, Erase, and Write Status Register). The device then goes into the Stand-by Power mode. The device consumption drops to I_{CC1}.
The Deep Power-down mode is entered when the specific instruction (the Enter Deep Power-down Mode (DP) instruction) is executed. The device consumption drops further to I_{CC2}. The device remains in this mode until another specific instruction (the Release from Deep Power-down Mode, and Read Device ID (RDI) and Software Reset instruction) is executed.
All other instructions are ignored while the device is in the Deep Power-down mode. This can be used as an extra software protection mechanism, when the device is not in active use, to protect the device from inadvertent Write, Program or Erase instructions.

Write Protection

Applications that use non-volatile memory must take into consideration the possibility of noise and other adverse system conditions that may compromise data integrity. To address this concern the device provides the following data protection mechanisms:

- Power-On Reset and an internal timer (t_{PUW}) can provide protection against inadvertent changes while the power supply is outside the operating specification.
- Program, Erase and Write Status Register instructions are checked that they consist of a number of clock pulses that is a multiple of eight, before they are accepted for execution.
- All instructions that modify data must be preceded by a Write Enable (WREN) instruction to set the Write Enable Latch (WEL) bit. This bit is returned to its reset state by the following events:
  - Power-up
  - Write Disable (WRDI) instruction completion or Write Status Register (WRSR) instruction completion or Page Program (PP) instruction completion or Sector Erase (SE) instruction completion or Half Block Erase (HBE) / Block Erase (BE) instruction completion or Chip Erase (CE) instruction completion
- The Block Protect (BP2, BP1, BP0) bits allow part of the memory to be configured as read-only. This is the Software Protected Mode (SPM).
- The Write Protect (WP#) signal allows the Block Protect (BP2, BP1, BP0) bits and Status Register Protect (SRP) bit to be protected. This is the Hardware Protected Mode (HPM).
- In addition to the low power consumption feature, the Deep Power-down mode offers extra software protection from inadvertent Write, Program and Erase instructions, as all instructions are ignored except one particular instruction (the Release from Deep Power-down instruction).

Table 3. Protected Area Sizes Sector Organization

Status Register Content			Memory Content			
BP2	**BP1**	**BP0**	**Protect Areas**	**Addresses**	**Density (KB)**	**Portion**
0	0	0	None	None	None	None
0	0	1	Sector 0 to 29	000000h-01DFFFh	120KB	Lower 15/16
0	1	0	Sector 0 to 27	000000h-01BFFFh	112KB	Lower 7/8
0	1	1	Sector 0 to 23	000000h-017FFFh	96KB	Lower 3/4
1	0	0	Sector 0 to 15	000000h-00FFFFh	64KB	Lower 1/2
1	0	1	All	000000h-01FFFFh	128KB	All
1	1	0	All	000000h-01FFFFh	128KB	All
1	1	1	All	000000h-01FFFFh	128KB	All

INSTRUCTIONS

All instructions, addresses and data are shifted in and out of the device, most significant bit first. Serial Data Input (DI) is sampled on the first rising edge of Serial Clock (CLK) after Chip Select (CS#) is driven Low. Then, the one-byte instruction code must be shifted in to the device, most significant bit first, on Serial Data Input (DI), each bit being latched on the rising edges of Serial Clock (CLK).

The instruction set is listed in Table 4. Every instruction sequence starts with a one-byte instruction code. Depending on the instruction, this might be followed by address bytes, or by data bytes, or by both or none. Chip Select (CS#) must be driven High after the last bit of the instruction sequence has been shifted in. In the case of a Read Data Bytes (READ), Read Data Bytes at Higher Speed (Fast_Read), Dual Output Fast Read (3Bh), Read Status Register (RDSR) or Release from Deep Power-down, and Read Device ID (RDI) instruction, the shifted-in instruction sequence is followed by a data-out sequence. Chip Select (CS#) can be driven High after any bit of the data-out sequence is being shifted out.

In the case of a Page Program (PP), Sector Erase (SE), Half Block Erase (HBE), Block Erase (BE), Chip Erase (CE), Write Status Register (WRSR), Write Enable (WREN), Write Disable (WRDI) or Deep Power-down (DP) instruction, Chip Select (CS#) must be driven High exactly at a byte boundary, otherwise the instruction is rejected, and is not executed. That is, Chip Select (CS#) must driven High when the number of clock pulses after Chip Select (CS#) being driven Low is an exact multiple of eight. For Page Program, if at any time the input byte is not a full byte, nothing will happen and WEL will not be reset.

In the case of multi-byte commands of Page Program (PP) and Release from Deep Power Down (RES) minimum number of bytes specified has to be given, without which, the command will be ignored.

In the case of Page Program, if the number of byte after the command is less than 4 (at least 1 data byte), it will be ignored too. In the case of SE, HBE and BE, exact 24-bit address is a must, any less or more will cause the command to be ignored.

All attempts to access the memory array during a Write Status Register cycle, Program cycle or Erase cycle are ignored, and the internal Write Status Register cycle, Program cycle or Erase cycle continues unaffected.

Table 4A. Instruction Set

Instruction Name	Byte 1 Code	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	n-Bytes
RSTEN	66h						
RST(2)	99h						
Write Enable	06h						
Write Disable	04h						
Read Status Register	05h	(S7-S0)(3)					continuous(4)
Write Status Register	01h	S7-S0					
Page Program	02h	A23-A16	A15-A8	A7-A0	D7-D0	Next byte	continuous
Sector Erase	20h	A23-A16	A15-A8	A7-A0			
32KB Half Block Erase (HBE)	52h	A23-A16	A15-A8	A7-A0			
64KB Block Erase	D8h	A23-A16	A15-A8	A7-A0			
Chip Erase	C7h/ 60h						
Deep Power-down	B9h						
Release from Deep Power-down, and read Device ID	ABh	dummy	dummy	dummy	(ID7-ID0)		(6)
Release from Deep Power-down							
Manufacturer/ Device ID	90h	dummy	dummy	00h	(M7-M0)	(ID7-ID0)	(7)
				01h	(ID7-ID0)	(M7-M0)	
Read Identification	9Fh	(M7-M0)	(ID15-ID8)	(ID7-ID0)	(7)		

Notes:
1. Device accepts eight-clocks command in Standard SPI mode
2. RST command only executed if RSTEN command is executed first. Any intervening command will disable Reset.
3. Data bytes are shifted with Most Significant Bit first. Byte fields with data in parenthesis “( )” indicate data being read from the device on the DO pin
4. The Status Register contents will repeat continuously until CS# terminate the instruction
5. The Device ID will repeat continuously until CS# terminates the instruction
6. The Manufacturer ID and Device ID bytes will repeat continuously until CS# terminates the instruction. 00h on Byte 4 starts with MID and alternate with DID, 01h on Byte 4 starts with DID and alternate with MID
7. (M7-M0) : Manufacturer, (ID15-ID8) : Memory Type, (ID7-ID0) : Memory Capacity

Table 4B. Instruction Set (Read Instruction)

Instruction Name	OP Code	Address bits	Dummy bits / Clocks (Default)	Data Out	Remark
Read Data	03h	24 bits	0	(D7-D0, …)	(Next Byte) continuous
Fast Read	0Bh	24 bits	8 bits / 8 clocks	(D7-D0, …)	(Next Byte) continuous
Dual Output Fast Read	3Bh	24 bits	8 bits / 8 clocks	(D7-D0, …)	(one byte Per 4 clocks, continuous)

Table 5. Manufacturer and Device Identification

OP Code	(M7-M0)	(ID15-ID0)	(ID7-ID0)
ABh			10h
90h	1Ch		10h
9Fh	1Ch	4211h	

Reset-Enable (RSTEN) (66h) and Reset (RST) (99h)

The Reset operation is used as a system (software) reset that puts the device in normal operating Ready mode. This operation consists of two commands: Reset-Enable (RSTEN) and Reset (RST).

To reset the device the host drives CS# low, sends the Reset-Enable command (66h), and drives CS# high. Next, the host drives CS# low again, sends the Reset command (99h), and drives CS# high.
The Reset operation requires the Reset-Enable command followed by the Reset command. Any command other than the Reset command after the Reset-Enable command will disable the Reset-Enable.

A successful command execution will reset the status register to original setting vaule , see Figure 4. A device reset during an active Program or Erase operation aborts the operation, which can cause the data of the targeted address range to be corrupted or lost. Depending on the prior operation, the reset timing may vary. Recovery from a Write operation requires more software latency time (t_{SR}) than recovery from other operations. Please Figure 4.1.

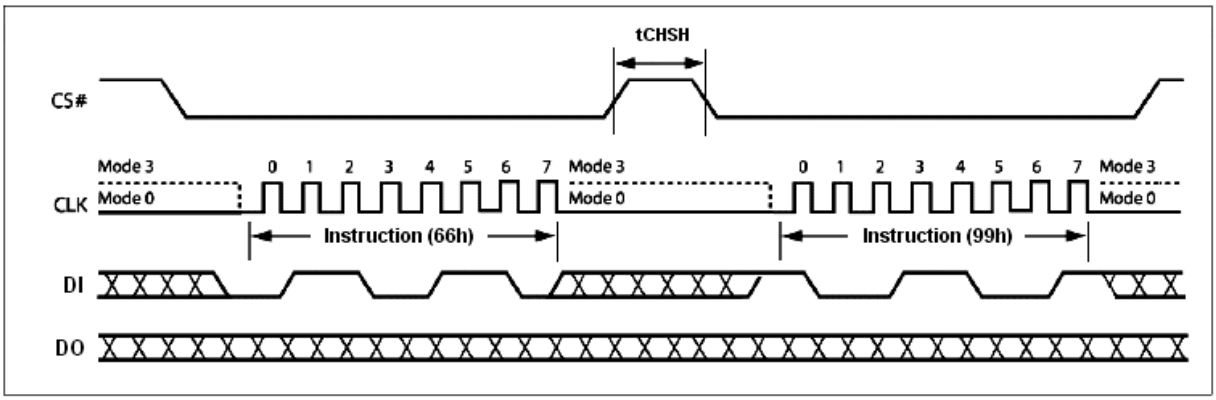


Figure 4. Reset-Enable and Reset Sequence Diagram

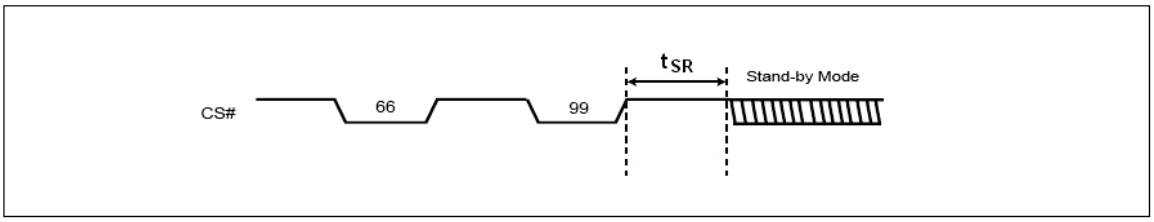
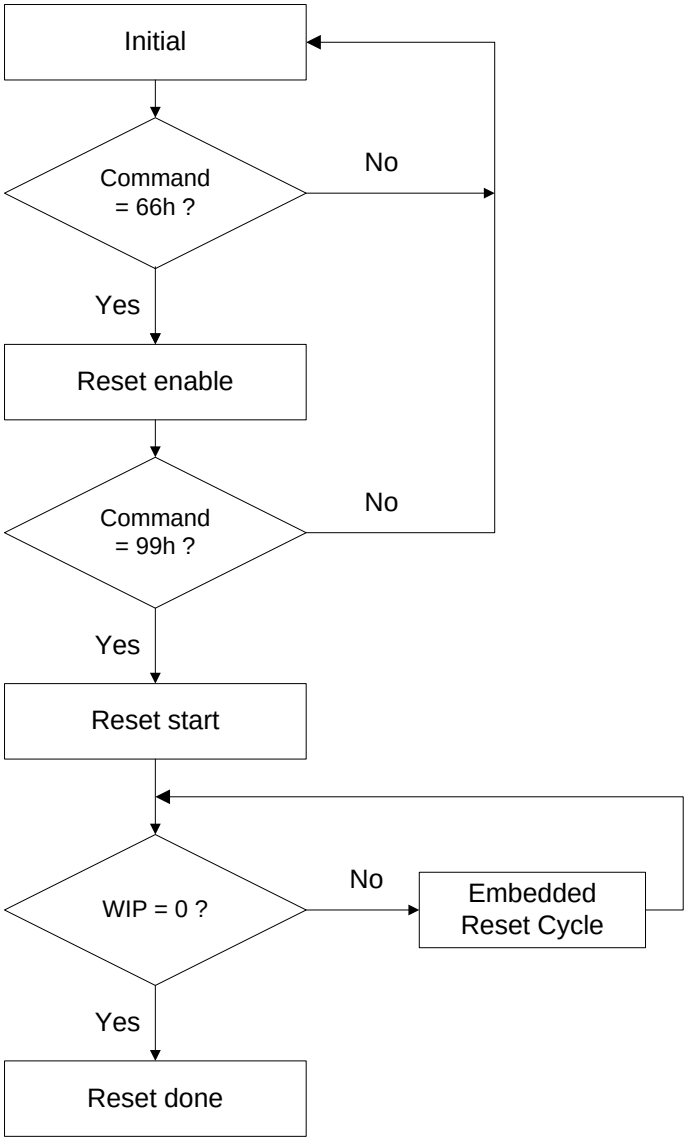


Figure 4.1 Software Reset Recovery

Software Reset Flow



Note:

1. Reset-Enable (RSTEN) (66h) and Reset (RST) (99h) commands need to match standard SPI mode.
2. The reset command could be executed during embedded program and erase process.
3. This flow cannot release the device from Deep power down mode.
4. The Status Register Bit will reset to original setting value after reset done.
5. If user reset device during erase, the embedded reset cycle software reset latency will take about 28us in worst case.

Write Enable (WREN) (06h)

The Write Enable (WREN) instruction (Figure 5) sets the Write Enable Latch (WEL) bit. The Write Enable Latch (WEL) bit must be set prior to every Page Program (PP), Sector Erase (SE), Half Block Erase (HBE), Block Erase (BE), Chip Erase (CE) and Write Status Register (WRSR) instruction.
The Write Enable (WREN) instruction is entered by driving Chip Select (CS#) Low, sending the instruction code, and then driving Chip Select (CS#) High.

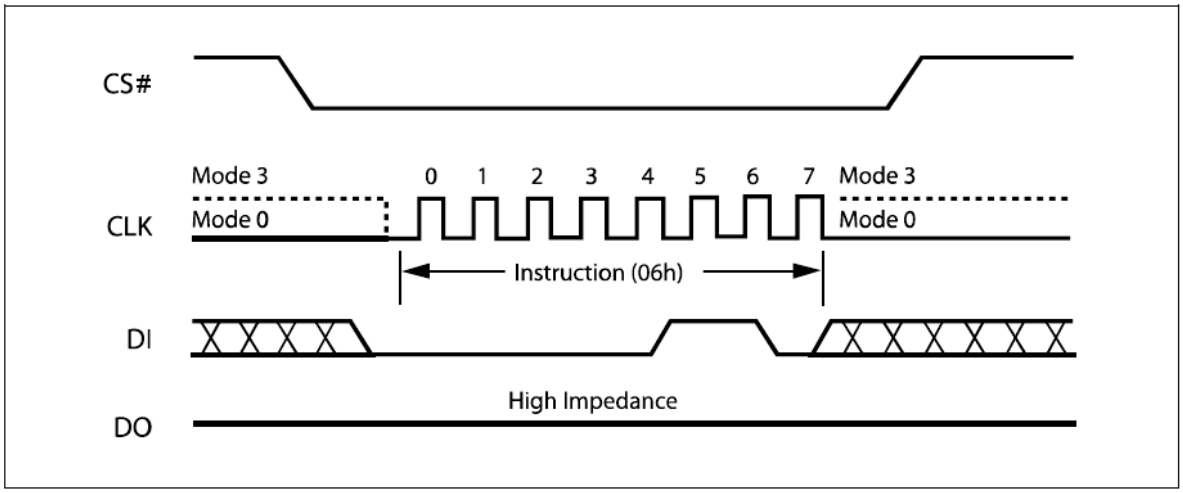


Figure 5. Write Enable Instruction Sequence Diagram

Write Disable (WRDI) (04h)

The Write Disable instruction (Figure 6) resets the Write Enable Latch (WEL) bit in the Status Register to a 0 or exit from OTP mode to normal mode. The Write Disable instruction is entered by driving Chip Select (CS#) low, shifting the instruction code “04h” into the DI pin and then driving Chip Select (CS#) high. Note that the WEL bit is automatically reset after Power-up and upon completion of the Write Status Register, Page Program, Sector Erase, Half Block Erase (HBE), Block Erase (BE) and Chip Erase instructions.

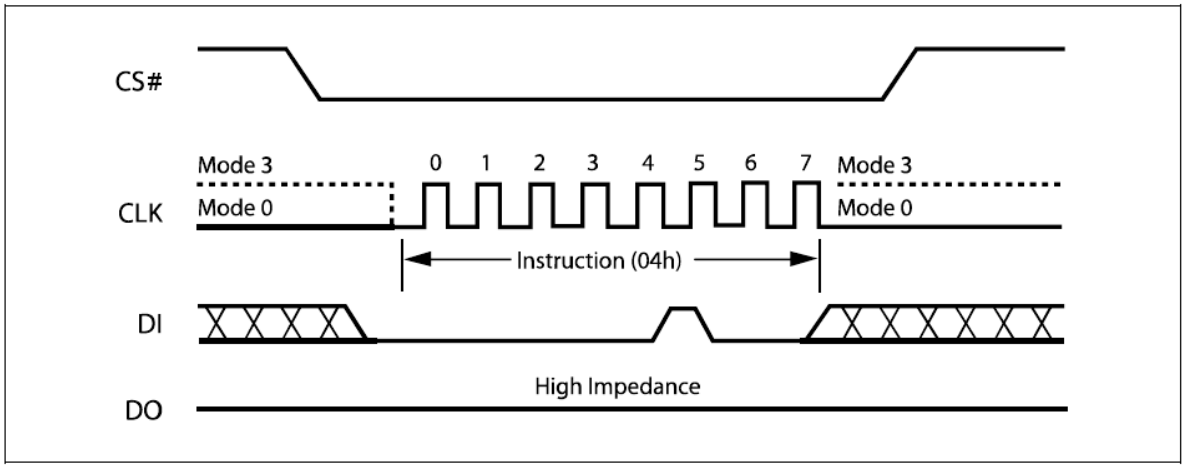


Figure 6. Write Disable Instruction Sequence Diagram

Read Status Register (RDSR) (05h)

The Read Status Register (RDSR) instruction allows the Status Register to be read. The Status Register may be read at any time, even while a Program, Erase or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write In Progress (WIP) bit before sending a new instruction to the device. It is also possible to read the Status Register continuously, as shown in Figure 7.

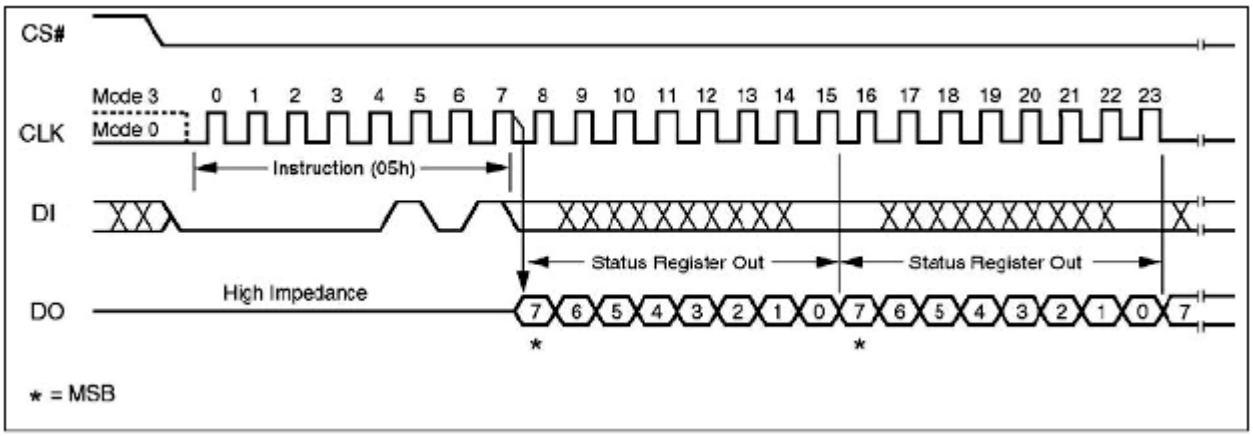


Figure 7. Read Status Register Instruction Sequence Diagram

Table 6. Status Register Bit Locations

S7	S6	S5	S4	S3	S2	S1	S0
SRP Status Register Protect	WPDIS (WP#disable)	Blank check	BP2 (Block Protected bits)	BP1 (Block Protected bits)	BP0 (Block Protected bits)	WEL (Write Enable Latch)	WIP (Write In Progress bit) (Note 3)
1 = status register write disable	1 = WP#disable 0 = WP# enable **(default 0)**	**1 = flash is blank after ship out (default)** 0 = flash had been programmed	(note 2)	(note 2)	(note 2)	1 = write enable 0 = not write enable	1 = write operation 0 = not in write operation
Non-volatile bit	Non-Volatile	indicator bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	volatile bit	volatile bit

Note

1. See the table “Protected Area Sizes Sector Organization”.

The status and control bits of the Status Register are as follows:

WIP bit. The Write In Progress (WIP) bit indicates whether the memory is busy with a Write Status Register, Program or Erase cycle. When set to 1, such a cycle is in progress, when reset to 0 no such cycle is in progress.

WEL bit. The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write Status Register, Program or Erase instruction is accepted.

BP2, BP1, BP0 bits. The Block Protect (BP2, BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase instructions. These bits are written with the Write Status Register (WRSR) instruction. When one or both of the Block Protect (BP2, BP1, BP0) bits is set to 1, the relevant memory area (as defined in Table 3.) becomes protected against Page Program (PP) Sector Erase (SE) and , Block Erase (BE), instructions. The Block Protect (BP2, BP1, BP0) bits can be written provided that the Hardware Protected mode has not been set. The Chip Erase (CE) instruction is executed if, and only if, all Block Protect (BP2, BP1, BP0) bits are 0.

WPDIS bit. The Write Protect disable (WPDIS) bit, non-volatile bit, when it is reset to “0” (factory default) to enable WP# function or is set to “1” to disable WP# function. User can use Flash Programmer to set WPDIS bit as “1” and then the host system can let WP# keep floating in SPI mode.

Blank check bit. This bit is related with whole chip blank as factory default. Once any **byte** is programmed, this bit turns to 0 and will not be restored by further erase operation.

SRP bit. The Status Register Protect (SRP) bit operates in conjunction with the Write Protect (WP#) signal. The Status Register Write Protect (SRP) bit and Write Protect (WP#) signal allow the device to be put in the Hardware Protected mode (when the Status Register Protect (SRP) bit is set to 1, and Write Protect (WP#) is driven Low). In this mode, the non-volatile bits of the Status Register (SRP, BP2, BP1, BP0) become read-only bits and the Write Status Register (WRSR) instruction is no longer accepted for execution.

Write Status Register (WRSR) (01h)

The Write Status Register (WRSR) instruction allows new values to be written to the Status Register. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded and executed, the device sets the Write Enable Latch (WEL).

The Write Status Register (WRSR) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code and the data byte on Serial Data Input (DI).

The instruction sequence is shown in Figure 8. The Write Status Register (WRSR) instruction has no effect on S1 and S0 of the Status Register. Chip Select (CS#) must be driven High after the eighth bit of the data byte has been latched in. If not, the Write Status Register (WRSR) instruction is not executed. As soon as Chip Select (CS#) is driven High, the self-timed Write Status Register cycle (whose duration is t_W) is initiated. While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Write Status Register cycle, and is 0 when it is completed. When the cycle is completed, the Write Enable Latch (WEL) is reset.

The Write Status Register (WRSR) instruction allows the user to change the values of the Block Protect (BP2, BP1, BP0) bits, to define the size of the area that is to be treated as read-only, as defined in Table 3. The Write Status Register (WRSR) instruction also allows the user to set or reset the Status Register Protect (SRP) bit in accordance with the Write Protect (WP#) signal. The Status Register Protect (SRP) bit and Write Protect (WP#) signal allow the device to be put in the Hardware Protected Mode (HPM). The Write Status Register (WRSR) instruction is not executed once the Hardware Protected Mode (HPM) is entered.

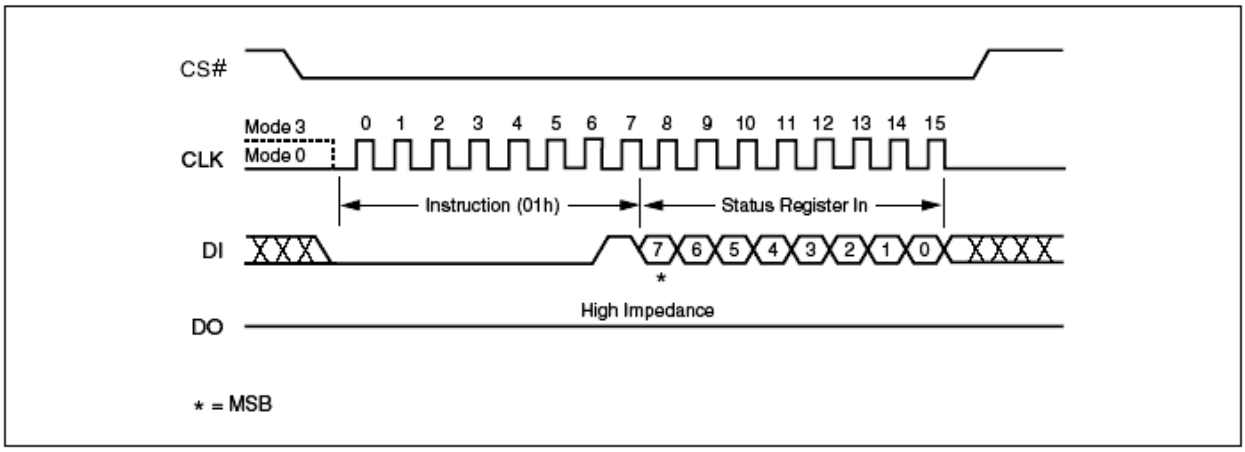


Figure 8. Write Status Register Instruction Sequence Diagram

Read Data Bytes (READ) (03h)

The device is first selected by driving Chip Select (CS#) Low. The instruction code for the Read Data Bytes (READ) instruction is followed by a 3-byte address (A23-A0), each bit being latched-in during the rising edge of Serial Clock (CLK). Then the memory contents, at that address, is shifted out on Serial Data Output (DO), each bit being shifted out, at a maximum frequency f_R, during the falling edge of Serial Clock (CLK).

The instruction sequence is shown in Figure 9. The first byte addresses can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes (READ) instruction. When the highest address is reached, the address counter rolls over to 000000h, allowing the read sequence to be continued indefinitely.

The Read Data Bytes (READ) instruction is terminated by driving Chip Select (CS#) High. Chip Select (CS#) can be driven High at any time during data output. Any Read Data Bytes (READ) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

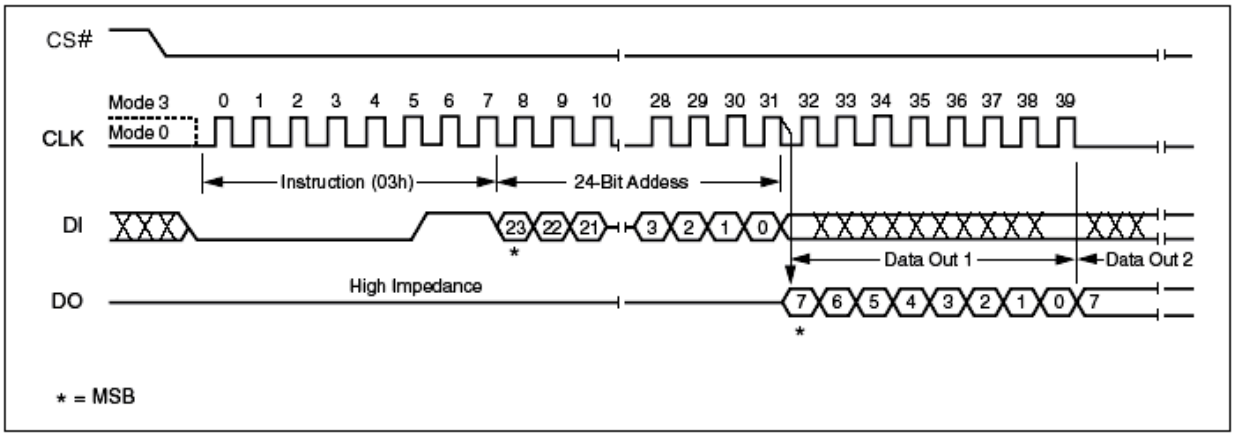


Figure 9. Read Data Instruction Sequence Diagram

Read Data Bytes at Higher Speed (FAST_READ) (0Bh)

The device is first selected by driving Chip Select (CS#) Low. The instruction code for the Read Data Bytes at Higher Speed (FAST_READ) instruction is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of Serial Clock (CLK). Then the memory contents, at that address, is shifted out on Serial Data Output (DO), each bit being shifted out, at a maximum frequency F_R, during the falling edge of Serial Clock (CLK).

The instruction sequence is shown in Figure 10. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes at Higher Speed (FAST_READ) instruction. When the highest address is reached, the address counter rolls over to 000000h, allowing the read sequence to be continued indefinitely.

The Read Data Bytes at Higher Speed (FAST_READ) instruction is terminated by driving Chip Select (CS#) High. Chip Select (CS#) can be driven High at any time during data output. Any Read Data Bytes at Higher Speed (FAST_READ) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

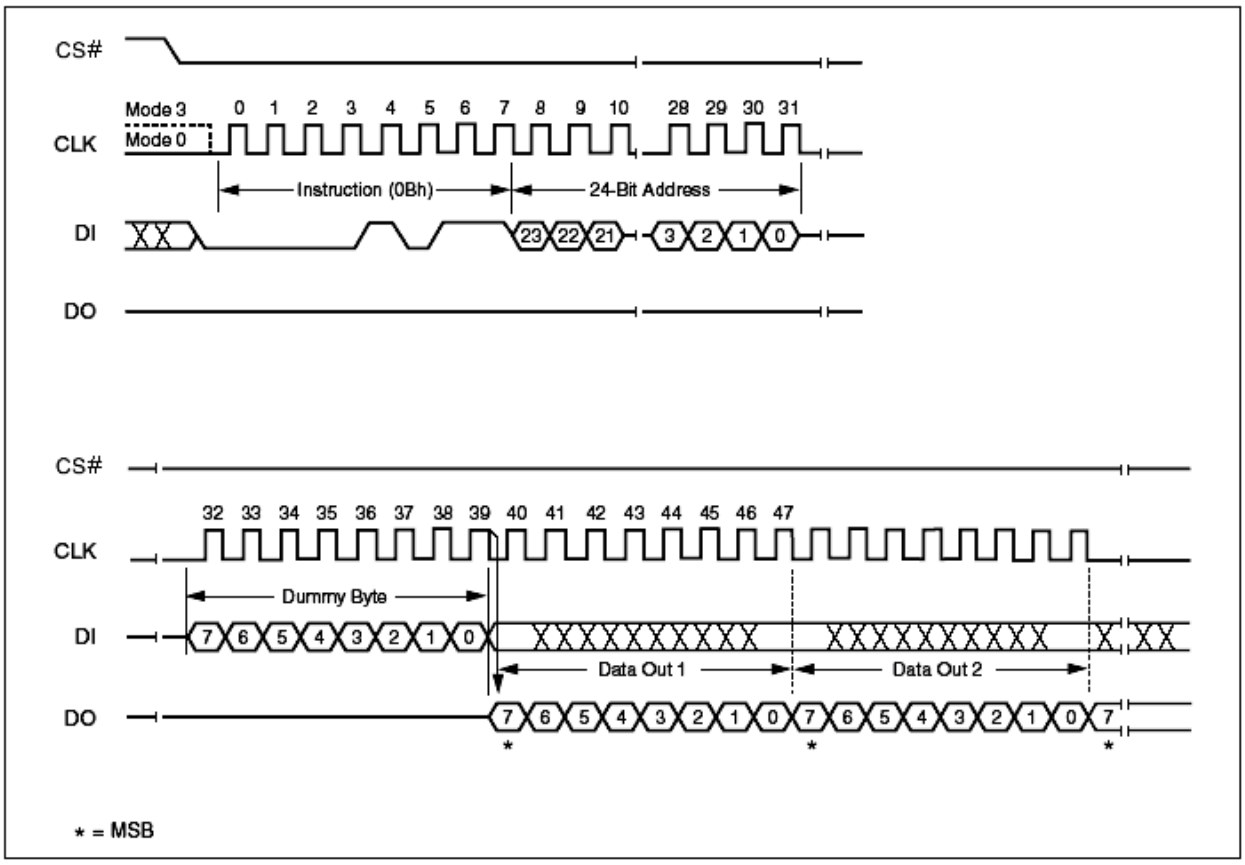


Figure 10. Fast Read Instruction Sequence Diagram

Dual Output Fast Read (3Bh)

The Dual Output Fast Read (3Bh) is similar to the standard Fast Read (0Bh) instruction except that data is output on two pins, DQ_0 and DQ_1, instead of just DQ_0. This allows data to be transferred from the device at twice the rate of standard SPI devices. The Dual Output Fast Read instruction is ideal for quickly downloading code from to RAM upon power-up or for applications that cache code-segments to RAM for execution.

Similar to the Fast Read instruction, the Dual Output Fast Read instruction can operation at the highest possible frequency of F_R (see AC Electrical Characteristics). This is accomplished by adding eight "dummy clocks after the 24-bit address as shown in Figure 11. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clock is "don't care". However, the DI pin should be high-impedance prior to the falling edge of the first data out clock.

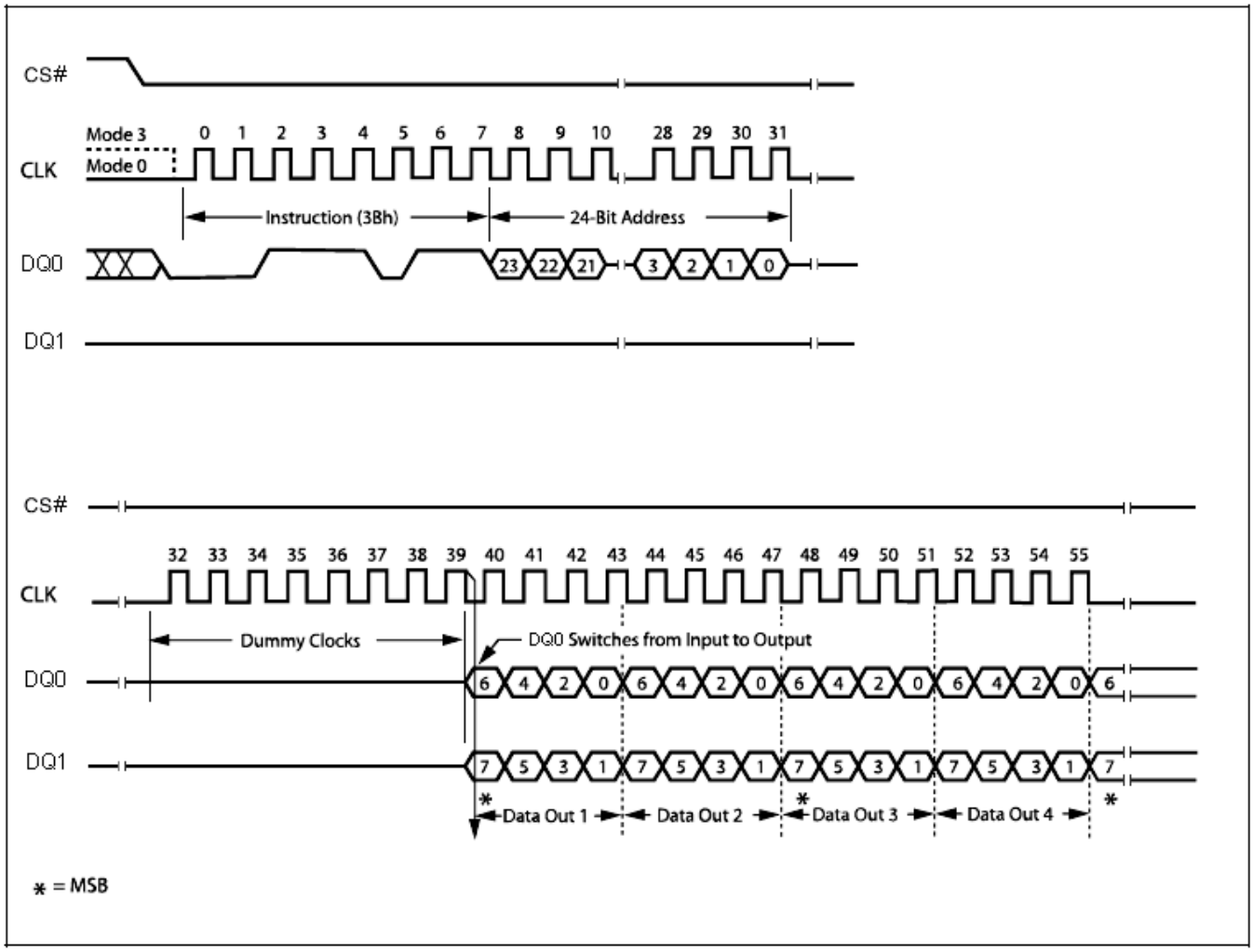


Figure 11. Dual Output Fast Read Instruction Sequence Diagram

Page Program (PP) (02h)

The Page Program (PP) instruction allows bytes to be programmed in the memory. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Page Program (PP) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code, three address bytes and at least one data byte on Serial Data Input (DI). If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). Chip Select (CS#) must be driven Low for the entire duration of the sequence.
The instruction sequence is shown in Figure 12. If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 Data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page.

Chip Select (CS#) must be driven High after the eighth bit of the last data byte has been latched in, otherwise the Page Program (PP) instruction is not executed.

As soon as Chip Select (CS#) is driven High, the self-timed Page Program cycle (whose duration is t_{PP}) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Page Program (PP) instruction applied to a page which is protected by the Block Protect (BP2, BP1, BP0) bits (see Table 3) is not executed.

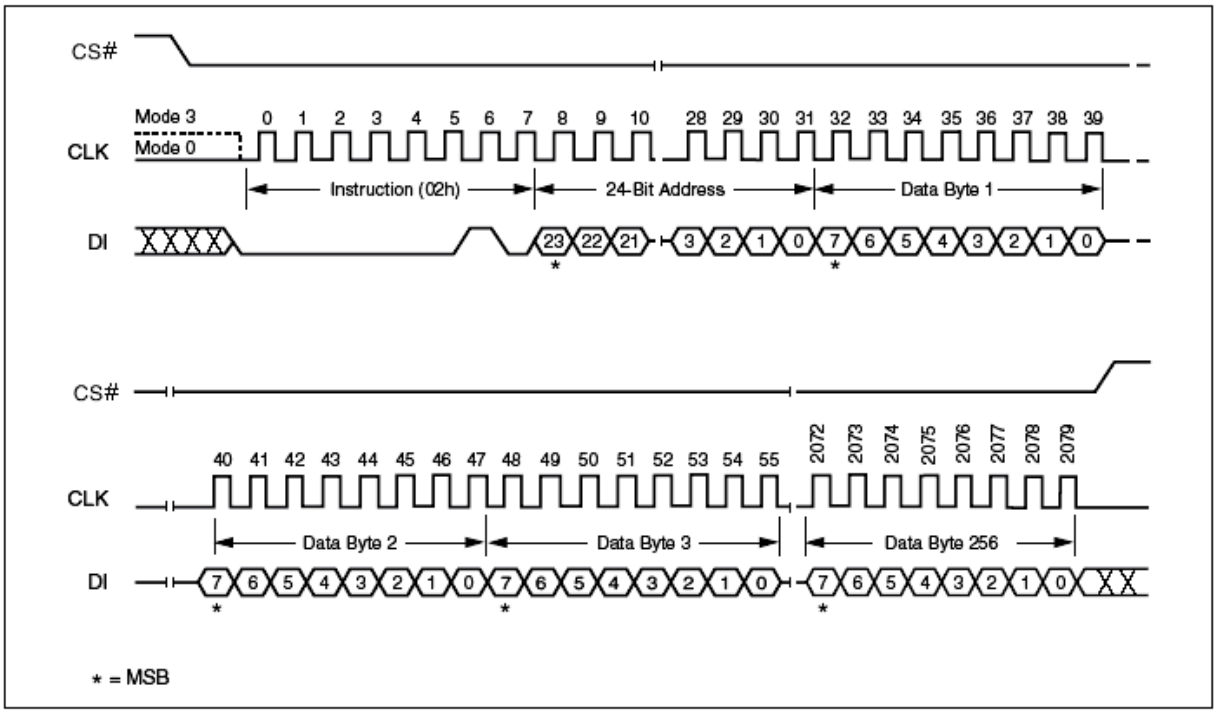


Figure 12. Page Program Instruction Sequence Diagram

Sector Erase (SE) (20h)

The Sector Erase (SE) instruction sets to 1 (FFh) all bits inside the chosen sector. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Sector Erase (SE) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code, and three address bytes on Serial Data Input (DI). Any address inside the Sector (see Table 2) is a valid address for the Sector Erase (SE) instruction. Chip Select (CS#) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in Figure 13. Chip Select (CS#) must be driven High after the eighth bit of the last address byte has been latched in, otherwise the Sector Erase (SE) instruction is not executed. As soon as Chip Select (CS#) is driven High, the self-timed Sector Erase cycle (whose duration is t_{SE}) is initiated. While the Sector Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Sector Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.
A Sector Erase (SE) instruction applied to a sector which is protected by the Block Protect (BP2, BP1, BP0) bits (see Table 3) is not executed.

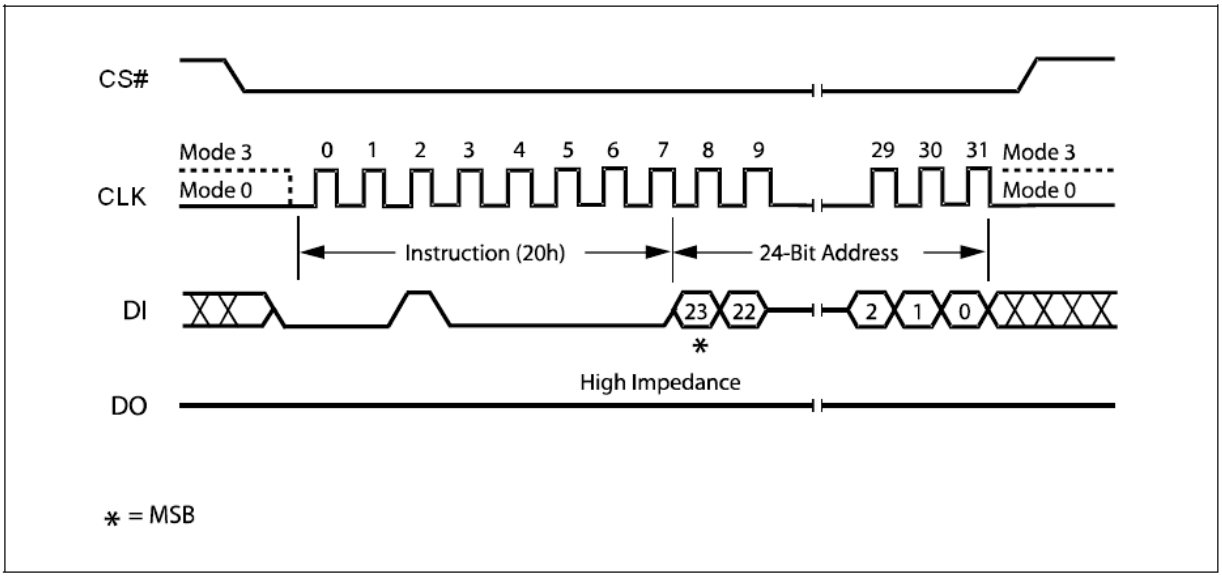


Figure 13. Sector Erase Instruction Sequence Diagram

32KB Half Block Erase (HBE) (52h)

The Half Block Erase (HBE) instruction sets to 1 (FFh) all bits inside the chosen block. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Half Block Erase (HBE) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code, and three address bytes on Serial Data Input (DI). Any address inside the Block (see Table 2) is a valid address for the Half Block Erase (HBE) instruction. Chip Select (CS#) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in Figure 14. Chip Select (CS#) must be driven High after the eighth bit of the last address byte has been latched in, otherwise the Half Block Erase (HBE) instruction is not executed. As soon as Chip Select (CS#) is driven High, the self-timed Half Block Erase cycle (whose duration is t_{HBE}) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Half Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Half Block Erase (HBE) instruction applied to a block which is protected by the Block Protect (BP2, BP1, BP0) bits (see Table 3) is not executed.

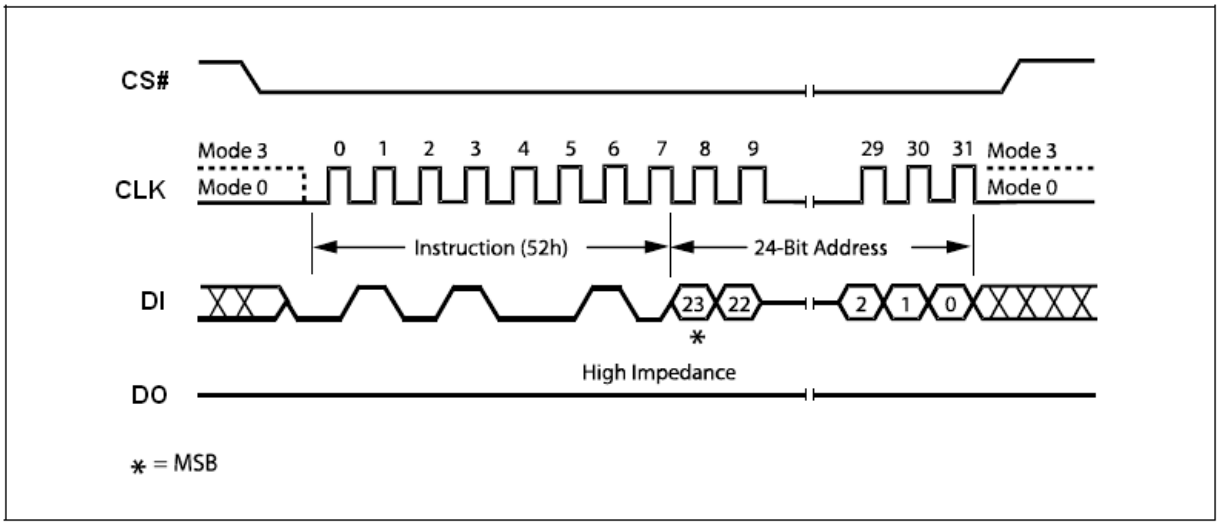


Figure 14. 32KB Half Block Erase Instruction Sequence Diagram

64KB Block Erase (BE) (D8h)

The Block Erase (BE) instruction sets to 1 (FFh) all bits inside the chosen block. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Block Erase (BE) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code, and three address bytes on Serial Data Input (DI). Any address inside the Block (see Table 2) is a valid address for the Block Erase (BE) instruction. Chip Select (CS#) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in Figure 15. Chip Select (CS#) must be driven High after the eighth bit of the last address byte has been latched in, otherwise the Block Erase (BE) instruction is not executed. As soon as Chip Select (CS#) is driven High, the self-timed Block Erase cycle (whose duration is t_{BE}) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.
A Block Erase (BE) instruction applied to a block which is protected by the Block Protect (BP2, BP1, BP0) bits (see Table 3) is not executed.

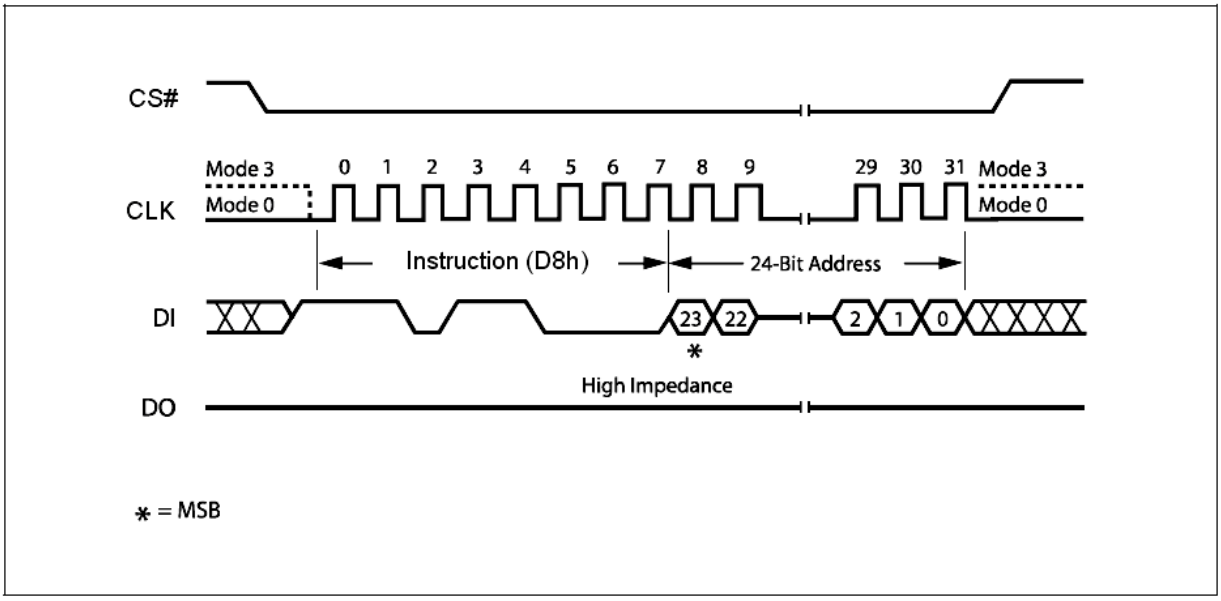


Figure 15. 64KB Block Erase Instruction Sequence Diagram

Chip Erase (CE) (C7h/60h)

The Chip Erase (CE) instruction sets all bits to 1 (FFh). Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Chip Erase (CE) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code on Serial Data Input (DI). Chip Select (CS#) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in Figure 16. Chip Select (CS#) must be driven High after the eighth bit of the instruction code has been latched in, otherwise the Chip Erase instruction is not executed. As soon as Chip Select (CS#) is driven High, the self-timed Chip Erase cycle (whose duration is t_{CE}) is initiated. While the Chip Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Chip Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

The Chip Erase (CE) instruction is executed only if all Block Protect (BP2, BP1, BP0) bits are 0. The Chip Erase (CE) instruction is ignored if one, or more blocks are protected.

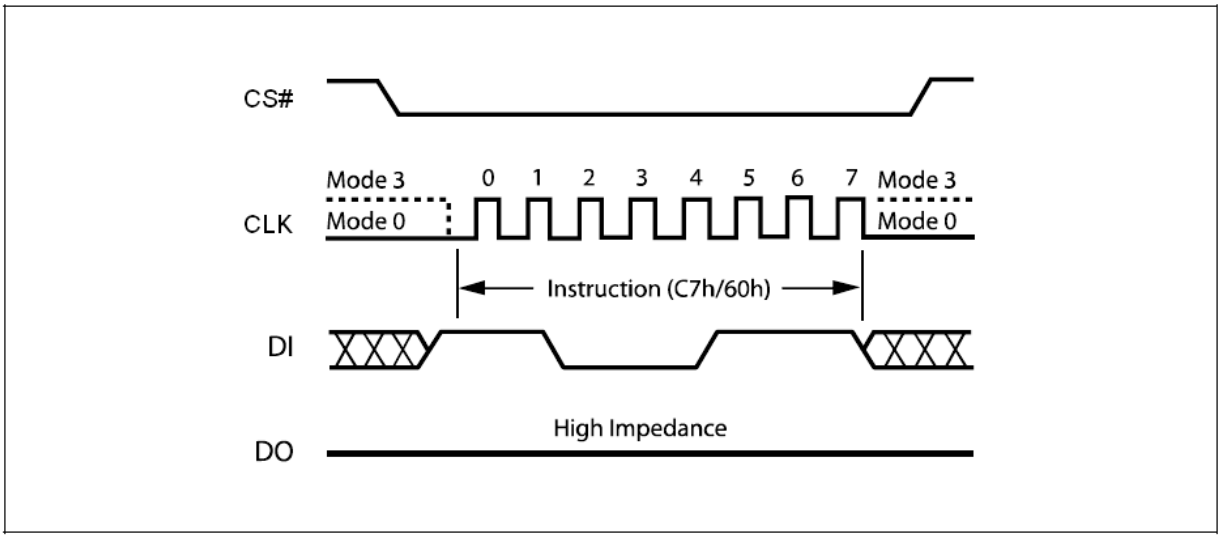


Figure 16. Chip Erase Instruction Sequence Diagram

Deep Power-down (DP) (B9h)

Executing the Deep Power-down (DP) instruction is the only way to put the device in the lowest consumption mode (the Deep Power-down mode). It can also be used as an extra software protection mechanism, while the device is not in active use, since in this mode, the device ignores all Write, Program and Erase instructions.

Driving Chip Select (CS#) High deselects the device, and puts the device in the Standby mode (if there is no internal cycle currently in progress). But this mode is not the Deep Power-down mode. The Deep Power-down mode can only be entered by executing the Deep Power-down (DP) instruction, to reduce the standby current (from I_{CC1} to I_{CC2}, as specified in Table 8.)

Once the device has entered the Deep Power-down mode, all instructions are ignored except the Release from Deep Power-down and Read Device ID (RDI) instruction. This releases the device from this mode. The Release from Deep Power-down and Read Device ID (RDI) instruction also allows the Device ID of the device to be output on Serial Data Output (DO).

The Deep Power-down mode automatically stops at Power-down, and the device always Powers-up in the Standby mode. The Deep Power-down (DP) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code on Serial Data Input (DI). Chip Select (CS#) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in Figure 17. Chip Select (CS#) must be driven High after the eighth bit of the instruction code has been latched in, otherwise the Deep Power-down (DP) instruction is not executed. As soon as Chip Select (CS#) is driven High, it requires a delay of t_{DP} before the supply current is reduced to I_{CC2} and the Deep Power-down mode is entered.

Any Deep Power-down (DP) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

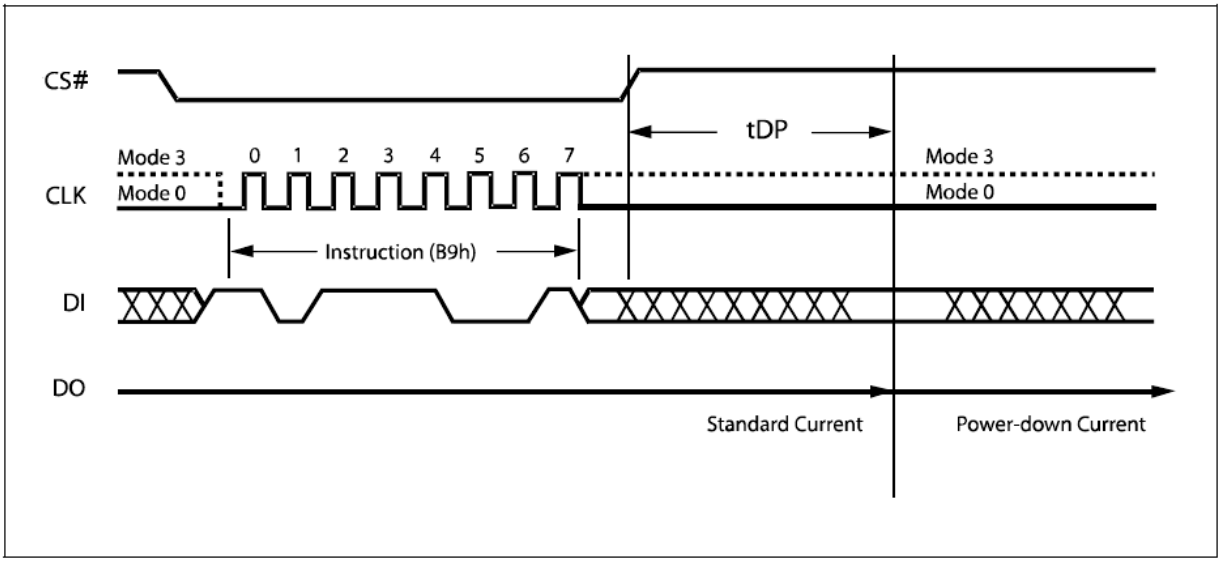


Figure 17. Deep Power-down Instruction Sequence Diagram

Release from Deep Power-down and Read Device ID (RDI)

Once the device has entered the Deep Power-down mode, all instructions are ignored except the Release from Deep Power-down and Read Device ID (RDI) instruction. Executing this instruction takes the device out of the Deep Power-down mode.
Please note that this is not the same as, or even a subset of, the JEDEC 16-bit Electronic Signature that is read by the Read Identifier (RDID) instruction. The old-style Electronic Signature is supported for reasons of backward compatibility, only, and should not be used for new designs. New designs should, instead, make use of the JEDEC 16-bit Electronic Signature, and the Read Identifier (RDID) instruction.

When used only to release the device from the power-down state, the instruction is issued by driving the CS# pin low, shifting the instruction code “ABh” and driving CS# high as shown in Figure 18. After the time duration of t_{RES1} (See AC Characteristics) the device will resume normal operation and other instructions will be accepted. The CS# pin must remain high during the t_{RES1} time duration.

When used only to obtain the Device ID while not in the power-down state, the instruction is initiated by driving the CS# pin low and shifting the instruction code “ABh” followed by 3-dummy bytes. The Device ID bits are then shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 19. The Device ID value for the device are listed in Table 5. The Device ID can be read continuously. The instruction is completed by driving CS# high.
When Chip Select (CS#) is driven High, the device is put in the Stand-by Power mode. If the device was not previously in the Deep Power-down mode, the transition to the Stand-by Power mode is immediate. If the device was previously in the Deep Power-down mode, though, the transition to the Standby Power mode is delayed by t_{RES2}, and Chip Select (CS#) must remain High for at least $t_{RES2\ (max)}$, as specified in Table 10. Once in the Stand-by Power mode, the device waits to be selected, so that it can receive, decode and execute instructions.
Except while an Erase, Program or Write Status Register cycle is in progress, the Release from Deep Power-down and Read Device ID (RDI) instruction always provides access to the 8bit Device ID of the device, and can be applied even if the Deep Power-down mode has not been entered.
Any Release from Deep Power-down and Read Device ID (RDI) instruction while an Erase, Program or Write Status Register cycle is in progress, is not decoded, and has no effect on the cycle that is in progress.

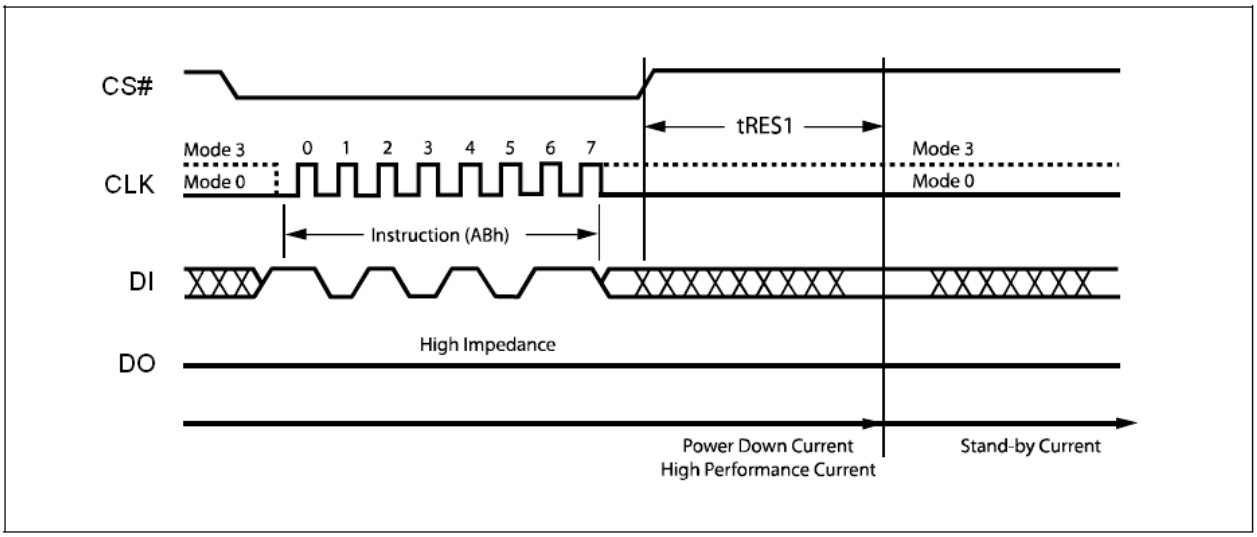


Figure 18. Release Power-down Instruction Sequence Diagram

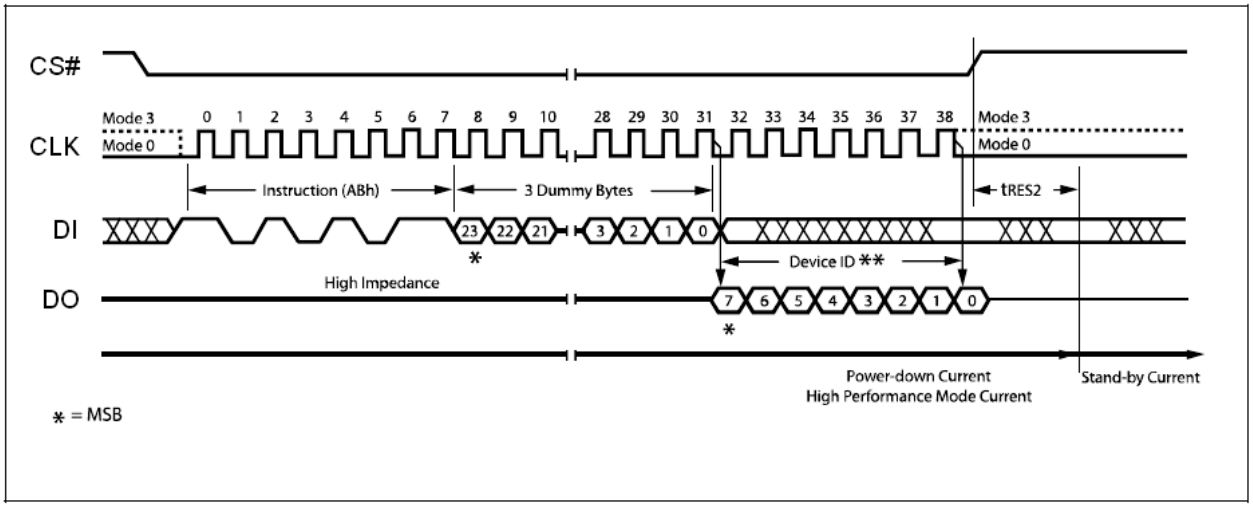


Figure 19. Release Power-down / Device ID Instruction Sequence Diagram

Read Manufacturer / Device ID (90h)

The Read Manufacturer/Device ID instruction is an alternative to the Release from Power-down / Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID.
The Read Manufacturer/Device ID instruction is very similar to the Release from Power-down / Device ID instruction. The instruction is initiated by driving the CS# pin low and shifting the instruction code "90h" followed by a 24-bit address of 000000h. After which, the Manufacturer ID for Eon (1Ch) and the Device ID are shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 20. The Device ID values for the device are listed in Table 5. If the 24-bit address is initially set to 000001h the Device ID will be read first

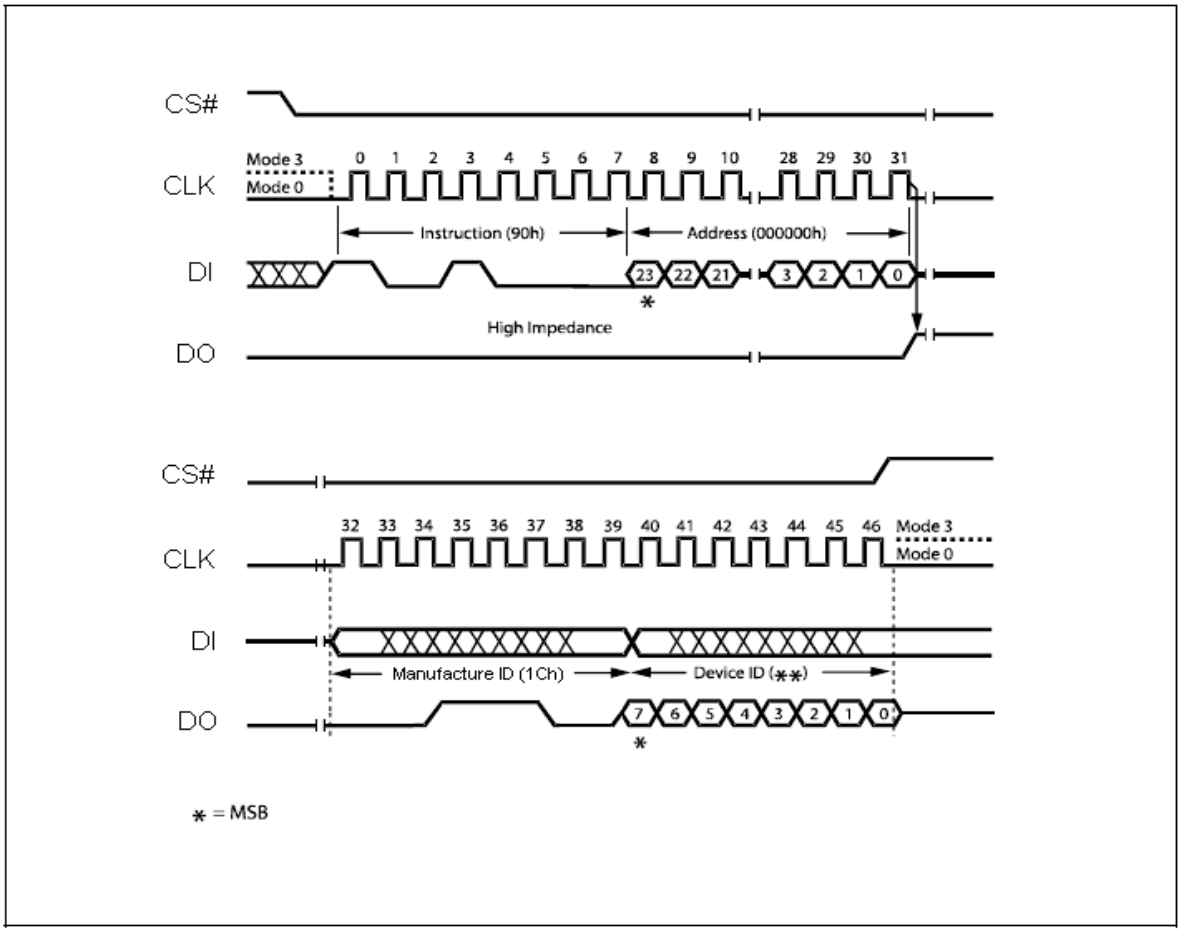


Figure 20. Read Manufacturer / Device ID Diagram

Read Identification (RDID) (9Fh)

The Read Identification (RDID) instruction allows the 8-bit manufacturer identification to be read, followed by two bytes of device identification. The device identification indicates the memory type in the first byte , and the memory capacity of the device in the second byte .

Any Read Identification (RDID) instruction while an Erase or Program cycle is in progress, is not decoded, and has no effect on the cycle that is in progress. The Read Identification (RDID) instruction should not be issued while the device is in Deep Power down mode.

The device is first selected by driving Chip Select Low. Then, the 8-bit instruction code for the instruction is shifted in. This is followed by the 24-bit device identification, stored in the memory, being shifted out on Serial Data Output, each bit being shifted out during the falling edge of Serial Clock. The instruction sequence is shown in Figure 21. The Read Identification (RDID) instruction is terminated by driving Chip Select High at any time during data output.

When Chip Select is driven High, the device is put in the Standby Power mode. Once in the Standby Power mode, the device waits to be selected, so that it can receive, decode and execute instructions.

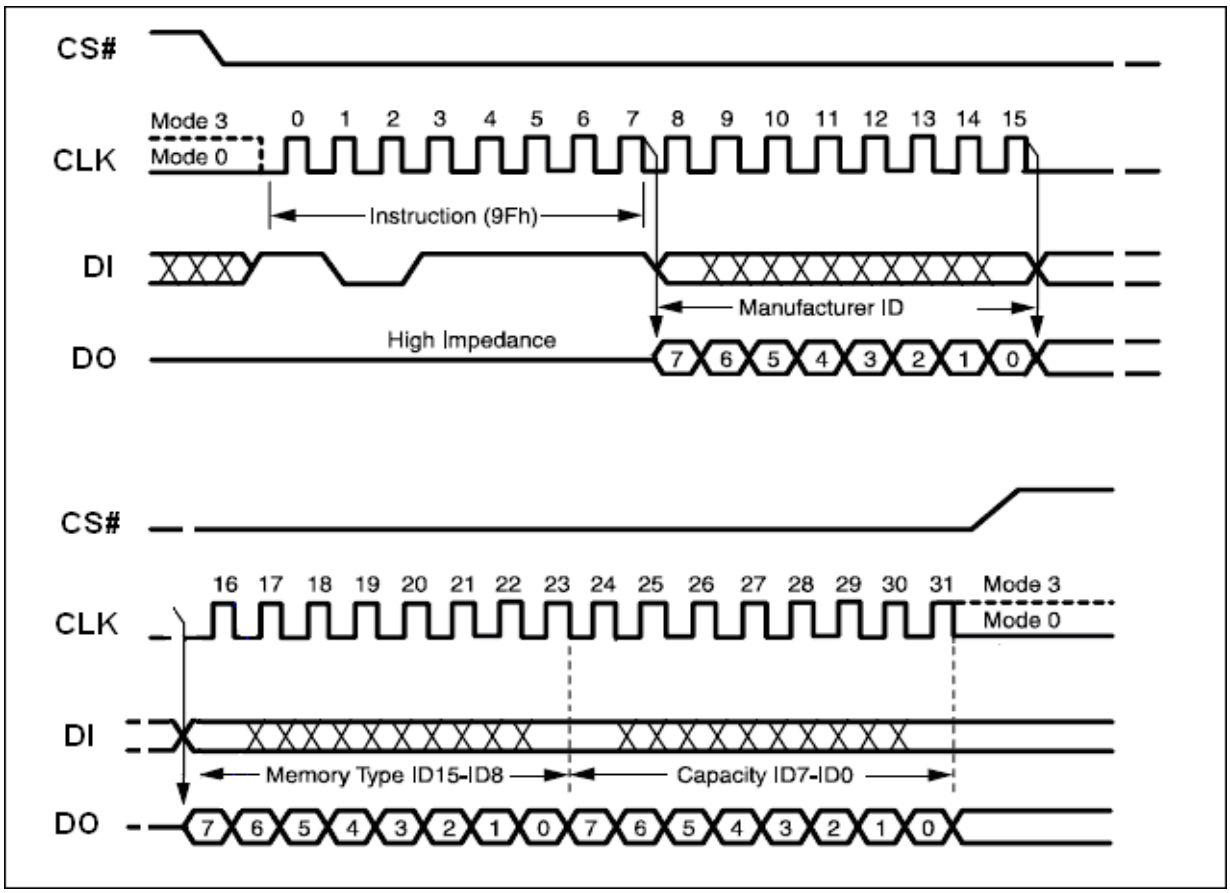


Figure 21. Read Identification (RDID)

Power-up Timing

All functionalities and DC specifications are specified for a V_{CC} ramp rate of greater than 1V per 100 ms. See Table 7 and Figure 22 for more information.

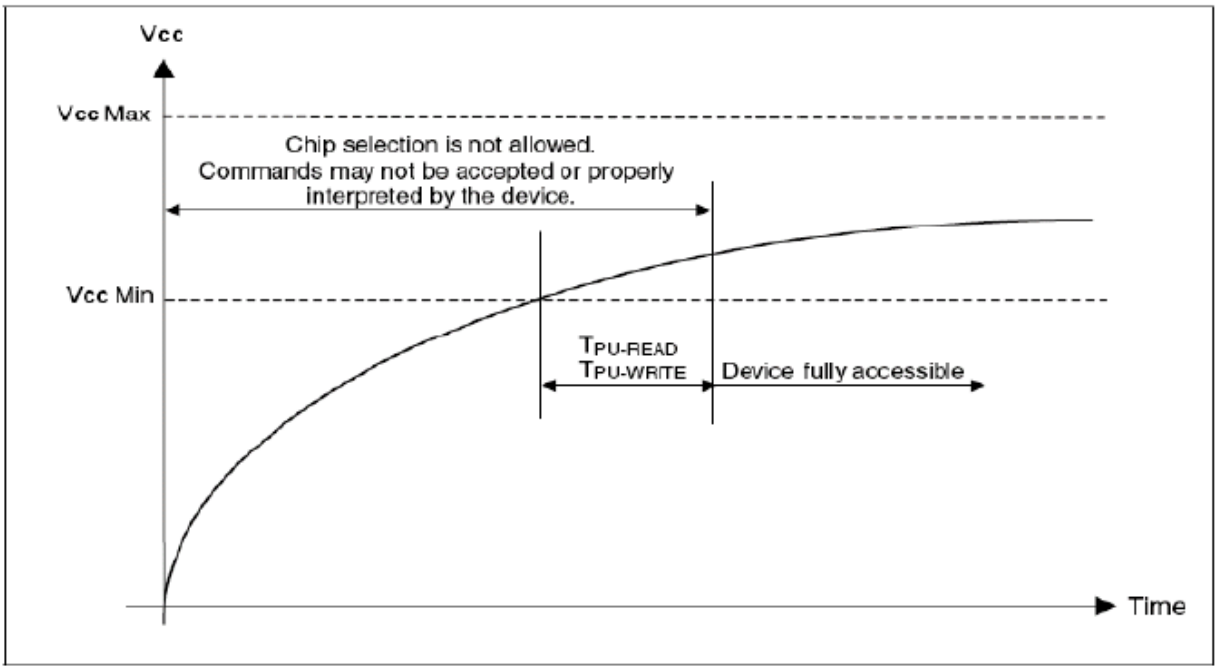


Figure 22. Power-up Timing

Table 7. Power-Up Timing and Write Inhibit Threshold

Symbol	Parameter	Min.	Unit
TPU-READ(1)	VCC Min to Read Operation	100	μs
TPU-WRITE(1)	VCC Min to Write Operation	100	μs

Note:
1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

INITIAL DELIVERY STATE

The device is delivered with the memory array erased: all bits are set to 1 (each byte contains FFh). The Status Register contains 00h (all Status Register bits are 0).

Table 8. DC Characteristics

(T_A = - 40°C to 85°C; V_{CC} = 2.3-3.6V)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{LI}	Input Leakage Current		-	1	± 2	µA
I_{LO}	Output Leakage Current		-	1	± 2	µA
I_{CC1}	Standby Current	CS# = V_{CC}, V_{IN} = V_{SS} or V_{CC}	-	1	20	µA
I_{CC2}	Deep Power-down Current	CS# = V_{CC}, V_{IN} = V_{SS} or V_{CC}	-	1	20	µA
I_{CC3}	Operating Current (READ)	CLK = 0.1 V_{CC} / 0.9 V_{CC} at 104MHz, DQ = open	-	5	10	mA
		CLK = 0.1 V_{CC} / 0.9 V_{CC} at 104MHz for Dual Output Read, DQ = open	-	7	13	mA
I_{CC4}	Operating Current (PP)	CS# = V_{CC}	-	9	20	mA
I_{CC5}	Operating Current (WRSR / WRSR4)	CS# = V_{CC}	-	-	12	mA
I_{CC6}	Operating Current (SE)	CS# = V_{CC}	-	9	20	mA
I_{CC7}	Operating Current (BE)	CS# = V_{CC}	-	9	20	mA
V_{IL}	Input Low Voltage		-0.5	-	0.2 V_{CC}	V
V_{IH}	Input High Voltage		0.7V_{CC}	-	V_{CC}+0.4	V
V_{OL}	Output Low Voltage	I_{OL} =100 µA, V_{CC}=V_{CC} Min.	-	-	0.3	V
V_{OH}	Output High Voltage	I_{OH} = –100 µA , V_{CC}=V_{CC} Min.	V_{CC}-0.2	-	-	V

Note:
1. Erase current measure on all cells = '0' state.

Table 9. AC Measurement Conditions

Symbol	Parameter	Min.	Max.	Unit
C_L	Load Capacitance	30		pF
	Input Rise and Fall Times		5	ns
	Input Pulse Voltages	0.2V_{CC} to 0.8V_{CC}		V
	Input Timing Reference Voltages	0.3V_{CC} to 0.7V_{CC}		V
	Output Timing Reference Voltages	V_{CC} / 2		V

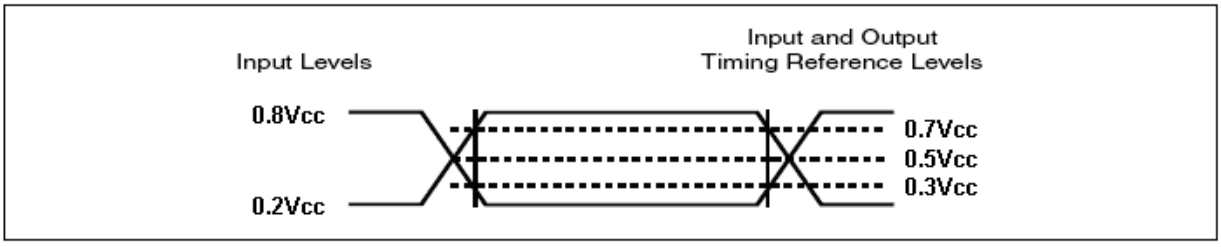


Figure 23. AC Measurement I/O Waveform

Table 10. AC Characteristics

(T_A = - 40°C to 85°C; V_{CC} = 2.3-3.6V)

Symbol	Alt	Parameter		Min	Typ	Max	Unit
F_R	f_C	Clock Frequency for all other instruction	2.7V ≦ V_{CC} ≦ 3.6V	D.C.	-	104	MHz
			2.3V ≦ V_{CC} < 2.7V	D.C	-	86	MHz
f_R		Clock Frequency for Read Data instruction (03h)		D.C.	-	50	MHz
t_{CH}[1]		Serial Clock High Time	2.7V ≦ V_{CC} ≦ 3.6V	3.5	-	-	ns
			2.3V ≦ V_{CC} < 2.7V	4	-	-	ns
t_{CL}[1]		Serial Clock Low Time	2.7V ≦ V_{CC} ≦ 3.6V	3.5	-	-	ns
			2.3V ≦ V_{CC} < 2.7V	4	-	-	ns
t_{CLCH}[2]		Serial Clock Rise Time (Slew Rate)		0.1	-	-	V / ns
t_{CHCL}[2]		Serial Clock Fall Time (Slew Rate)		0.1	-	-	V / ns
t_{SLCH}	t_{CSS}	CS# Active Setup Time (Relative to CLK)		5	-	-	ns
t_{CHSH}		CS# Active Hold Time (Relative to CLK)		5	-	-	ns
t_{SHCH}		CS# Not Active Setup Time (Relative to CLK)		5	-	-	ns
t_{CHSL}		CS# Not Active Hold Time (Relative to CLK)		5	-	-	ns
t_{SHSL}	t_{CSH}	CS# High Time		30	-	-	ns
t_{SHQZ}[2]	t_{DIS}	Output Disable Time		-	-	6	ns
t_{CLQX}	t_{HO}	Output Hold Time		0	-	-	ns
t_{DVCH}	t_{DSU}	Data In Setup Time		2	-	-	ns
t_{CHDX}	t_{DH}	Data In Hold Time		5	-	-	ns
t_{CLQV}	t_V	Output Valid from CLK for 30 pF	2.7V ≦ V_{CC} ≦ 3.6V	-	-	8	ns
			2.3V ≦ V_{CC} < 2.7V	-	-	10	ns
		Output Valid from CLK for 15 pF	2.7V ≦ V_{CC} ≦ 3.6V	-	-	6	ns
			2.3V ≦ V_{CC} < 2.7V	-	-	8	ns
t_{WHSL}[3]		Write Protect Setup Time before CS# Low		20	-	-	ns
t_{SHWL}[3]		Write Protect Hold Time after CS# High		100	-	-	ns
t_{DP}[2]		CS# High to Deep Power-down Mode		-	-	3	µs
t_{RES1}[2]		CS# High to Standby Mode without Electronic Signature read		-	-	3	µs
t_{RES2}[2]		CS# High to Standby Mode with Electronic Signature read		-	-	1.8	µs
t_W		Write Status Register Cycle Time	2.7V ≦ V_{CC} ≦ 3.6V	-	4	30	ms
			2.3V ≦ V_{CC} < 2.7V	-	10	50	ms
t_{PP}		Page Programming Time	2.7V ≦ V_{CC} ≦ 3.6V	-	0.6	3	ms
			2.3V ≦ V_{CC} < 2.7V	-	0.9	5	ms
t_{SE}		Sector Erase Time (4KB)	2.7V ≦ V_{CC} ≦ 3.6V	-	50	300	ms
			2.3V ≦ V_{CC} < 2.7V	-	150	1000	ms
t_{HBE}		32KB Block Erase Time	2.7V ≦ V_{CC} ≦ 3.6V	-	0.15	1	s
			2.3V ≦ V_{CC} < 2.7V	-	0.25	2	s

Table 10. AC Characteristics- Continued

Symbol	Alt	Parameter		Min	Typ	Max	Unit
t_{BE}		64KB Block Erase Time	2.7V ≦ V_{CC} ≦ 3.6V	-	0.3	2	s
			2.3V ≦ V_{CC} < 2.7V	-	0.4	3	s
t_{CE}		Chip Erase Time	2.7V ≦ V_{CC} ≦ 3.6V	-	0.7	4	s
			2.3V ≦ V_{CC} < 2.7V	-	0.9	6	s
t_{SR}		Software Reset Latency	WIP = write operation	-	-	28	µs
			WIP = not in write operation	-	-	0	µs

Note:
1. t_{CH} + t_{CL} must be greater than or equal to 1/ f_C
2. Value guaranteed by characterization, not 100% tested in production.

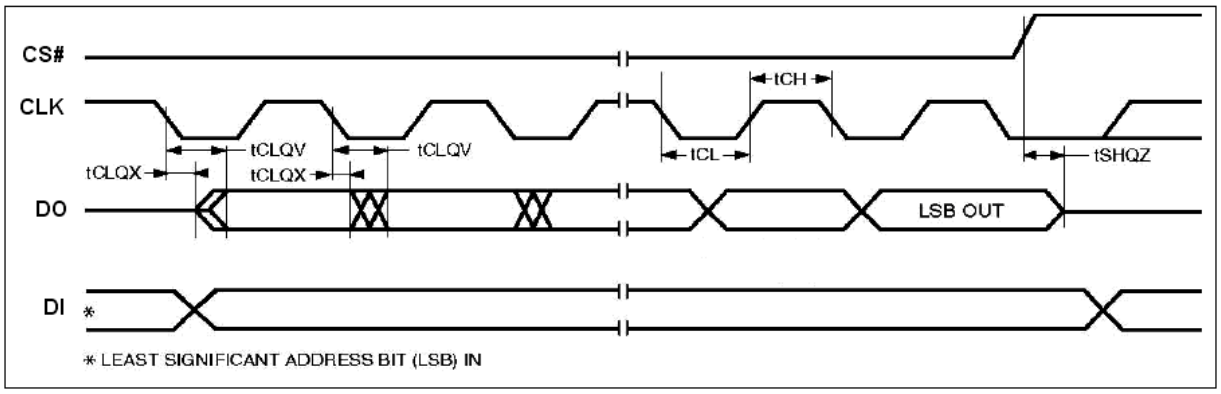


Figure 24. Serial Output Timing

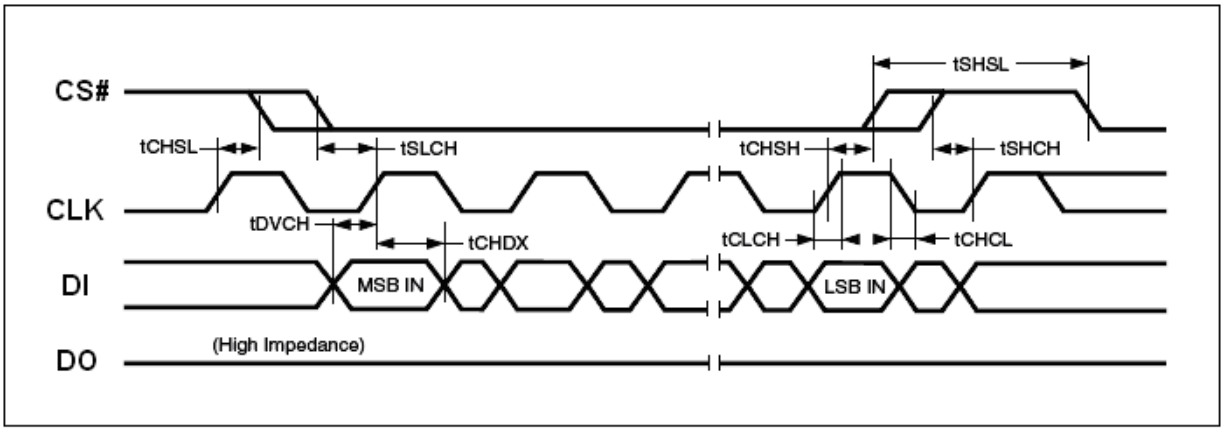


Figure 25. Input Timing

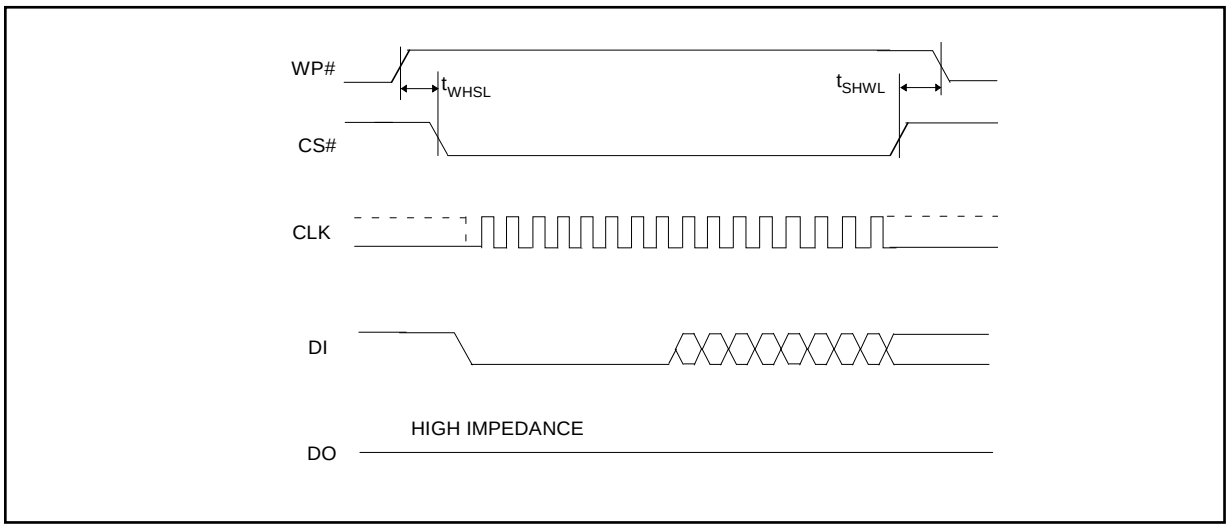


Figure 26. Write Protect setup and hold timing during WRSR when SRP = 1

ABSOLUTE MAXIMUM RATINGS

Stresses above the values so mentioned above may cause permanent damage to the device. These values are for a stress rating only and do not imply that the device should be operated at conditions up to or above these values. Exposure of the device to the maximum rating values for extended periods of time may adversely affect the device reliability.

Parameter	Value	Unit
Storage Temperature	-65 to +150	°C
Output Short Circuit Current[1]	200	mA
Input and Output Voltage (with respect to ground)[2]	-0.5 to +4.0	V
V_{CC}	-0.5 to +4.0	V

Note:

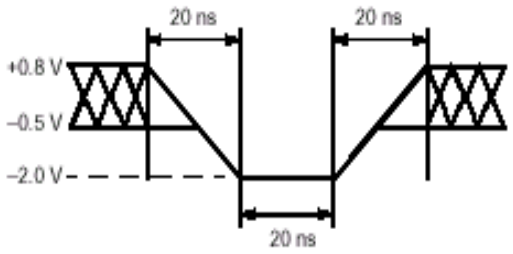
1. No more than one output shorted at a time. Duration of the short circuit should not be greater than one second.
2. Minimum DC voltage on input or I/O pins is -0.5V. During voltage transitions, inputs may undershoot V_{SS} to -1.0V for periods of up to 50ns and to -2.0 V for periods of up to 20ns. See figure below. Maximum DC voltage on output and I/O pins is V_{CC} + 0.5V. During voltage transitions, outputs may overshoot to V_{CC} + 1.5V for periods up to 20ns. See figure below.

RECOMMENDED OPERATING RANGES [1]

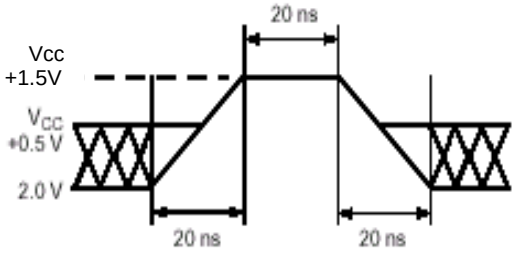
Parameter	Value	Unit
Ambient Operating Temperature Industrial Devices	-40 to 85	°C
Operating Supply Voltage V_{CC}	Full: 2.3 to 3.6	V

Note:

1. Recommended Operating Ranges define those limits between which the functionality of the device is guaranteed.



Maximum Negative Overshoot Waveform



Maximum Positive Overshoot Waveform

Table 11. CAPACITANCE

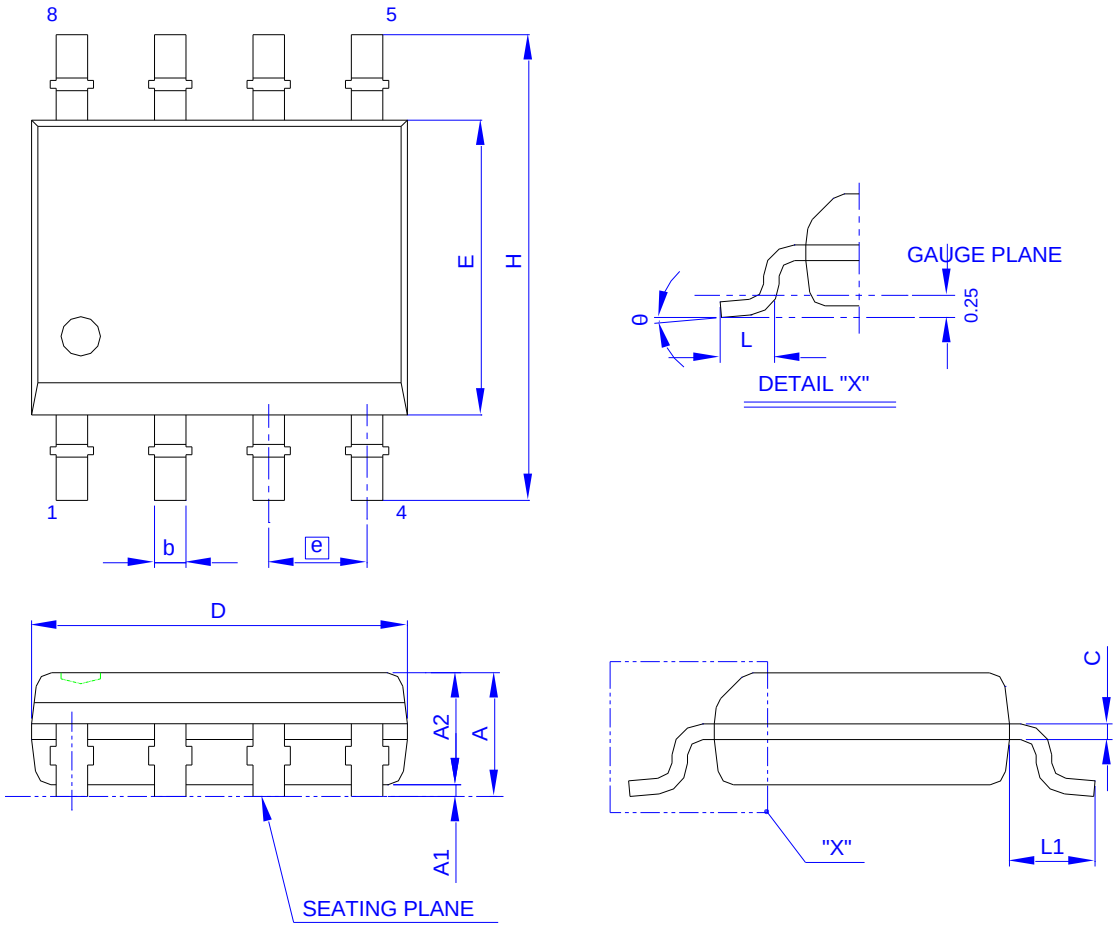
(V_{CC} = 2.3-3.6V)

Parameter Symbol	Parameter Description	Test Setup	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8	pF

Note : Sampled only, not 100% tested, at T_A = 25°C and a frequency of 20MHz.

PACKAGE MECHANICAL

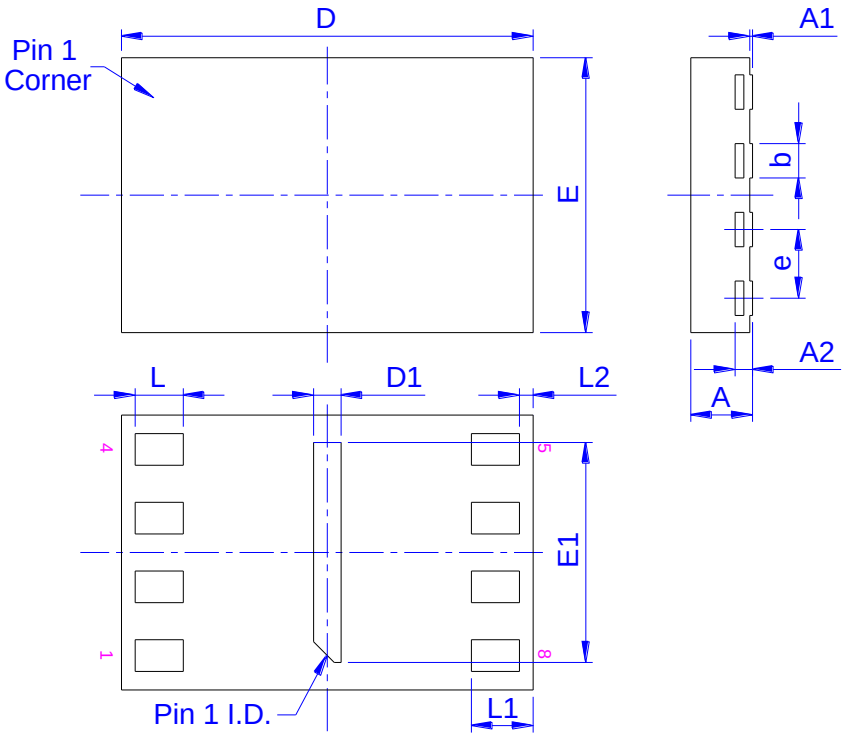
Figure 27. SOP 8 (150 mil)



Symbol	Dimension in mm			Dimension in inch			Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max		Min	Norm	Max	Min	Norm	Max
A	1.35	1.60	1.75	0.053	0.063	0.069	D	4.80	4.90	5.00	0.189	0.193	0.197
A_1	0.10	0.15	0.25	0.004	0.006	0.010	E	3.80	3.90	4.00	0.150	0.154	0.157
A_2	1.25	1.45	1.55	0.049	0.057	0.061	L	0.40	0.66	0.86	0.016	0.026	0.034
b	0.33	0.406	0.51	0.013	0.016	0.020	e	1.27 BSC			0.050 BSC		
c	0.19	0.203	0.25	0.0075	0.008	0.010	L_1	1.00	1.05	1.10	0.039	0.041	0.043
H	5.80	6.00	6.20	0.228	0.236	0.244	θ	0°	---	8°	0°	---	8°

Controlling dimension : millimenter

Figure 28. USON (8L 2x3x0.45mm)



Symbol	Dimension in mm		
	Min.	Norm.	Max.
A	0.40	0.45	0.50
A1	0.00	-	0.05
A2		0.152 REF	
b	0.20	0.25	0.30
D	2.90	3.00	3.10
D1	0.10	0.20	0.30
E	1.90	2.00	2.10
E1	1.50	1.60	1.70
e		0.50 BSC	
L	0.30	-	-
L1	0.40	0.45	0.50
L2	-	-	0.15

Controlling dimension: millimeter
(Revision date : Dec 22 2016)

ORDERING INFORMATION

EN25E10A - 104 G I P 2AQ

DIFFERENTIATION CODE

PACKAGING CONTENT
P = RoHS, Halogen-Free and REACH compliant

TEMPERATURE RANGE
I = Industrial (-40°C to +85°C)

PACKAGE
G = 8-pin 150mil SOP
XF = 8-pin USON (2x3x0.45 mm)

SPEED
104 = 104 MHz

BASE PART NUMBER
EN = Eon Silicon Solution Inc.
25E = 3V Serial Flash with 4KB Uniform-Sector, Dual
10 = 1 Megabit (128K x 8)
A = version identifier

Revisions List

Revision No	Description	Date
1.0	Initial Release	2021/08/16
1.1	1. Modify the specification of tCE 2. Delete Plastic Packages Temperature	2021/09/10

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