

General Description

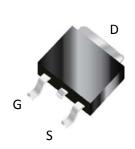
These N-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

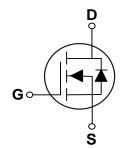
BV _{DSS}	R _{DS(ON)}	I _D
100 V	115 mΩ	12 A

Features

- 100V, 12A, $R_{DS(ON)}$ =115m Ω @ V_{GS} =10V
- · Improved dv/dt capability
- · Fast switching
- · Green Device Available

TO-252 Pin Configuration





Applications

- Networking
- · Load Switch
- LED applications

Symbol	Parameter	Rating	Units
V _{DS}	Drain-Source Voltage	100	V
V_{GS}	Gate-Source Voltage	±20	V
1	Drain Current - Continuous (T _C =25°C)	12	Α
I _D	Drain Current - Continuous (T _C =100°C)	7.6	^
I _{DM}	Drain Current - Pulsed (NOTE 1)	48	Α
E _{AS}	Single Pulse Avalanche Energy (NOTE 2)	6	mJ
I _{AS}	Single Pulse Avalanche Current (NOTE 2)	11	Α
P_{D}	Power Dissipation (T _C =25°C)	34.7	W
' D	Power Dissipation - Derate above 25°C	0.27	W/°C
T _J	Operating Junction Temperature Range	-50 to 150	°C
T _{STG}	Storage Temperature Range	-50 to 150	°C
Marking Code		NM115 / DD0956	

Thermal Characteristics						
Symbol	Parameter	Тур.	Max.	Unit		
$R_{\theta JA}$	Thermal Resistance Junction to Ambient		62	°C/W		
$R_{ heta JC}$	Thermal Resistance Junction to Case		3.1	°C/W		





Electrical Characteristics (T_J=25°C, unless otherwise noted)

Off Characteristics

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V , I _D =250uA	100			V
I _{DSS}	IDrain-Source Leakage Current	V_{DS} =100V , V_{GS} =0V , T_J =25°C		-	1	uA
		V _{DS} =80V , V _{GS} =0V , T _J =125°C			10	uA
I_{GSS}	Gate-Source Leakage Current	V_{GS} =±20V , V_{DS} =0V			±100	nA

On Characteristics

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
R _{DS(ON)}	IStatic Drain-Source On-Resistance	V _{GS} =10V , I _D =10A		95	115	mΩ
		V _{GS} =4.5V , I _D =8A		100	125	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}$, $I_D=250uA$	1.2	1.6	2.2	V
gfs	Forward Transconductance	V _{DS} =10V , I _D =2A		8.7		S

Dynamic and switching Characteristics

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
Q_g	Total Gate Charge (NOTE 3 \ 4)			20	40	
Q_gs	Gate-Source Charge (NOTE 3 · 4)	V_{DS} =50V , V_{GS} =10V , I_{D} =2A		3.2	6	nC
Q_{gd}	Gate-Drain Charge (NOTE 3 · 4)			3.6	7	
$T_{d(on)}$	Turn-On Delay Time (NOTE 3 \ 4)			18	36	
T_r	Rise Time (NOTE 3 \ 4)	V_{DD} =50V , V_{GS} =10V , R_{G} =3.3 Ω , I_{D} =1A		4	8	nS
$T_{d(off)}$	Turn-Off Delay Time (NOTE 3 \ 4)			40	80	113
T_f	Fall Time (NOTE 3 \ 4)			3	6	
C _{iss}	Input Capacitance			1400	2800	
C _{oss}	Output Capacitance	V_{DS} =25V , V_{GS} =0V , f=1MHz		60	120	pF
C_{rss}	Reverse Transfer Capacitance			35	70	
R_g	Gate Resistance	V_{DS} =0V , V_{GS} =0V , f=1MHz		2	4	Ω

Drain-Source Diode Characteristics and Ratings

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
Is	Continuous Source Current	−-V _G =V _D =0V , Force Current			12	Α
I _{SM}	Pulsed Source Current				24	Α
V_{SD}	Diode Forward Voltage	V_{GS} =0V , I_{S} =1A , T_{J} =25 $^{\circ}$ C			1	V
trr	Reverse Recovery Time (NOTE 3)	-I _S =1A , di/dt=100A/μs , T _J =25°C		38		nS
Qrr	Reverse Recovery Charge (NOTE 3)			27		nC

NOTES:

- 1. Repetitive Rating : Pulsed width limited by maximum junction temperature.
- 2. $\rm V_{DD}$ =25V, $\rm V_{GS}$ =10V, L=0.1mH, $\rm I_{AS}$ =11A, $\rm R_{G}$ =25 Ω , Starting $\rm T_{J}$ =25 ^{o}C .
- 3. The data tested by pulsed , pulse width \leq 300us , duty cycle \leq 2%.
- 4. Essentially independent of operating temperature.





Characteristics Curves

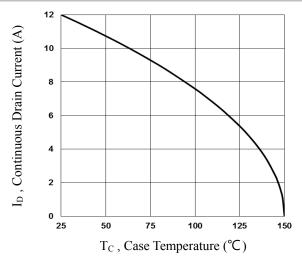


Fig.1 Continuous Drain Current vs. Tc

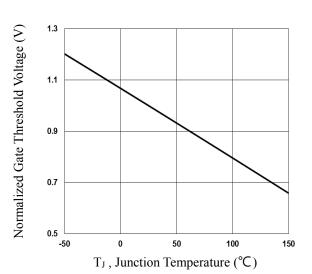


Fig.3 Normalized V_{th} vs. T_J

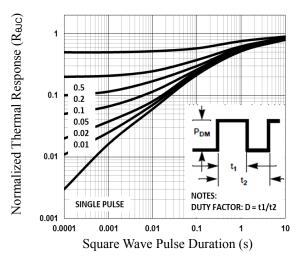


Fig.5 Normalized Transient Impedance

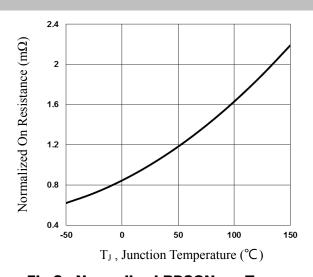


Fig.2 Normalized RDSON vs. T_J

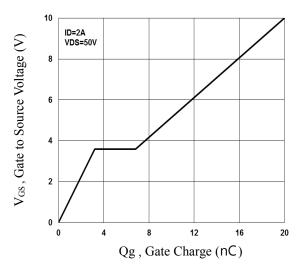


Fig.4 Gate Charge Waveform

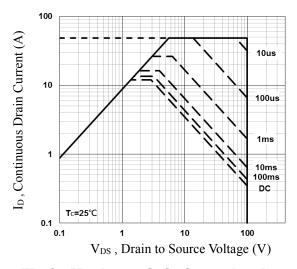
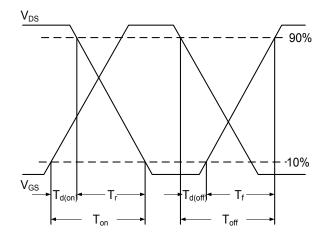


Fig.6 Maximum Safe Operation Area





Characteristics Curves



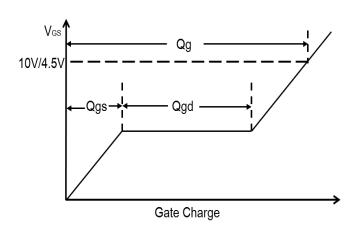
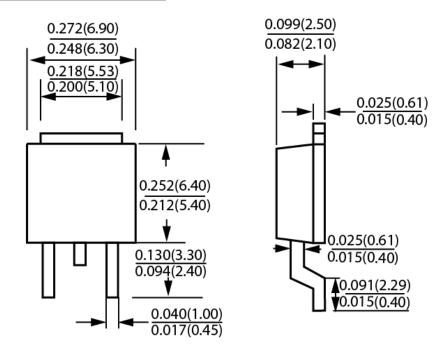


Fig.7 Switching Time Waveform

Fig.8 Gate Charge Waveform

Package Outline Dimensions



TO-252Dimensions in inches and (millimeters)





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