

256K X 32 BIT HIGH SPEED CMOS SRAM

Revision History AS7C325632-10BIN 90ball TFBGA PACKAGE

Revision	Details	Date
Rev 1.0	Initial Issue	Jan. 2017
Rev 1.1	Revise Package outline dimension	Sep. 2019

Alliance Memory Inc. 511 Taylor Way, San Carlos, CA 94070 TEL: (650) 610-6800 FAX: (650) 620-9211 Alliance Memory Inc. reserves the right to change products or specification without notice

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FEATURES

Fast access time : 10nsLow power consumption:

Operating current : 125mA (TYP.) Standby current : 4mA (TYP.)

■ Single 3.3V power supply

■ All inputs and outputs TTL compatible

Fully static operationTri-state output

■ Data byte control : B0# (DQ0 ~ DQ7)

B1# (DQ8 ~ DQ15) B2# (DQ16~DQ23) B3# (DQ24~DQ31)

■ Data retention voltage : 1.5V (MIN.)

ROHS Compliant/Pb and Halogen free

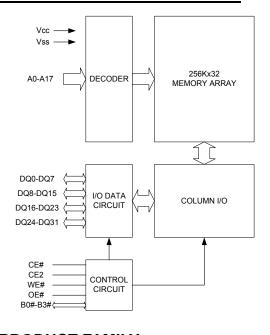
■ Package: 90-ball 8mm x 13mm TFBGA

GENERAL DESCRIPTION

The AS7C325632-10BIN is a 8M-bit high speed CMOS static random access memory organized as 256K words by 32 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

The AS7C325632-10BIN operates from a single power supply of 3.3V and all inputs and outputs are fully TTL compatible

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A17	Address Inputs
DQ0 - DQ31	Data Inputs/Outputs
CE#, CE2	Chip Enable Input
WE#	Write Enable Input
OE#	Output Enable Input
B0# - B3#	Byte Control
Vcc	Power Supply
Vss	Ground
NC	No Connection

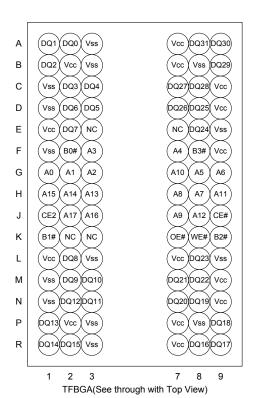
PRODUCT FAMILY

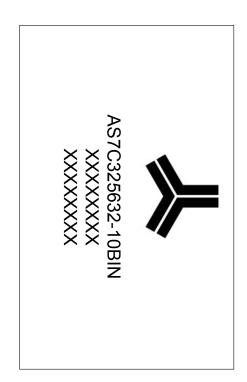
Product	Operating	V Banga	Spood	Power Dissipation		
Family	Temperature	V _{CC} Range	Speed	Standby(I _{SB1} ,TYP.)	Operating(Icc, TYP.)	
AS7C325632-10BIN	-40 ~ 85℃	2.7 ~ 3.6V	10ns	4mA	125mA	

ORDERING INFORMATION

Package Type	Access Time (Speed/ns)	Temperature Range(°C)	Packing Type	Alliance Part Number
90-ball (8mm x 13mm)			Tray	AS7C325632-10BIN
TFBGA	10	3 30 0	Tape Reel	AS7C325632-10BINTR

PIN CONFIGURATION





TFBGA (Top View)

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ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on Vcc relative to Vss	V _{T1}	-0.5 to 4.6	V
Voltage on any other pin relative to Vss	V _{T2}	-0.5 to Vcc+0.5	V
Operating Temperature	TA	-40 to 85(I grade)	$^{\circ}\!\mathbb{C}$
Storage Temperature	T _{STG}	-65 to 150	$^{\circ}\!\mathbb{C}$
Power Dissipation	P _D	1	W
DC Output Current	louт	50	mA

^{*}Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE#	CE2	OE#	E# WE# B0# I		B1#	B1# B0#		I/O OPERATION				SUPPLY
WIODE	ODE CE# CE2 OE# WE# B0# B1# B0		DU#	B1#	DQ0-7	DQ8-15	DQ16-23	DQ24-31	CURRENT				
Standby	Н	Χ	Х	Χ	Χ	Χ	Χ	Χ	High-Z	High-Z	High-Z	High-Z	lan:
Standby	Χ	L	Х	Χ	Χ	Х	Χ	Χ	High-Z	High-Z	High-Z	High-Z	I _{SB1}
Output Disable	L	Н	Н	Н	Χ	Χ	Х	Χ	High-Z	High-Z	High-Z	High-Z	Icc
Output Disable	L	Н	Х	Χ	Ι	Н	Н	Н	High-Z	High-Z	High-Z	High-Z	icc
	L	Н	L	Η	L	Н	Н	Н	Dout	High-Z	High-Z	High-Z	
	L	Н	L	Н	Н	L	Н	Н	High-Z	Dout	High-Z	High-Z	
Read	L	Н	L	Н	Н	Н	L	Н	High-Z	High-Z	Dout	High-Z	Icc
	L	Н	L	Н	Н	Н	Н	L	High-Z	High-Z	High-Z	Dout	
	L	Н	L	Н	L	L	L	L	Dout	D оит	D оит	Dоит	
	L	Н	Х	L	L	Н	Н	Н	Din	High-Z	High-Z	High-Z	
	L	Н	Χ	L	Н	L	Н	Н	High-Z	Din	High-Z	High-Z	
Write	L	Н	Χ	L	Н	Н	L	Н	High-Z	High-Z	Din	High-Z	Icc
	L	Н	Х	L	Н	Н	Н	L	High-Z	High-Z	High-Z	Din	
	L	Н	Х	L	L	L	L	L	D_IN	Din	Din	D _{IN}	

Note: $H = V_{IH}$, $L = V_{IL}$, X = Don't care.

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DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYM.	TEST CONDITION		MIN.	TYP. *4	MAX.	UNIT
Supply Voltage	Vcc			2.7	3.3	3.6	V
Input High Voltage	V _{IH} *1			2.2	-	V _{CC} +0.3	V
Input Low Voltage	V _{IL} *2			- 0.3	-	0.8	V
Input Leakage Current	ILI	$V_{CC} \ge V_{IN} \ge V_{SS}$		- 1	-	1	μA
Output Leakage Current	Іго	Vcc ≧ Vouт ≧ Vss, Output Disabled		- 1	-	1	μA
Output High Voltage	Vон	I _{OH} = -4mA		2.4	-	-	V
Output Low Voltage	Vol	I _{OL} = 8mA		-	-	0.4	V
Average Operating Power supply Current	Icc	CE# \leq 0.2V and CE2 \geq Vcc-0.2V, other pins at 0.2V or Vcc-0.2V, I _{I/O} = 0mA; f=max.	10	-	125	180	mA
Standby Power Supply Current	I _{SB1}	CE# \geq V _{CC} - 0.2V; other pins at 0.2V or V _{CC} -0.2V.		-	4	40	mA

- 1. $V_{IH}(MAX.) = V_{CC} + 2.0V$ for pulse width less than 6ns.
- 2. V_{IL}(MIN.) = Vss 2.0V for pulse width less than 6ns.
 3. Over/Undershoot specifications are characterized on engineering evaluation stage, not for mass production test.
- 4. Typical values are included for reference only and are not guaranteed or tested.

CAPACITANCE $(T_A = 25^{\circ}C, f = 1.0MHz)$

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Input Capacitance	Cin	-	8	pF
Input/Output Capacitance	CI/O	-	10	pF

Note: These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Speed	10 ns
Input Pulse Levels	0.2V to Vcc-0.2V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	V _{CC} /2
Output Load	$C_L = 30pF + 1TTL$, $I_{OH}/I_{OL} = -4mA/8mA$

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Typical valued are measured at V_{CC} = V_{CC} (TYP.) and T_A = 25 $^{\circ}$ C



AC ELECTRICAL CHARACTERISTICS

(1) READ CYCLE

PARAMETER	SYM.	AS7C325	UNIT	
PARAMETER	STIVI.	MIN.	MAX.	UNII
Read Cycle Time	trc	10	-	ns
Address Access Time	taa	-	10	ns
Chip Enable Access Time	tace	-	10	ns
Output Enable Access Time	toe	-	4.5	ns
Chip Enable to Output in Low-Z	tcLz*	2	-	ns
Output Enable to Output in Low-Z	toLz*	0	-	ns
Chip Disable to Output in High-Z	tcHz*	-	4	ns
Output Disable to Output in High-Z	tonz*	-	4	ns
Output Hold from Address Change	tон	2	-	ns
Byte Control Access Time	t _{BA}	-	4.5	ns
Byte Control to High-Z Output	t _{BHZ} *	-	4	ns
Byte Control to Low-Z Output	t _{BLZ} *	0	-	ns

(2) WRITE CYCLE

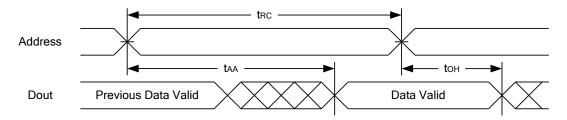
DADAMETED	SYM.	AS7C325	UNIT	
PARAMETER	STIVI.	MIN.	MAX.	UNII
Write Cycle Time	twc	10	-	ns
Address Valid to End of Write	taw	8	-	ns
Chip Enable to End of Write	tcw	8	-	ns
Address Set-up Time	tas	0	-	ns
Write Pulse Width	twp	8	-	ns
Write Recovery Time	twr	0	-	ns
Data to Write Time Overlap	t _{DW}	6	-	ns
Data Hold from End of Write Time	t DH	0	-	ns
Output Active from End of Write	tow*	2	-	ns
Write to Output in High-Z	twnz*	-	4	ns
Byte Control Valid to End of Write	t _{BW}	8	-	ns

^{*}These parameters are guaranteed by device characterization, but not production tested.

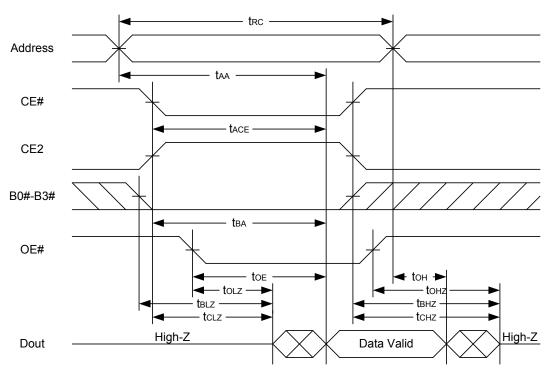
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TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)



READ CYCLE 2 (CE# and CE2 and OE# Controlled) (1,3,4,5)



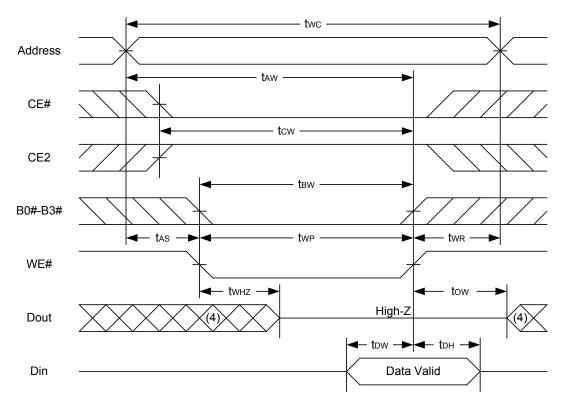
Notes:

- 1.WE# is high for read cycle.
- 2.Device is continuously selected OE# = low, CE# = low, CE2 = high, and B0#, B1#, B2# or B3# = low.
- 3.Address must be valid prior to or coincident with CE# = low, CE2 = high, and B0#, B1#, B2# or B3# = low transition; otherwise t_{AA} is the limiting parameter.
- 5.At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ}, t_{BHZ} is less than t_{BLZ}, t_{OHZ} is less than t_{OLZ}.

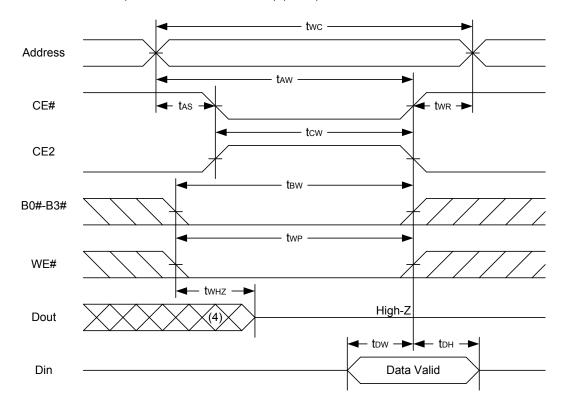
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WRITE CYCLE 1 (WE# Controlled) (1,2,4,5)

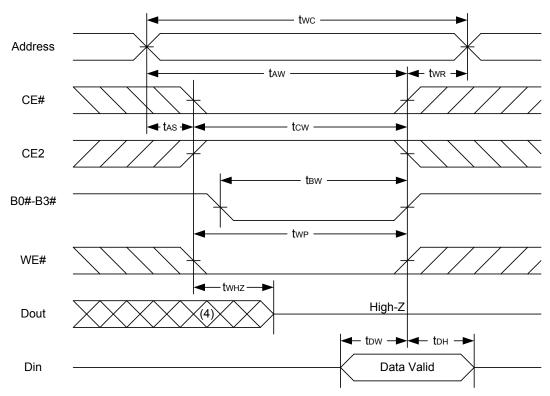


WRITE CYCLE 2 (CE# and CE2 Controlled) (1,4,5)





WRITE CYCLE 3 (B0# ~ B3# Controlled) (1,4,5)



Notes:

- 1.A write occurs during the overlap of a low CE#, high CE2, low WE#, and B0#, B1#, B2# or B3# = low.
- 2. During a WE# controlled write cycle with OE# low, twp must be greater than twnz + tow to allow the drivers to turn off and data to be placed on the bus.
- 3.During this period, I/O pins are in the output state, and input signals must not be applied.
 4.If the CE#, B0# ~ B3# low transition and CE2 high transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
- $5.t_{\text{OW}}$ and t_{WHZ} are specified with C_L = 5pF. Transition is measured $\pm 500 \text{mV}$ from steady state.

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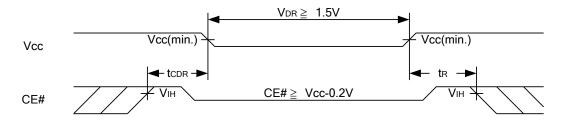
DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Vcc for Data Retention	V_{DR}	$CE\# \geq V_{CC} - 0.2V$ or $CE2 \leq 0.2V$	1.5	-	3.6	V
Data Retention Current	I_{DR}	V_{CC} = 1.5V CE# $\geq V_{CC}$ - 0.2V or CE2 ≤ 0.2 V Other pins at 0.2V or V_{CC} -0.2V	-	4	40	mA
Chip Disable to Data Retention Time	tcdr	See Data Retention Waveforms (below)	0	-	-	ns
Recovery Time	t _R		t _{RC*}	-	-	ns

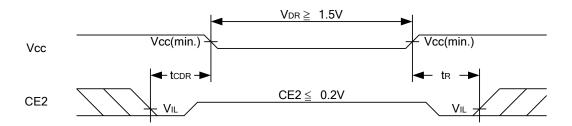
 t_{RC^*} = Read Cycle Time

DATA RETENTION WAVEFORM

Low Vcc Data Retention Waveform (1) (CE# controlled)



Low Vcc Data Retention Waveform (2) (CE2 controlled)



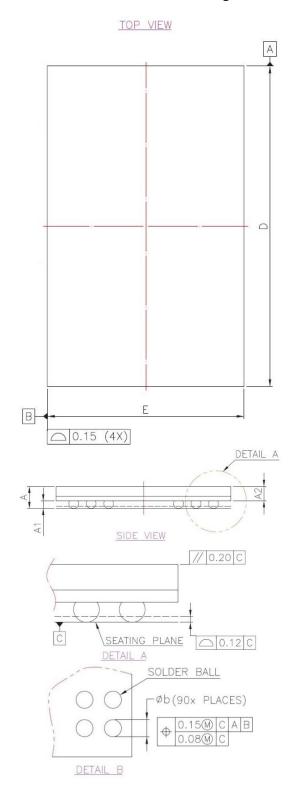
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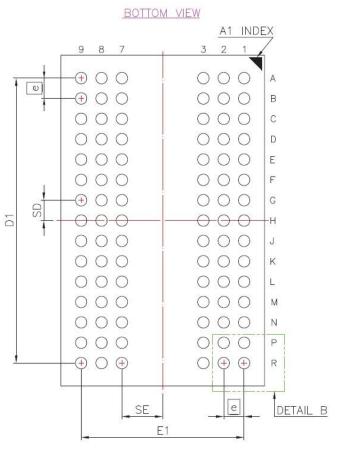


256K X 32 BIT HIGH SPEED CMOS SRAM

PACKAGE OUTLINE DIMENSION

90-ball 8mm × 13mm TFBGA Package Outline Dimension





SYM.	DIMENSION (mm)			DIMENSION (inch)			
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
А		_	1.20	8		0.047	
A1	0.25		0.40	0.010		0.016	
A2	-	0.81			0.032		
b	0.40	0.45	0.50	0.016	0.018	0.020	
D	12.90	13.00	13.10	0.508	0.512	0.516	
D1	11.200 BSC			0.441 BSC			
E	7.90	8.00	8.10	0.311	0.315	0.319	
E1	6.400 BSC			0.252 BSC			
SE	1.600 TYP			0.063 TYP			
SD	0.800 TYP			0.031 TYP			
е	0.800 BSC			0.031 BSC			

NOTE:

- 1. CONTROLLING DIMENSION: MILLIMETER.
- 2. REFERENCE DOCUMENT : JEDEC MO-210.

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PART NUMBERING SYSTEM

AS7C	325632	10	В	I	N
SRAM	3=3.3v 25632=256K x 32	10=10 ns	B = TFBGA	I=Industrial (-40° C~+85° C)	Indicates Pb and Halogen Free



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