2x30W Stereo / 1x60W Mono Digital Audio Amplifier With 36 Bands EQ Functions

Features

- 16/18/20/24-bits input with I^2S, Left-alignment and Right-alignment data format
- Multiple sampling frequencies (Fs)
  8kHz and 32kHz / 44.1kHz / 48kHz and
  64kHz / 88.2kHz / 96kHz and
  128kHz / 176.4kHz / 192kHz
- System clock = 64x, 128x, 192x, 256x, 384x, 512x, 576x, 768x, 1024x Fs
  MCLK system:
  256x~4096x Fs for 8kHz
  64x~1024x Fs for 32kHz / 44.1kHz / 48kHz
  64x~512x Fs for 64kHz / 88.2kHz / 96kHz
  64x~256x Fs for 128kHz / 176.4kHz / 192kHz
  BCLK system:
  64xFs for 32kHz / 44.1kHz / 48kHz
  64xFs for 64kHz / 88.2kHz / 96kHz
  64xFs for 128kHz / 176.4kHz / 192kHz
- Supply voltage
  1.8V or 3.3V for digital I/O
  3.3V for analog circuit and headphone driver
  4.5V~26V for loudspeaker driver
- Speaker or headphone out selection
- Line-driver maximum output swing into 10kΩ - 2Vrms at 3.3V supply voltage
- Headphone output power
  25mW x 2ch into 32Ω @ 0.1% THD+N
- Speaker output power
  30W x 2ch into 8Ω @ <1% THD+N@24V
- Sound processing including：
  36 bands parametric speaker EQ
  Volume control (+24dB~-103dB, 0.125dB/step)
  Dynamic range control
  Three Band plus post Dynamic range control
  Power Clipping
  Programmed 3D surround sound
  Channel mixing
  Noise gate with hysteresis window
  Bass/Treble tone control
  DC-blocking high-pass filter
  Pre-scale/post-scale
  Virtual Bass/exciter
  Dynamic bass
- Anti-pop design
- Level meter and power meter
- I^2S output with selectable audio DSP point
- Supports I^2C control without clock
- I^2C control interface with selectable device address
- Internal PLL
- Protection
  - OCP
  - OVP
  - UVP
  - OTP
  - DCP
- Closed-loop structure with good PSRR

Applications

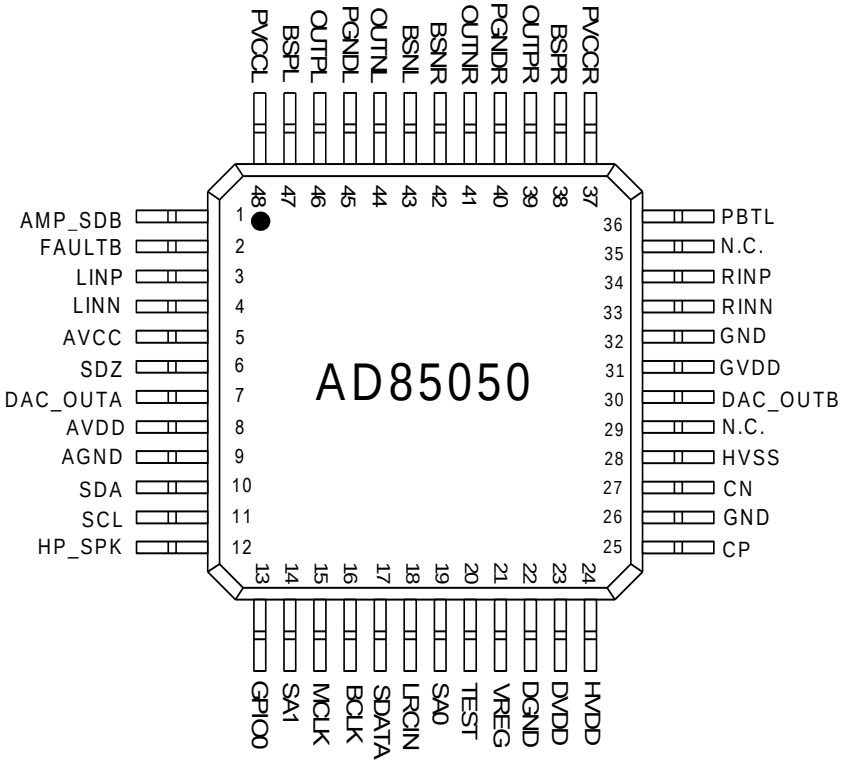
- Boom-box, CD and DVD receiver, docking system
- Powered speaker
- Wireless audio
- AI speaker

Description

AD85050 is a digital audio amplifier capable of driving. a pair of 8Ω,30W or a single 4Ω,60W speaker output. In headphone output mode, it can delivered 25mW into 32Ω load for head phone output.

AD85050 provides advanced audio processing functions, such as volume control, 36 EQ bands, audio mixing, 3D surround sound and Dynamic Range Control (DRC). These are fully programmable via a simple I^2C control interface. Robust protection circuits are provided to protect AD85050 from damage due to accidental erroneous operating condition. The full digital circuit design of AD85050 is tolerant of noise and PVT (Process, Voltage, and Temperature) variation. AD85050 is pop free during instantaneous power on/off or mute/shut down switching because of its robust built-in anti-pop circuit.

Pin Assignment

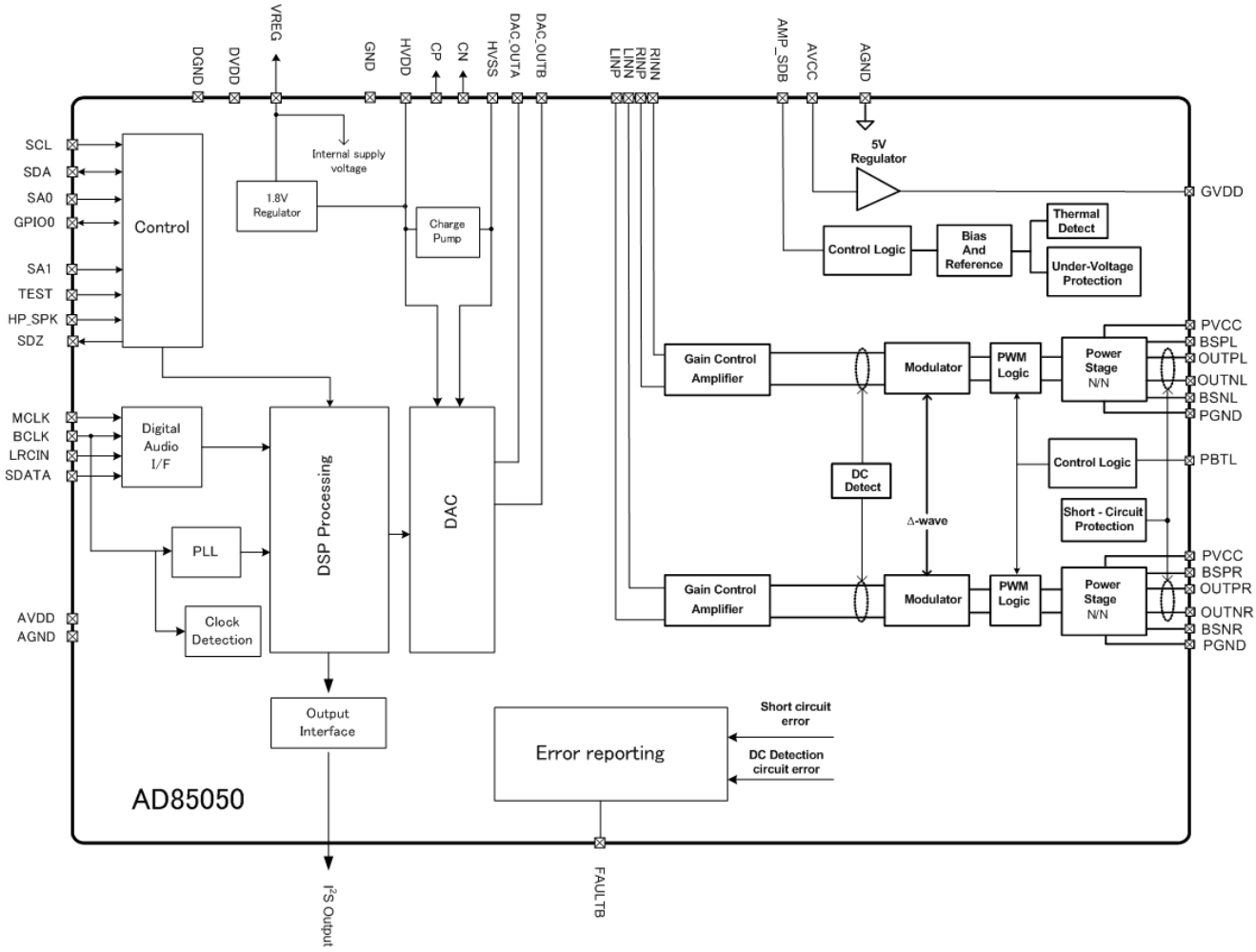


PIN	NAME	TYPE	DESCRIPTION	CHARACTERISTICS
1	AMP_SDB	I	Shut down for AMP, low active.	With pull low resistor (250Kohm).
2	FAULTB	O	Open drain output used to display short circuit or dc detect fault. Voltage compliant to AVCC. Short circuit faults can be set to auto-recovery by connecting FAULTB pin to AMP_SDB pin. Otherwise, dc detect faults must be reset by cycling AVCC.	
3	LINP	I	Positive audio input for left channel.	
4	LINN	I	Negative audio input for left channel.	
5	AVCC	P	Analog supply.	
6	SDZ	O	Shut down control for AMP.	
7	DAC_OUTA	O	Analog output from DAC A channel.	
8	AVDD	P	Power supply for analog circuit, 3.3V	
9	AGND	P	Ground for analog circuit.	
10	SDA	I/O	I^2C bi-directional serial data.	Schmitt trigger TTL input buffer
11	SCL	I	I^2C serial clock input.	Schmitt trigger TTL input buffer

12	HP_SPK	I	Head phone and speaker switch.	Schmitt trigger TTL input buffer, with pull low resistor internally.
13	GPIO0	I/O	General purpose digital input and output. Port 0.	Schmitt trigger TTL input buffer, with pull low resistor internally.
14	SA1	I	I^2C select address 1.	Schmitt trigger TTL input buffer, with pull low resistor internally.
15	MCLK	I	Master clock input.	Schmitt trigger TTL input buffer.
16	BCLK	I	Bit clock input (64Fs).	Schmitt trigger TTL input buffer.
17	SDATA	I	Serial audio data input.	Schmitt trigger TTL input buffer
18	LRCIN	I	Left/Right clock input (Fs).	Schmitt trigger TTL input buffer.
19	SA0	I	I^2C select address 0.	Schmitt trigger TTL input buffer, with pull low resistor internally.
20	TEST	I	This pin must connect to GND.	With pull low resistor internally.
21	VREG	O	1.8V Regulator voltage output.	
22	DGND	P	Digital Ground.	
23	DVDD	P	Digital I/O power, 1.8V or 3.3V.	
24	HVDD	P	Supply voltage for headphone driver, 3.3V.	
25	CP	O	Charge-pump flying capacitor positive terminal.	
26	GND	P	Power ground.	
27	CN	O	Charge-pump flying capacitor negative terminal.	
28	HVSS	P	Negative supply voltage for headphone driver.	
29	N.C.		Not connected.	
30	DAC_OUTB	O	Analog output from DAC B channel.	
31	GVDD	O	5V regulated output, also used as supply for PLIMIT function.	
32	GND	P	Power ground.	
33	RINN	I	Negative audio input for right channel.	
34	RINP	I	Positive audio input for right channel.	
35	N.C.	I	Not connected.	
36	PBTL	I	Parallel BTL mode switch, high for parallel BTL output. Voltage compliance to AVCC.	With pull low resistor internally.
37	PVCCR	P	High-voltage power supply for right-channel. Channel power supply inputs are connected in chip internally.	

38	BSPR	O	Bootstrap I/O for right channel, positive high side FET	
39	OUTPR	O	Class-D H-bridge positive output for right channel	
40	PGNDR	P	Power ground for the H-bridges.	
41	OUTNR	O	Class-D H-bridge negative output for right channel.	
42	BSNR	O	Bootstrap I/O for right channel, negative high side FET.	
43	BSNL	O	Bootstrap I/O for left channel, negative high side FET.	
44	OUTNL	O	Class-D H-bridge negative output for left channel.	
45	PGNDL	P	Power ground for the H-bridges.	
46	OUTPL	O	Class-D H-bridge positive output for left channel.	
47	BSPL	O	Bootstrap I/O for left channel, positive high side FET.	
48	PVCCL	P	High-voltage power supply for left-channel. Left channel and Right channel power supply inputs are connected in chip internally.	

Functional Block Diagram



Ordering Information

Product ID	Package	Packing / MPQ	Comments
AD85050-LG48NRY	E-LQFP 48L (7mm x 7mm)	250 Units / Tray 2.5K Units / Box (10 Trays)	Green
AD85050-LG48NRR	E-LQFP 48L (7mm x 7mm)	2K Units / Reel 1 Reel / Small box	Green

Available Package

Package Type	Device No.	θ_{ja}(℃/W)	Ψ_{jt}(℃/W)	θ_{jt}(℃/W)	Exposed Thermal Pad
E-LQFP 48L	AD85050	22.9	1.64	34.9	Yes (Note1)

Note 1.1: The thermal pad is located at the bottom of the package. To optimize thermal performance, soldering the thermal pad to the PCB's ground plane is suggested.

Note 1.2: θ_{ja}, the junction-to-ambient thermal resistance is simulated on a room temperature (T_A=25℃), natural convection environment test board, which is constructed with a thermally efficient, 4-layers PCB (2S2P). The simulation is tested using the JESD51-5 thermal measurement standard.

Note 1.3: Ψ_{jt} represents the thermal parameter for the heat flow between the chip junction and the package's top surface center. It's extracted from the simulation data for obtainingθ_{ja}, using a procedure described in JESD51-2.

Note 1.4: θ_{jt} represents the thermal resistance for the heat flow between the chip junction and the package's top surface. It's extracted from the simulation data with obtaining a cold plate on the package top.

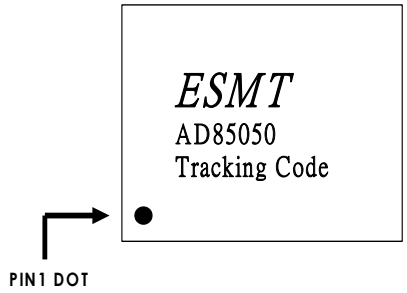
Marking Information

AD85050

Line 1 : LOGO

Line 2 : Product no.

Line 3 : Tracking Code



Absolute Maximum Ratings (AMR)

Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device.

Symbol	Parameter		Min	Max	Units
DVDD	Supply for Digital I/O Circuit		-0.3	3.6	V
AVDD	Supply for Analog Circuit		-0.3	3.6	V
HVDD	Supply for Headphone Driver		-0.3	3.6	V
PVCCL/R	Supply for Driver Stage		-0.3	30	V
AVCC	Supply for Driver Stage Analog Circuit		-0.3	30	V
V_i	Input Voltage for AMP_SDB, FAULTB, PBTL		-0.3	30	V
	Input Voltage for the other pins		-0.3	3.6	V
T_{stg}	Storage Temperature		-65	150	^oC
T_J	Junction Operating Temperature		0	150	^oC
R_L	Minimum Load Resistance	BTL (Stereo)	3.2		Ω
		PBTL (Mono) ＞ 18V	3.2		Ω
		PBTL (Mono) ≦ 18V	1.6		Ω
ESD	Human Body Model			±2K	V
	Charged Device Model			±500	V

Recommended Operating Conditions

Symbol	Parameter	Typ	Units
DVDD	Supply for Digital I/O Circuit for 1.8V	1.65~1.95	V
	Supply for Digital I/O Circuit for 3.3V	3.0~3.6	
AVDD	Supply for Analog Circuit	3.0~3.6	V
HVDD	Supply for Headphone Driver	3.0~3.6	V
PVCC	Supply for Driver Stage PVCCL/R	4.5~26	V
AVCC	Supply for Driver Stage Analog Circuit	4.5~26	V
T_J	Junction Operating Temperature	-40~125	^oC
T_A	Ambient Operating Temperature	-40~85	^oC

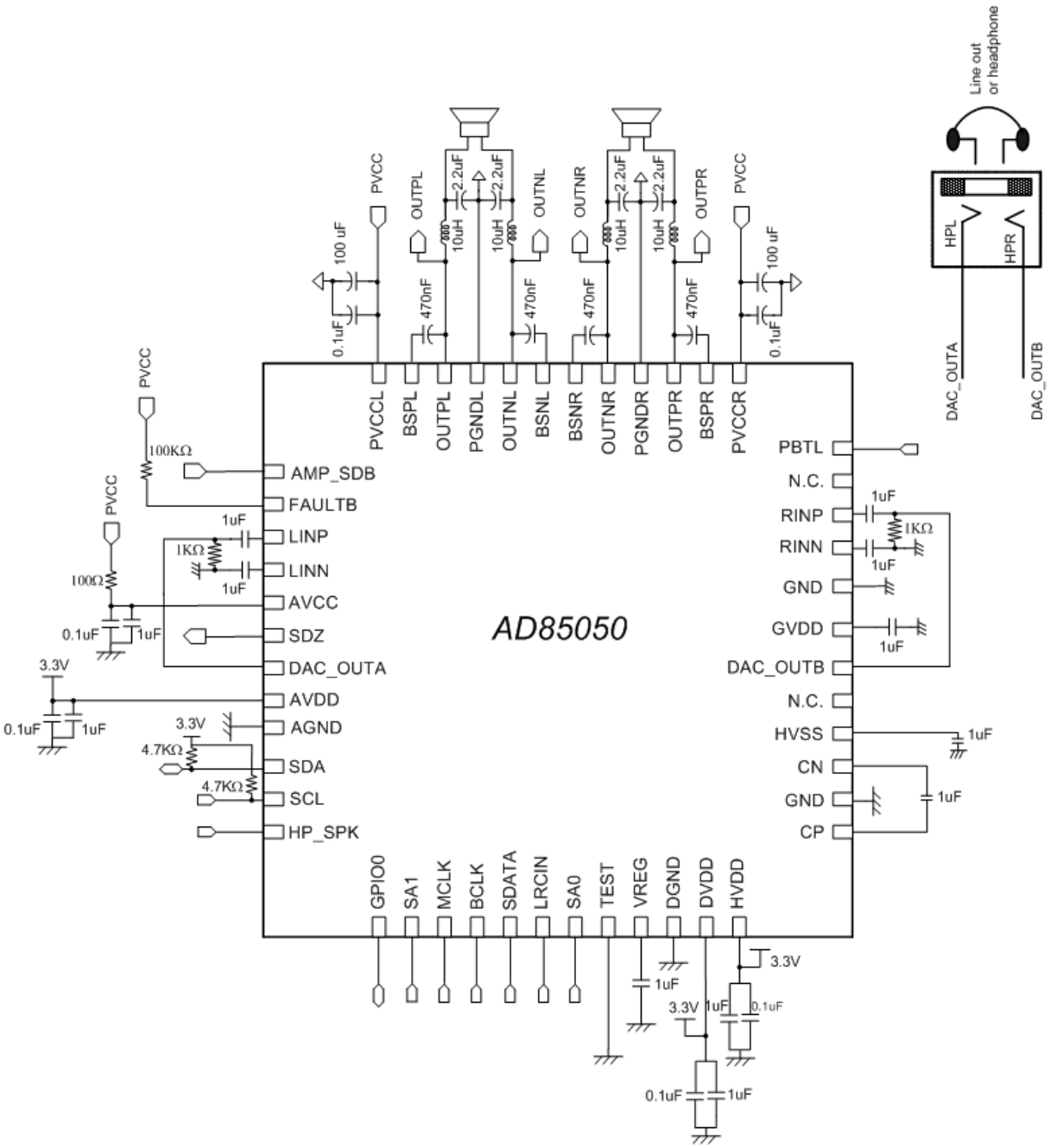
General Electrical Characteristics

Condition: PVCC=24V, R_L=8Ω, T_A=25°C, (unless otherwise noted).

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
$I_{Q(PVCC)}$	Quiescent supply current	AMP_SDB=2V, no load, PVCC=12V		13	26	mA
$I_{Q(AVCC)}$	Quiescent supply current for PVCC			7.1	15	mA
$I_{Q(HVDD)}$	Quiescent supply current for HVDD			47	53	mA
$I_{Q(AVDD)}$	Quiescent supply current for AVDD			12	20	mA
$I_{Q(DVDD)}$	Quiescent supply current for DVDD	DVDD=1.8V		15	50	uA
		DVDD=3.3V		29	65	
$I_{SD(PVCC)}$	Quiescent supply current in shutdown mode	AMP_SDBD=0.8V, no load, PVCC=12V		< 12	25	uA
$UV_{(AVDD)}$	AVDD Under-Voltage Active Threshold			2.66		V
	AVDD Under-Voltage Release Threshold			2.74		
$UV_{(HVDD)}$	HVDD Under-Voltage Active Threshold			2.66		V
	HVDD Under-Voltage Release Threshold			2.74		
$R_{DS(on)}$	Drain-source on-state resistance-High side NMOS	PVCC=12V, Id=500mA, T_J=25 °C		90		mΩ
	Drain-source on-state resistance-Low side NMOS			90		mΩ
$\|V_{OS}\|$	Class-D output offset voltage (measured differential)	PVCC=12V V_i=0V		1.5	15	mV
t_{ON}	Turn-on time	AMP_SDB=2V		90		ms
t_{OFF}	Turn-off time	AMP_SDB=0.8V		2		us
GVDD	5V regulator output	I_{GVDD}=0.1mA	4.75	5	5.25	V

VREG	1.8V regulator output		1.71	1.8	1.89	V
G	Gain	Value represents the "peak voltage" disregarding clipping due to lower PVCC). Measured at 0 dB input(1FS) and all volume gain at 0dB		28		V
f_{OSC}	Oscillator frequency		250	310	370	kHz
I_{SC}	LI Channel Over Current Protection			8		A
	Mono Over-Current Protection			16		A
V_{IH}	High-Level Input Voltage	DVDD=1.8V	1.3			V
		DVDD=3.3V	2.0			
		AMP_SDB ; PBTL pin	2.0			
V_{IL}	Low-level Input Voltage	DVDD=1.8V			0.5	V
		DVDD=3.3V			0.8	
		AMP_SDB ; PBTL pin			0.8	
V_{OH}	High-Level Output Voltage	DVDD=1.8V	1.2			V
		DVDD=3.3V	2.4			
V_{OL}	Low-Level Output Voltage	DVDD=1.8V			0.2	V
		DVDD=3.3V			0.4	
C_I	Input Capacitance			6.4		pF

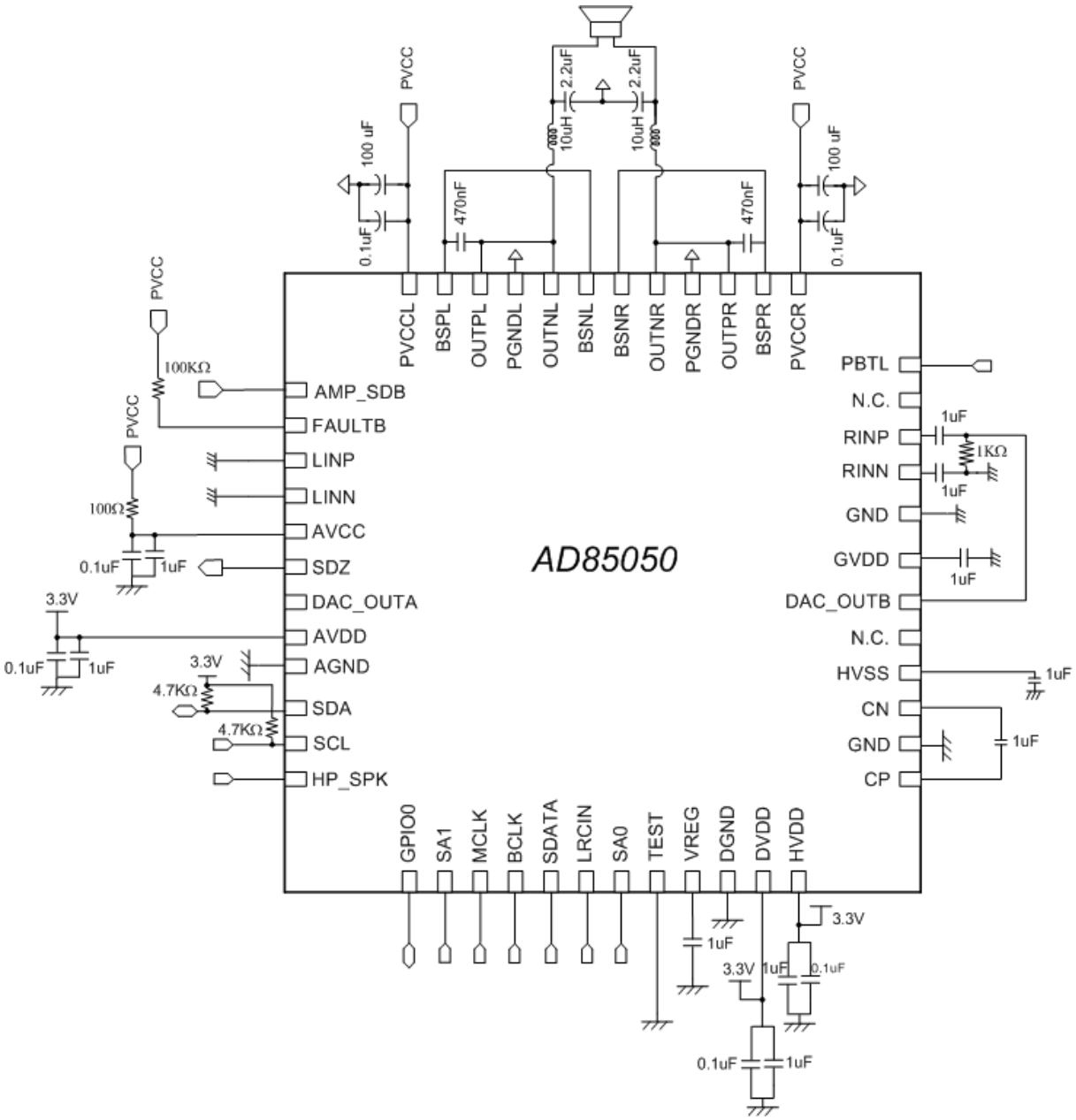
Application Circuit Example for Stereo



Note. The under-voltage threshold for AVCC could be adjusted by R_{AVCC}, the formula will be followed

$R_{AVCC} \leq \frac{AVCC - 4}{30} \ (K\Omega)$, R_{AVCC}=100ohm minimum is requirement in AD85050.

Application Circuit Example for Mono



Note. The under-voltage threshold for AVCC could be adjusted by R_{AVCC}, the formula will be followed

$R_{AVCC} \le \frac{AVCC - 4}{30} \ (K\Omega)$, R_{AVCC}=100ohm minimum is requirement in AD85050.

Electrical Characteristics and Specifications for Loudspeaker

● BTL (Bridge-Tied-Load) output for Stereo

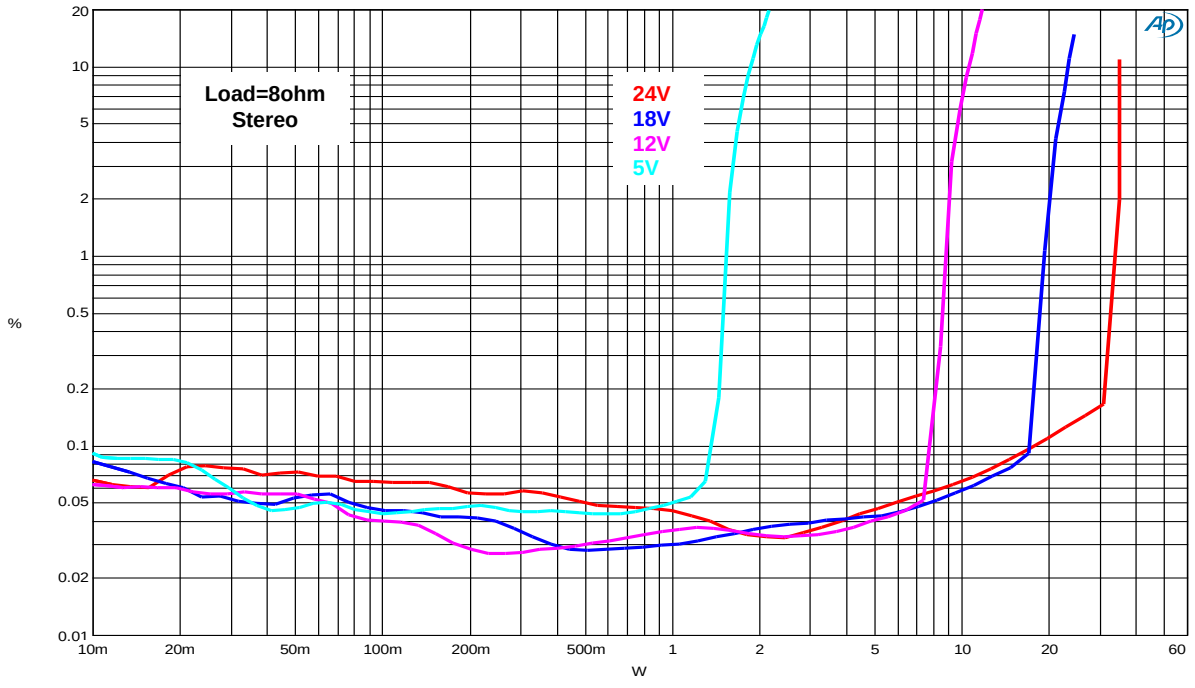
Condition: T_A=25°C, DVDD=HVDD=AVDD=3.3V, PVCC=24V, F_S=48kHz, Load=8Ω; Input is 1kHz sine-wave unless otherwise specified.

Symbol	Parameter	Condition	Input Level	Min	Typ	Max	Units
P_O (Note 3)	RMS Output Power (THD+N < 1%)				30		W
	RMS Output Power (THD+N=0.1%)				15		W
	RMS Output Power (THD+N=10%) for PVCC=12V				10		W
THD+N	Total Harmonic Distortion + Noise	P_O=10W			0.08		%
SNR	Signal to Noise Ratio (Note 2)	Maximum power at THD < 1% @1kHz			103		dB
DR	Dynamic Range (Note 2)		-60dB		108		dB
Vn	Output Noise (Note 2)	20Hz to 20kHz			120		uV
PSRR	Power Supply Rejection Ratio	V_{RIPPLE}=1V_{RMS} at 1kHz			-70		dB
	Channel Separation	1W @1kHz			-95		dB

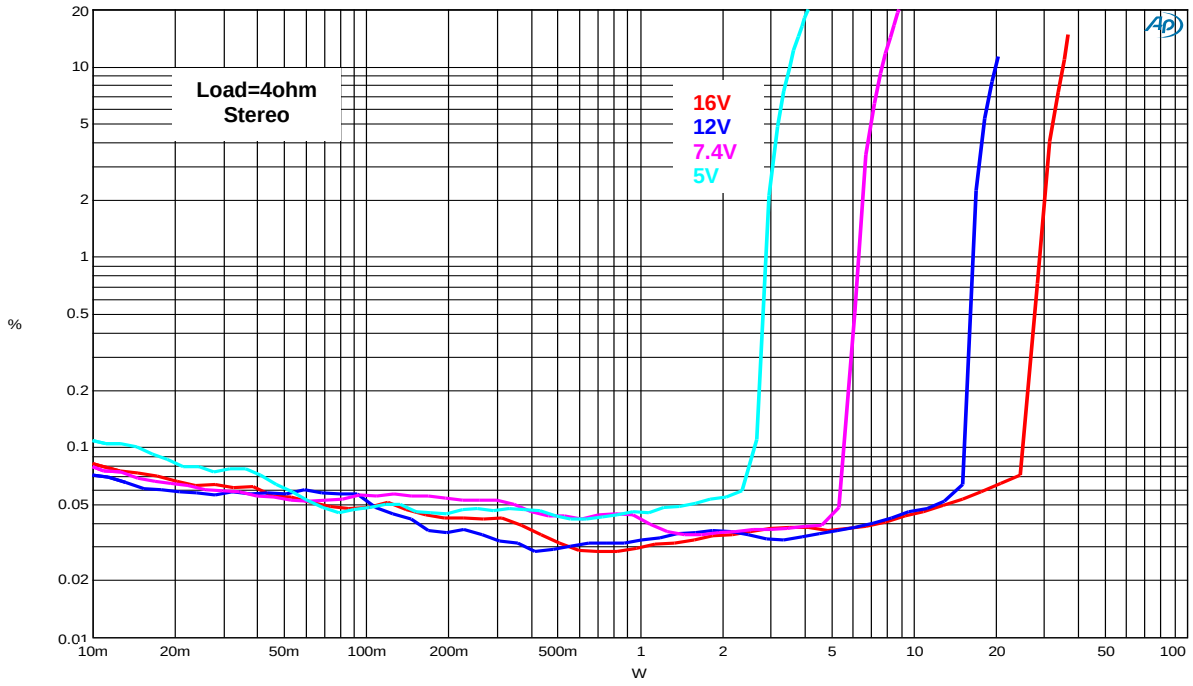
Note 2: Measured with A-weighting filter.

Note 3: Thermal dissipation is limited by package type and PCB design. The external heat-sink or system cooling method should be adopted for maximum power output.

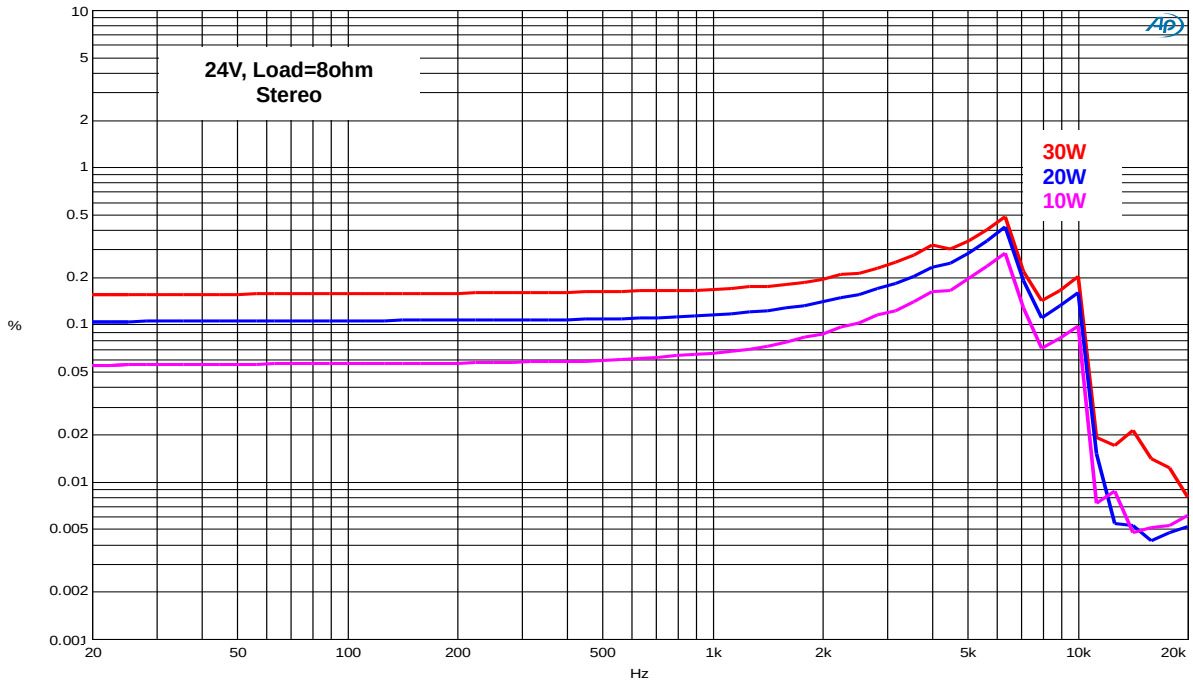
Total Harmonic Distortion + Noise vs. Output Power



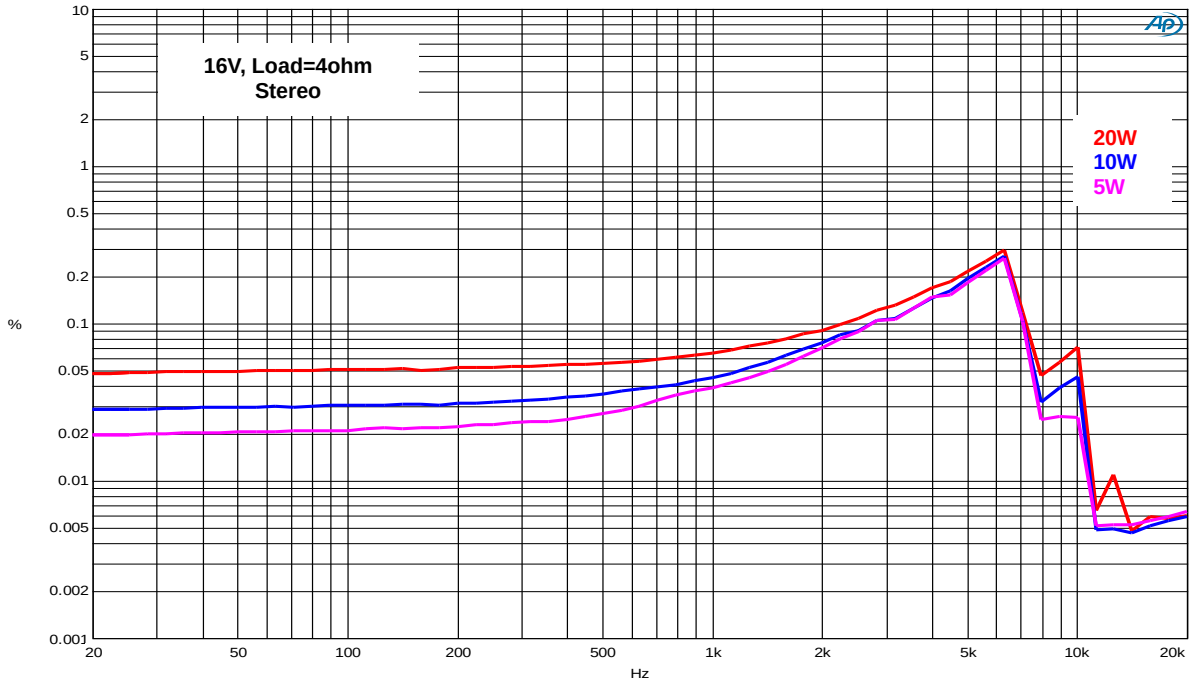
Total Harmonic Distortion + Noise vs. Output Power



Total Harmonic Distortion + Noise vs. Frequency



Total Harmonic Distortion + Noise vs. Frequency



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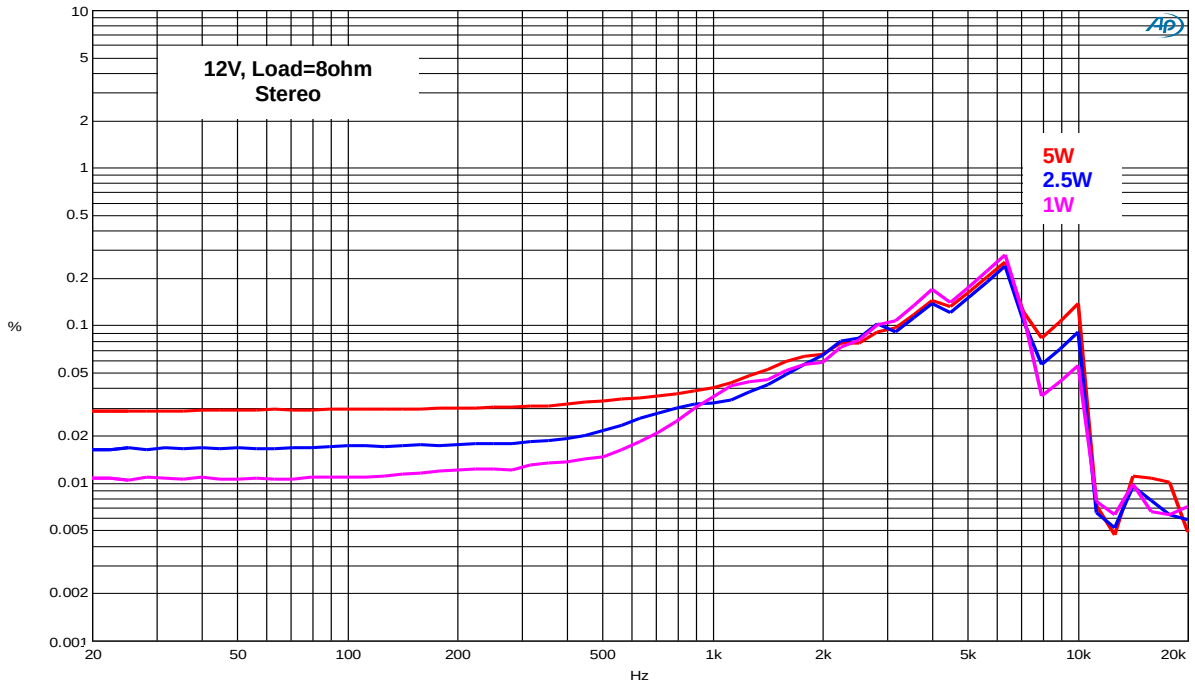
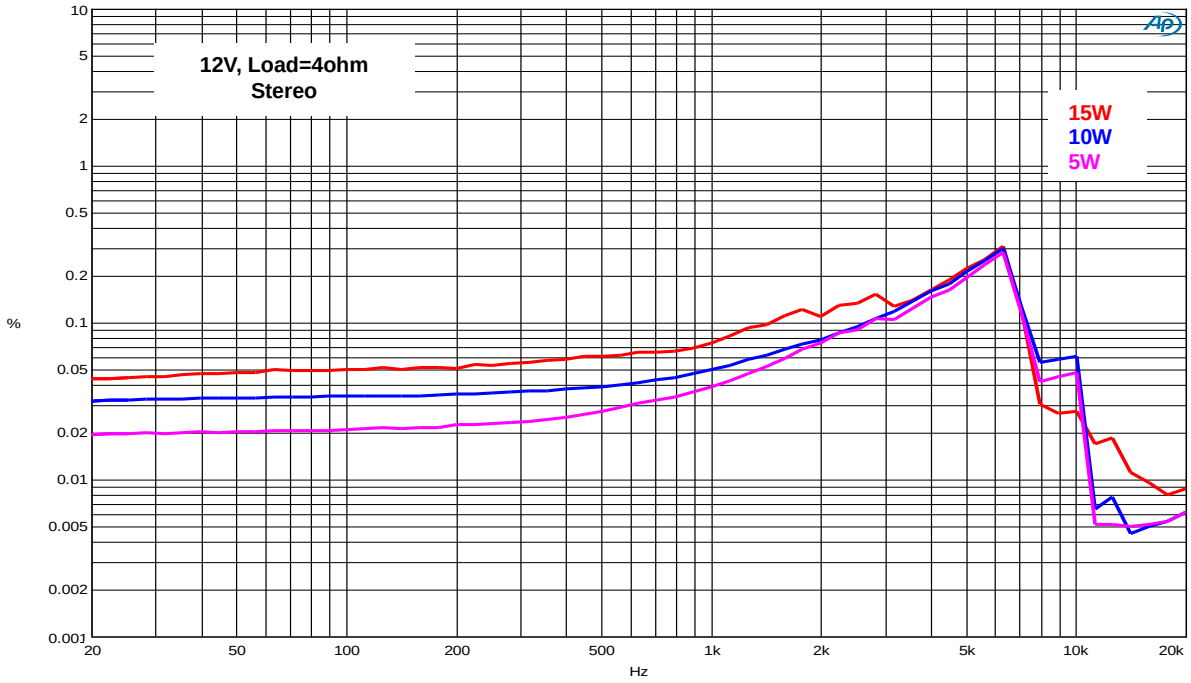
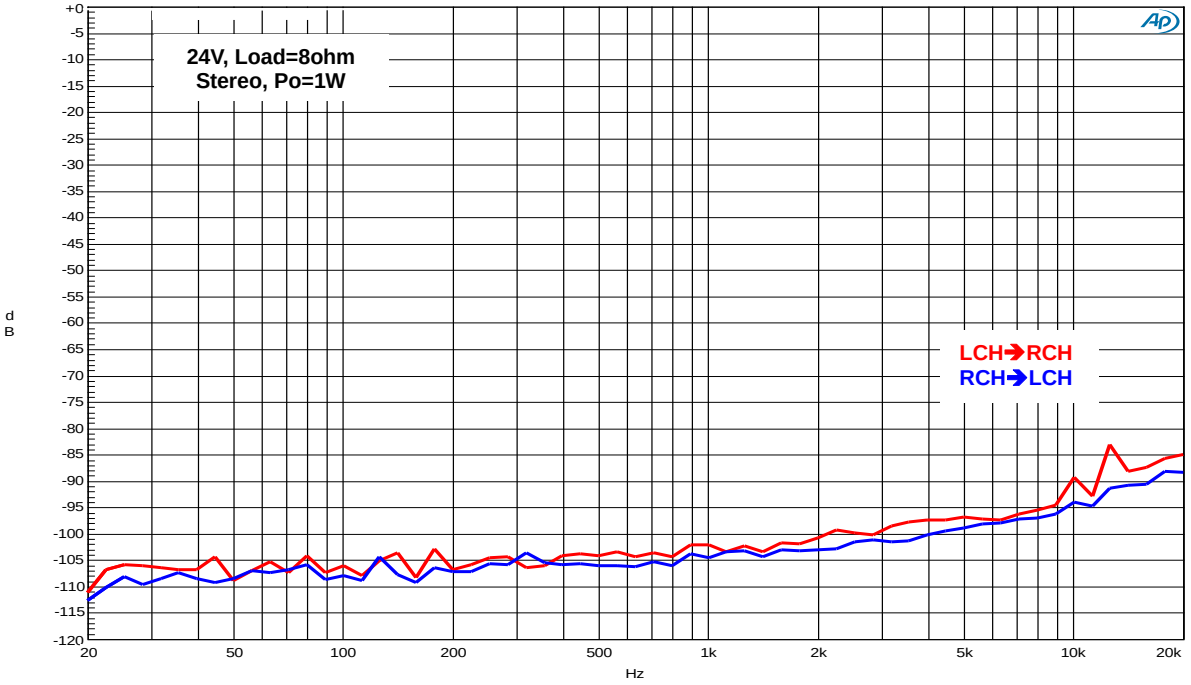
Total Harmonic Distortion + Noise vs. Frequency



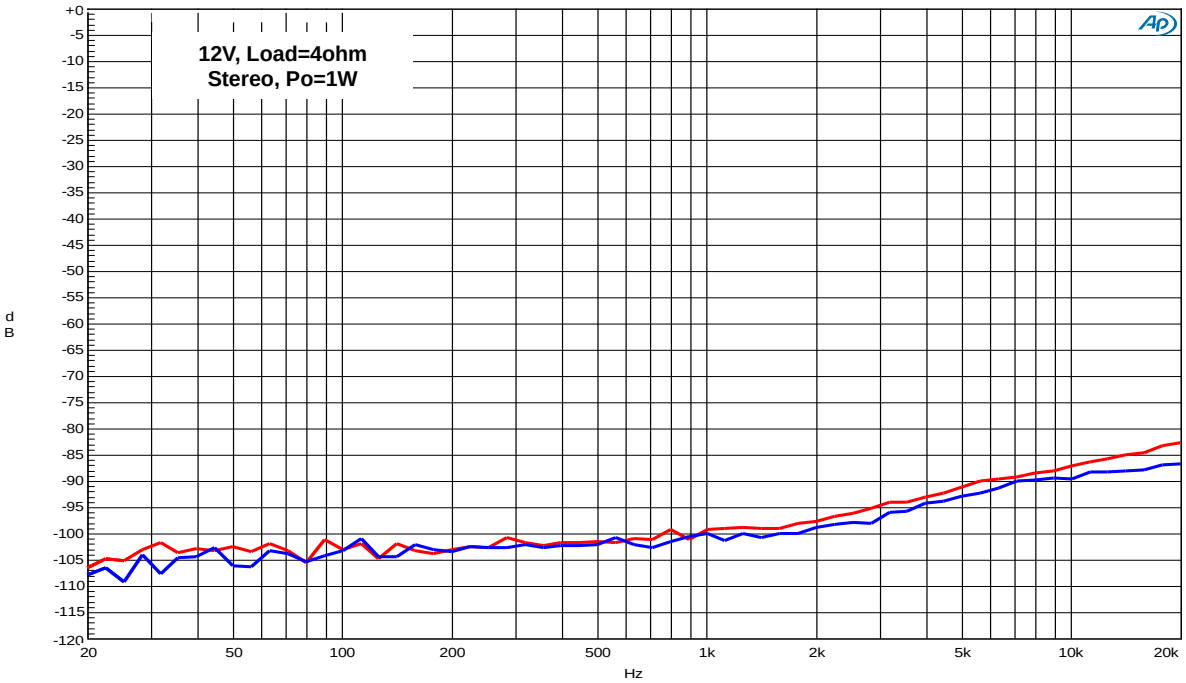
Total Harmonic Distortion + Noise vs. Frequency



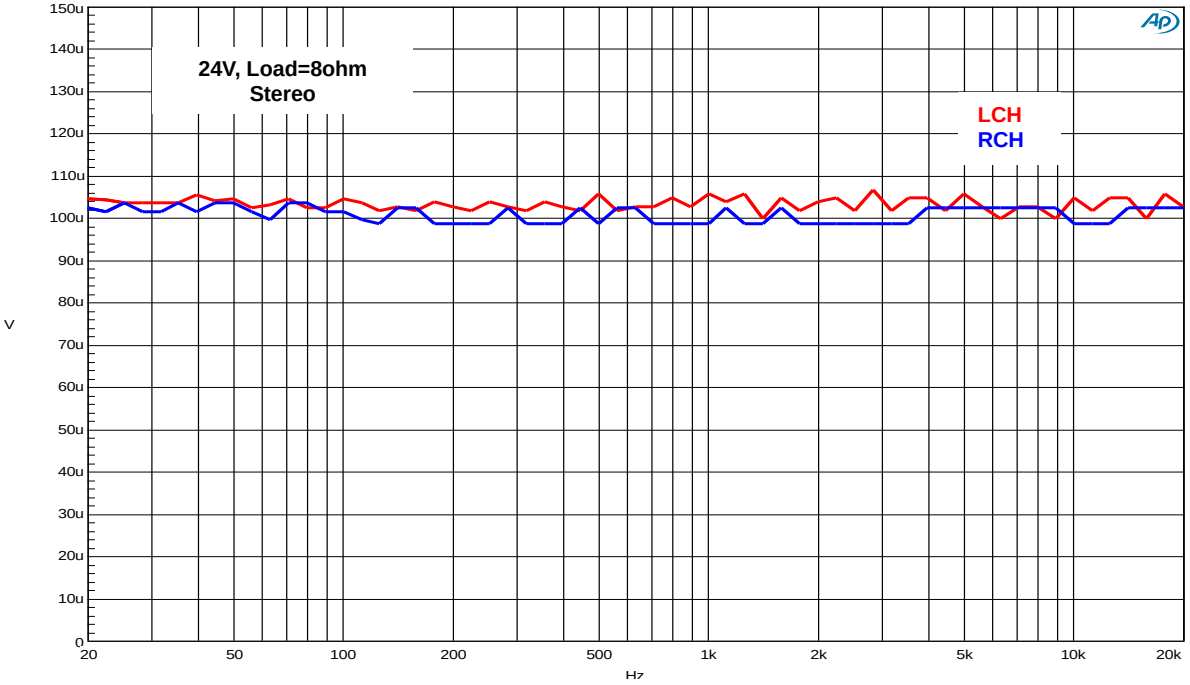
Cross-talk



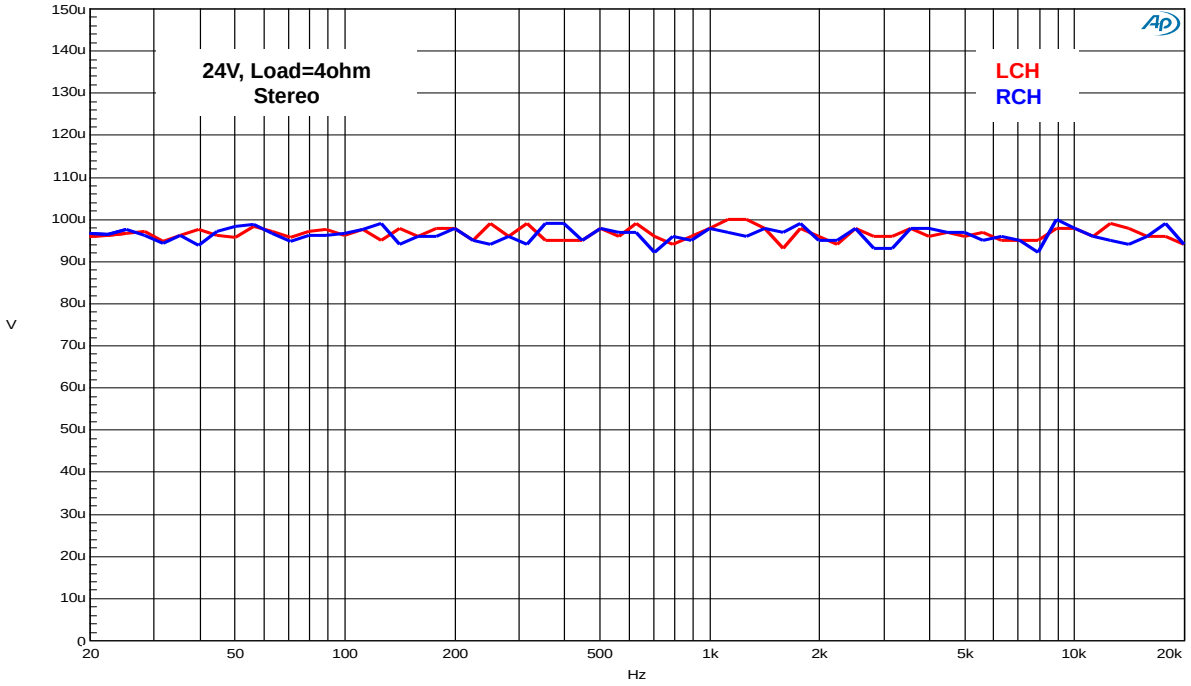
Cross-talk



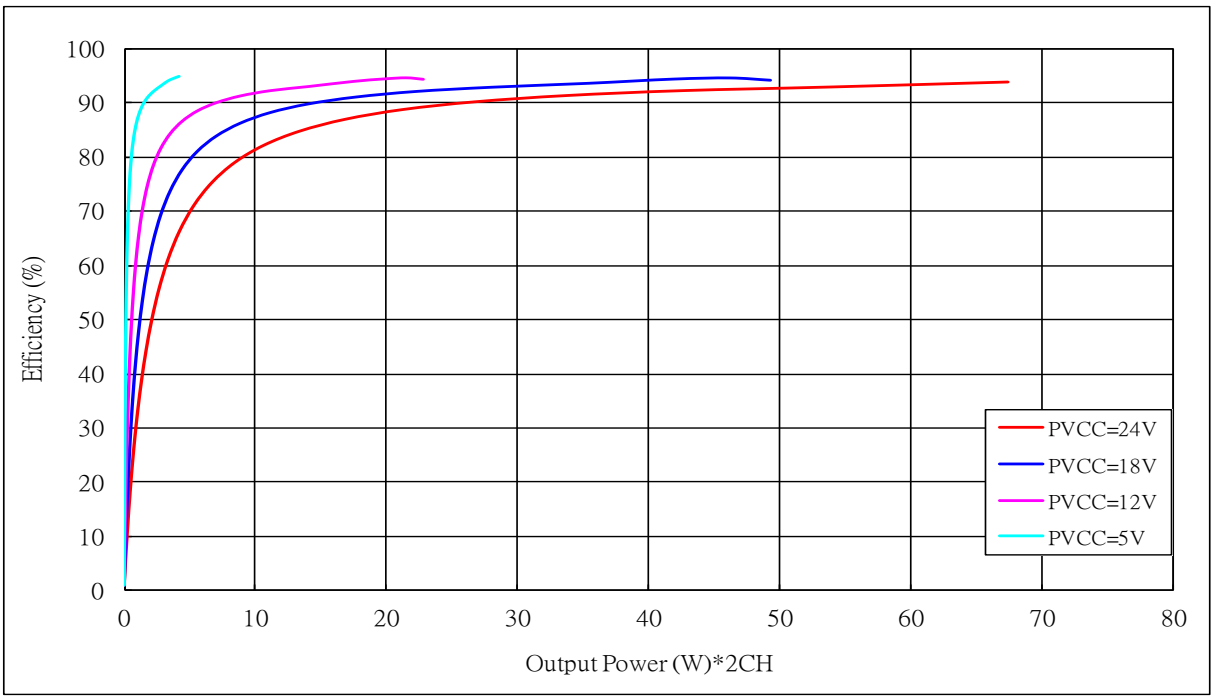
Noise Level



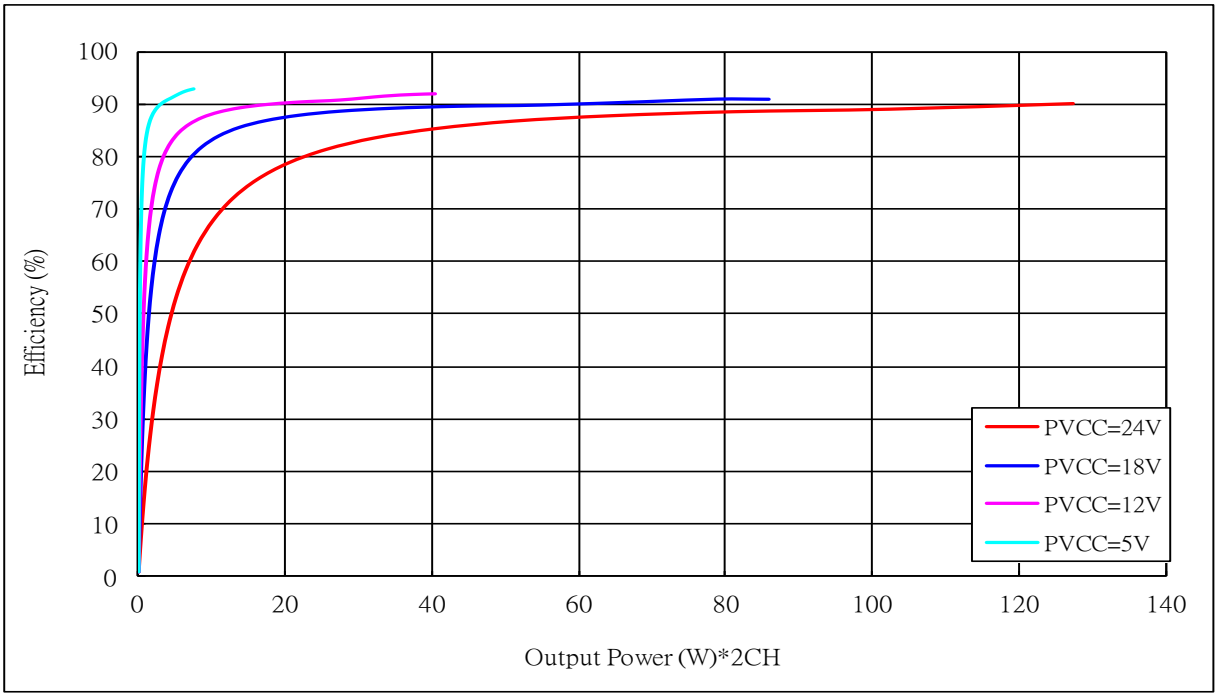
Noise Level



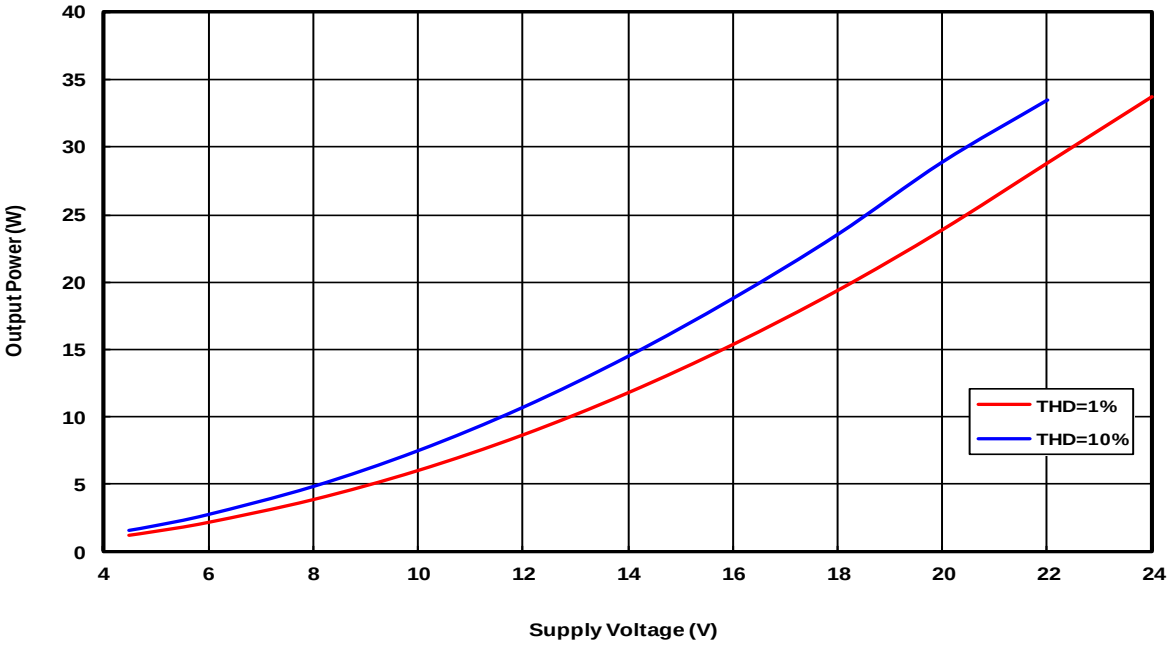
Efficiency (Stereo 8ohm load) / 2ch



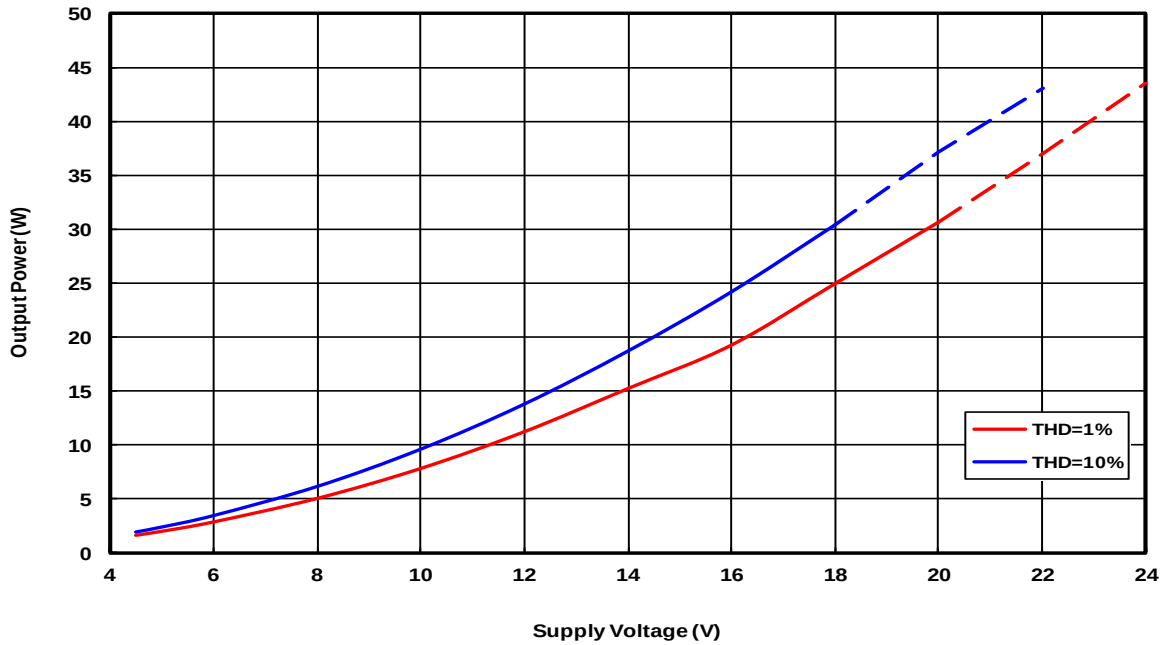
Efficiency (Stereo 4ohm load) / 2ch



Output Power vs. Supply Voltage (BTL, 8ohm)

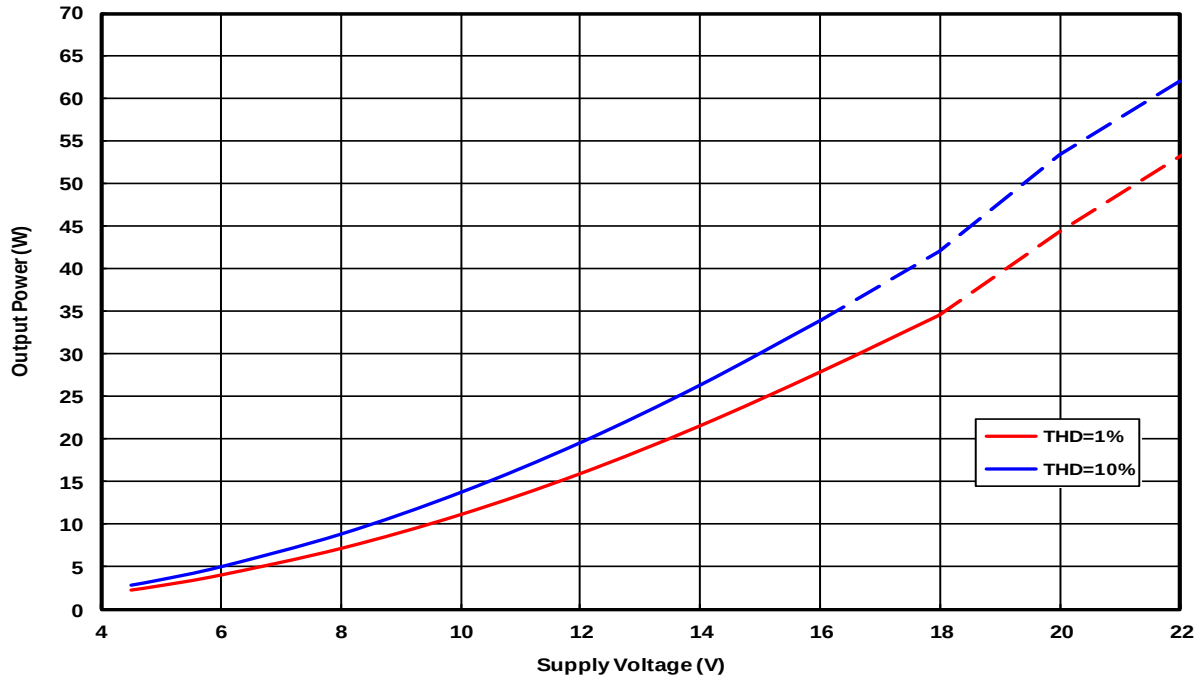


Output Power vs. Supply Voltage (BTL, 6ohm)



Note: Dashed Line represent thermally limited regions.

Output Power vs. Supply Voltage (BTL, 4ohm)



Note: Dashed Line represent thermally limited regions.

Electrical Characteristics and Specifications for Loudspeaker

● PBTL (Parallel Bridge-Tied-Load) output for Mono

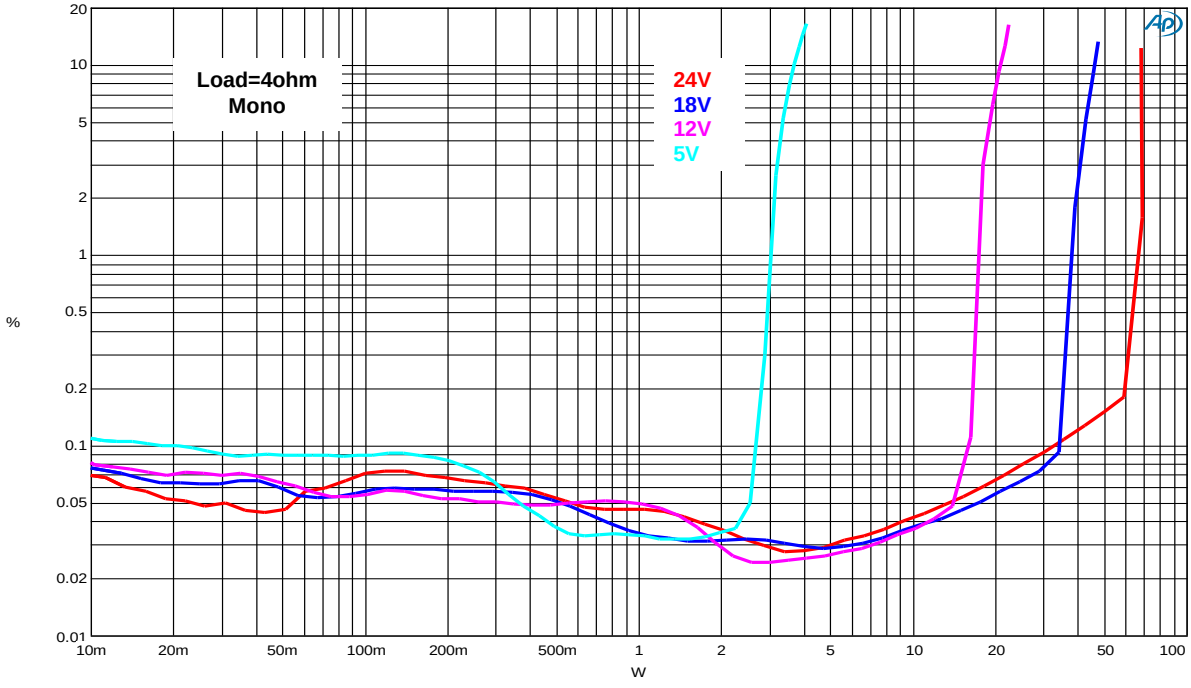
Condition: T_A=25°C, DVDD=HVDD=AVDD=3.3V, PVCC=24V, F_S=48kHz, Load=4Ω; Input is 1kHz sine-wave unless otherwise specified.

Symbol	Parameter	Condition	Input Level	Min	Typ	Max	Units
P_O (Note 3)	RMS Output Power (THD+N < 1%)				60		W
	RMS Output Power (THD+N=0.1%)				30		W
	RMS Output Power (THD+N=10%) for PVCC=12V				20		W
THD+N	Total Harmonic Distortion + Noise	P_O=20W			0.08		%
SNR	Signal to Noise Ratio (Note 2)	Maximum power at THD < 1% @1kHz			103		dB
DR	Dynamic Range (Note 2)		-60dB		109		dB
Vn	Output Noise (Note 2)	20Hz to 20kHz			105		uV

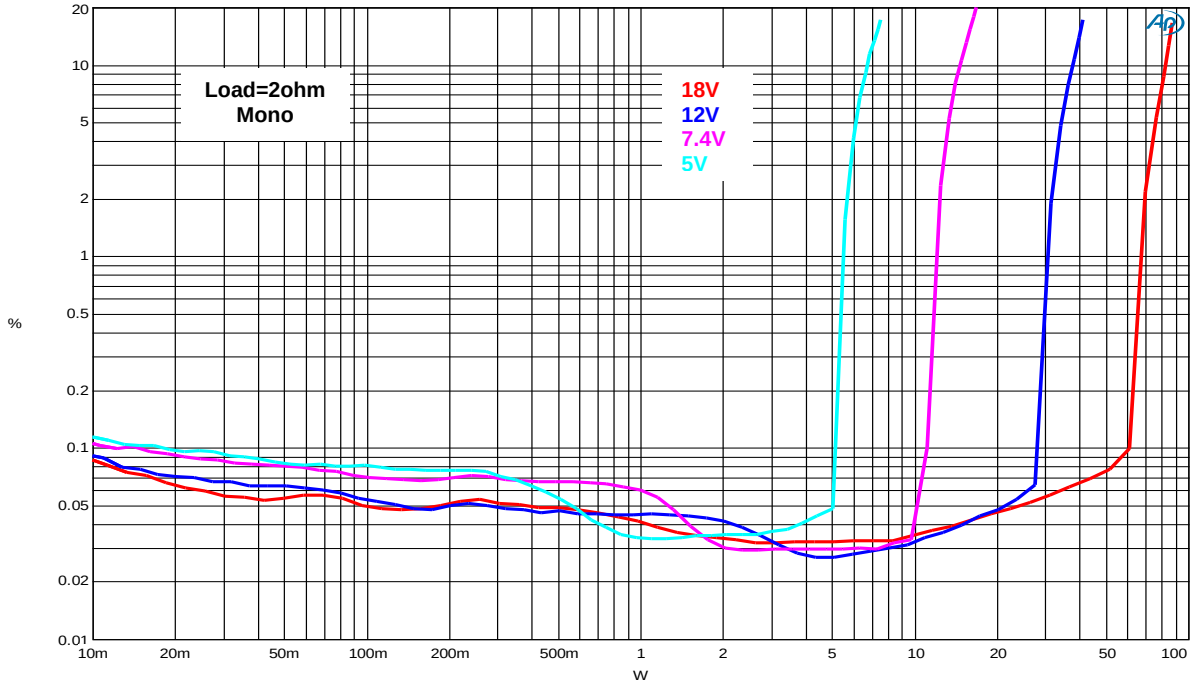
Note 2: Measured with A-weighting filter.

Note 3: Thermal dissipation is limited by package type and PCB design. The external heat-sink or system cooling method should be adopted for maximum power output.

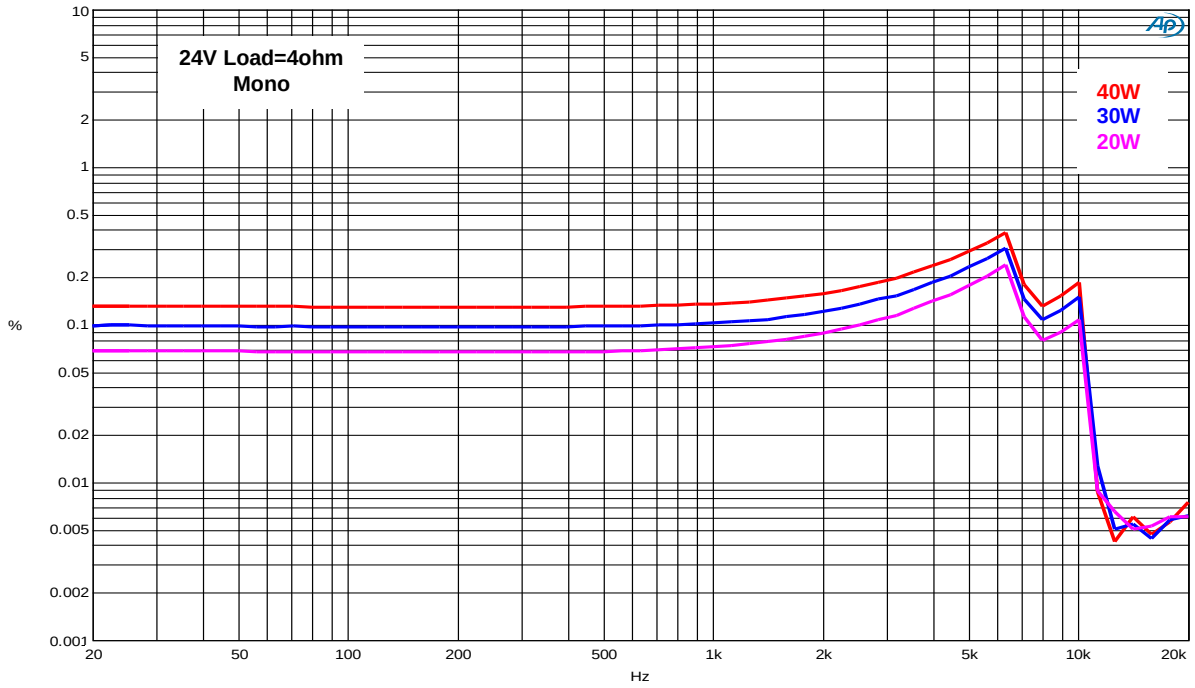
Total Harmonic Distortion + Noise vs. Output Power



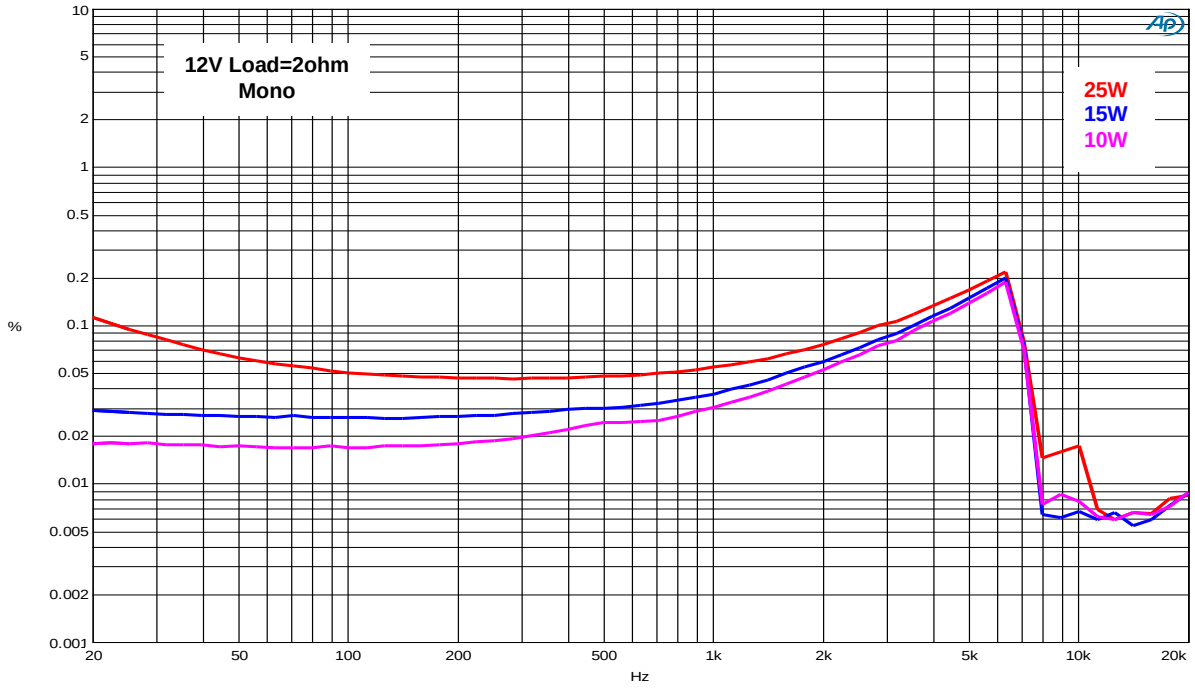
Total Harmonic Distortion + Noise vs. Output Power



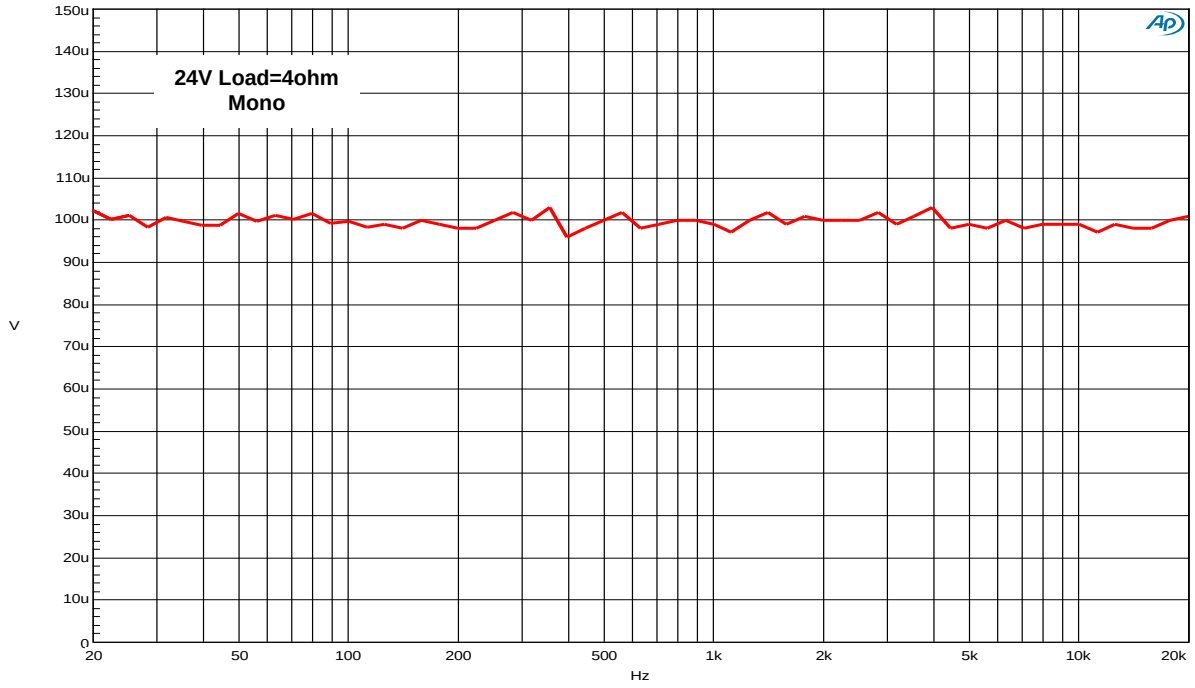
Total Harmonic Distortion + Noise vs. Frequency



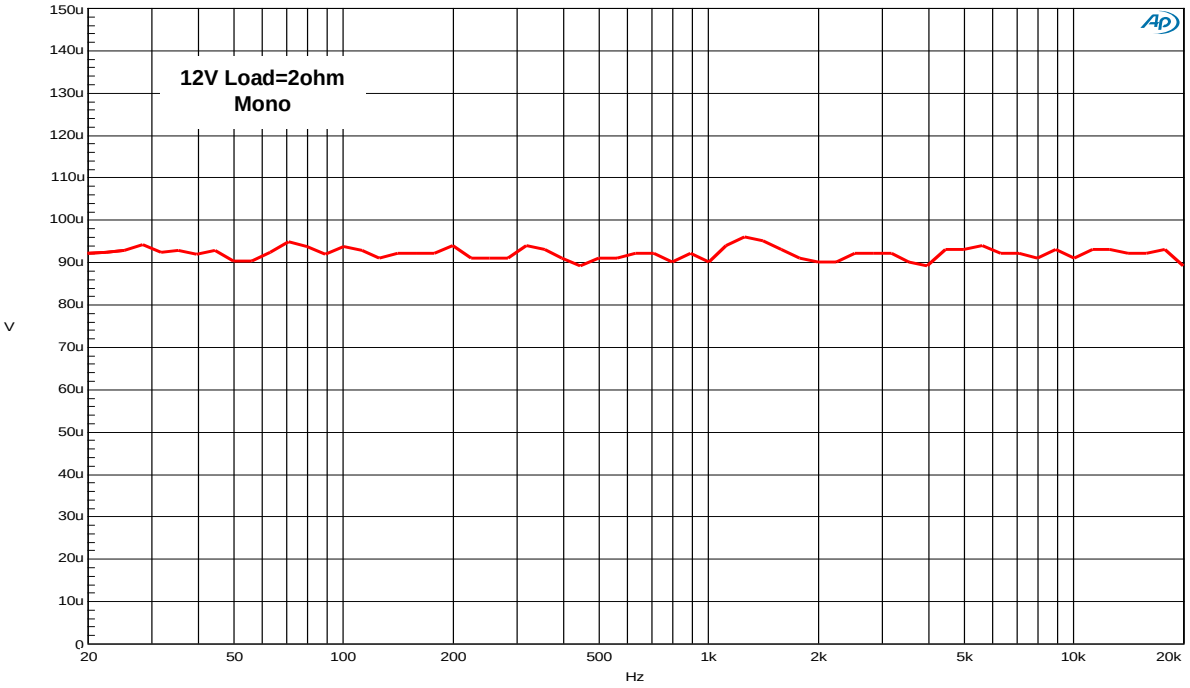
Total Harmonic Distortion + Noise vs. Frequency



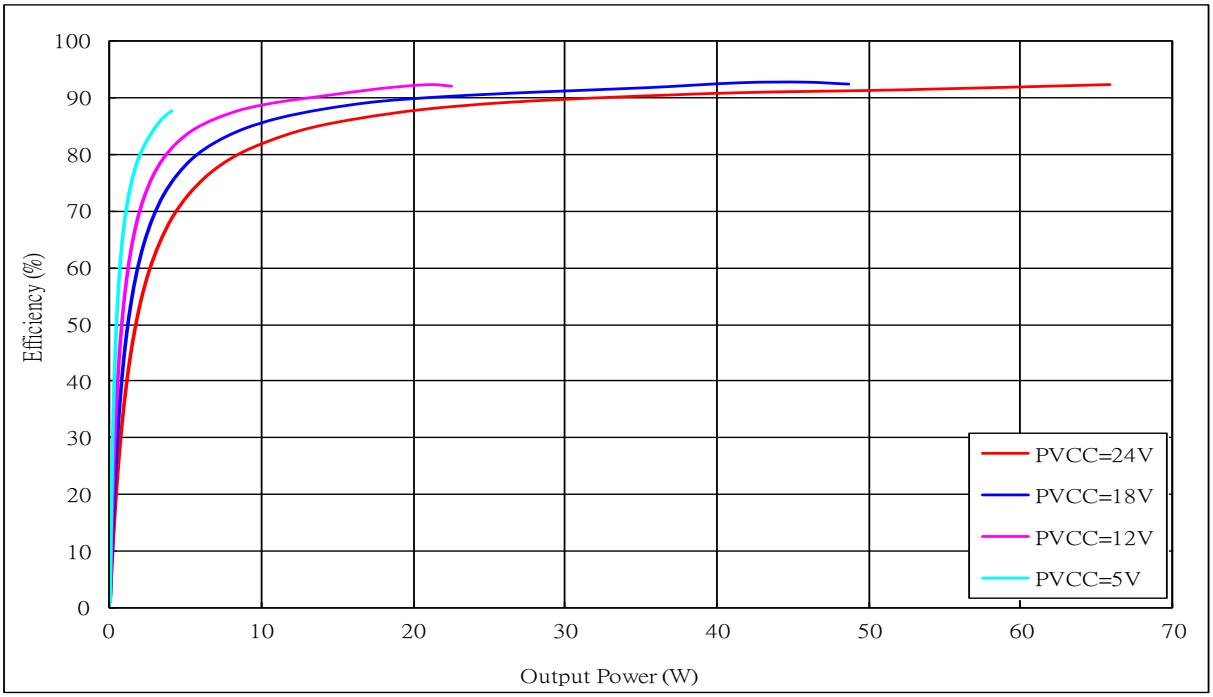
Noise



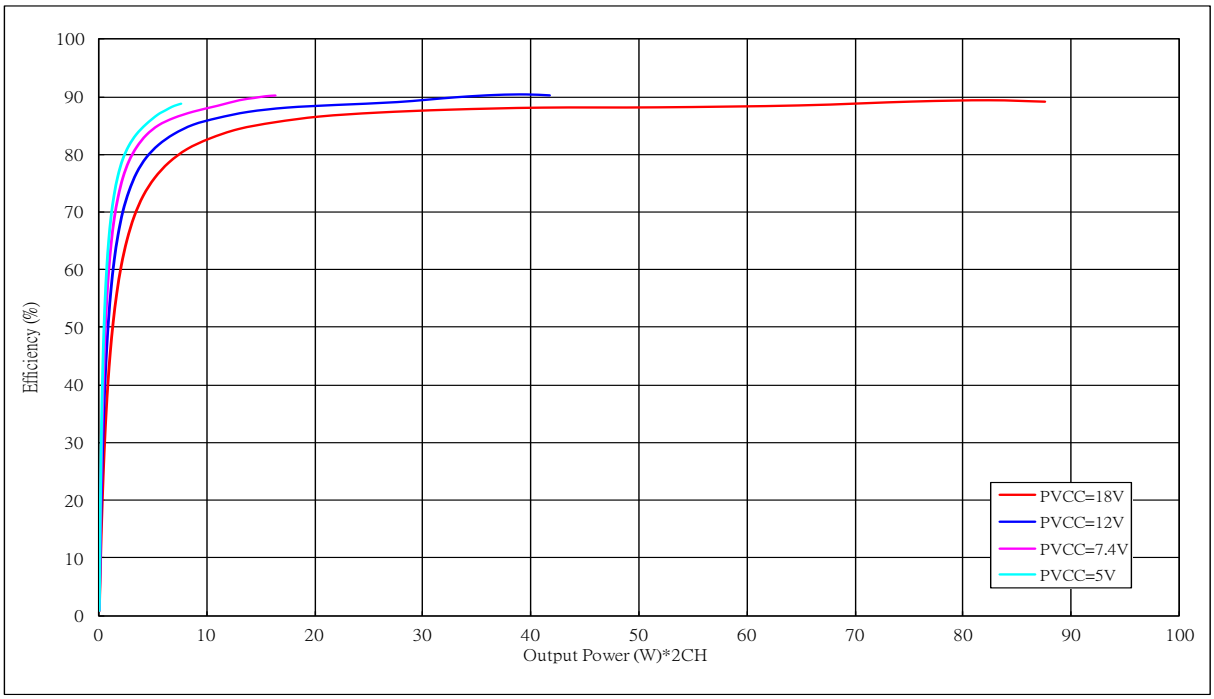
Noise



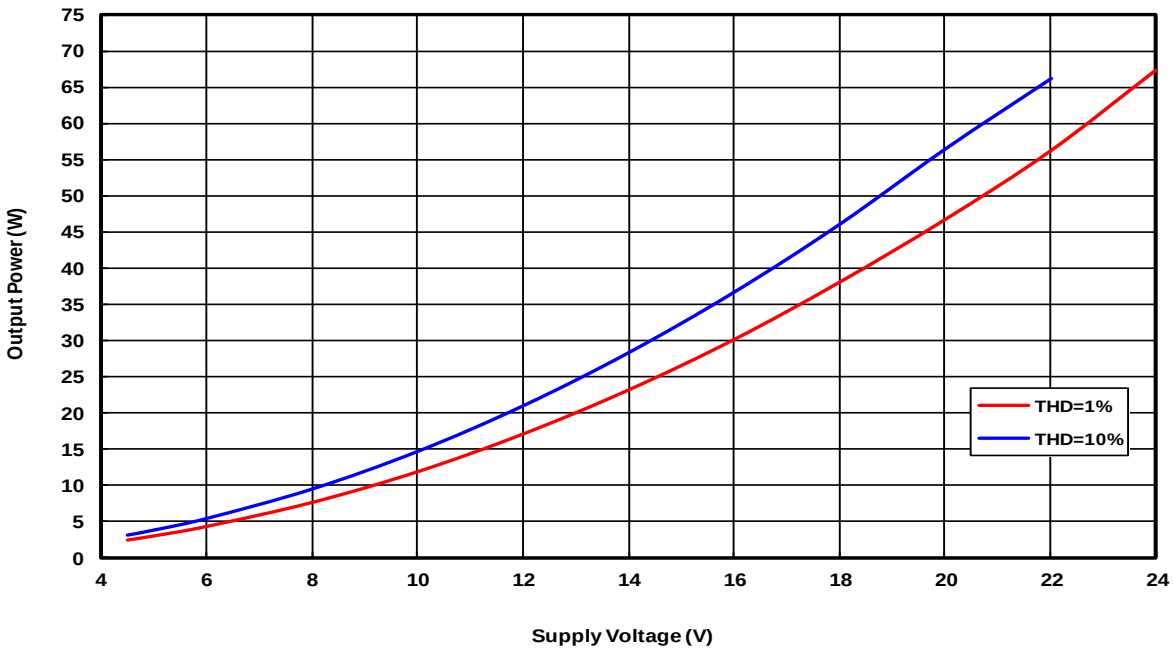
Efficiency (Mono 4ohm load)



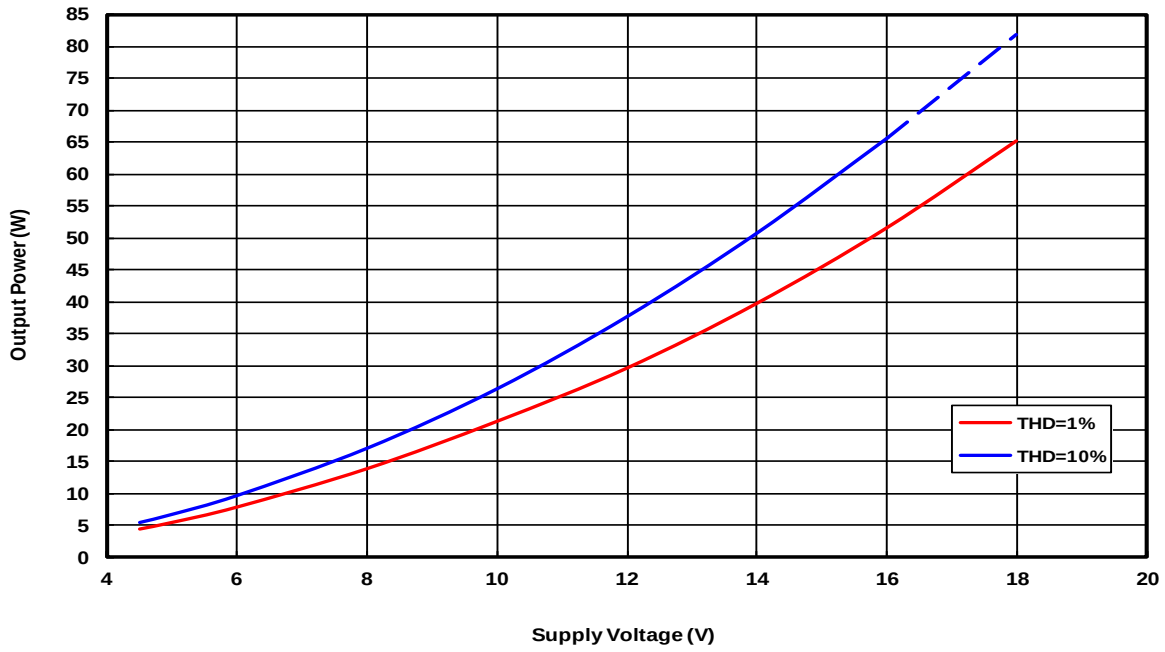
Efficiency (Mono 2ohm load)



Output Power vs. Supply Voltage (PBTL, 4ohm)



Output Power vs. Supply Voltage (PBTL, 2ohm)



Note: Dashed Line represent thermally limited regions.

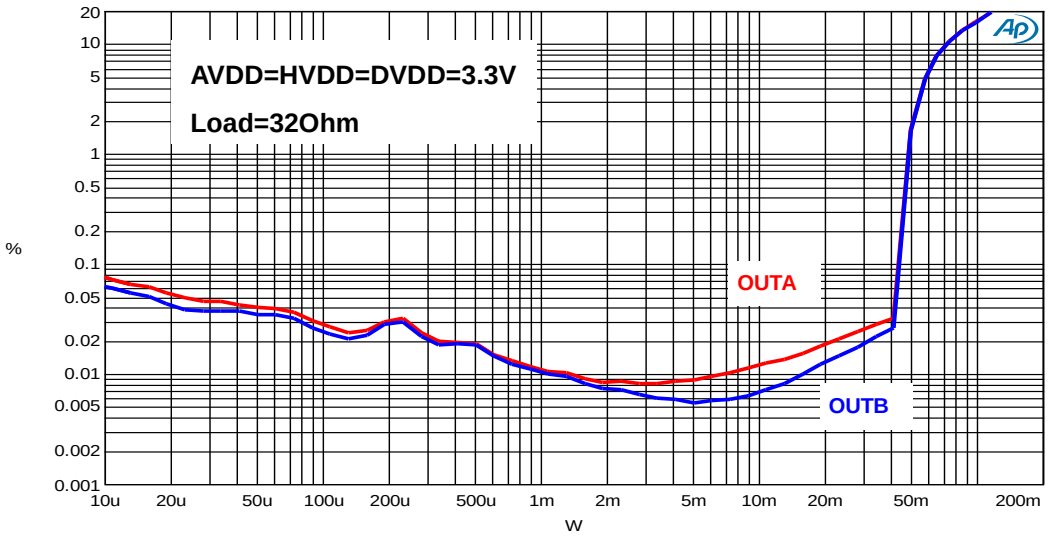
Electrical Characteristics and Specifications for DAC Output

● DAC output for Stereo

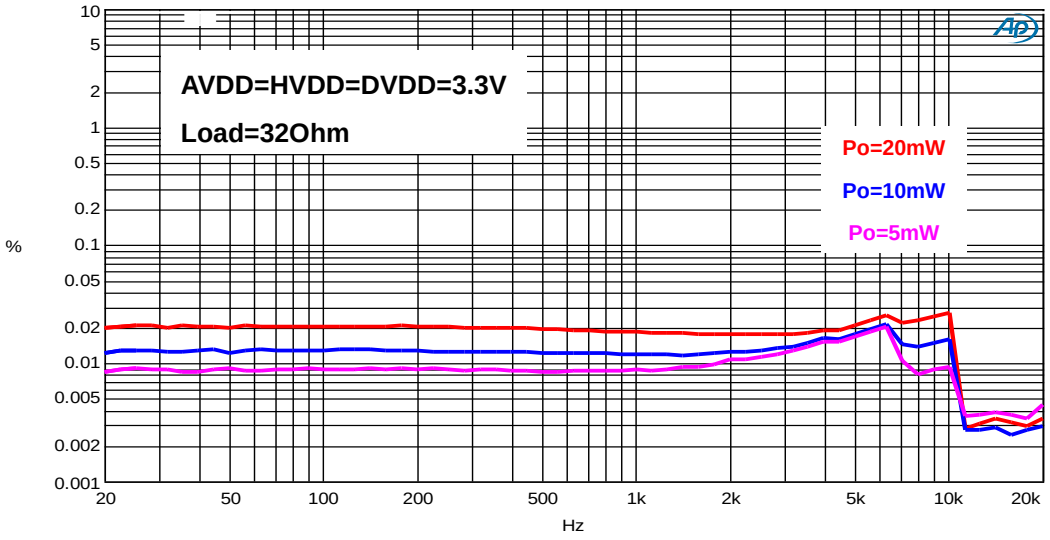
Condition: AVDD=HVDD=DVDD=3.3V, Fs=48kHz, C_{FLY}=C_{HVSS}=1μF, C_{HVDD}=1μF, R_L=10kΩ, T_A=25°C (unless otherwise noted)

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
V_O	Output Voltage (In Phase)	At THD+N=1%, f_{IN}=1kHz	2.0	2.3		Vrms
		At THD+N=1%, f_{IN}=1kHz, R_L=32ohm	25			mW
THD+N	Total Harmonic Distortion Plus Noise	V_O=2Vrms, f_{IN}=1kHz		0.17		%
		Pout=20mW, f_{IN}=1kHz, R_L=32ohm		0.02		
SNR	Signal to Noise Ratio	Output at THD+N=1%, f_{IN}=1kHz	100	109		*dB*
		Output at THD+N=1%, f_{IN}=1kHz, R_L=32ohm	95	103		
Crosstalk	Channel Separation	V_O=2Vrms, f_{IN}=1kHz	-90			dB
		Pout=10mW, f_{IN}=1kHz, R_L=32ohm	-80			
$\|V_{OS}\|$	Output Offset Voltage	Input Grounded		±1		mV
V_N	Output Noise			8	18	μVrms
PSRR		f_{IN}=1kHz, 200mVpp ripple	63	70		dB

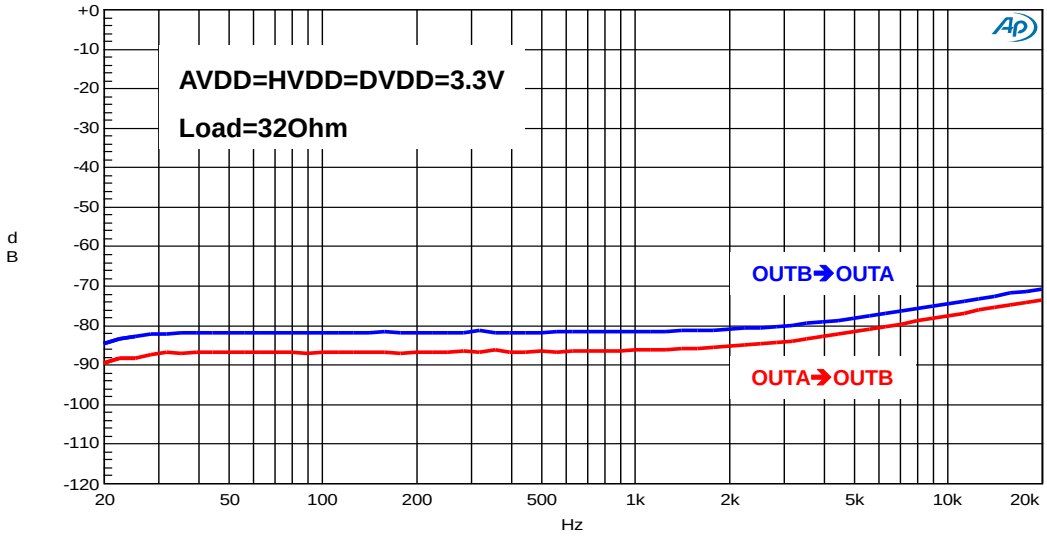
THD + N (%) v.s. Output power



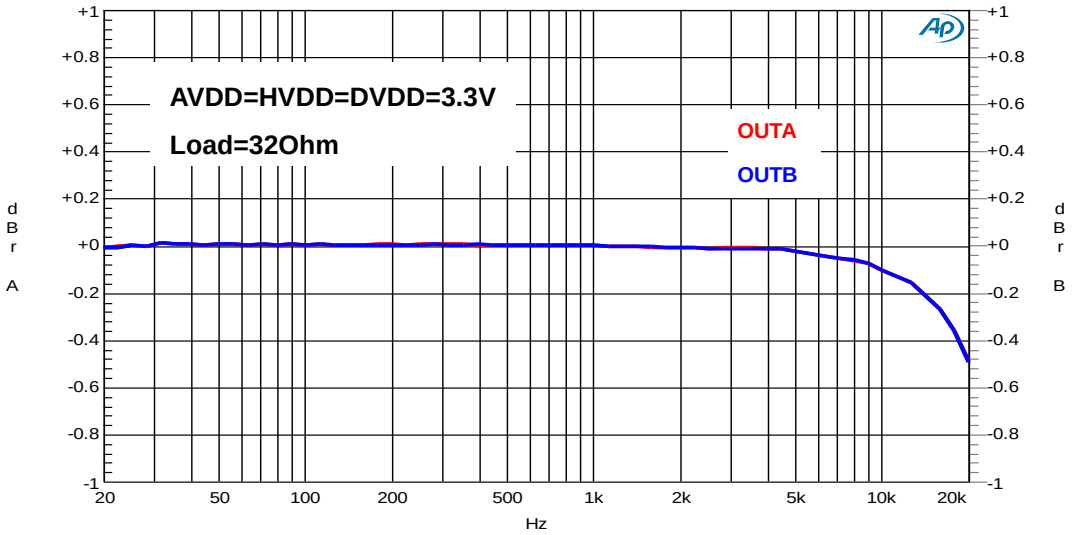
THD + N (%) v.s. Frequency



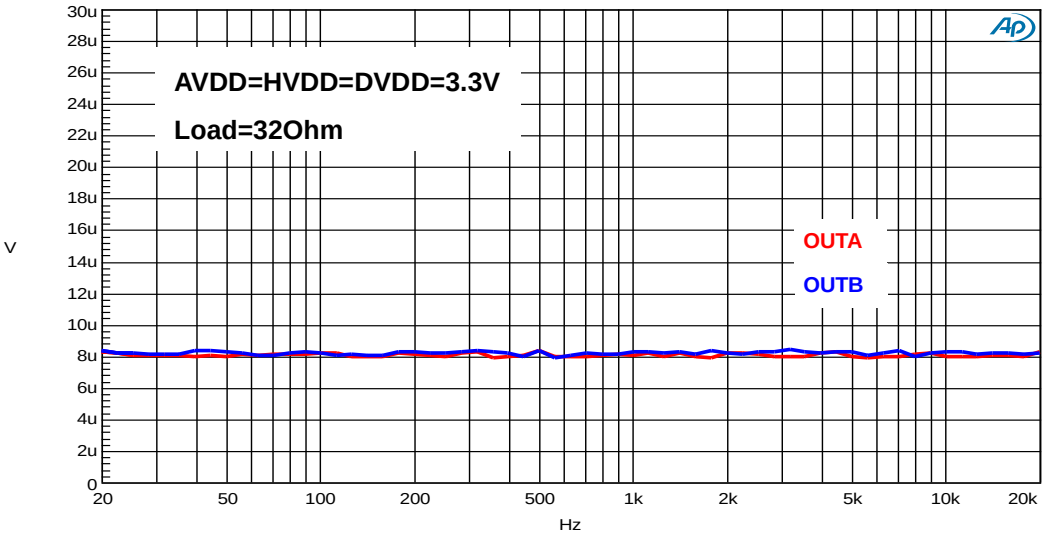
Crosstalk



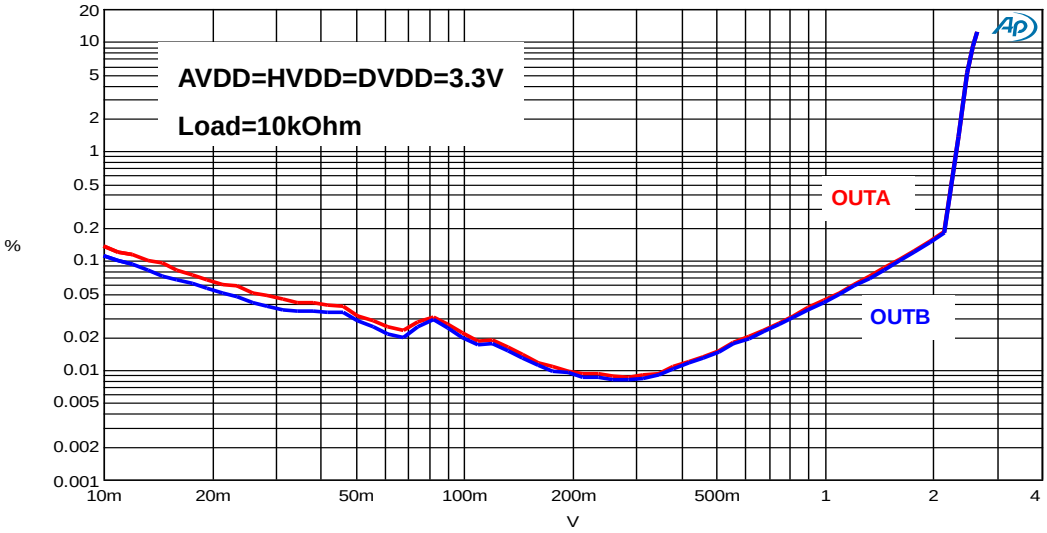
Frequency Response



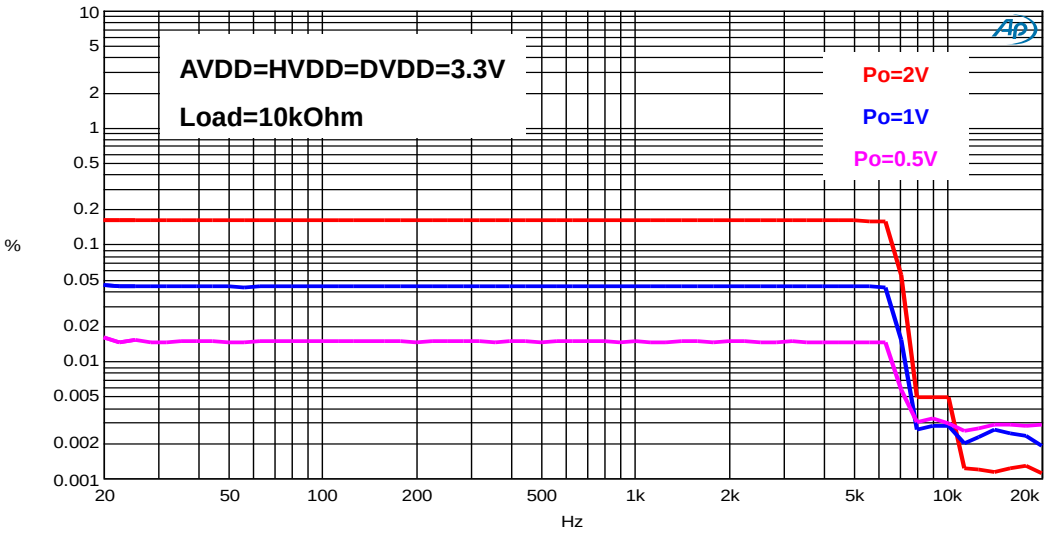
Noise


AVDD=HVDD=DVDD=3.3V
Load=32Ohm
OUTA
OUTB
V
Hz
30u
28u
26u
24u
22u
20u
18u
16u
14u
12u
10u
8u
6u
4u
2u
0
20
50
100
200
500
1k
2k
5k
10k
20k

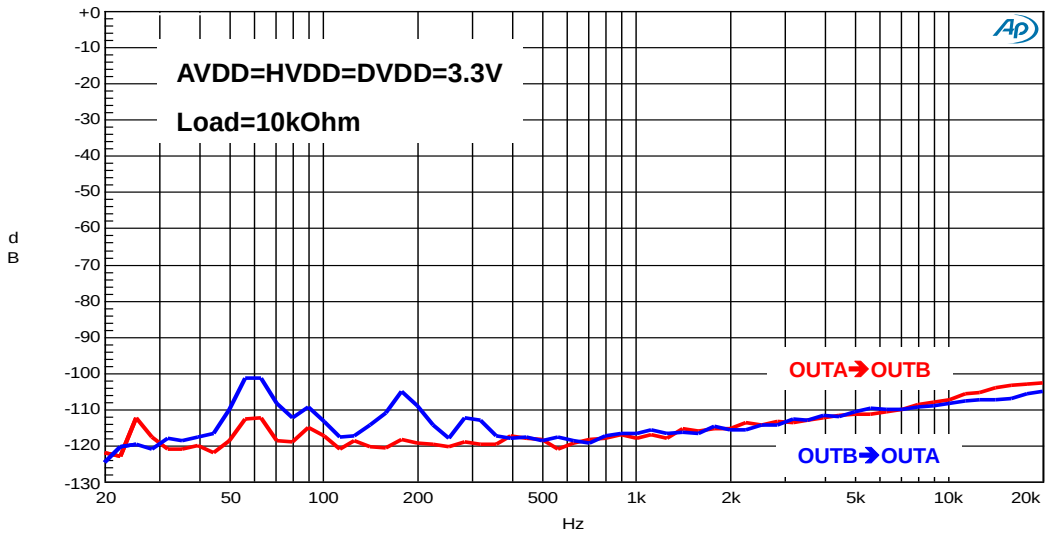
THD + N (%) v.s. Output power



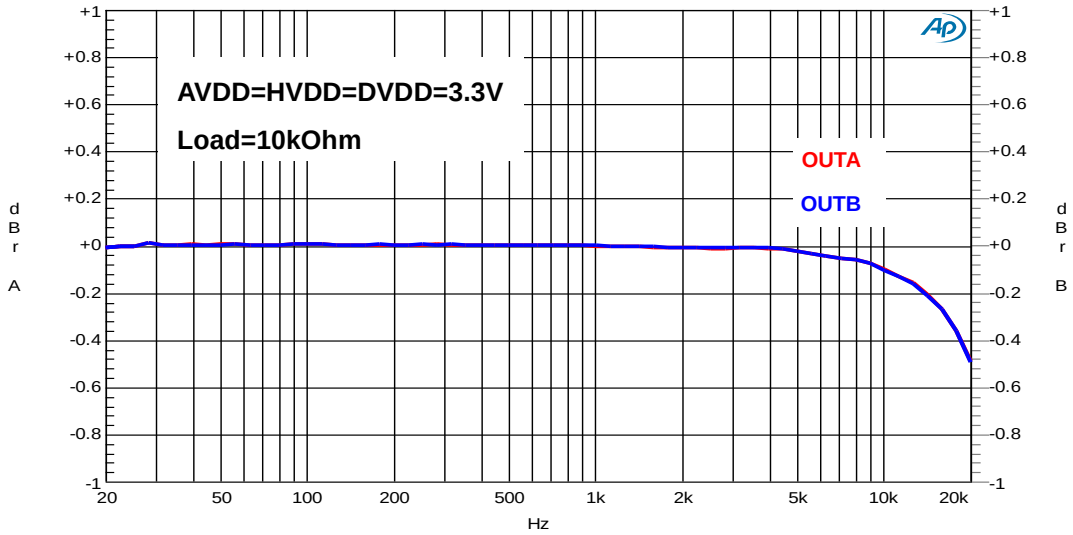
THD + N (%) v.s. Frequency



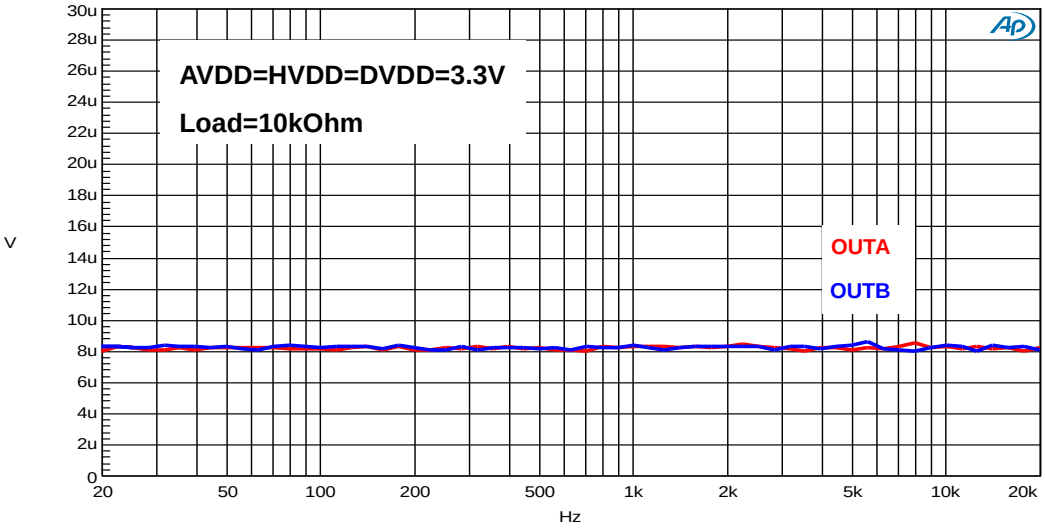
Crosstalk



Frequency Response

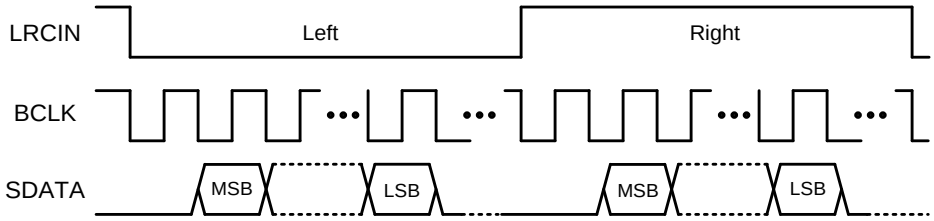


Noise

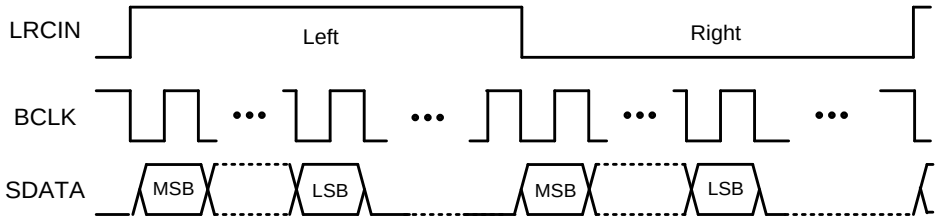

AVDD=HVDD=DVDD=3.3V
Load=10kOhm
OUTA
OUTB
V
Hz
30u
28u
26u
24u
22u
20u
18u
16u
14u
12u
10u
8u
6u
4u
2u
0
20
50
100
200
500
1k
2k
5k
10k
20k

Interface configuration

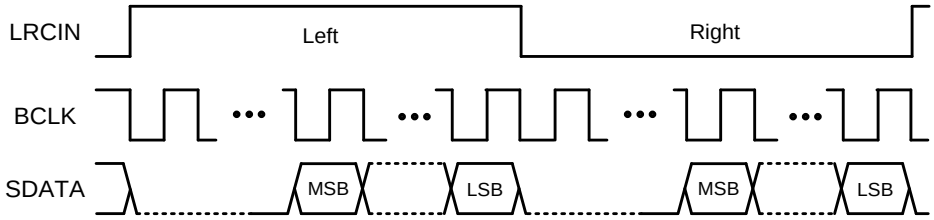
- I^2S



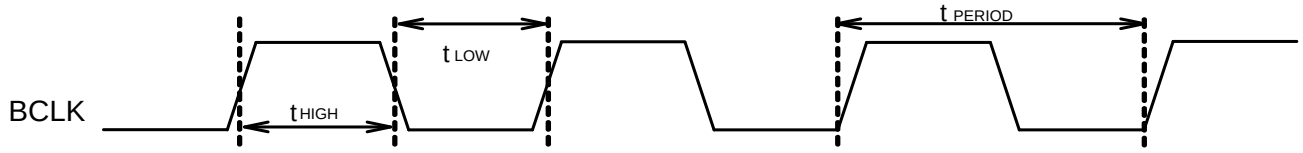
- Left-Alignment



- Right-Alignment



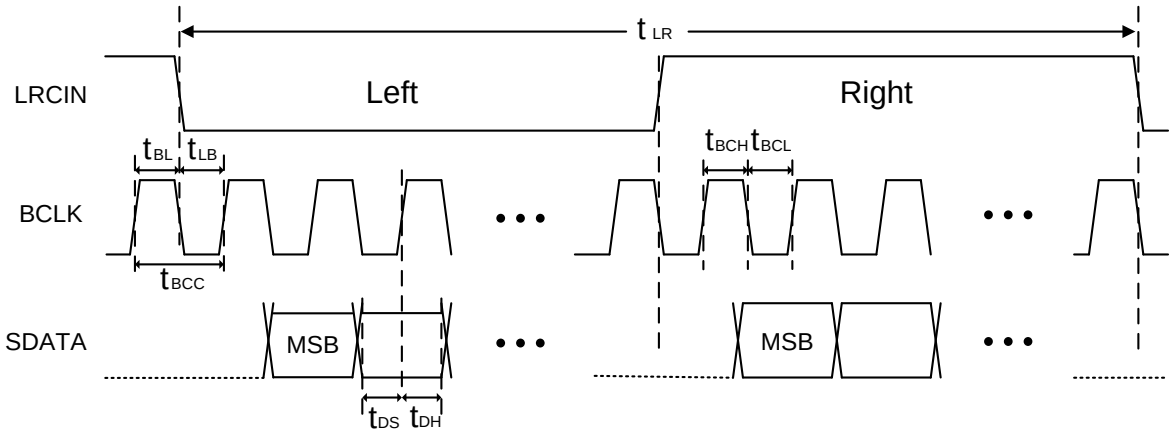
- System Clock Timing



$t_{HIGH} \geqq 162.7$ ns , $t_{LOW} \geqq 162.7$ ns , $t_{PERIOD} \geqq 325.4$ ns

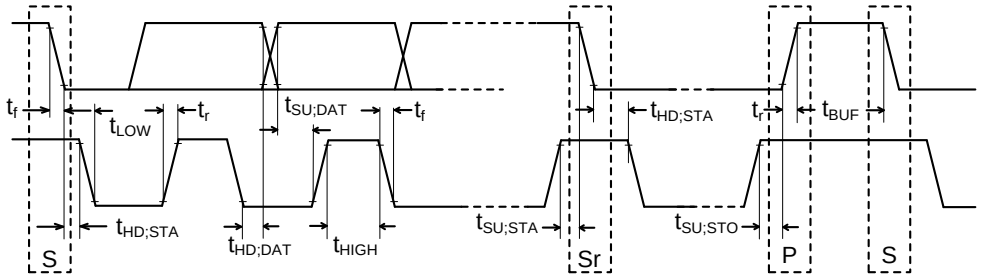
Default setting,PLL is enable
BCLK system

- Timing Relationship (Using I^2S format as an example)



Symbol	Parameter	Min	Typ	Max	Units
t_{LR}	LRCIN Period ($1/F_S$)	5.2		31.25	μs
t_{BL}	BCLK Rising Edge to LRCIN Edge	25			ns
t_{LB}	LRCIN Edge to BCLK Rising Edge	25			ns
t_{BCC}	BCLK Period ($1/64F_S$)	81.38		488.3	ns
t_{BCH}	BCLK Pulse Width High	40.69		244	ns
t_{BCL}	BCLK Pulse Width Low	40.69		244	ns
t_{DS}	SDATA Set-Up Time	25			ns
t_{DH}	SDATA Hold Time	25			ns

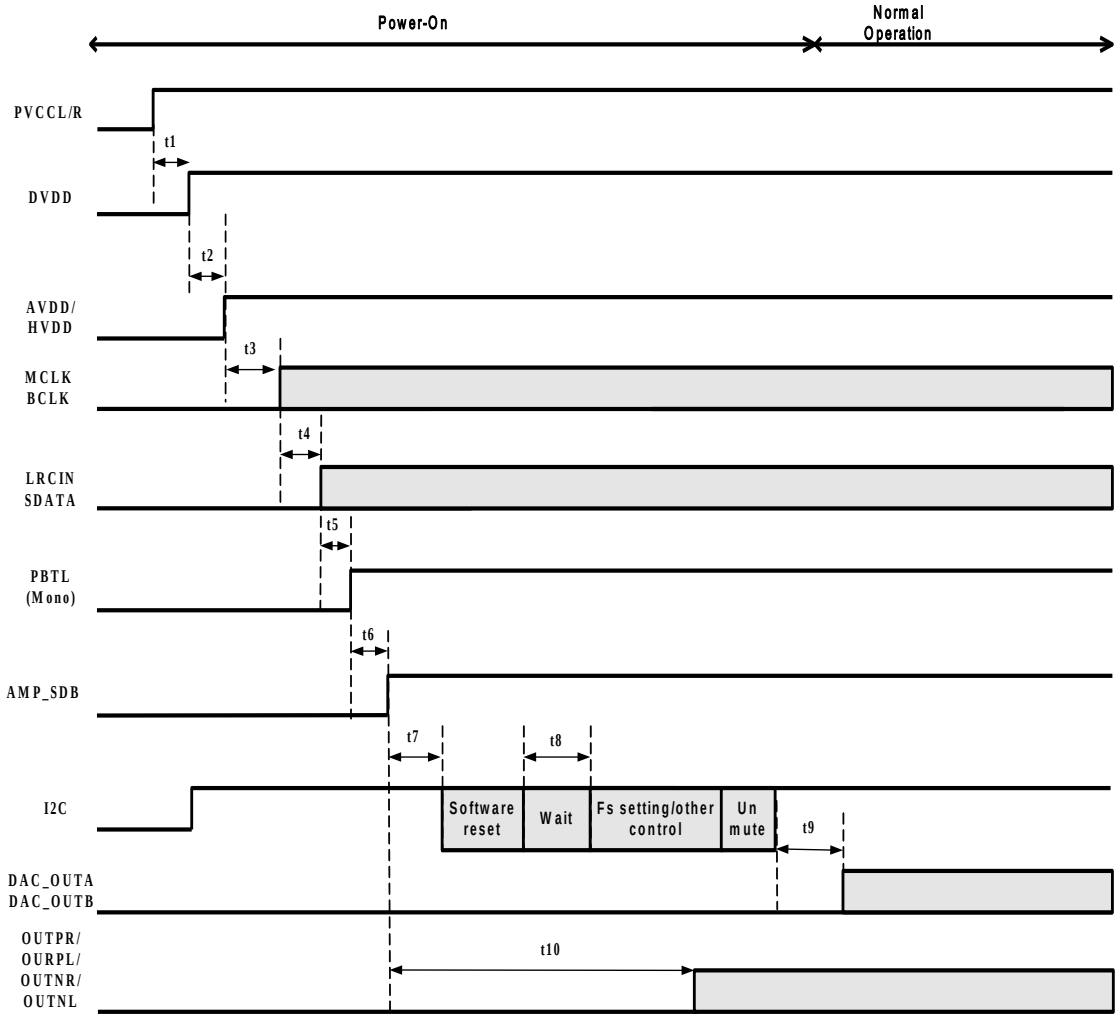
- I^2C Timing



Parameter	Symbol	Standard Mode		Fast Mode		Unit
		MIN.	MAX.	MIN.	MAX.	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Hold time for repeated START condition	$t_{HD,STA}$	4.0	---	0.6	---	μs
LOW period of the SCL clock	t_{LOW}	4.7	---	1.3	---	μs
HIGH period of the SCL clock	t_{HIGH}	4.0	---	0.6	---	μs
Setup time for repeated START condition	$t_{SU;STA}$	4.7	---	0.6	---	μs
Hold time for I^2C bus data	$t_{HD;DAT}$	0	3.45	0	0.9	μs
Setup time for I^2C bus data	$t_{SU;DAT}$	250	---	100	---	ns

Rise time of both SDA and SCL signals	t_r	---	1000	---	300	ns
Fall time of both SDA and SCL signals	t_f	---	300	---	300	ns
Setup time for STOP condition	$t_{SU;STO}$	4.0	---	0.6	---	µs
Bus free time between STOP and the next START condition	t_{BUF}	4.7	---	1.3	---	µs
Capacitive load for each bus line	C_b		400		400	pF

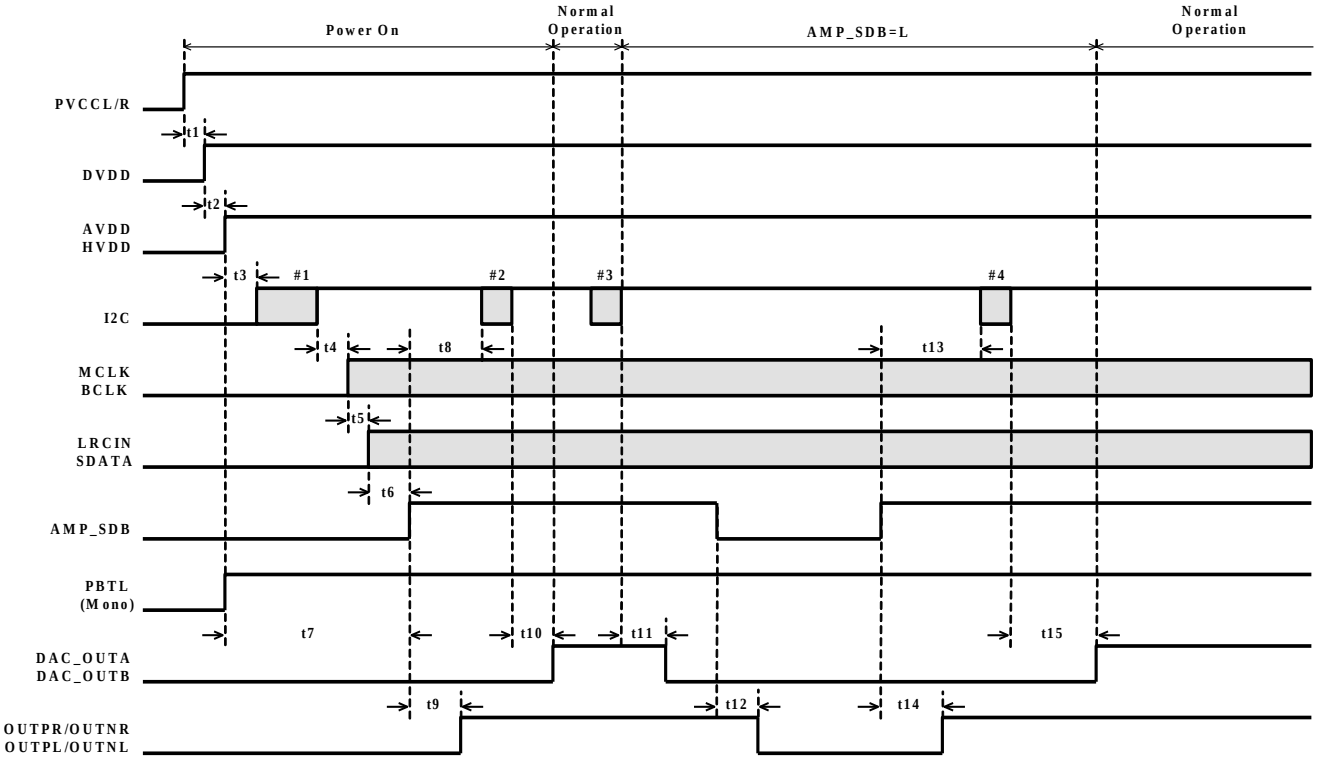
- Power on sequence for Fs=48KHz



Symbol	Condition	Min	Max	Units
t1		0	-	msec

t2		0	-	msec
t3		0	-	msec
t4		0	-	msec
t5		0	-	msec
t6		1		msec
t7		20	-	msec
t8		20	-	msec
t9		10		msec
t10			150	msec

- Power on sequence for 96KHz



#1: Steps

1) Set s/w reset bit=0
2) Delay 5ms
3) Set s/w reset bit=1
4) Delay 20ms
5) Set all channels=mute
6) Set I2S as Fs=96KHz
7) Set other registers, except (all channels=mute)

#2: Steps

1) Set all channel=unmute

#3: Steps

1) Set all channel=mute

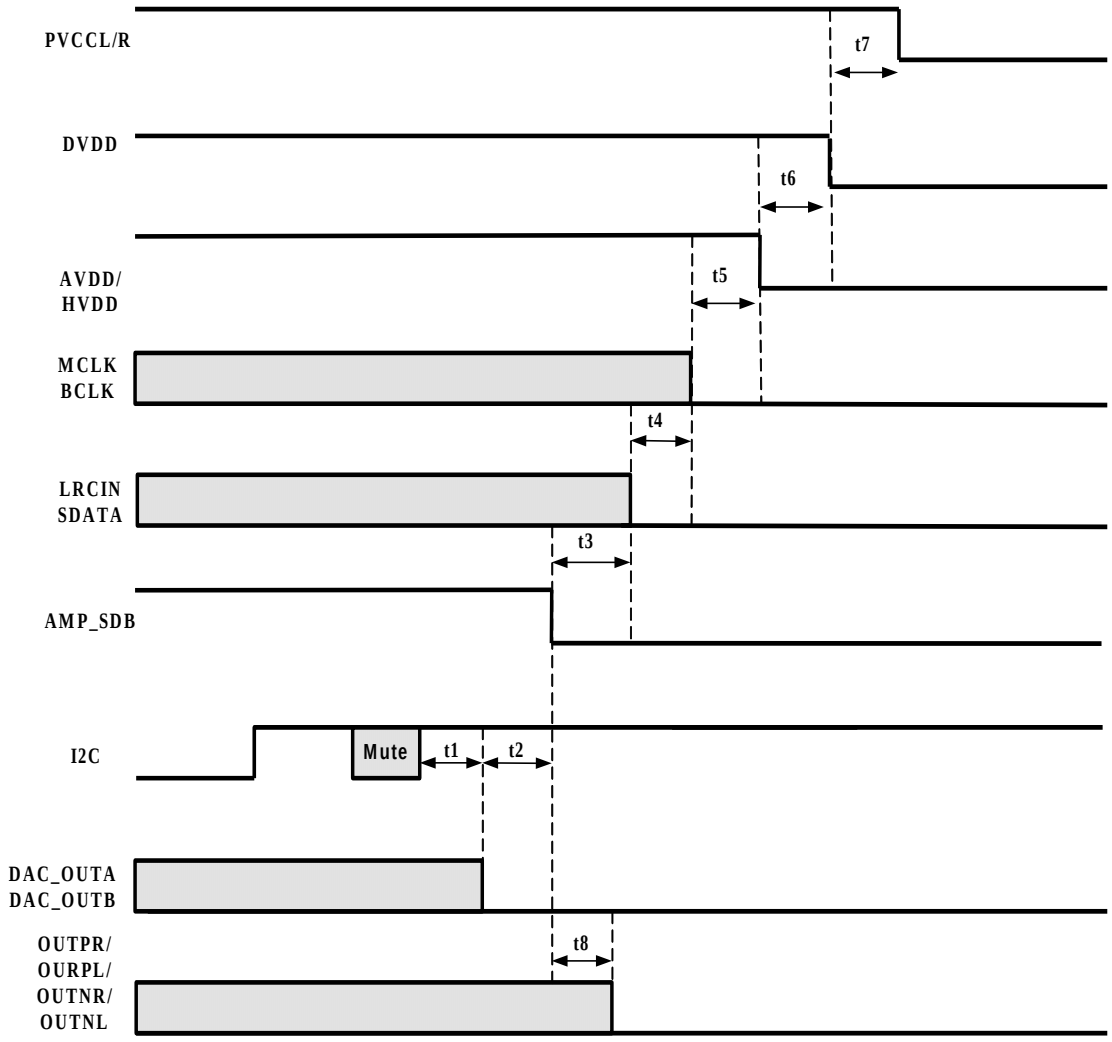
#4: Steps

1) Set all channel=unmute

#5: If reg0x1C B[2]=0, max. is 35ms
If reg0x1C B[2]=1, max. is 280ms

Symbol	Min	Max	Units	Symbol	Min	Max	Units
t1	0	-	msec	t10	10	-	msec
t2	0	-	msec	t11	-	#5	msec
t3	5	-	msec	t12	0.01	-	msec
t4	20	-	msec	t13	160	-	msec
t5	0	-	msec	t14	-	150	msec
t6	0	-	msec	t15	10	-	msec
t7	1		msec				
t8	160	-	msec				
t9	-	150	msec				

- Power off sequence



Symbol	Condition	Min	Max	Units

t1		35 (FADE_SPEED=0) 280 (FADE_SPEED=1)	-	msec
t2		0.1	-	msec
t3		0.1	-	msec
t4		1	-	msec
t5		1	-	msec
t6		0	-	msec
t7		1		msec
t8			0.01	msec

Operation Description

AD85050 has a built-in PLL internally, the default volume is muted. AD85050 will activate while the de-mute command via I^2C is programmed.

- DAC Output for headphone

  A conventional inverting headphone amplifier always requires an output dc-blocking capacitor and a bypass capacitor. DC blocking capacitors are large in size and cost a lot. It also restricts the output low frequency response. POP will occur if the charge and discharge processes on output capacitors are not carefully take cared. Besides, it needs to wait for a long time to charge output from 0V to 1/2 bias voltage.

  A cap-less DAC, a negative supply voltage is produced by the integrated charge-pump, and feeds to headphone driver's negative supply instead of ground. The DAC output is biased at ground which can eliminate the output dc-blocking capacitors. The output voltage swing is doubled compared to conventional amplifiers.

- Anti-pop design

  AD85050 will generate appropriate control signals to suppress pop sounds during initial power on/off, power down/up, mute, and volume level changes.

- 3D surround sound

  AD85050 provides the virtual surround sound technology with greater separation and depth voice quality for stereo signals.

- Shutdown control

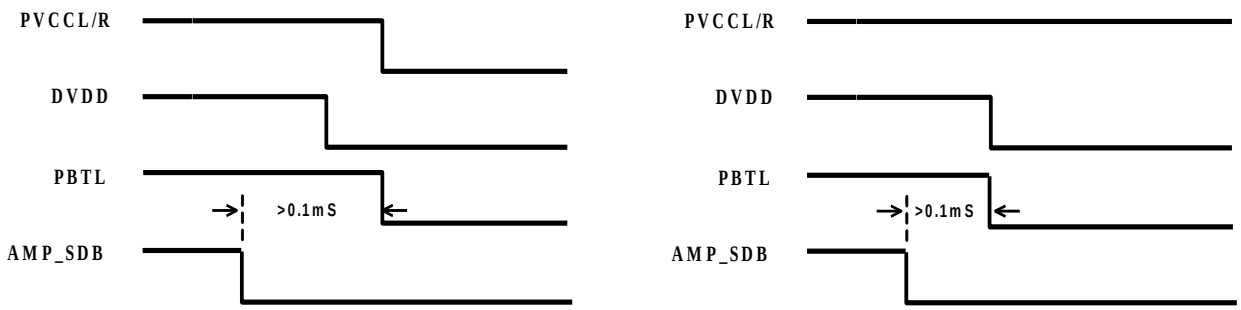
  Pulling AMP_SDB pin low will let AD85050 operate in low-current state for power conservation. The AD85050 outputs will enter mute once AMP_SDB pin is pulled low, and regulator (GVDD) will also disable to save power. If let AMP_SDB pin floating, the chip will enter shutdown mode because of the internal pull low resistor. For the best power-off performance, place the chip in the shutdown mode in advance of removing the power supply.

- HP_SPK control

  Pulling HP_SPK pin high (HP mode) will let SDZ pin operate in low state, connect the SDZ pin directly to AMP_SDB pin. The AMP output will be turned off. Pulling HP_SPK pin low (SPK mode) will let SDZ pin operate in high state, connect the SDZ pin directly to AMP_SDB pin. The AMP output will be turned on.

- PBTL (mono) function

AD85050 provides the application of parallel BTL operation with two outputs of each channel connected directly. If the PBTL pin is tied high, the positive and negative outputs of left and right channel are synchronized and in phase. Apply the input signal to the RIGHT channel input in PBTL mode and let the LEFT channel input grounded, and place the speaker between the LEFT and RIGHT outputs. The output swing is doubled of that in normal mode. See the application circuit example for PBTL (Mono) mode operation. For normal BTL (Stereo) operation, connect the PBTL pin to ground. Due to the positive and negative outputs are synchronized and in phase, PBTL pin voltage threshold shall be taken care in power off state to avoid the output channel short directly in mono configuration. The PBTL pin can't go to Low status when AMP_SDB=High.



The timing shall be taken care in Mono configuration

- Under-voltage detection

When the GVDD voltage is lower than 2.8V or the AVCC voltage is lower than 4V, loudspeaker drivers of right/left channel will be disabled and kept at low state. Otherwise, AD85050 return to normal operation.

When HVDD and AVDD voltage are lower than 2.6V, DAC output will be off.

- DC detection

AD85050 has dc detection circuit to protect the speakers from DC current which might be occurred as input capacitor defect or inputs short on printed circuit board. The detection circuit detects first volume amplifier stage output, when both differential outputs' voltage become higher than a determined voltage or lower than a determined voltage for more than 420ms, the dc detect error will occur and report to FAULTB pin. At the same time, loudspeaker drivers of right/left channel will disable and enter Hi-Z. This fault can not be cleared by cycling AMP_SDB pin, it is necessary to cycle the PVCC supply.

The equivalent class-D output duty of the DC detect threshold is listed in table 1.

Table 1. Output DC Detect Duty (for Either Channel)

PVCC (V)	Output Duty Exceeds
8	20.8%
12	20.8%
24	20.8%

- Over-voltage protection

When the PVCC voltage is higher than 29.5V, loudspeaker will be disabled kept at low state. The protection status will be released as PVCC lower than 29V.

- Short-circuit protection

To protect loudspeaker drivers from over-current damage, AD85050 has built-in short-circuit protection circuit. When the wires connected to loudspeakers are shorted to each other or shorted to GND or to PVCC, overload detectors may activate. Once one of right and left channel overload detectors are active, the amplifier outputs will enter a Hi-Z state and the protection latch is engaged. The short protection fault is reported on FAULTB pin as a low state. The latch can be cleared by reset AMP_SDB pin or power supply cycling.

The short circuit protection latch can have auto-recovery function by connect the FAULTB pin directly to AMP_SDB pin. The latch state will be released after 420msec, and the short protection latch will re-cycle if output overload is detected again.

- Thermal protection

If the internal junction temperature is higher than 150^{o}C, the outputs of loudspeaker drivers will be disabled and at low state. The temperature for AD85050 returning to normal operation is about 125^{o}C. The variation of protected temperature is about 10%. Thermal protection faults are NOT reported on the FAULTB pin.

- Internal PLL

AD85050 has a built-in PLL internally, the BCLK/FS or MCLK/FS ratio, which is selected by I^2C control interface. The clock inputted into the BCLK or MCLK pin becomes the frequency of multiple edge evaluation in chip internally.

Fs	BCLK/FS Setting Ratio for PLL	BCLK Frequency	Multiple edge evaluation for bit clock	PWM Frequency
48kHz	64x	3.072MHz	16x	310kHz
44.1kHz	64x	2.8224MHz	16x	310kHz
32kHz	64x	2.048MHz	16x	310kHz

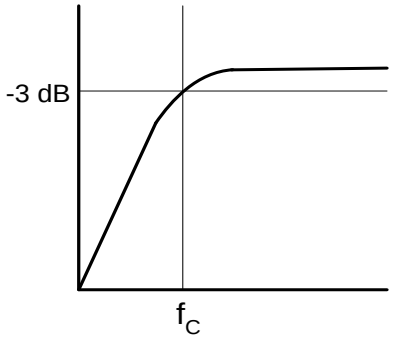
Fs	MCLK/FS Setting Ratio for PLL	MCLK Frequency	Multiple edge evaluation for Master clock	PWM Frequency
48kHz	256x	12.288MHz	4x	310kHz
44.1kHz	256x	11.2896MHz	4x	310kHz
32kHz	256x	8.192MHz	4x	310kHz
8kHz	256x	2.048MHz	16x	310kHz

Application information

- Input capacitors (C_{in})

  The performance at low frequency (bass) is affected by the corner frequency (f_c) of the high-pass filter composed of input resistor (R_{in}=60KΩ) and input capacitor (C_{in}), determined in equation (2). Typically, a 0.1μF or 1μF ceramic capacitor is suggested for C_{in}.

$$f_c = \frac{1}{2\pi R_{in} C_{in}} \ (\text{Hz})$$



- Ferrite Bead selection

  If the traces from the AD85050 to speaker are short, the ferrite bead filters can reduce the high frequency emissions to meet FCC requirements. A ferrite bead that has very low impedance at low frequency and high impedance at high frequency (above 1MHz) is recommended. The impedance of the ferrite bead can be used along with a small capacitor with a value around 1000pF to reduce the frequency spectrum of the signal to an acceptable level.

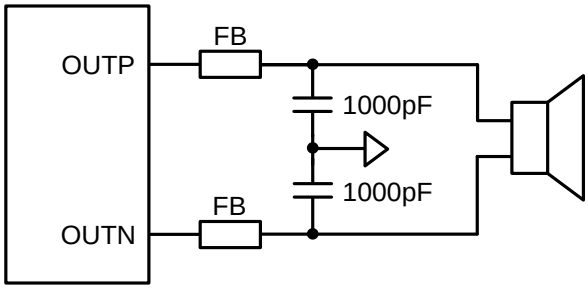


Figure 1. Typical Ferrite Bead Filter

- Output LC Filter

  If the traces from the AD85050 to speaker are not short, it is recommended to add the output LC filter to eliminate the high frequency emissions. Figure 2 shows the typical output filter for 8ohm speaker with a cut-off frequency of 61 kHz and Figure 3 shows the typical output filter for 4ohm speaker with a cut-off frequency of 34 kHz.

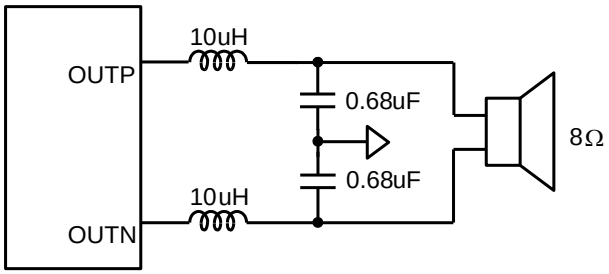


Figure 2. Typical LC Output Filter for 8Ω Speaker

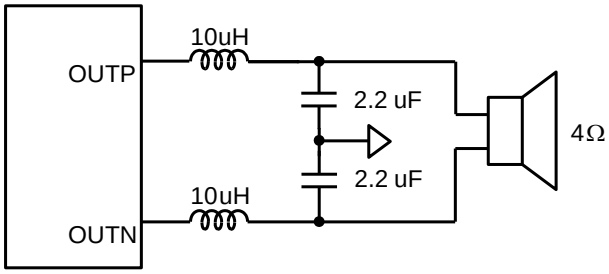


Figure 3. Typical LC Output Filter for 4Ω Speaker

- Power supply decoupling capacitor (Cs)

Because of the power loss on the trace between the device and decoupling capacitor, the decoupling capacitor should be placed close to PVCC and PGND to reduce any parasitic resistor or inductor. A low ESR ceramic capacitor, typically 1000pF, is suggested for high frequency noise rejection. For mid-frequency noise filtering, place a capacitor typically 0.1μF or 1μF as close as possible to the device PVCC leads works best. For low frequency noise filtering, a 100μF or greater capacitor (tantalum or electrolytic type) is suggested.

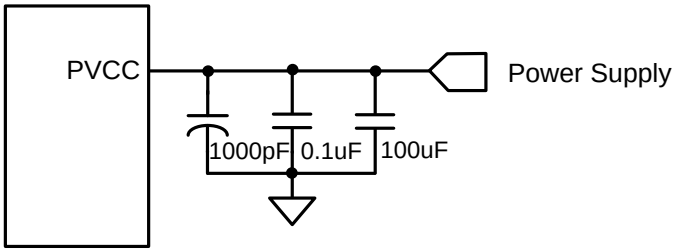


Figure 4. Recommended Power Supply Decoupling Capacitors.

I²C-Bus Transfer Protocol

- Introduction

AD85050 employs I²C-bus transfer protocol. Two wires, serial data and serial clock carry information between the devices connected to the bus. Each device is recognized by a unique 7-bit address and can operate as either a transmitter or a receiver. The master device initiates a data transfer and provides the serial clock on the bus. AD85050 is always an I²C slave device.

- Protocol

  - START and STOP condition

START is identified by a high to low transition of the SDA signal. A START condition must precede any command for data transfer. A STOP is identified by a low to high transition of the SDA signal. A STOP condition terminates communication between AD85050 and the master device on the bus. In both START and STOP, the SCL is stable in the high state.

  - Data validity

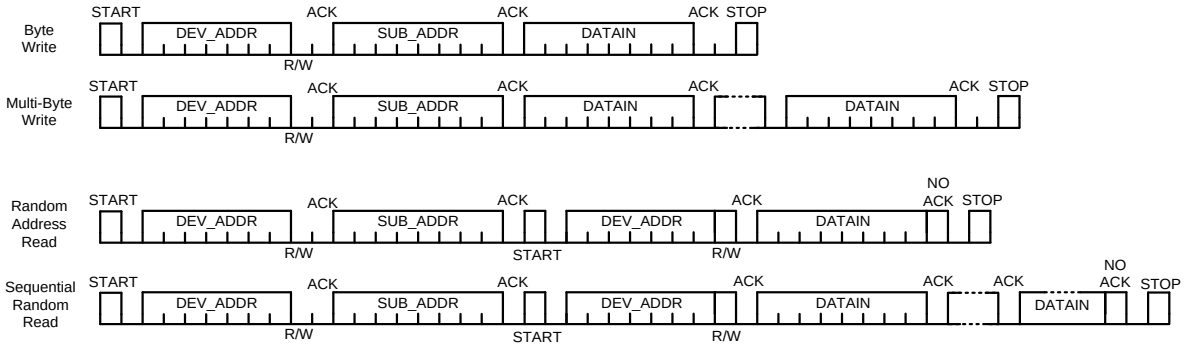
The SDA signal must be stable during the high period of the clock. The high or low change of SDA only occurs when SCL signal is low. AD85050 samples the SDA signal at the rising edge of SCL signal.

  - Device addressing

The master generates 7-bit address to recognize slave devices. When AD85050 receives 7-bit address matched with 0110x0y (where x and y can be selected by external SA0 and SA1 pins, respectively), AD85050 will acknowledge at the 9th bit (the 8th bit is for R/W bit). The bytes following the device identification address are for AD85050 internal sub-addresses.

  - Data transferring

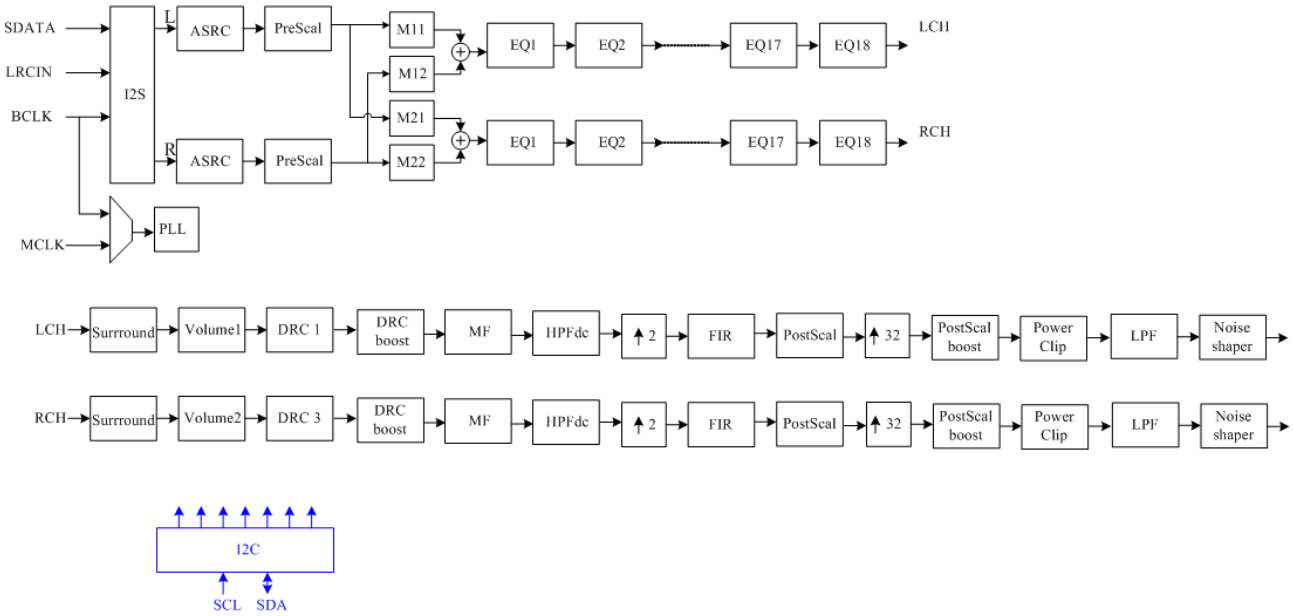
Each byte of SDA signaling must consist of 8 consecutive bits, and the byte is followed by an acknowledge bit. Data is transferred with MSB first, as shown in the figure below. In both write and read operations, AD85050 supports both single-byte and multi-byte transfers. Refer to the figure below for detailed data-transferring protocol.



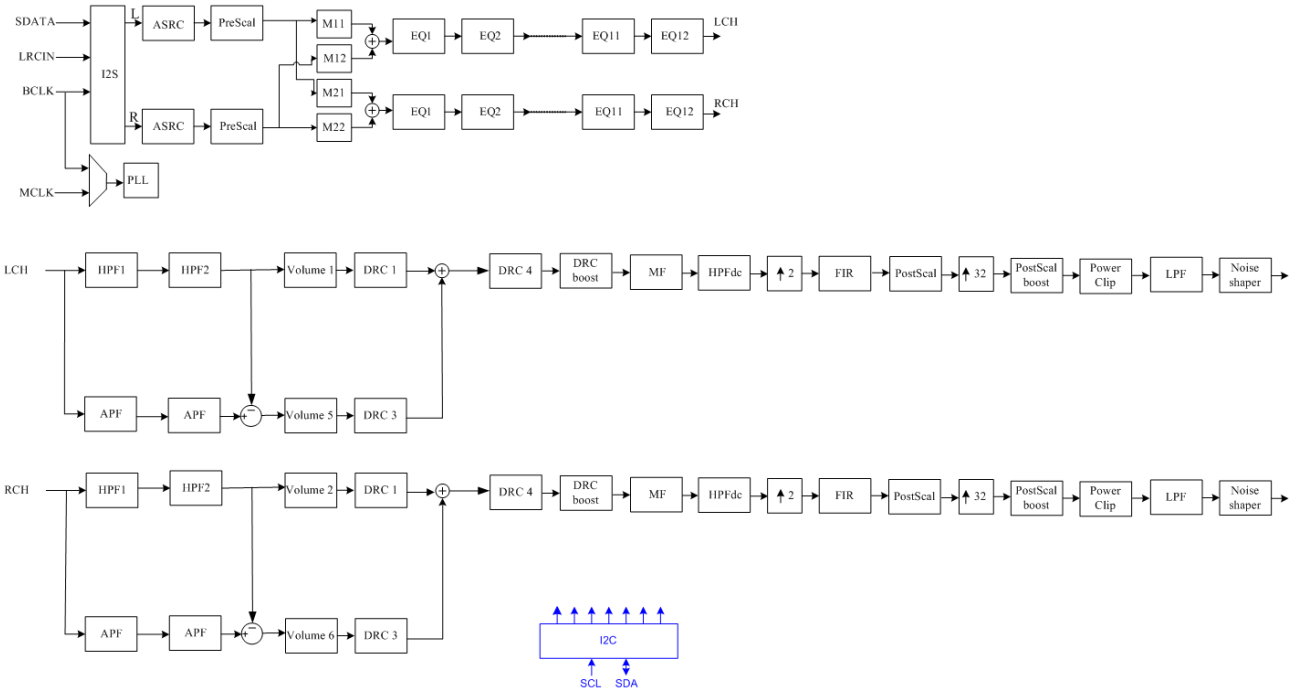
Register Table

The AD85050's audio signal processing data flow is shown below. Users can control these functions by programming appropriate settings in the register table. In this section, the register table is summarized first. The definition of each register follows in the next section.

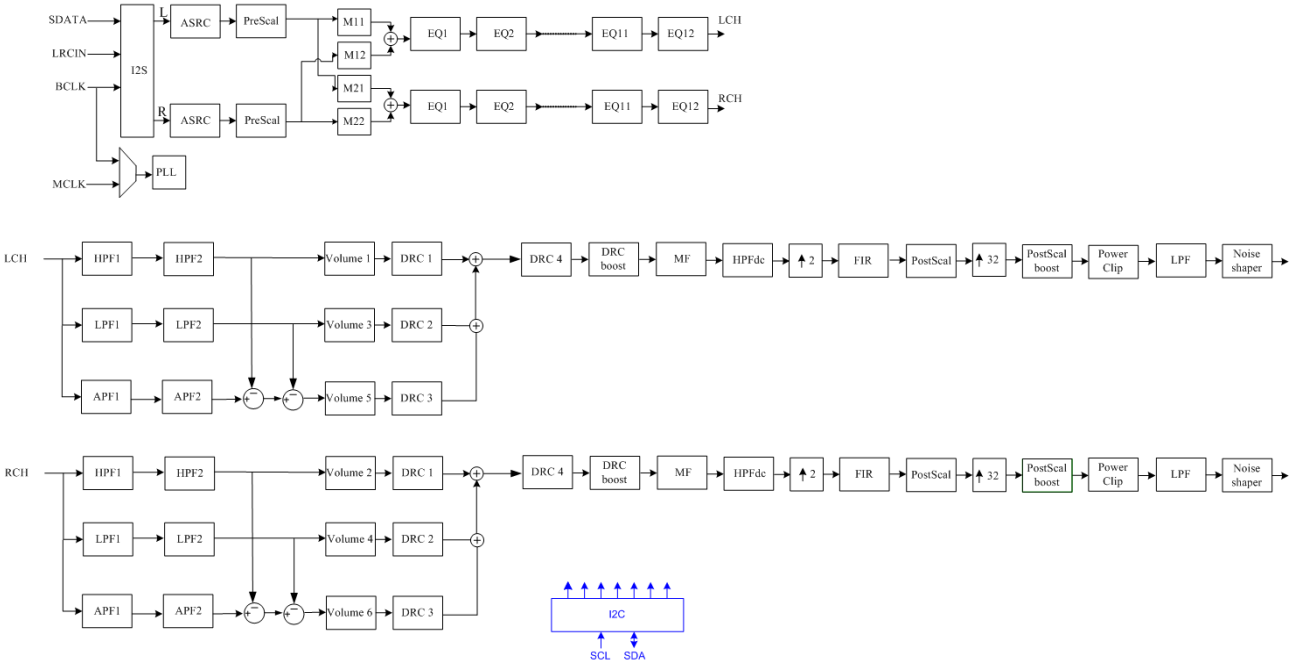
One band DRC



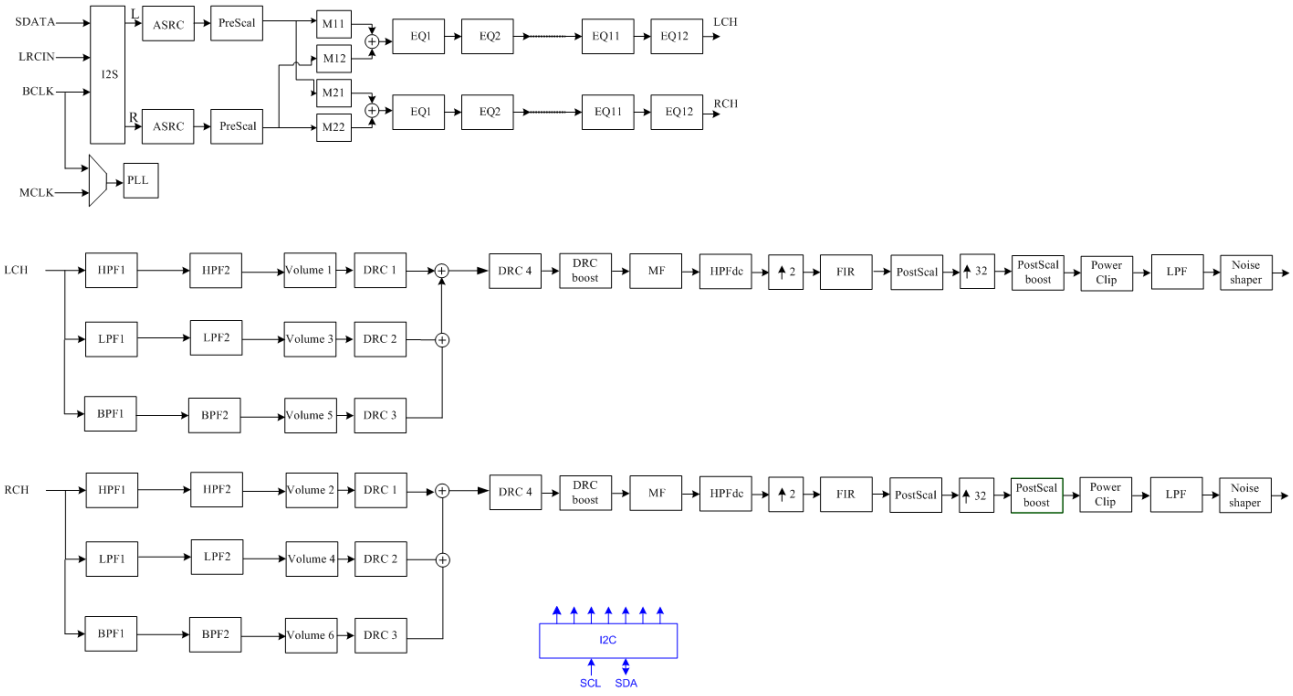
Dual band DRC



Three bands DRC – Type 1



Three bands DRC – Type 2



Register Table

Address	Name	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]	Default
0X00	SCTL1	IF[2]	IF[1]	IF[0]	Reserved	Reserved	Reserved	Reserved	LREXC	0X00
0X01	SCTL2	BCLK_SEL	FS[2]	FS[1]	FS[0]	PMF[3]	PMF[2]	PMF[1]	PMF[0]	0X91
0X02	SCTL3	Reserved	MUTE	CM1	CM2	CM3	CM4	CM5	CM6	0X00
0X03	MVOL	MV[7]	MV[6]	MV[5]	MV[4]	MV[3]	MV[2]	MV[1]	MV[0]	0XFF
0X04	C1VOL	C1V[7]	C1V[6]	C1V[5]	C1V[4]	C1V[3]	C1V[2]	C1V[1]	C1V[0]	0X18
0X05	C2VOL	C2V[7]	C2V[6]	C2V[5]	C2V[4]	C2V[3]	C2V[2]	C2V[1]	C2V[0]	0X18
0X06	C3VOL	C3V[7]	C3V[6]	C3V[5]	C3V[4]	C3V[3]	C3V[2]	C3V[1]	C3V[0]	0X18
0X07	C4VOL	C4V[7]	C4V[6]	C4V[5]	C4V[4]	C4V[3]	C4V[2]	C4V[1]	C4V[0]	0X18
0X08	C5VOL	C5V[7]	C5V[6]	C5V[5]	C5V[4]	C5V[3]	C5V[2]	C5V[1]	C5V[0]	0X18
0X09	C6VOL	C6V[7]	C6V[6]	C6V[5]	C6V[4]	C6V[3]	C6V[2]	C6V[1]	C6V[0]	0X18
0X0A	BTONE	Reserved			BTC[4]	BTC[3]	BTC[2]	BTC[1]	BTC[0]	0X10
0X0B	TTONE	Reserved			TTC[4]	TTC[3]	TTC[2]	TTC[1]	TTC[0]	0X10
0X0C	SCTL4	SRBP	BTE	DEQE	NGE	EQL	PSL	DSPB	HPB	0X90
0X0D	C1CFG	Reserved				C1PCBP	C1DRCBP	Reserved	C1VBP	0X00
0X0E	C2CFG	Reserved				C2PCBP	C2DRCBP	Reserved	C2VBP	0X00
0X0F	C3CFG	Reserved					C3DRCBP	Reserved	C3VBP	0X00
0X10	C4CFG	Reserved					C4DRCBP	Reserved	C4VBP	0X00
0X11	C5CFG	Reserved					C5DRCBP	Reserved	C5VBP	0X00
0X12	C6CFG	Reserved					C6DRCBP	Reserved	C6VBP	0X00
0X13	C7CFG	Reserved					C7DRCBP	Reserved	C7VBP	0X00
0X14	C8CFG	Reserved					C8DRCBP	Reserved	C8VBP	0X00
0X15	LAR1	LA1[3]	LA1[2]	LA1[1]	LA1[0]	LR1[3]	LR1[2]	LR1[1]	LR1[0]	0X6A
0X16	LAR2	LA2[3]	LA2[2]	LA2[1]	LA2[0]	LR2[3]	LR2[2]	LR2[1]	LR2[0]	0X6A
0X17	LAR3	LA3[3]	LA3[2]	LA3[1]	LA3[0]	LR3[3]	LR3[2]	LR3[1]	LR3[0]	0X6A
0X18	LAR4	LA4[3]	LA4[2]	LA4[1]	LA4[0]	LR4[3]	LR4[2]	LR4[1]	LR4[0]	0X6A
0X19	SCTL5	Reserved		HP_SPK_ON	DRCM	DRC_LINK	DB_CTRL_INV	DB_EN	MF_EN	0x10
0X1A	SCTL6	Reserved	PDB_REG	SW_RSTB	LVUV_FADE	Reserved	DIS_MCLK_DET	Reserved		0X70
0X1B	SCTL7	DRC_SEL[1]	DRC_SEL[0]	HOP[1]	HOP[0]	32X3	FS8K	TriBDRC_TYPE	Reserved	0X00
0X1C	SCTL8	Reserved	Reserved	POST_BOOST	DIS_NG_FADE	DRC_BOOST	FADE_SPEED	NG_GAIN[1]	NG_GAIN[0]	0X00
0X1D	CFADDR	CFA[7]	CFA[6]	CFA[5]	CFA[4]	CFA[3]	CFA[2]	CFA[1]	CFA[0]	0X00
0X1E	A1CF1	C1B[23]	C1B[22]	C1B[21]	C1B[20]	C1B[19]	C1B[18]	C1B[17]	C1B[16]	0X00
0X1F	A1CF2	C1B[15]	C1B[14]	C1B[13]	C1B[12]	C1B[11]	C1B[10]	C1B[9]	C1B[8]	0X00
0X20	A1CF3	C1B[7]	C1B[6]	C1B[5]	C1B[4]	C1B[3]	C1B[2]	C1B[1]	C1B[0]	0X00

0X21	A2CF1	C2B[23]	C2B[22]	C2B[21]	C2B[20]	C2B[19]	C2B[18]	C2B[17]	C2B[16]	0X00
0X22	A2CF2	C2B[15]	C2B[14]	C2B[13]	C2B[12]	C2B[11]	C2B[10]	C2B[9]	C2B[8]	0X00
0X23	A2CF3	C2B[7]	C2B[6]	C2B[5]	C2B[4]	C2B[3]	C2B[2]	C2B[1]	C2B[0]	0X00
0X24	B1CF1	C3B[23]	C3B[22]	C3B[21]	C3B[20]	C3B[19]	C3B[18]	C3B[17]	C3B[16]	0X00
0X25	B1CF2	C3B[15]	C3B[14]	C3B[13]	C3B[12]	C3B[11]	C3B[10]	C3B[9]	C3B[8]	0X00
0X26	B1CF3	C3B[7]	C3B[6]	C3B[5]	C3B[4]	C3B[3]	C3B[2]	C3B[1]	C3B[0]	0X00
0X27	B2CF1	C4B[23]	C4B[22]	C4B[21]	C4B[20]	C4B[19]	C4B[18]	C4B[17]	C4B[16]	0X00
0X28	B2CF2	C4B[15]	C4B[14]	C4B[13]	C4B[12]	C4B[11]	C4B[10]	C4B[9]	C4B[8]	0X00
0X29	B2CF3	C4B[7]	C4B[6]	C4B[5]	C4B[4]	C4B[3]	C4B[2]	C4B[1]	C4B[0]	0X00
0X2A	A0CF1	C5B[23]	C5B[22]	C5B[21]	C5B[20]	C5B[19]	C5B[18]	C5B[17]	C5B[16]	0X40
0X2B	A0CF2	C5B[15]	C5B[14]	C5B[13]	C5B[12]	C5B[11]	C5B[10]	C5B[9]	C5B[8]	0X00
0X2C	A0CF3	C5B[7]	C5B[6]	C5B[5]	C5B[4]	C5B[3]	C5B[2]	C5B[1]	C5B[0]	0X00
0X2D	CFRW	Reserved	RBS	R3	W3	RA	R1	WA	W1	0X00
0X2E	PRS	Prohibited								0X00
0X2F	MBIST	Prohibited								0X00
0X30	MSATEST	Prohibited								0X00
0X31	Reserved	Reserved								0X00
0X32	TM_CTRL	Prohibited								0X00
0X33	TM2_CTRL	Prohibited								0X00
0X34	VFT1	MV_FT[1]	MV_FT[0]	C1V_FT[1]	C1V_FT[0]	C2V_FT[1]	C2V_FT[0]	C3V_FT[1]	C3V_FT[0]	0X00
0X35	VFT2	C4V_FT[1]	C4V_FT[0]	C5V_FT[1]	C5V_FT[0]	C6V_FT[1]	C6V_FT[0]	Reserved		0X00
0X36	HP_CTRL	DAC_GAIN[1]	DAC_GAIN[0]	Reserved						0X00
0X37	ID	DN[3]	DN[2]	DN[1]	DN[0]	VN[3]	VN[2]	VN[1]	VN[0]	0XC8
0X38	R1ADDR	Prohibited								0X00
0X39	R1D1	Prohibited								0X00
0X3A	R1D2	Prohibited								0X00
0X3B	R1D3	Prohibited								0X00
0X3C	R1RW	Prohibited								0X00
0X3D	R3ADDR	Prohibited								0X00
0X3E	R3D1	Prohibited								0X00
0X3F	R3D2	Prohibited								0X00
0X40	R3D3	Prohibited								0X00
0X41	R3RW	Prohibited								0X00
0X42	LMC	C1_CLR	C2_CLR	C3_CLR	C4_CLR	C5_CLR	C6_CLR	C7_CLR	C8_CLR	0X00
0X43	PMC	C1_CLR_RMS	C2_CLR_RMS	C3_CLR_RMS	C4_CLR_RMS	C5_CLR_RMS	C6_CLR_RMS	C7_CLR_RMS	C8_CLR_RMS	0X00
0X44	TC1LM	C1_LEVEL[23]	C1_LEVEL[22]	C1_LEVEL[21]	C1_LEVEL[20]	C1_LEVEL[19]	C1_LEVEL[18]	C1_LEVEL[17]	C1_LEVEL[16]	Read only

0X45	MC1LM	C1_LEVEL[15]	C1_LEVEL[14]	C1_LEVEL[13]	C1_LEVEL[12]	C1_LEVEL[11]	C1_LEVEL[10]	C1_LEVEL[9]	C1_LEVEL[8]	read only
0X46	BC1LM	C1_LEVEL[7]	C1_LEVEL[6]	C1_LEVEL[5]	C1_LEVEL[4]	C1_LEVEL[3]	C1_LEVEL[2]	C1_LEVEL[1]	C1_LEVEL[0]	read only
0X47	TC2LM	C2_LEVEL[23]	C2_LEVEL[22]	C2_LEVEL[21]	C2_LEVEL[20]	C2_LEVEL[19]	C2_LEVEL[18]	C2_LEVEL[17]	C2_LEVEL[16]	read only
0X48	MC2LM	C2_LEVEL[15]	C2_LEVEL[14]	C2_LEVEL[13]	C2_LEVEL[12]	C2_LEVEL[11]	C2_LEVEL[10]	C2_LEVEL[9]	C2_LEVEL[8]	read only
0X49	BC2LM	C2_LEVEL[7]	C2_LEVEL[6]	C2_LEVEL[5]	C2_LEVEL[4]	C2_LEVEL[3]	C2_LEVEL[2]	C2_LEVEL[1]	C2_LEVEL[0]	read only
0X4A	TC3LM	C3_LEVEL[23]	C3_LEVEL[22]	C3_LEVEL[21]	C3_LEVEL[20]	C3_LEVEL[19]	C3_LEVEL[18]	C3_LEVEL[17]	C3_LEVEL[16]	read only
0X4B	MC3LM	C3_LEVEL[15]	C3_LEVEL[14]	C3_LEVEL[13]	C3_LEVEL[12]	C3_LEVEL[11]	C3_LEVEL[10]	C3_LEVEL[9]	C3_LEVEL[8]	read only
0X4C	BC3LM	C3_LEVEL[7]	C3_LEVEL[6]	C3_LEVEL[5]	C3_LEVEL[4]	C3_LEVEL[3]	C3_LEVEL[2]	C3_LEVEL[1]	C3_LEVEL[0]	read only
0X4D	TC4LM	C4_LEVEL[23]	C4_LEVEL[22]	C4_LEVEL[21]	C4_LEVEL[20]	C4_LEVEL[19]	C4_LEVEL[18]	C4_LEVEL[17]	C4_LEVEL[16]	read only
0X4E	MC4LM	C4_LEVEL[15]	C4_LEVEL[14]	C4_LEVEL[13]	C4_LEVEL[12]	C4_LEVEL[11]	C4_LEVEL[10]	C4_LEVEL[9]	C4_LEVEL[8]	read only
0X4F	BC4LM	C4_LEVEL[7]	C4_LEVEL[6]	C4_LEVEL[5]	C4_LEVEL[4]	C4_LEVEL[3]	C4_LEVEL[2]	C4_LEVEL[1]	C4_LEVEL[0]	read only
0X50	TC5LM	C5_LEVEL[23]	C5_LEVEL[22]	C5_LEVEL[21]	C5_LEVEL[20]	C5_LEVEL[19]	C5_LEVEL[18]	C5_LEVEL[17]	C5_LEVEL[16]	read only
0X51	MC5LM	C5_LEVEL[15]	C5_LEVEL[14]	C5_LEVEL[13]	C5_LEVEL[12]	C5_LEVEL[11]	C5_LEVEL[10]	C5_LEVEL[9]	C5_LEVEL[8]	read only
0X52	BC5LM	C5_LEVEL[7]	C5_LEVEL[6]	C5_LEVEL[5]	C5_LEVEL[4]	C5_LEVEL[3]	C5_LEVEL[2]	C5_LEVEL[1]	C5_LEVEL[0]	read only
0X53	TC6LM	C6_LEVEL[23]	C6_LEVEL[22]	C6_LEVEL[21]	C6_LEVEL[20]	C6_LEVEL[19]	C6_LEVEL[18]	C6_LEVEL[17]	C6_LEVEL[16]	read only
0X54	MC6LM	C6_LEVEL[15]	C6_LEVEL[14]	C6_LEVEL[13]	C6_LEVEL[12]	C6_LEVEL[11]	C6_LEVEL[10]	C6_LEVEL[9]	C6_LEVEL[8]	read only
0X55	BC6LM	C6_LEVEL[7]	C6_LEVEL[6]	C6_LEVEL[5]	C6_LEVEL[4]	C6_LEVEL[3]	C6_LEVEL[2]	C6_LEVEL[1]	C6_LEVEL[0]	read only
0X56	TC7LM	C7_LEVEL[23]	C7_LEVEL[22]	C7_LEVEL[21]	C7_LEVEL[20]	C7_LEVEL[19]	C7_LEVEL[18]	C7_LEVEL[17]	C7_LEVEL[16]	read only
0X57	MC7LM	C7_LEVEL[15]	C7_LEVEL[14]	C7_LEVEL[13]	C7_LEVEL[12]	C7_LEVEL[11]	C7_LEVEL[10]	C7_LEVEL[9]	C7_LEVEL[8]	read only
0X58	BC7LM	C7_LEVEL[7]	C7_LEVEL[6]	C7_LEVEL[5]	C7_LEVEL[4]	C7_LEVEL[3]	C7_LEVEL[2]	C7_LEVEL[1]	C7_LEVEL[0]	read only
0X59	TC8LM	C8_LEVEL[23]	C8_LEVEL[22]	C8_LEVEL[21]	C8_LEVEL[20]	C8_LEVEL[19]	C8_LEVEL[18]	C8_LEVEL[17]	C8_LEVEL[16]	read only
0X5A	MC8LM	C8_LEVEL[15]	C8_LEVEL[14]	C8_LEVEL[13]	C8_LEVEL[12]	C8_LEVEL[11]	C8_LEVEL[10]	C8_LEVEL[9]	C8_LEVEL[8]	read only
0X5B	BC8LM	C8_LEVEL[7]	C8_LEVEL[6]	C8_LEVEL[5]	C8_LEVEL[4]	C8_LEVEL[3]	C8_LEVEL[2]	C8_LEVEL[1]	C8_LEVEL[0]	read only
0X5C	I2S_OUT	Reserved					2S_DO_SEL[2]	2S_DO_SEL[1]	2S_DO_SEL[0]	0X05
0X5D	CHK_STATE	CHK_DRC_E	CHK_DRC_AM	CHK_DRC_R	CHK_DRC_EN	CHK_BEQ_E	CHK_BEQ_AM	CHK_BEQ_R	CHK_BEQ_EN	0X00
0X5E	DRC_CHK_TSV	CHS_DRC_V[23]	CHS_DRC_V[22]	CHS_DRC_V[21]	CHS_DRC_V[20]	CHS_DRC_V[19]	CHS_DRC_V[18]	CHS_DRC_V[17]	CHS_DRC_V[16]	0X00
0X5F	DRC_CHK_MSV	CHS_DRC_V[15]	CHS_DRC_V[14]	CHS_DRC_V[13]	CHS_DRC_V[12]	CHS_DRC_V[11]	CHS_DRC_V[10]	CHS_DRC_V[9]	CHS_DRC_V[8]	0X00
0X60	DRC_CHK_BSV	CHS_DRC_V[7]	CHS_DRC_V[6]	CHS_DRC_V[5]	CHS_DRC_V[4]	CHS_DRC_V[3]	CHS_DRC_V[2]	CHS_DRC_V[1]	CHS_DRC_V[0]	0X00
0X61	BEQ_CHK_TSV	CHS_BEQ_V[23]	CHS_BEQ_V[22]	CHS_BEQ_V[21]	CHS_BEQ_V[20]	CHS_BEQ_V[19]	CHS_BEQ_V[18]	CHS_BEQ_V[17]	CHS_BEQ_V[16]	0X00
0X62	BEQ_CHK_MSV	CHS_BEQ_V[15]	CHS_BEQ_V[14]	CHS_BEQ_V[13]	CHS_BEQ_V[12]	CHS_BEQ_V[11]	CHS_BEQ_V[10]	CHS_BEQ_V[9]	CHS_BEQ_V[8]	0X00
0X63	BEQ_CHK_BSV	CHS_BEQ_V[7]	CHS_BEQ_V[6]	CHS_BEQ_V[5]	CHS_BEQ_V[4]	CHS_BEQ_V[3]	CHS_BEQ_V[2]	CHS_BEQ_V[1]	CHS_BEQ_V[0]	0X00
0X64	DRC_CHK_TRT	CHS_DRC_R[23]	CHS_DRC_R[22]	CHS_DRC_R[21]	CHS_DRC_R[20]	CHS_DRC_R[19]	CHS_DRC_R[18]	CHS_DRC_R[17]	CHS_DRC_R[16]	read only
0X65	DRC_CHK_BRT	CHS_DRC_R[15]	CHS_DRC_R[14]	CHS_DRC_R[13]	CHS_DRC_R[12]	CHS_DRC_R[11]	CHS_DRC_R[10]	CHS_DRC_R[9]	CHS_DRC_R[8]	read only
0X66	DRC_CHK_BRT	CHS_DRC_R[7]	CHS_DRC_R[6]	CHS_DRC_R[5]	CHS_DRC_R[4]	CHS_DRC_R[3]	CHS_DRC_R[2]	CHS_DRC_R[1]	CHS_DRC_R[0]	read only
0X67	BEQ_CHK_TRT	CHS_BEQ_R[23]	CHS_BEQ_R[22]	CHS_BEQ_R[21]	CHS_BEQ_R[20]	CHS_BEQ_R[19]	CHS_BEQ_R[18]	CHS_BEQ_R[17]	CHS_BEQ_R[16]	read only
0X68	BEQ_CHK_MRT	CHS_BEQ_R[15]	CHS_BEQ_R[14]	CHS_BEQ_R[13]	CHS_BEQ_R[12]	CHS_BEQ_R[11]	CHS_BEQ_R[10]	CHS_BEQ_R[9]	CHS_BEQ_R[8]	read only

0X69	BEQ_CHK_BRT	CHS_BEQ_R[7]	CHS_BEQ_R[6]	CHS_BEQ_R[5]	CHS_BEQ_R[4]	CHS_BEQ_R[3]	CHS_BEQ_R[2]	CHS_BEQ_R[1]	CHS_BEQ_R[0]	read only
0X6A~0X6F	Reserved	Reserved								0X00
0X70	Dither_CT	Prohibited								0X78
0X71~0X73	Reserved	Reserved								0X00
0X74	MKHB	MK_HBYTE[7]								MK_HBYTE[6]
0X75	MKLB	MK_LBYTE[7]								MK_LBYTE[6]
0X76	Reserved	Reserved								0X00
0X77	HI_RES	Prohibited								0X07
0X78	TMR	Prohibited								0XFC
0X79	VOS	Prohibited								0X58
0X7A	Reserved	Reserved								0X00
0X7B	MBIST_UPT_E	Prohibited								0X55
0X7C	MBIST_UPT_E	Prohibited								0X55
0X7D	MBIST_UPT_E	Prohibited								0X55
0X7E	MBIST_UPT_O	Prohibited								0X55
0X7F	MBIST_UPT_O	Prohibited								0X55
0X80	MBIST_UPT_O	Prohibited								0X55
0X81	GPIO0_CTRL	Reserved			GPIO0_STATUS	GPIO0_CTRL[3]	GPIO0_CTRL[2]	GPIO0_CTRL[1]	GPIO0_CTRL[0]	0X00
0X82	GPIO1_CTRL	Reserved								0X00
0X83	GPIO2_CTRL	Reserved								0X00
0X84	ERR_REG	A_LVDET_N	A_OTP_N	Reserved			A_CKERR	Reserved		read only
0X85	ERR_RECORD	A_LVDET_N_LATCH	A_OTP_N__LATCH	Reserved			A_CKERR__LATCH	Reserved		read only
0X86	ERR_CLEAR	A_LVDET_N_CLEAR	A_OTP_N_CLEAR	Reserved			A_CKERR_CLEAR	Reserved		0X00
0X87	MV_HP	MV_HP[7]	MV_HP[6]	MV_HP[5]	MV_HP[4]	MV_HP[3]	MV_HP[2]	MV_HP[1]	MV_HP[0]	0XFF
0X88	C1V_HP	C1V_HP[7]	C1V_HP[6]	C1V_HP[5]	C1V_HP[4]	C1V_HP[3]	C1V_HP[2]	C1V_HP[1]	C1V_HP[0]	0X18
0X89	C2V_HP	C2V_HP[7]	C2V_HP[6]	C2V_HP[5]	C2V_HP[4]	C2V_HP[3]	C2V_HP[2]	C2V_HP[1]	C2V_HP[0]	0X18
0X8A	C3V_HP	C3V_HP[7]	C3V_HP[6]	C3V_HP[5]	C3V_HP[4]	C3V_HP[3]	C3V_HP[2]	C3V_HP[1]	C3V_HP[0]	0X18
0X8B	C4V_HP	C4V_HP[7]	C4V_HP[6]	C4V_HP[5]	C4V_HP[4]	C4V_HP[3]	C4V_HP[2]	C4V_HP[1]	C4V_HP[0]	0X18
0X8C	C5V_HP	C5V_HP[7]	C5V_HP[6]	C5V_HP[5]	C5V_HP[4]	C5V_HP[3]	C5V_HP[2]	C5V_HP[1]	C5V_HP[0]	0X18
0X8D	C6V_HP	C6V_HP[7]	C6V_HP[6]	C6V_HP[5]	C6V_HP[4]	C6V_HP[3]	C6V_HP[2]	C6V_HP[1]	C6V_HP[0]	0X18
0X8E	HPV_FT1	MV_FT_HP[1]	MV_FT_HP[0]	C1V_FT_HP[1]	C1V_FT_HP[0]	C2V_FT_HP[1]	C2V_FT_HP[0]	C3V_FT_HP[1]	C3V_FT_HP[0]	0X00
0x8F	HPV_FT2	C4V_FT_HP[1]	C4V_FT_HP[0]	C5V_FT_HP[1]	C5V_FT_HP[0]	C6V_FT_HP[1]	C6V_FT_HP[0]	Reserved		0X00
0X90	SMB_DB_L_AL	SMB_LA1[3]	SMB_LA1[2]	SMB_LA1[1]	SMB_LA1[0]	SMB_LR1[3]	SMB_LR1[2]	SMB_LR1[1]	SMB_LR1[0]	0X6A
0X91	SMB_DB_R_AL	SMB_RA1[3]	SMB_RA1[2]	SMB_RA1[1]	SMB_RA1[0]	SMB_RR1[3]	SMB_RR1[2]	SMB_RR1[1]	SMB_RR1[0]	0X6A
0X92	R2ADDR	Prohibited								0X00
0X93	R2D1	Prohibited								0X00

0X94	R2D2	Prohibited	0X00
0X95	R2D3	Prohibited	0X00
0X96	R2RW	Prohibited	0X00
0X97	R4ADDR	Prohibited	0X00
0X98	R4D1	Prohibited	0X00
0X99	R4D2	Prohibited	0X00
0X9A	R4D3	Prohibited	0X00
0X9B	R4RW	Prohibited	0X00

Detail Description for Register

Note that the highlighted columns are default values of these tables. If there is no highlighted value, the default setting of this bit is determined by the external pin.

- Address 0X00 : State control 1

  AD85050 supports multiple serial data input formats including I^2S, Left-alignment and Right-alignment. These formats are selected by users via bit7~bit5 of address 0X00. The left/right channels can be exchanged to each other by programming to address 0/bit0, LREXC.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:5]	IF[2:0]	Input Format	000	I^2S 16-24 bits
			001	Left-alignment 16-24 bits
			010	Right-alignment 16 bits
			011	Right-alignment 18 bits
			100	Right-alignment 20 bits
			101	Right-alignment 24 bits
B[4:1]		Reserved		
B[0]	LREXC	Left/Right (L/R) Channel exchanged	0	No exchanged
			1	L/R exchanged

- Address 0X01 : State control 2

AD85050 has a built-in PLL and supports multiple MCLK/Fs or BCLK/Fs ratios.

If BCLK_SEL is high, the ratio is changed to BCLK/FS ratios.

On the contrary, the ratio is changed to MCLK/FS ratios.

AD85050 has 8K sample rate application via 0X1B, bit 2 to enable it.

Detail setting is shown in the following table.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	BCLK_SEL	MCLK-less (BCLK system)	0	Disable
			1	Enable
B[6:4]	FS[2:0]	Sampling Frequency	000	32kHz
			001	44.1kHz, 48kHz
			010	64kHz
			011	88.2kHz, 96kHz
			100	128KHz
			101	176kHz, 192kHz

Multiple MCLK/FS in MCLK system or BCLK/FS in BCLK system ratio setting table

BIT	NAME	DESCRIPTION	VALUE	B[6:5]=00	B[6:5]=01	B[6:5]=1x
B[3:0]	PMF[3:0]	MCLK/Fs or BCLK/Fs setup	0000	1024x	512x	256x
			0001	Reset Default (64x)	Reset Default (64x)	Reset Default (64x)
			0010	128x	128x	128x
			0011	192x	192x	192x
			0100	256x	256x	256x
			0101	384x	384x	Reserved
			0110	512x	512x	
			0111	576x	Reserved	
			1000	768x		
			1001	1024x		

Multiple MCLK/FS ratio setting table of 8K application

BIT	NAME	DESCRIPTION	VALUE	0X1B, B[2]=1
B[3:0]	PMF[3:0]	MCLK/Fs Setup	0000	4096x
			0001	Reset Default (256x)
			0010	512x
			0011	768x
			0100	1024x
			0101	1536x
			0110	2048x
			0111	2304x
			1000	3072x
			1001	4096x

- Address 0X02 : State control 3

AD85050 has mute function including master mute and channel mute.

In one band DRC, master, channel 1, and channel 2 mute will be active.

When master mute is enabled, all 2 processing channels are muted. User can mute these 2 channels individually by channel mute. When the mute function is enabled or disabled, the fade-out or fade-in process will be initiated.

In three bands DRC, master, channel 1 to channel 6 mute will be active.

When master mute is enabled, all 6 processing channels are muted. User can mute these 6 channels individually by channel mute. When the mute function is enabled or disabled, the fade-out or fade-in process will be initiated.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]		Reserved		
B[6]	MMUTE	Master Mute	0	All channel not muted
			1	All channel muted
B[5]	CM1	Channel 1 Mute	0	Ch1 not muted
			1	Only Ch1 muted
B[4]	CM2	Channel 2 Mute	0	Ch2 not muted
			1	Only Ch2 muted
B[3]	CM3	Channel 3 Mute	0	Ch3 not muted
			1	Only Ch3 muted
B[2]	CM4	Channel 4 Mute	0	Ch4 not muted
			1	Only Ch4 muted
B[1]	CM5	Channel 5 Mute	0	Ch5 not muted
			1	Only Ch5 muted
B[0]	CM6	Channel 6 Mute	0	Ch6 not muted
			1	Only Ch6 muted

- Address 0X03 : Master volume control

AD85050 supports both master-volume (Address 0X03) and channel-volume control (Address 0X04, 0X05, 0X06, 0X07, 0X08, 0X09) modes. Both volume control settings range from +12dB ~ -103dB and 0.5dB per step. Note that the master volume control is added to the individual channel volume control as the total volume control. For example, if the master volume level is set at, Level A (in dB unit) and the channel volume level is set at Level B (in dB unit), the total volume control setting is equal to Level A plus with Level B.

-103dB ≦ Total volume (Level A + Level B) ≦ +24dB.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
BIT[7:0]	MV[7:0]	Master Volume	00000000	+12.0dB
			00000001	+11.5dB
			00000010	+11.0dB
			:	:
			00010111	+0.5dB
			00011000	0.0dB
			00011001	-0.5dB
			:	:
			11100110	-103.0dB
			11100111	-∞dB
			:	:
			11111111	-∞dB

- Address 0X04 : Channel 1 volume

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
BIT[7:0]	C1V[7:0]	Channel1 Volume	00000000	+12.0dB
			00000001	+11.5dB
			:	:
			00010100	+2dB
			:	:
			00011000	0.0dB
			00011001	-0.5dB
			:	:
			11100110	-103.0dB
			11100111	-∞dB
			:	:
			11111111	-∞dB

- Address 0X05 : Channel 2 volume

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
BIT[7:0]	C2V[7:0]	Channel2 Volume	00000000	+12.0dB
			00000001	+11.5dB
			:	:
			00010100	+2dB
			:	:
			00011000	0.0dB
			00011001	-0.5dB
			:	:
			11100110	-103.0dB
			11100111	-∞dB
			:	:
			11111111	-∞dB

- Address 0X06 : Channel 3 volume

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
BIT[7:0]	C3V[7:0]	Channel3 Volume	00000000	+12.0dB
			00000001	+11.5dB
			:	:
			00010100	+2dB
			:	:
			00011000	0.0dB
			00011001	-0.5dB
			:	:
			11100110	-103.0dB
			11100111	-∞dB
			:	:
			11111111	-∞dB

- Address 0X07 : Channel 4 volume

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
BIT[7:0]	C4V[7:0]	Channel 4 Volume	00000000	+12.0dB
			00000001	+11.5dB
			:	:
			00010100	+2dB
			:	:
			00011000	0.0dB
			00011001	-0.5dB
			:	:
			11100110	-103.0dB
			11100111	-∞dB
			:	:
			11111111	-∞dB

- Address 0X08 : Channel 5 volume

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
BIT[7:0]	C5V[7:0]	Channel 5 Volume	00000000	+12.0dB
			00000001	+11.5dB
			:	:
			00010100	+2dB
			:	:
			00011000	0.0dB
			00011001	-0.5dB
			:	:
			11100110	-103.0dB
			11100111	-∞dB
			:	:
			11111111	-∞dB

- Address 0X09 : Channel 6 volume

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
BIT[7:0]	C6V[7:0]	Channel 6 Volume	00000000	+12.0dB
			00000001	+11.5dB
			:	:
			00010100	+2dB
			:	:
			00011000	0.0dB
			00011001	-0.5dB
			:	:
			11100110	-103.0dB
			11100111	-∞dB
			:	:
			11111111	-∞dB

- Address 0X0A/0X0B : Bass/Treble tone boost and cut

EQ11 and EQ12 can be programmed as bass/treble tone boost and cut. When, register with address-0X0C, bit-6, BTE is set to high, the EQ11 and EQ12 will perform as bass and treble respectively. The -3dB corner frequency of bass is 360Hz, and treble is 7kHz. The gain range for both filters is +12db ~ -12dB with 1dB per step.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:5]		Reserved		
B[4:0]	BTC[4:0] / TTC[4:0]	The gain setting of boost and cut	00000	+12dB
			…	…
			00100	+12dB
			00101	+11dB
			00110	+10dB
			…	…
			01110	+2dB
			01111	+1dB
			10000	0dB
			10001	-1dB
			10010	-2dB
			…	…
			11010	-10dB
			11011	-11dB
			11100	-12dB
			…	…
			11111	-12dB

- Address 0X0C : State control 4

The AD85050 provides several DSP setting as following,

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	SRBP	Surround bypass	0	Surround enable
			1	Surround bypass
B[6]	BTE	Bass/Treble Selection bypass	0	Bass/Treble Disable
			1	Bass/Treble Enable
B[5]	DEQE	Dynamic EQ enable	0	DEQ Disable
			1	DEQ enable
B[4]	NGE	Noise gate enable	0	Noise gate disable
			1	Noise gate enable
B[3]	EQL	EQ Link	0	Each channel uses individual EQ
			1	Channel-2 uses channel-1 EQ
B[2]	PSL	Post-scale link	0	Each channel uses individual post-scale
			1	Use channel-1 post-scale
B[1]	DSPB	EQ bypass	0	EQ enable
			1	EQ bypass
B[0]	HPB	DC blocking HPF bypass	0	HPF dc enable
			1	HPF dc bypass

- Address 0X0D, 0X0E ,0X0F,0X10,0X11,0X12, 0X13,0X14 : Channel configuration registers

  AD85050 can configure each channel to enable or bypass DRC and channel volume and select the limiter set.

Address 0X0D and 0X0E; where x=1 or 2

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:4]		Reserved		
B[3]	CxPCBP	Channel x Power Clipping bypass	0	Channel x PC enable
			1	Channel x PC bypass
B[2]	CxDRCBP	Channel x DRC bypass	0	Channel x DRC enable
			1	Channel x DRC bypass
B[1]		Reserved		
B[0]	CxVBP	Channel x Volume bypass	0	Channel x's master volume operation
			1	Channel x's master volume bypass

Address 0X0F, 0X10, 0X11, and 0X12; where x=3,4,5,6

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:3]		Reserved		
B[2]	CxDRCBP	Channel x DRC bypass	0	Channel x DRC enable
			1	Channel x DRC bypass
B[1]		Reserved		
B[0]	CxVBP	Channel x Volume bypass	0	Channel x volume operation
			1	Channel x volume bypass

Address 0X13, and 0X14; where x=7 or 8

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:3]		Reserved		
B[2]	CxDRCBP	Channel x DRC bypass	0	Channel x DRC enable
			1	Channel x DRC bypass
B[1:0]		Reserved		

- Address 0X15, 0X16, 0X17, 0X18 : DRC limiter attack/release rate

The AD85050 has 4 independent DRC set, each DRC has its own attack/release rate.

Address 0X15, 0X16, 0X17, and 0X18; where x=1, 2, 3, 4

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:5]	Lax[3:0]	DRC attack rate	0000	3 dB/ms
			0001	2.667 dB/ms
			0010	2.182 dB/ms
			0011	1.846 dB/ms
			0100	1.333 dB/ms
			0101	0.889 dB/ms
			0110	0.4528 dB/ms
			0111	0.2264 dB/ms
			1000	0.15 dB/ms
			1001	0.1121 dB/ms
			1010	0.0902 dB/ms
			1011	0.0752 dB/ms
			1100	0.0645 dB/ms
			1101	0.0563 dB/ms
			1110	0.0501 dB/ms
			1111	0.0451 dB/ms
B[3:0]	LRx[3:0]	DRC release rate	0000	0.5106 dB/ms
			0001	0.1371 dB/ms
			0010	0.0743 dB/ms
			0011	0.0499 dB/ms
			0100	0.0360 dB/ms
			0101	0.0299 dB/ms
			0110	0.0264 dB/ms
			0111	0.0208 dB/ms
			1000	0.0198 dB/ms
			1001	0.0172 dB/ms
			1010	0.0147 dB/ms
			1011	0.0137 dB/ms
			1100	0.0134 dB/ms
			1101	0.0117 dB/ms
			1110	0.0112 dB/ms
			1111	0.0104 dB/ms

- Address 0X19 : State control 5

DRC mode: The selection of DRC calculation is peak or RMS.

DRC link: When DRC_LINK=1, left channel and right channel use the same coefficient and threshold.

HP and SPK on: Turn on headphone and speaker at the same time. When HP_SPK_ON=1, SDZ pin is always high, connect the SDZ pin directly to AMP_SDB pin. The AMP output will be turned on. When HP_SPK_ON=0, SDZ pin is controlled by HP_SPK pin.

Dynamic Bass: A processing block that allows for optimizing the bass response of the system by setting
DB_EN = 1:
With DB_CTRL_INV=0, if the energy of lower frequency is bigger than Dynamic bass DRC attack threshold, the missing fundamental function will be enable, while energy of lower frequency is smaller than Dynamic bass DRC release threshold, true bass will be enable.
On the other side, with DB_CTRL_INV=1, if the energy of lower frequency is bigger than Dynamic bass DRC attack threshold, true bass will be enable, while energy of lower frequency is smaller than Dynamic bass DRC release threshold, the missing fundamental will be enable.
Note: it needs to set BTE=1 and MF_EN=1 while enable dynamic bass
DB_EN = 0:
True bass and missing fundamental will be controlled by BTE and MF_EN individually.

Missing fundamental: This method is a well-known psychoacoustic effect invoking a perception of the bass frequencies even though the fundamental of those frequencies has been filtered out. A missing fundamental is used as a function of regenerating a bass that is filtered out by pre-filter.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:6]		Reserved		
B[5]	HP_SPK_ON	HP and SPK turn on simultaneously	0	Disable
			1	Enable
B[4]	DRCM	DRC Mode	0	PEAK mode
			1	RMS mode
B[3]	DRC_LINK	DRC link	0	Disable
			1	Enable
B[2]	DB_CTRL_INV	DB CTRL inversion	0	Normal
			1	Invert
B[1]	DB_EN	Dynamic Bass enable	0	Disable
			1	Enable

B[0]	MF_EN	Missing fundamental enable	0	Disable
			1	Enable

● Address 0X1A : State control 6

Power down register: When PDB_REG=0, power down is happened (SDZ pin is pulled low).

Software reset: When SW_RSTB=1, software reset is happened.

Lower under voltage fade: If LVUV_FADE=1, system will fade out when LVUV occur.

Disable MCLK detect circuit: enable/disable MCLK detect circuit.

PWM modulation: PWM select qua-ternary or ternary.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]		Reserved		
B[6]	PDB_REG	Power down register	0	Power down
			1	Normal operation
B[5]	SW_RSTB	Software reset	0	Reset
			1	Normal operation
B[4]	LVUV_FADE	Low Under Voltage Fade	0	No Fade
			1	Fade
B[3]		Reserved		
B[2]	DIS_MCLK_DET	Disable MCLK detect circuit	0	Enable MCLK detect circuit
			1	Disable MCLK detect circuit
B[1:0]		Reserved		

- Address 0X1B : State control 7

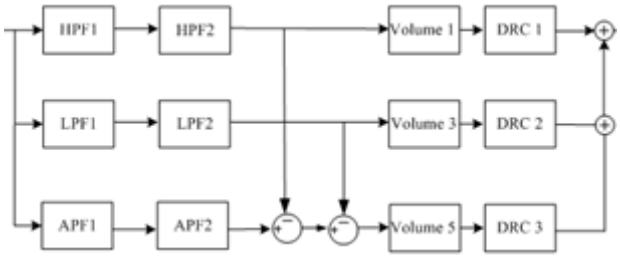
AD85050 can support one band, two band, and three band DRC selection via bit7~bit6.

AD85050 can support x3 oversampling.

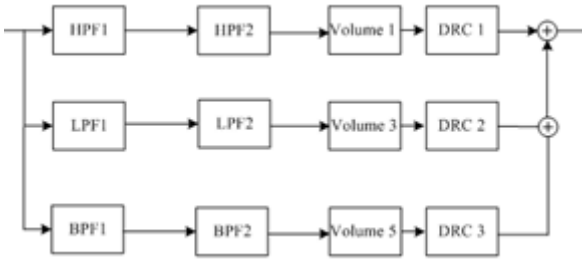
AD85050 can support application of 8KHZ (human speech voice).

AD85050 can support two types in three bands DRC.

Type 1:



Type 2:



BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:6]	DRC_SEL	DRC mode selection	00	1 Band DRC
			01	2 Bands DRC
			1x	3 Bands DRC
B[3]	32X3	X3 oversampling	0	X2 oversampling
			1	X3 oversampling
B[2]	FS8K	FS8K	0	Disable
			1	Enable
B[1]	TriBDRC_TYPE	3 Band DRC type selection	0	Type 1
			1	Type 2
B[0]		Reserved		

- Address 0X1C: State control 8

AD85050 provides invert left channel output by bit 7.

AD85050 provides invert right channel output by bit 6.

AD85050 provides post boost +48dB support via bit 5.

AD85050, user can select fade out or not for noise gate via bit 4.

AD85050 provides DRC boost +36dB support via bit 3.

AD85050 provides 2 kind of fade in/out speed via bit 2. One is 1.25ms from mute to 0dB. The other one is 10ms from mute to 0dB.

AD85050 provides noise gate function if receiving 2048 signal sample points smaller than noise gate attack level. User can change noise gate gain via bit1~ bit0. When noise gate function occurs, input signal will multiply noise gate gain (x1/8, x1/4 x1/2, Mute).

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]		Reserved		
B[6]		Reserved		
B[5]	POST_BOOST	POST boost +48dB	0	0dB
			1	+48dB
B[4]	DIS_NG_FADE	Disable noise gate fade	0	Fade
			1	No fade
B[3]	DRC_BOOST	DRC boost +36dB	0	0dB
			1	+36dB
B[2]	FADE_SPEED	Fade in/out speed selection	0	1.25ms
			1	10ms
B[1:0]	NG_GAIN[1:0]	Noise gate gain	00	x1/8
			01	x1/4
			10	x1/2
			11	Mute

- Address 0X1D ~0X2D : User-defined coefficients registers

An on-chip RAM in AD85050 stores user-defined EQ, mixing, pre-scale, post-scale coefficients…etc. The content of this coefficient RAM is indirectly accessed via coefficient registers, which consist of one base address register (address 0X1D), five sets of registers (address 0X1E to 0X2C) of three consecutive 8-bit entries for each 24-bit coefficient, and one control register (address 0X2D) to control access of the coefficients in the RAM..

Address 0X1D

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]		Reserved		
B[6:0]	CFA[6:0]	Coefficient RAM base address	0000000	

Address 0X1E, A1cf1

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C1B[23:16]	Top 8-bits of coefficients A1		

Address 0X1F, A1cf2

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C1B[15:8]	Middle 8-bits of coefficients A1		

Address 0X20, A1cf3

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C1B[7:0]	Bottom 8-bits of coefficients A1		

Address 0X21, A2cf1

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C2B[23:16]	Top 8-bits of coefficients A2		

Address 0X22, A2cf2

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C2B[15:8]	Middle 8-bits of coefficients A2		

Address 0X23, A2cf3

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C2B[7:0]	Bottom 8-bits of coefficients A2		

Address 0X24, B1cf1

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C3B[23:16]	Top 8-bits of coefficients B1		

Address 0X25, B1cf2

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C3B[15:8]	Middle 8-bits of coefficients B1		

Address 0X26, B1cf3

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C3B[7:0]	Bottom 8-bits of coefficients B1		

Address 0X27, B2cf1

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C4B[23:16]	Top 8-bits of coefficients B2		

Address 0X28, B2cf2

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C4B[15:8]	Middle 8-bits of coefficients B2		

Address 0X29, B2cf3

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C4B[7:0]	Bottom 8-bits of coefficients B2		

Address 0X2A, A0cf1

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C5B[23:16]	Top 8-bits of coefficients A0		

Address 0X2B, A0cf2

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C5B[15:8]	Middle 8-bits of coefficients A0		

Address 0X2C, A0cf3

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C5B[7:0]	Bottom 8-bits of coefficients A0		

Address 0X2D, CfRW

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]		Reserved		
B[6]	RBS	RAM bank selection	0	Select RAM bank 0
			1	Select RAM bank 1
B[5]	R3	Enable of reading three coefficients from RAM	0	Read complete
			1	Read enable
B[4]	W3	Enable of writing three coefficients to RAM	0	Write complete
			1	Write enable
B[3]	RA	Enable of reading a set of coefficients from RAM	0	Read complete
			1	Read enable
B[2]	R1	Enable of reading a single coefficients from RAM	0	Read complete
			1	Read enable
B[1]	WA	Enable of writing a set of coefficients to RAM	0	Write complete
			1	Write enable
B[0]	W1	Enable of writing a single coefficient to RAM	0	Write complete
			1	Write enable

- Address 0X34/0X35 : Volume fine tune

AD85050 supports both master-volume fine tune and channel-volume control fine tune modes. Both volume control settings range from 0dB ~ -0.375dB and 0.125dB per step. Note that the master volume fine tune is added to the individual channel volume fine tune as the total volume fine tune.

Address 0X34

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:6]	MV_FT	Master Volume Fine Tune	00	0dB
			01	-0.125dB
			10	-0.25dB
			11	-0.375dB
B[5:4]	C1V_FT	Channel 1 Volume Fine Tune	00	0dB
			01	-0.125dB
			10	-0.25dB
			11	-0.375dB
B[3:2]	C2V_FT	Channel 2 Volume Fine Tune	00	0dB
			01	-0.125dB
			10	-0.25dB
			11	-0.375dB
B[1:0]	C3V_FT	Channel 3 Volume Fine Tune	00	0dB
			01	-0.125dB
			10	-0.25dB
			11	-0.375dB

Address 0X35

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:6]	C4V_FT	Channel 4 Volume Fine Tune	00	0dB
			01	-0.125dB
			10	-0.25dB
			11	-0.375dB
B[5:4]	C5V_FT	Channel 5 Volume Fine Tune	00	0dB
			01	-0.125dB
			10	-0.25dB
			11	-0.375dB
B[3:2]	C6V_FT	Channel 6 Volume Fine Tune	00	0dB
			01	-0.125dB
			10	-0.25dB
			11	-0.375dB
B[1:0]		Reserved		

- Address 0X36 : DAC gain control

AD85050 supports DAC analog gain control by bit [7:6].

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:6]	DAC_GAIN	DAC gain control	00	1.5dB
			01	1.0dB
			00	-3.5dB
			11	-4dB
B[5:0]	Reserved	Reserved		

- Address 0X42 : level meter clear

AD85050 has 8 set of level meters which hold the maximum absolute value.

Each level meter has its own level meter clear.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	C1_CLR	Clear CH1 level meter	0	No clear
			1	Clear
B[6]	C2_CLR	Clear CH2 level meter	0	No clear
			1	Clear
B[5]	C3_CLR	Clear CH3 level meter	0	No clear
			1	Clear
B[4]	C4_CLR	Clear CH4 level meter	0	No clear
			1	Clear
B[3]	C5_CLR	Clear CH5 level meter	0	No clear
			1	Clear
B[2]	C6_CLR	Clear CH6 level meter	0	No clear
			1	Clear
B[1]	C7_CLR	Clear CH7 level meter	0	No clear
			1	Clear
B[0]	C8_CLR	Clear CH8 level meter	0	No clear
			1	Clear

- Address 0X43 : Power meter clear

AD85050 has 8 set of level meters which continue update RMS value.

Each level meter has its own power meter clear.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	C1_CLR_RMS	Clear CH1 power meter	0	No clear
			1	Clear
B[6]	C2_CLR_RMS	Clear CH2 power meter	0	No clear
			1	Clear
B[5]	C3_CLR_RMS	Clear CH3 power meter	0	No clear
			1	Clear
B[4]	C4_CLR_RMS	Clear CH4 power meter	0	No clear
			1	Clear
B[3]	C5_CLR_RMS	Clear CH5 level meter	0	No clear
			1	Clear
B[2]	C6_CLR_RMS	Clear CH6 level meter	0	No clear
			1	Clear
B[1]	C7_CLR_RMS	Clear CH7 level meter	0	No clear
			1	Clear
B[0]	C8_CLR_RMS	Clear CH8 level meter	0	No clear
			1	Clear

- Address 0X44 : Top 8 bit of C1 level meter

In one band DRC, channel-1 level meter is used for L channel.

In two/three bands DRC, channel-1 level meter is high frequency path of L channel.

The addresses to show channel-1 level meter are 0X44, 0X45, and 0X46.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C1_LEVEL_T	Top 8 bits of channel 1 level meter	0000000	Reset value
			X	Read out

- Address 0X45 : Middle 8 bit of C1 level meter

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C1_LEVEL_M	Middle 8 bits of channel 1 level meter	0000000	Reset value
			X	Read out

- Address 0X46 : Bottom 8 bit of C1 level meter

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C1_LEVEL_B	Bottom 8 bits of channel 1 level meter	0000000	Reset value
			X	Read out

- Address 0X47 : Top 8 bit of C2 level meter

  In one band DRC, channel-2 level meter is used for R channel.

  In two/three bands DRC, channel-2 level meter is high frequency path of R channel.

  The addresses to show channel-2 level meter are 0X47, 0X48, and 0X49.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C2_LEVEL_T	Top 8 bits of channel 2 level meter	0000000	Reset value
			X	Read out

- Address 0X48 : Middle 8 bit of C2 level meter

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C2_LEVEL_M	Middle 8 bits of channel 2 level meter	0000000	Reset value
			X	Read out

- Address 0X49 : Bottom 8 bit of C2 level meter

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C2_LEVEL_B	Bottom 8 bits of channel 2 level meter	0000000	Reset value
			X	Read out

- Address 0X4A : Top 8 bit of C3 level meter

  In one/two bands DRC, channel-3 level meter is no use.

  In three bands DRC, channel-3 level meter is low frequency path of L channel.

  The addresses to show channel-3 level meter are 0X4A, 0X4B, and 0X4C.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C3_LEVEL_T	Top 8 bits of channel 3 level meter	0000000	Reset value
			X	Read out

- Address 0X4B : Middle 8 bit of C3 level meter

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C3_LEVEL_M	Middle 8 bits of channel 3 level meter	0000000	Reset value
			X	Read out

- Address 0X4C : Bottom 8 bit of C3 level meter

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C3_LEVEL_B	Bottom 8 bits of channel 3 level meter	0000000	Reset value
			X	Read out

- Address 0X4D : Top 8 bit of C4 level meter

  In one/two bands DRC, channel-4 level meter is no use.

  In three bands DRC, channel-4 level meter is low frequency path of R channel.

  The addresses to show channel-4 level meter are 0X4D, 0X4E, and 0X4F.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C4_LEVEL_T	Top 8 bits of channel 4 level meter	0000000	Reset value
			X	Read out

- Address 0X4E : Middle 8 bit of C4 level meter

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C4_LEVEL_M	Middle 8 bits of channel 4 level meter	0000000	Reset value
			X	Read out

- Address 0X4F : Bottom 8 bit of C4 level meter

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C4_LEVEL_B	Bottom 8 bits of channel 4 level meter	0000000	Reset value
			X	Read out

- Address 0X50 : Top 8 bit of C5 level meter

  In one band DRC, channel-5 level meter is no use.

  In two/three bands DRC, channel-5 level meter is band pass frequency path of L channel.

  The addresses to show channel-5 level meter are 0X50, 0X51, and 0X52.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C5_LEVEL_T	Top 8 bits of channel 5 level meter	0000000	Reset value
			X	Read out

- Address 0X51 : Middle 8 bit of C5 level meter

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C5_LEVEL_M	Middle 8 bits of channel 5 level meter	0000000	Reset value
			X	Read out

- Address 0X52 : Bottom 8 bit of C5 level meter

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C5_LEVEL_B	Bottom 8 bits of channel 5 level meter	0000000	Reset value
			X	Read out

- Address 0X53 : Top 8 bit of C6 level meter

  In one band DRC, channel-6 level meter is no use.

  In two/three bands DRC, channel-6 level meter is band pass frequency path of R channel.

  The addresses to show channel-6 level meter are 0X53, 0X54, and 0X55.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C6_LEVEL_T	Top 8 bits of channel 6 level meter	0000000	Reset value
			X	Read out

- Address 0X54 : Middle 8 bit of C6 level meter

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C6_LEVEL_M	Middle 8 bits of channel 6 level meter	0000000	Reset value
			X	Read out

- Address 0X55 : Bottom 8 bit of C6 level meter

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C6_LEVEL_B	Bottom 8 bits of channel 6 level meter	0000000	Reset value
			X	Read out

- Address 0X56 : Top 8 bit of C7 level meter

  In one band DRC, channel-7 level meter is no use.

  In two/three bands DRC, channel-7 level meter is summation path of L channel.

  The addresses to show channel-7 level meter are 0X56, 0X57, and 0X58.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C7_LEVEL_T	Top 8 bits of channel 7 level meter	0000000	Reset value
			X	Read out

- Address 0X57 : Middle 8 bit of C7 level meter

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C7_LEVEL_M	Middle 8 bits of channel 7 level meter	0000000	Reset value
			X	Read out

- Address 0X58 : Bottom 8 bit of C7 level meter

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C7_LEVEL_B	Bottom 8 bits of channel 7 level meter	0000000	Reset value
			X	Read out

- Address 0X59 : Top 8 bit of C8 level meter

  In one band DRC, channel-8 level meter is no use.

  In two/three bands DRC, channel-8 level meter is summation path of R channel.

  The addresses to show channel-8 level meter are 0X59, 0X5A, and 0X5B.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C8_LEVEL_T	Top 8 bits of channel 8 level meter	0000000	Reset value
			X	Read out

- Address 0X5A : Middle 8 bit of C8 level meter

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C8_LEVEL_M	Middle 8 bits of channel 8 level meter	0000000	Reset value
			X	Read out

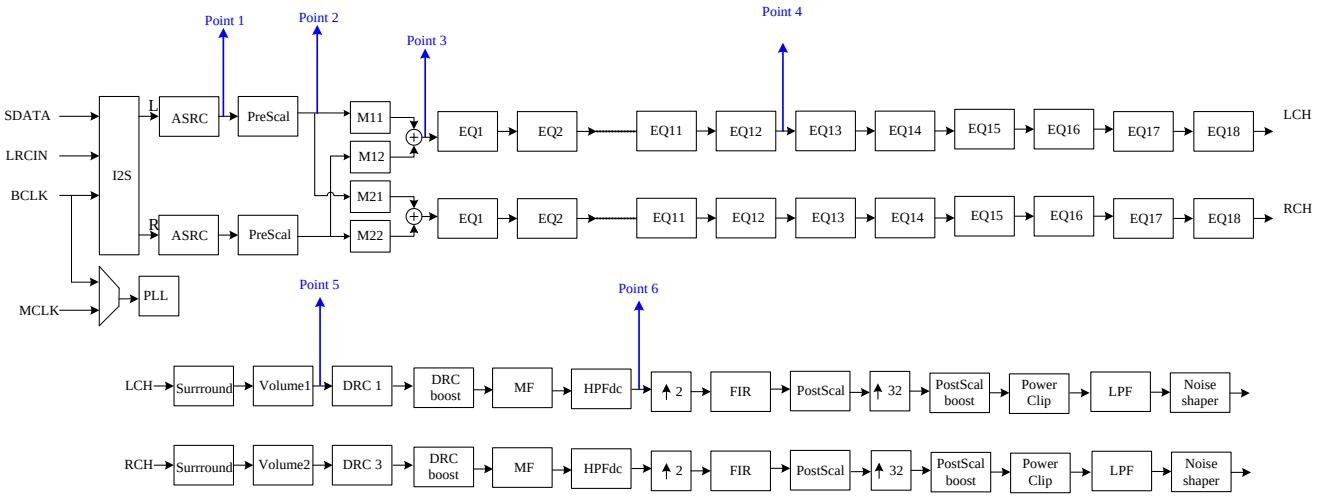
- Address 0X5B : Bottom 8 bit of C8 level meter

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C8_LEVEL_B	Bottom 8 bits of channel 8 level meter	0000000	Reset value
			X	Read out

- Address 0X5C : I²S output selection

AD85050 provide I²S output function via GPIO pins and the output point can be selected via bit 2~bit 0.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:3]		Reserved		
B[2:0]	I²S_DO_SEL	I²S DATA OUTPUT selection	Others	Reserved
			110	Reserved
			101	Point6 : DC blocking HPF output
			100	Point5 : volume output
			011	Point4 : EQ12 output
			010	Point3 : Mixer output
			001	Point2 : pre-scale output
			000	Ponit1 : DSP input



- Address 0x5D:CHS_stat

AD85050 provides check sum status for user via bit 5 / bits 1(read only). And you can enable DRC/BEQ check sum function via bit 4 / bit 0.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	CHK_DRC_E	ERROR link DRC_CHK	0	No link
			1	ERROR link
B[6]	CHK_DRC_AM	Auto Mute DRC_CHK	0	Disable
			1	Enable
B[5]	CHK_DRC_R	Result DRC_CHK	0	No error
			1	Error occurred
B[4]	CHK_DRC_EN	Enable DRC_CHK	0	Disable
			1	Enable
B[3]	CHK_BEQ_E	PROTN link BEQ_CHK	0	No link
			1	ERROR link
B[2]	CHK_BEQ_AM	Auto Mute BEQ_CHK	0	Disable
			1	Enable
B[1]	CHK_BEQ_R	Result BEQ_CHK	0	No error
			1	Error occurred
B[0]	CHK_BEQ_EN	Enable BEQ_CHK	0	Disable
			1	Enable

Set up DRC check value

- Address 0X5E : Top 8 bits of DRC_CHK set value.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	CHS_DRC_V[23:16]	Top 8-bits of DRC_CHK set value	0000000	Initial value
			x	Set value

- Address0x5F : Middle 8 bits of DRC_CHK set value

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	CHS_DRC_V[15:8]	Middle 8-bits of DRC_CHK set value	0000000	Initial value
			x	Set value

- Address0x60 : Bottom 8 bits of DRC_CHK set value

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	CHS_DRC_V[7:0]	Bottom 8-bits of DRC_CHK set value	0000000	Initial value
			x	Set value

Set up BEQ check value

- Address0x61 : Top 8 bits of BEQ_CHK set value

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	CHS_BEQ_V[23:16]	Top 8-bits of BEQ_CHK set value	0000000	Initial value
			x	Set value

- Address0x62 : Middle 8 bits of BEQ_CHK set value

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	CHS_BEQ_V[15:8]	Middle 8-bits of BEQ_CHK set value	0000000	Initial value
			x	Set value

- Address0x63 : Bottom 8 bits of BEQ_CHK set value

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	CHS_BEQ_V[7:0]	Bottom 8-bits of BEQ_CHK set value	0000000	Initial value
			x	Set value

DRC check result

- Address0x64 : Top 8 bits of DRC_CHK result

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	CHS_DRC_R[23:16]	Top 8-bits of DRC_CHK result	x	Result

- Address0x65 : Middle 8 bits of DRC_CHK result

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	CHS_DRC_R15:8]	Middle 8-bits of DRC_CHK result	x	Result

- Address0x66: Bottom 8 bits of DRC_CHK result

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	CHS_DRC_R[7:0]	Bottom 8-bits of DRC_CHK result	x	Result

BEQ check result

- Address0x67 : Top 8 bits of BEQ_CHK result

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	CHS_BEQ_R[23:16]	Top 8-bits of BEQ_CHK result	x	Result

- Address0x68 : Middle 8 bits of BEQ_CHK result

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	CHS_BEQ_R[15:8]	Middle 8-bits of BEQ_CHK result	x	Result

- Address0x69 : Bottom 8 bits of BEQ_CHK result

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	CHS_BEQ_R[7:0]	Bottom 8-bits of BEQ_CHK result	x	Result

- Address 0x81: GPIO0 control

GPIO0 of AD85050 is input or output via bit 4. Select output types of GPIO0 by setting bit 3-0.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:5]	Reserved	Reserved		
B[4]	GPIO0_STATUS	GPIO0_status	0	GPIO0 act as input (initial MCLK/Fs setting)
			1	GPIO0 act as output
B[3:0]	GPIO0_CTRL	GPIO0 Control	0000	Clock error output
			0001	Under voltage output
			0010	OTP output
			0011	PLL clock output
			0100	charge pump clock output
			0101	Serial audio interface data output
			0110	Reserved
			0111	Checksum error output
			…..	Reserved

●Address0x84 : Error register

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	A_LVDET_N	LVDET register	0	LVDET ever occur
			1	Normal
B[6]	A_OTP_N	OTP register	0	OTP ever occur
			1	Normal
B[5:3]	Reserved	Reserved		
B[2]	A_CKEER	CKEER register	0	CKEER ever occur
			1	Normal
B[1:0]	Reserved	Reserved		

● Address0x85 : Error latch register

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	A_LVDET_N_LATCH	LVDET latch register	0	LVDET latched
			1	Normal
B[6]	A_OTP_N_LATCH	OTP latch register	0	OTP latched
			1	Normal
B[5:3]	Reserved	Reserved		
B[2]	A_CKEER_LATCH	CKEER latch register	0	CKEER latched
			1	Normal
B[1:0]	Reserved	Reserved		

● Address0x86 : Error clear register

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	A_LVDET_N	LVDET register	0	No clear
			1	clear
B[6]	A_OTP_N_CLEAR	OTP latch clear register	0	No clear
			1	clear
B[5:3]	Reserved	Reserved		
B[2]	A_CKEER_CLEAR	CLOCK ERROR latch clear register	0	No clear
			1	clear
B[1:0]	Reserved	Reserved		

- Address 0X87 : HP Master volume

AD85050 can tune head phone master volume by setting bit7-0.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	MV_HP[7:0]	HP Master Volume	00000000	+12dB
			00000001	+11.5dB
			00000010	+11dB
			:	:
			00010111	0.5dB
			00011000	0dB
			00011001	-0.5dB
			:	:
			11100110	-103dB
			11100111	-∞dB
			:	:
			11111111	-∞dB

- Address 0X88, 0X89, 0X8A, 0X8B, 0X8C, 0X8D

  AD85050 can tune head phone channel1-6 volume by setting bit7-0.

Address 0X88 ~ 0X8D; where x=1, 2 , 3 , 4, 5 , 6

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	CxV_HP[7:0]	HP Channel Volume	00000000	+12dB
			00000001	+11.5dB
			:	:
			00010100	2dB
			:	:
			00011000	0dB
			00011001	-0.5dB
			:	:
			11100110	-103dB
			11100111	-∞dB
			:	:
			11111111	-∞dB

- Address 0X8E : HP Volume fine tune for master volume and Channel 1~3

  AD85050 can fine tune head phone master volume by setting bit7-6.

  AD85050 can fine tune head phone channel1 volume by setting bit5-4.

  AD85050 can fine tune head phone channel2 volume by setting bit3-2.

  AD85050 can fine tune head phone channel3 volume by setting bit1-0.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:6]	MV_FT_HP	HP Master Volume Fine Tune	00	0dB
			01	-0.125dB
			10	-0.25dB
			11	-0.375dB
B[5:4]	C1V_FT_HP	HP Channel 1 Volume Fine Tune	00	0dB
			01	-0.125dB
			10	-0.25dB
			11	-0.375dB
B[3:2]	C2V_FT_HP	HP Channel 2 Volume Fine Tune	00	0dB
			01	-0.125dB
			10	-0.25dB
			11	-0.375dB
B[1:0]	C3V_FT_HP	HP Channel 3 Volume Fine Tune	00	0dB
			01	-0.125dB
			10	-0.25dB
			11	-0.375dB

- Address 0X8F : HP Volume fine tune for channel 4~6

  AD85050 can fine tune head phone channel4 volume by setting bit7-6.

  AD85050 can fine tune head phone channel5 volume by setting bit5-4.

  AD85050 can fine tune head phone channel6 volume by setting bit3-2.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:6]	C4V_FT_HP	HP Channel 4 Volume Fine Tune	00	0dB
			01	-0.125dB
			10	-0.25dB
			11	-0.375dB
B[5:4]	C5V_FT_HP	HP Channel 5 Volume Fine Tune	00	0dB
			01	-0.125dB
			10	-0.25dB
			11	-0.375dB
B[3:2]	C6V_FT_HP	HP Channel 6 Volume Fine Tune	00	0dB
			01	-0.125dB
			10	-0.25dB
			11	-0.375dB
B[1:0]	Reserved	Reserved		

- Address 0X90 : Lch limiter attack/release time for DB

The AD85050 has left channel DB (dynamic bass) set, this DB has its own attack/release time.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:4]	LA1[3:0]	DB attack time	0000	41.67us
			0001	52.1us
			0010	62.5us
			0011	72.92us
			0100	93.75us
			0101	145.8us
			0110	281.25us
			0111	562.5us
			1000	833.3us
			1001	1.114ms
			1010	1.385ms
			1011	1.667ms
			1100	1.937ms
			1101	2.218ms
			1110	2.5ms
			1111	2.65ms
B[3:0]	LR1[3:0]	DB release time	0000	250us
			0001	916.6us
			0010	1.687ms
			0011	2.51ms
			0100	3.479ms
			0101	4.187ms
			0110	4.739ms
			0111	6.01ms
			1000	6.312ms
			1001	7.27ms
			1010	8.51ms
			1011	9.12ms
			1100	9.33ms
			1101	10.68ms
			1110	11.36ms

- Address 0X91 : Rch limiter attack/release time for DB

The AD85050 has right channel DB (dynamic bass) set, this DB has its own attack/release time.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:4]	RA1[3:0]	DB attack time	0000	41.67us
			0001	52.1us
			0010	62.5us
			0011	72.92us
			0100	93.75us
			0101	145.8us
			0110	281.25us
			0111	562.5us
			1000	833.3us
			1001	1.114ms
			1010	1.385ms
			1011	1.667ms
			1100	1.937ms
			1101	2.218ms
			1110	2.5ms
			1111	2.65ms
B[3:0]	RR1[3:0]	DB release time	0000	250us
			0001	916.6us
			0010	1.687ms
			0011	2.51ms
			0100	3.479ms
			0101	4.187ms
			0110	4.739ms
			0111	6.01ms
			1000	6.312ms
			1001	7.27ms
			1010	8.51ms
			1011	9.12ms
			1100	9.33ms
			1101	10.68ms
			1110	11.36ms

- RAM access

The procedure to read/write coefficient(s) from/to RAM is as followings:

Read a single coefficient from RAM:

1. Write 7-bis of address to I2C address-0X1D
2. Write 1 to R1 bit and write 1/0 to RBS in address-0X2D
3. Read top 8-bits of coefficient in I2C address-0X1E
4. Read middle 8-bits of coefficient in I2C address-0X1F
5. Read bottom 8-bits of coefficient in I2C address-0X20

Read three coefficients from RAM:

1. Write 7-bis of address to I2C address-0X1D
2. Write 1 to R3 bit and write 1/0 to RBS in address-0X2D
3. Read top 8-bits of coefficient in I2C address-0X1E
4. Read middle 8-bits of coefficient in I2C address-0X1F
5. Read bottom 8-bits of coefficient A1 in I2C address-0X20
6. Read top 8-bits of coefficient A2 in I2C address-0X21
7. Read middle 8-bits of coefficient A2 in I2C address-0X22
8. Read bottom 8-bits of coefficient A2 in I2C address-0X23
9. Read top 8-bits of coefficient B1 in I2C address-0X24
10. Read middle 8-bits of coefficient B1 in I2C address-0X25
11. Read bottom 8-bits of coefficient B1 in I2C address-0X26

Read a set of coefficients from RAM:

1. Write 7-bits of address to I2C address-0X1D
2. Write 1 to RA bit and write 1/0 to RBS in address-0X2D
3. Read top 8-bits of coefficient A1 in I2C address-0X1E
4. Read middle 8-bits of coefficient A1in I2C address-0X1F
5. Read bottom 8-bits of coefficient A1 in I2C address-0X20
6. Read top 8-bits of coefficient A2 in I2C address-0X21
7. Read middle 8-bits of coefficient A2 in I2C address-0X22
8. Read bottom 8-bits of coefficient A2 in I2C address-0X23
9. Read top 8-bits of coefficient B1 in I2C address-0X24
10. Read middle 8-bits of coefficient B1 in I2C address-0X25
11. Read bottom 8-bits of coefficient B1 in I2C address-0X26
12. Read top 8-bits of coefficient B2 in I2C address-0X27
13. Read middle 8-bits of coefficient B2 in I2C address-0X28
14. Read bottom 8-bits of coefficient B2 in I2C address-0X29
15. Read top 8-bits of coefficient A0 in I2C address-0X2A
16. Read middle 8-bits of coefficient A0 in I2C address-0X2B

17. Read bottom 8-bits of coefficient A0 in I2C address-0X2C

Write a single coefficient to RAM:

1. Write 7-bis of address to I2C address-0X1D
2. Write top 8-bits of coefficient in I2C address-0X1E
3. Write middle 8-bits of coefficient in I2C address-0X1F
4. Write bottom 8-bits of coefficient in I2C address-0X20
5. Write 1 to W1 bit and write 1/0 to RBS in address-0X2D

Write three coefficients to RAM:

1. Write 7-bis of address to I2C address-0X1D
2. Write top 8-bits of coefficient A1 in I2C address-0X1E
3. Write middle 8-bits of coefficient A1 in I2C address-0X1F
4. Write bottom 8-bits of coefficient A1 in I2C address-0X20
5. Write top 8-bits of coefficient A2 in I2C address-0X21
6. Write middle 8-bits of coefficient A2 in I2C address-0X22
7. Write bottom 8-bits of coefficient A2 in I2C address-0X23
8. Write top 8-bits of coefficient B1 in I2C address-0X24
9. Write middle 8-bits of coefficient B1 in I2C address-0X25
10. Write bottom 8-bits of coefficient B1 in I2C address-0X26

Write 1 to W3 bit and write 1/0 to RBS in address-0X2D

Write a set of coefficients to RAM:

1. Write 7-bits of address to I2C address-0X1D
2. Write top 8-bits of coefficient A1 in I2C address-0X1E
3. Write middle 8-bits of coefficient A1 in I2C address-0X1F
4. Write bottom 8-bits of coefficient A1 in I2C address-0X20
5. Write top 8-bits of coefficient A2 in I2C address-0X21
6. Write middle 8-bits of coefficient A2 in I2C address-0X22
7. Write bottom 8-bits of coefficient A2 in I2C address-0X23
8. Write top 8-bits of coefficient B1 in I2C address-0X24
9. Write middle 8-bits of coefficient B1 in I2C address-0X25
10. Write bottom 8-bits of coefficient B1 in I2C address-0X26
11. Write top 8-bits of coefficient B2 in I2C address-0X27
12. Write middle 8-bits of coefficient B2 in I2C address-0X28
13. Write bottom 8-bits of coefficient B2 in I2C address-0X29
14. Write top 8-bits of coefficient A0 in I2C address-0X2A
15. Write middle 8-bits of coefficient A0 in I2C address-0X2B
16. Write bottom 8-bits of coefficient A0 in I2C address-0X2C
17. Write 1 to WA bit and write 1/0 to RBS in address-0X2D

Note that: the read and write operation on RAM coefficients works only if LRCIN (pin-15) switching on rising edge. And, before each writing operation, it is necessary to read the address-0X2D to confirm whether RAM is writable current in first. If the logic of W1 or W3 or WA is high, the coefficient writing is prohibited.

- User-defined equalizer

The AD85050 provides 30 parametric Equalizer (EQ). Users can program suitable coefficients via I^2C control interface to program the required audio band frequency response for every EQ. The transfer function

$$H(z) = \frac{A_0 + A_1 z^{-1} + A_2 z^{-2}}{1 + B_1 z^{-1} + B_2 z^{-2}}$$

The data format of 2's complement binary code for EQ coefficient is 3.21. i.e., 3-bits for integer (MSB is the sign bit) and 21-bits for mantissa. Each coefficient range is from 0x800000 (-4) to 0x7FFFFF (+3.999999523). These coefficients are stored in User Defined RAM and are referenced in following manner:

$$CHxEQyA0 = A0$$
$$CHxEQyA1 = A1$$
$$CHxEQyA2 = A2$$
$$CHxEQyB1 = -B1$$
$$CHxEQyB2 = -B2$$

Where *x* and *y* represents the number of channel and the band number of EQ biquard.

All user-defined filters are path-through, where all coefficients are defaulted to 0 after being powered up, except the A0 that is set to 0x200000 which represents 1.

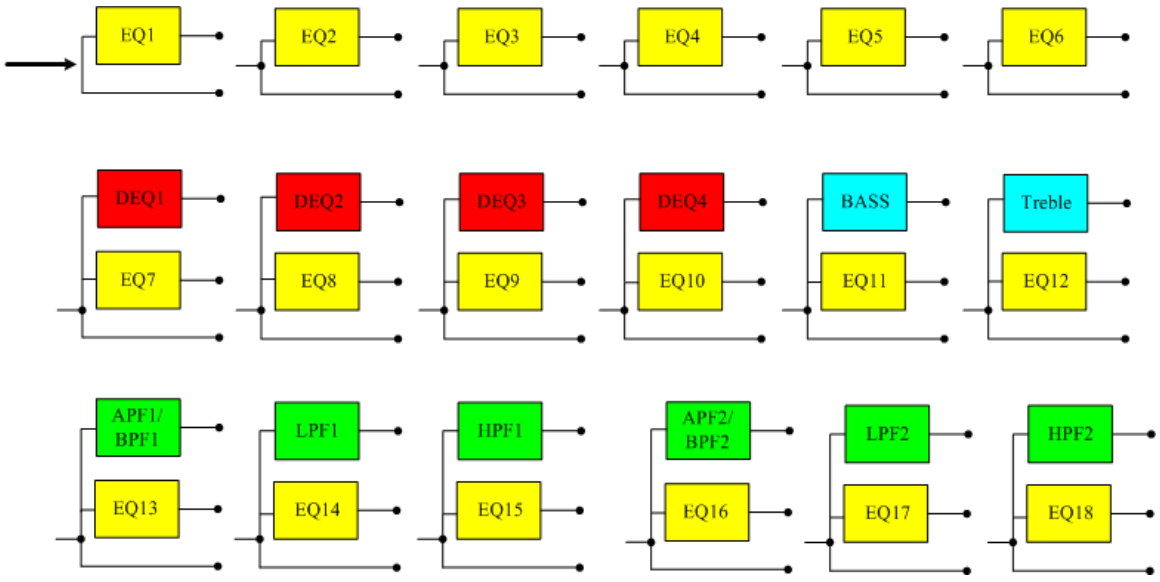
- EQ arrangement

AD85050 provides 18 Eqs per channel.

When, register with address-0X0C, bit-5, DEQE is set to high, the EQ7, EQ8, EQ9, and EQ10 will use another filter coefficient stored in used defined RAM 0X68~0X7B.

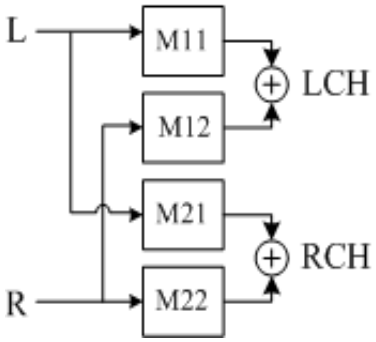
When, register with address-0X0C, bit-6, BTE is set to high, the EQ11 and EQ12 will perform as bass and treble respectively.

When three bands DRC enable, EQ13, EQ14, and EQ15, EQ16, EQ17, EQ18 will perform as APF1/BPF1, LPF1, HPF1, APF2/BPF2, LPF2 and HPF2 respectively.



- Mixer

The AD85050 provides mixers to generate the extra audio source from the input left and right channels. The coefficients of mixers are defined in range from 0x800000 (-1) to 0x7FFFFF (0.9999998808). The function block diagram is as following:



- Pre-scale

For each audio channel, AD85050 can scale input signal level prior to EQ processing which is realized by a 24-bit signed fractional multiplier. The pre-scale factor, ranging from -1 (0x800000) to 0.9999998808 (0x7FFFFF), for this multiplier, can be loaded into RAM. The default values of the pre-scaling factors are set to 0x7FFFFF. Programming of RAM is described in RAM access.

- Post-scale

The AD85050 provides an additional multiplication after equalizing and before interpolation stage, which is realized by a 24-bit signed fractional multiplier. The post-scaling factor, ranging from -1 (0x800000) to 0.9999998808 (0x7FFFFF), for this multiplier, can be loaded into RAM. The default values of the post-scaling factors are set to 0x7FFFFF. All channels can use the channel-1 post-scale factor by setting the post-scale link. Programming of RAM is described in RAM access.

- Power Clipping

The AD85050 provides power clipping function to avoid excessive signal that may destroy loud speaker. 3. The power clipping level is defined by 24-bit representation and is stored in RAM address 0X55 of RAM bank 0. The following table shows the power clipping level's numerical representation.

Sample calculation for power clipping

Max amplitude	dB	Linear	Decimal	Hex (3.21 format)
PVCC	0	1	2097152	200000
PVCC*0.707	-3	0.707	1482686	169FBE
PVCC*0.5	-6	0.5	1048576	100000
PVCC*L	x	$L=10^{(x/20)}$	D=2097152xL	H=dec2hex(D)

- Attack threshold

The AD85050 provides DRC function. When the input RMS exceeds the programmable attack threshold value, the output power will be limited by this threshold power level via gradual gain reduction. Four sets of DRC are provided. DRC1 is used for high frequency path in three bands DRC and used for L/R channel in one band DRC. DRC2 is used for low frequency path in three bands DRC. DRC3 is used for band pass frequency path in three bands DRC. DRC4 is used for the post DRC.

Attack threshold is defined by 24-bit presentation and is stored in RAM address 0X56, 0X58, 0X5A, 0X5C of RAM bank 0.

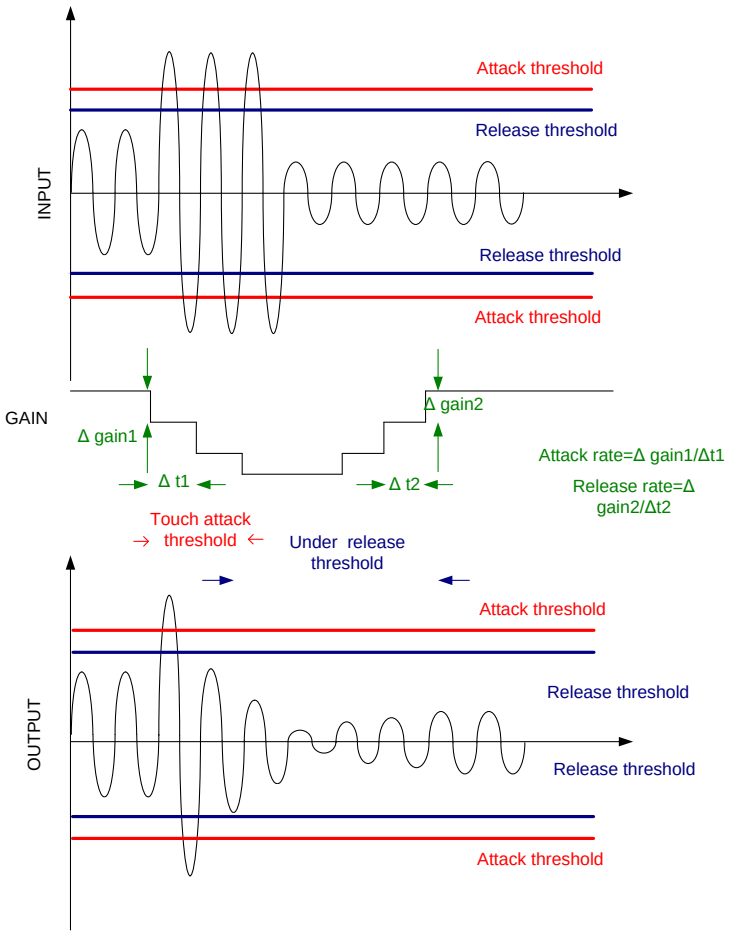
- Release threshold

After AD85050 has reached the attack threshold, its output power will be limited to that level. The output power level will be gradually adjusted to the programmable release threshold level. Release threshold is defined by 24-bit representation and is stored in RAM address 0X57, 0X59, 0X5B, and 0X5D of RAM bank 0. The following table shows the attack and release threshold's numerical representation.

Sample calculation for attack and release threshold

Power	dB	Linear	Decimal	Hex (3.21 format)
(PVCC^2)/R	0	1	2097152	200000
(PVCC^2)/2R	-3	0.5	1048576	100000
(PVCC^2)/4R	-6	0.25	524288	80000
((PVCC^2)/R)*L	x	$L=10^{(x/10)}$	D=2097152xL	H=dec2hex(D)

To best illustrate the power limit function, please refer to the following figure.



- Noise Gate Attack Level

  When both left and right signals have 2048 consecutive sample points less than the programmable noise gate attack level, the audio signal will multiply noise gate gain, which can be set at x1/8, x1/4, x1/2, or zero if the noise gate function is enabled. Noise gate attack level is defined by 24-bit representation and is stored in RAM address 0X5E of RAM bank 0.

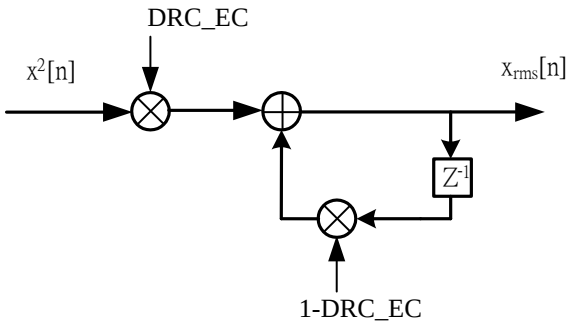
- Noise Gate Release Level

  After entering the noise gating status, the noise gain will be removed whenever AD85050 receives any input signal that is more than the noise gate release level. Noise gate release level is defined by 24-bit representation and is stored in RAM address 0X5F of RAM bank 0. The following table shows the noise gate attack and release threshold level's numerical representation.

Sample calculation for noise gate attack and release level

Input amplitude (dB)	Linear	Decimal	Hex (1.23 format)
0	1	8388607	7FFFFF
-100	10^{-5}	83	53
-110	$10^{-5.5}$	26	1A
x	$L=10^{(x/20)}$	D=8388607xL	H=dec2hex(D)

- DRC Energy Coefficient



The above figure illustrates the digital processing of calculating RMS signal power. In this processing, a DRC energy coefficient is required, which can be programmed for different frequency range. Four sets of energy coefficients are provided and used for respective DRC. Energy coefficient is defined by 24-bit representation and is stored in RAM address 0X60, 0X61, 0X62, and 0X63 of RAM bank 0. The following table shows the DRC energy coefficient numerical representation.

Sample calculation for DRC energy coefficient

DRC energy coefficient	dB	Linear	Decimal	Hex (1.23 format)
1	0	1	8388607	7FFFFF
1/256	-48.2	1/256	32768	8000
1/1024	-60.2	1/1024	8192	2000
L	x	$L=10^{(x/20)}$	D=8388607xL	H=dec2hex(D)

The user defined RAM

The contents of user defined RAM is represented in following table.

Ram Bank selection = 0

Address	NAME	Coefficient	Default
0x00	1st SET Channel-1 EQ1	CH1EQ1A1	0x000000
0x01		CH1EQ1A2	0x000000
0x02		CH1EQ1B1	0x000000
0x03		CH1EQ1B2	0x000000
0x04		CH1EQ1A0	0x200000
0x05	1st SET Channel-1 EQ2	CH1EQ2A1	0x000000
0x06		CH1EQ2A2	0x000000
0x07		CH1EQ2B1	0x000000
0x08		CH1EQ2B2	0x000000
0x09		CH1EQ2A0	0x200000
0x0A	1st SET Channel-1 EQ3	CH1EQ3A1	0x000000
0x0B		CH1EQ3A2	0x000000
0x0C		CH1EQ3B1	0x000000
0x0D		CH1EQ3B2	0x000000
0x0E		CH1EQ3A0	0x200000
0x0F	1st SET Channel-1 EQ4	CH1EQ4A1	0x000000
0x10		CH1EQ4A2	0x000000
0x11		CH1EQ4B1	0x000000
0x12		CH1EQ4B2	0x000000
0x13		CH1EQ4A0	0x200000
0x14	1st SET Channel-1 EQ5	CH1EQ5A1	0x000000
0x15		CH1EQ5A2	0x000000
0x16		CH1EQ5B1	0x000000
0x17		CH1EQ5B2	0x000000
0x18		CH1EQ5A0	0x200000

0x19	1st SET Channel-1 EQ6	CH1EQ6A1	0x000000
0x1A		CH1EQ6A2	0x000000
0x1B		CH1EQ6B1	0x000000
0x1C		CH1EQ6B2	0x000000
0x1D		CH1EQ6A0	0x200000
0x1E	1st SET Channel-1 EQ7	CH1EQ7A1	0x000000
0x1F		CH1EQ7A2	0x000000
0x20		CH1EQ7B1	0x000000
0x21		CH1EQ7B2	0x000000
0x22		CH1EQ7A0	0x200000
0x23	1st SET Channel-1 EQ8	CH1EQ8A1	0x000000
0x24		CH1EQ8A2	0x000000
0x25		CH1EQ8B1	0x000000
0x26		CH1EQ8B2	0x000000
0x27		CH1EQ8A0	0x200000
0x28	1st SET Channel-1 EQ9	CH1EQ9A1	0x000000
0x29		CH1EQ9A2	0x000000
0x2A		CH1EQ9B1	0x000000
0x2B		CH1EQ9B2	0x000000
0x2C		CH1EQ9A0	0x200000
0x2D	1st SET Channel-1 EQ10	CH1EQ10A1	0x000000
0x2E		CH1EQ10A2	0x000000
0x2F		CH1EQ10B1	0x000000
0x30		CH1EQ10B2	0x000000
0x31		CH1EQ10A0	0x200000
0x32	1st SET Channel-1 EQ11	CH1EQ11A1	0x000000
0x33		CH1EQ11A2	0x000000
0x34		CH1EQ11B1	0x000000
0x35		CH1EQ11B2	0x000000
0x36		CH1EQ11A0	0x200000
0x37	1st SET Channel-1 EQ12	CH1EQ12A1	0x000000
0x38		CH1EQ12A2	0x000000
0x39		CH1EQ12B1	0x000000
0x3A		CH1EQ12B2	0x000000
0x3B		CH1EQ12A0	0x200000
0x3C	1st SET Channel-1 EQ13	CH1EQ13A1	0x000000
0x3D		CH1EQ13A2	0x000000

0x3E		CH1EQ13B1	0x000000
0x3F		CH1EQ13B2	0x000000
0x40		CH1EQ13A0	0x200000
0x41	1st SET Channel-1 EQ14	CH1EQ14A1	0x000000
0x42		CH1EQ14A2	0x000000
0x43		CH1EQ14B1	0x000000
0x44		CH1EQ14B2	0x000000
0x45		CH1EQ14A0	0x200000
0x46	1st SET Channel-1 EQ15	CH1EQ15A1	0x000000
0x47		CH1EQ15A2	0x000000
0x48		CH1EQ15B1	0x000000
0x49		CH1EQ15B2	0x000000
0x4A		CH1EQ15A0	0x200000
0x4B	Channel-1 Mixer1	M11	0x7FFFFF
0x4C	Channel-1 Mixer2	M12	0x000000
0x4D	Channel-1 Prescale	C1PRS	0x080000
0x4E	Channel-1 Postscale	C1POS	0x200000
0X4F	A0 of L channel SRS HPF	LSRSH_A0	C7B691
0X50	A1 of L channel SRS HPF	LSRSH_A1	38496E
0X51	B1 of L channel SRS HPF	LSRSH_B1	C46f8
0X52	A0 of L channel SRS LPF	LSRSL_A0	E81B9
0X53	A1 of L channel SRS LPF	LSRSL_A1	F22C12
0X54	B1 of L channel SRS LPF	LSRSL_ B1	FCABB
0x55	CH1.2 Power Clipping	PC1	0x200000
0X56	CH1 DRC1 Attack threshold	DRC1_ATH	0x200000
0X57	CH1 DRC1 Release threshold	DRC1_RTH	0x80000
0X58	CH3 DRC2 Attack threshold	DRC2_ATH	0x200000
0X59	CH3 DRC2 Release threshold	DRC2_RTH	0x80000
0x5A	CH5 DRC3 Attack threshold	DRC3_ATH	0x200000
0x5B	CH5 DRC3 Release threshold	DRC3_RTH	0x80000

0x5C	CH7 DRC4 Attack threshold	DRC4_ATH	0x200000
0x5D	CH7 DRC4 Release threshold	DRC4_RTH	0x80000
0x5E	Noise Gate Attack Level	NGAL	0x00001A
0x5F	Noise Gate Release Level	NGRL	0x000053
0x60	DRC1 Energy Coefficient	DRC1_EC	0x8000
0X61	DRC2 Energy Coefficient	DRC2_EC	0x2000
0x62	DRC3 Energy Coefficient	DRC3_EC	0x8000
0X63	DRC4 Energy Coefficient	DRC4_EC	0x2000
0X64	DRC1 Power Meter	C1_RMS	
0X65	DRC3 Power Meter	C3_RMS	
0X66	DRC5 Power Meter	C5_RMS	
0X67	DRC7 Power Meter	C7_RMS	
0x68	2^{nd} SET Channel-1 EQ1	CH1DEQ1A1	0x000000
0x69		CH1DEQ1A2	0x000000
0x6A		CH1DEQ1B1	0x000000
0x6B		CH1DEQ1B2	0x000000
0x6C		CH1DEQ1A0	0x200000
0x6D	2^{nd} SET Channel-1 EQ2	CH1DEQ2A1	0x000000
0x6E		CH1DEQ2A2	0x000000
0x6F		CH1DEQ2B1	0x000000
0x70		CH1DEQ2B2	0x000000
0x71		CH1DEQ2A0	0x200000
0x72	2^{nd} SET Channel-1 EQ3	CH1DEQ3A1	0x000000
0x73		CH1DEQ3A2	0x000000
0x74		CH1DEQ3B1	0x000000
0x75		CH1DEQ3B2	0x000000
0x76		CH1DEQ3A0	0x200000
0x77	2^{nd} SET Channel-1 EQ4	CH1DEQ4A1	0x000000
0x78		CH1DEQ4A2	0x000000
0x79		CH1DEQ4B1	0x000000
0x7A		CH1DEQ4B2	0x000000
0x7B		CH1DEQ4A0	0x200000
0X7C~0X7F	Reserved		
0x80	MF LPF1 Channel-1	CH1MFLPF1A1	0x0000D3
0x81		CH1MFLPF1A2	0x000069

0x82		CH1MFLPF1B1	0x3F594D
0x83		CH1MFLPF1B2	0xE0A50D
0x84		CH1MFLPF1A0	0x000069
0x85	MF LPF2 Channel-1	CH1MFLPF2A1	0x0000D3
0x86		CH1MFLPF2A2	0x000069
0x87		CH1MFLPF2B1	0x3F594D
0x88		CH1MFLPF2B2	0xE0A50D
0x89		CH1MFLPF2A	0x000069
0x8A	MF BPF1 Channel-1	CH1MFBPF1A1	0x000000
0x8B		CH1MFBPF1A2	0xFFC63B
0x8C		CH1MFBPF1B1	0x3F594D
0x8D		CH1MFBPF1B2	0xE0A50D
0x8E		CH1MFBPF1A0	0x0039C5
0x8F	MF BPF2 Channel-1	CH1MFBPF2A1	0x000000
0x90		CH1MFBPF2A2	0xFFC63B
0x91		CH1MFBPF2B1	0x3F594D
0x92		CH1MFBPF2B2	0xE0A50D
0x93		CH1MFBPF2A0	0x0039C5
0x94	MF positive CLIP Channel-1	CH1MFPCLP	0x080000
0x95	MF G1 Channel-1	CH1MFG1	0x019AFD
0x96	MF G2 Channel-1	CH1MFG2	0x080000
0x97	MF G3 Channel-1	CH1MFG3	0x0B4CE0
0X98	MF negative CLIP Channel-1	CH1MFNCLP	0x080000
0X99	MF G4 Channel-1	CH1MFG4	0X080000
0X9A~0X9F	Reserved		
0xA0	1st SET Channel-1 EQ16	CH1EQ16A1	0x000000
0XA1		CH1EQ16A2	0x000000
0xA2		CH1EQ16B1	0x000000
0XA3		CH1EQ16B2	0x000000
0XA4		CH1EQ16A0	0x200000
0XA5	1st SET	CH1EQ17A1	0x000000

0XA6	Channel-1 EQ17	CH1EQ17A2	0x000000
0XA7		CH1EQ17B1	0x000000
0xA8		CH1EQ17B2	0x000000
0xA9		CH1EQ17A0	0x200000
0xAA	1st SET Channel-1 EQ18	CH1EQ18A1	0x000000
0xAB		CH1EQ18A2	0x000000
0xAC		CH1EQ18B1	0x000000
0xAD		CH1EQ18B2	0x000000
0xAE		CH1EQ18A0	0x200000
0xAF	Dynamic bass DRC attack threshold Channel-1	CH1SMBDRCATH	0x200000
0xB0	Dynamic bass DRC release threshold Channel-1	CH1SMBDRCRTH	0x080000
0xB1	Boost chip control attack threshold1	BSTCHIP_ATH1	0x020000
0xB2	Boost chip control attack threshold2	BSTCHIP_ATH2	0x008000
0xB3	Boost chip control attack threshold3	BSTCHIP_ATH3	0x002000

Ram Bank selection = 1

Address	NAME	Coefficient	Default
0x00	1st SET Channel-2 EQ1	CH2EQ1A1	0x000000
0x01		CH2EQ1A2	0x000000
0x02		CH2EQ1B1	0x000000
0x03		CH2EQ1B2	0x000000
0x04		CH2EQ1A0	0x200000
0x05	1st SET Channel-2 EQ2	CH2EQ2A1	0x000000
0x06		CH2EQ2A2	0x000000
0x07		CH2EQ2B1	0x000000
0x08		CH2EQ2B2	0x000000
0x09		CH2EQ2A0	0x200000
0x0A	1st SET Channel-2 EQ3	CH2EQ3A1	0x000000
0x0B		CH2EQ3A2	0x000000
0x0C		CH2EQ3B1	0x000000
0x0D		CH2EQ3B2	0x000000
0x0E		CH2EQ3A0	0x200000
0x0F	1st SET Channel-2 EQ4	CH2EQ4A1	0x000000
0x10		CH2EQ4A2	0x000000
0x11		CH2EQ4B1	0x000000
0x12		CH2EQ4B2	0x000000
0x13		CH2EQ4A0	0x200000
0x14	1st SET Channel-2 EQ5	CH2EQ5A1	0x000000
0x15		CH2EQ5A2	0x000000
0x16		CH2EQ5B1	0x000000
0x17		CH2EQ5B2	0x000000
0x18		CH2EQ5A0	0x200000
0x19	1st SET Channel-2 EQ6	CH2EQ6A1	0x000000
0x1A		CH2EQ6A2	0x000000
0x1B		CH2EQ6B1	0x000000
0x1C		CH2EQ6B2	0x000000
0x1D		CH2EQ6A0	0x200000
0x1E	1st SET Channel-2 EQ7	CH2EQ7A1	0x000000
0x1F		CH2EQ7A2	0x000000
0x20		CH2EQ7B1	0x000000
0x21		CH2EQ7B2	0x000000
0x22		CH2EQ7A0	0x200000

0x23	1st SET Channel-2 EQ8	CH2EQ8A1	0x000000
0x24		CH2EQ8A2	0x000000
0x25		CH2EQ8B1	0x000000
0x26		CH2EQ8B2	0x000000
0x27		CH2EQ8A0	0x200000
0x28	1st SET Channel-2 EQ9	CH2EQ9A1	0x000000
0x29		CH2EQ9A2	0x000000
0x2A		CH2EQ9B1	0x000000
0x2B		CH2EQ9B2	0x000000
0x2C		CH2EQ9A0	0x200000
0x2D	1st SET Channel-2 EQ10	CH2EQ10A1	0x000000
0x2E		CH2EQ10A2	0x000000
0x2F		CH2EQ10B1	0x000000
0x30		CH2EQ10B2	0x000000
0x31		CH2EQ10A0	0x200000
0x32	1st SET Channel-2 EQ11	CH2EQ11A1	0x000000
0x33		CH2EQ11A2	0x000000
0x34		CH2EQ11B1	0x000000
0x35		CH2EQ11B2	0x000000
0x36		CH2EQ11A0	0x200000
0x37	1st SET Channel-2 EQ12	CH2EQ12A1	0x000000
0x38		CH2EQ12A2	0x000000
0x39		CH2EQ12B1	0x000000
0x3A		CH2EQ12B2	0x000000
0x3B		CH2EQ12A0	0x200000
0x3C	1st SET Channel-2 EQ13	CH2EQ13A1	0x000000
0x3D		CH2EQ13A2	0x000000
0x3E		CH2EQ13B1	0x000000
0x3F		CH2EQ13B2	0x000000
0x40		CH2EQ13A0	0x200000
0x41	1st SET Channel-2 EQ14	CH2EQ14A1	0x000000
0x42		CH2EQ14A2	0x000000
0x43		CH2EQ14B1	0x000000
0x44		CH2EQ14B2	0x000000
0x45		CH2EQ14A0	0x200000
0x46	1st SET Channel-2 EQ15	CH2EQ15A1	0x000000
0x47		CH2EQ15A2	0x000000

0x48		CH2EQ15B1	0x000000
0x49		CH2EQ15B2	0x000000
0x4A		CH2EQ15A0	0x200000
0x4b	Channel-2 Mixer1	M21	0x000000
0x4c	Channel-2 Mixer2	M22	0x7FFFFF
0x4D	Channel-2 Prescale	C2PRS	0x080000
0x4E	Channel-2 Postscale	C2POS	0x200000
0X4F	A0 of R channel SRS HPF	RSRSH_A0	C7B691
0X50	A1 of R channel SRS HPF	RSRSH_A1	38496E
0X51	B1 of R channel SRS HPF	RSRSH_B1	C46f8
0X52	A0 of R channel SRS LPF	RSRSL_A0	E81B9
0X53	A1 of R channel SRS LPF	RSRSL_A1	F22C12
0X54	B1 of R channel SRS LPF	RSRSL_ B1	FCABB
0x55	Reserved		
0X56	Reserved		
0X57	Reserved		
0X58	Reserved		
0X59	Reserved		
0x5A	Reserved		
0x5B	Reserved		
0x5C	Reserved		
0x5D	Reserved		
0x5E	Reserved		
0x5F	Reserved		
0x60	Reserved		
0X61	Reserved		
0x62	Reserved		
0X63	Reserved		
0X64	DRC2 Power Meter	C2_RMS	
0X65	DRC4 Power Meter	C4_RMS	
0X66	DRC6 Power Meter	C6_RMS	
0X67	DRC8 Power Meter	C8_RMS	
0x68	2^{nd} SET Channel-2 EQ1	CH2EQ1A1	0x000000
0x69		CH2EQ1A2	0x000000
0x6A		CH2EQ1B1	0x000000
0x6B		CH2EQ1B2	0x000000
0x6C		CH2EQ1A0	0x200000

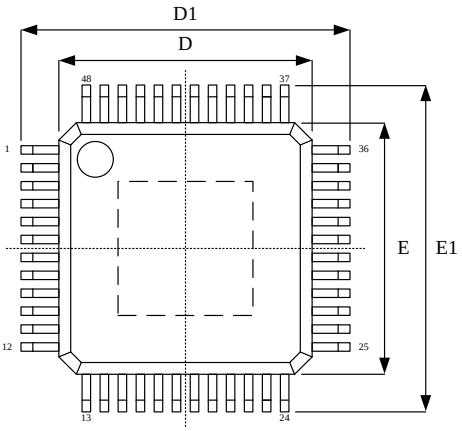
0x6D	2nd SET Channel-2 EQ2	CH2EQ2A1	0x000000
0x6E		CH2EQ2A2	0x000000
0x6F		CH2EQ2B1	0x000000
0x70		CH2EQ2B2	0x000000
0x71		CH2EQ2A0	0x200000
0x72	2nd SET Channel-2 EQ3	CH2EQ3A1	0x000000
0x73		CH2EQ3A2	0x000000
0x74		CH2EQ3B1	0x000000
0x75		CH2EQ3B2	0x000000
0x76		CH2EQ3A0	0x200000
0x77	2nd SET Channel-2 EQ4	CH2EQ4A1	0x000000
0x78		CH2EQ4A2	0x000000
0x79		CH2EQ4B1	0x000000
0x7A		CH2EQ4B2	0x000000
0x7B		CH2EQ4A0	0x200000
0x80	MF LPF1 Channel-2	CH2MFLPF1A1	0x0000D3
0x81		CH2MFLPF1A2	0x000069
0x82		CH2MFLPF1B1	0x3F594D
0x83		CH2MFLPF1B2	0xE0A50D
0x84		CH2MFLPF1A0	0x000069
0x85	MF LPF2 Channel-2	CH2MFLPF2A1	0x0000D3
0x86		CH2MFLPF2A2	0x000069
0x87		CH2MFLPF2B1	0x3F594D
0x88		CH2MFLPF2B2	0xE0A50D
0x89		CH2MFLPF2A0	0x000069
0x8A	MF BPF1 Channel-2	CH2MFBPF1A1	0x000000
0x8B		CH2MFBPF1A2	0xFFC63B
0x8C		CH2MFBPF1B1	0x3F594D
0x8D		CH2MFBPF1B2	0xE0A50D
0x8E		CH2MFBPF1A0	0x0039C5
0x8F	MF BPF2 Channel-2	CH2MFBPF2A1	0x000000
0x90		CH2MFBPF2A2	0xFFC63B
0x91		CH2MFBPF2B1	0x3F594D
0x92		CH2MFBPF2B2	0xE0A50D
0x93		CH2MFBPF2A0	0x0039C5
0x94	MF CLIP Channel-2	CH2MFCLP	0x080000

0x95	MF G1 Channel-2	CH2MFG1	0x019AFD
0x96	MF G2 Channel-2	CH2MFG2	0x080000
0x97	MF G3 Channel-2	CH2MFG3	0x0B4CE0
0X98	MF negative CLIP Channel-1	CH1MFNCLP	0x080000
0X99	MF G4 Channel-1	CH1MFG4	0X080000
0X9A~0X9F	Reserved		
0xA0	1st SET Channel-2 EQ16	CH2EQ16A1	0x000000
0XA1		CH2EQ16A2	0x000000
0xA2		CH2EQ16B1	0x000000
0XA3		CH2EQ16B2	0x000000
0XA4		CH2EQ16A0	0x200000
0XA5	1st SET Channel-2 EQ17	CH2EQ16A1	0x000000
0XA6		CH2EQ17A2	0x000000
0XA7		CH2EQ17B1	0x000000
0xA8		CH2EQ17B2	0x000000
0xA9		CH2EQ17A0	0x200000
0xAA	1st SET Channel-2 EQ18	CH2EQ17A1	0x000000
0xAB		CH2EQ18A2	0x000000
0xAC		CH2EQ18B1	0x000000
0xAD		CH2EQ18B2	0x000000
0xAE		CH2EQ18A0	0x200000
0xAF	Dynamic bass DRC attack threshold Channel-2	CH2SMBDRCATH	0x200000
0xB0	Dynamic bass DRC release threshold Channel-2	CH2SMBDRCRTH	0x080000
0xB1	Boost chip control release threshold1	BSTCHIP_RTH1	0x010000
0xB2	Boost chip control release threshold2	BSTCHIP_RTH2	0x004000

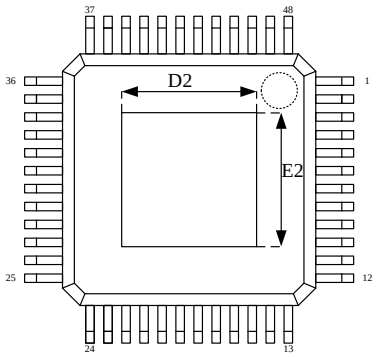
0xB3	Boost chip control release threshold3	BSTCHIP_RTH3	0x001000

Package Dimensions

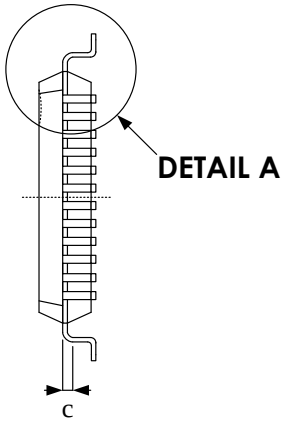
E-LQFP-48L (7mm x 7mm)

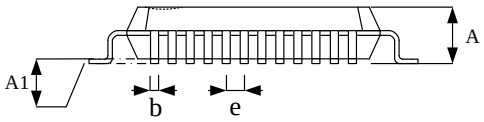


TOP VIEW

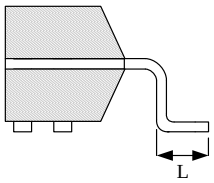


BOTTOM VIEW





SIDE VIEW



DETAIL A

Symbol	Dimension in mm	
	Min	Max
A	--	1.60
A1	0.05	0.15
b	0.17	0.27
c	0.09	0.20
D	6.90	7.10
D1	8.90	9.10
E	6.90	7.10
E1	8.90	9.10
e	0.50 BSC	
L	0.45	0.75

Exposed pad

	Dimension in mm	
	Min	Max
D2	4.31	5.21
E2	4.31	5.21

Revision History

Revision	Date	Description
0.1	2019.03.29	Initial draft version.
0.2	2019.05.13	Add DAC performance
0.3	2019.07.09	Update address 0X01 : state control 2
1.0	2019.08.01	Remove “Preliminary” and revise to 1.0
1.1	2019.09.02	1. Modify recommended Operating Conditions 2. Modify general Electrical Characteristics 3. Modify register table 4. Modify HP Master volume 5. Modify Write a single coefficient to RAM
1.2	2019.11.07	Modify Recommended Operating Conditions. Modify General Electrical Characteristics. Modify Function block. Modify Application Circuit Example for Stereo. Modify Application Circuit Example for Mono. Modify Power on sequence for Fs=48KHz & 96KHz. Modify PBTL (Mono) function. Add address 0x84~0x86 register table.
1.3	2019.12.02	Modify Application Circuit Example for Mono.
1.4	2020.01.06	1.Modify application Circuit Example for stereo mono. 2.Add System Clock Timing. 3.Modify under voltage detection.
1.5	2020.03.03	Modify Pin Assignment description.
1.6	2021.09.13	Modify address 0x1C data.
1.7	2022.08.30	Remove "Support initial EEPROM setting".

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