2x37W Stereo / 1x74W Mono Digital Audio Amplifier With 46 bands EQ and DRC Functions

Features

- 16/18/20/24-bits input with I^2S, Left-alignment, Right-alignment and TDM data format
- PSNR & DR(A-weighting)
  Loudspeaker: 108dB (PSNR), 112dB (DR)@24V
- Multiple sampling frequencies (Fs)
  8kHz, 16kHz, 32kHz/44.1kHz/48kHz and 88.2kHz/96kHz
- System clock = 32x, 48x, 64x, 96x, 128x, 192x, 256x,384x, and 512xFs
- Supply voltage
  1.65~3.6V for DVDD
  4.5~26V for PVDD
- Supports 2.0CH/Mono configuration
- Loudspeaker output power@12V for stereo
  8W x 2CH into 8Ω @ 1% THD+N
  15W x 2CH into 4Ω @ 1% THD+N
- Loudspeaker output power@24V for stereo
  30W x 2CH into 8Ω @ 1% THD+N
  32W x 2CH into 8Ω @ 2% THD+N at 24V
  37W x 2CH into 8Ω @ 10% THD+N at 24V
- Sound processing including：
  46 bands parametric speaker EQ
  Volume control (+24dB~-103dB, 0.125dB/step)
  Dynamic range control
  Three Band plus post Dynamic range control
  Auto Gain Limiter
  Power Clipping
  Programmed 3D surround sound
  Noise gate with hysteresis window
  DC-blocking high-pass filter
  Pre-scale/post-scale
  Post-Boost (+48dB)
  I2S output with user programmed gain (+24dB~mute)
  Compensate filter
  DPEQ
  DTC
  Auto clock detection
- Anti-pop design
- I^2S output with selectable Audio DSP point
- Short circuit and over-temperature protection
- Supports I^2C control without clock
- I^2C control interface with selectable device address
- Internal PLL
- LV Under-voltage shutdown and HV Under-voltage detection
- Over voltage protection
- Power saving mode

Applications

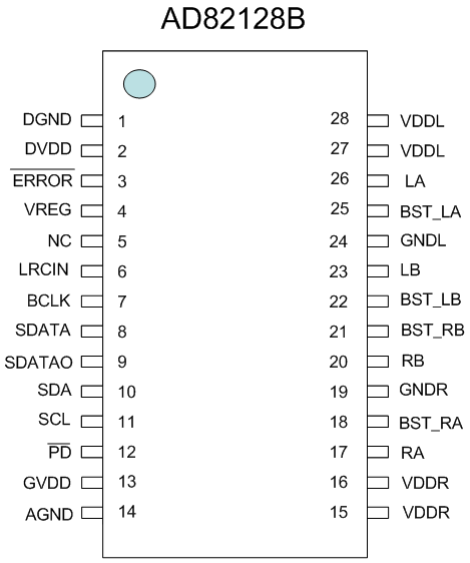
- TV audio
- Boom-box, CD and DVD receiver, docking system
- Powered speaker
- Wireless audio

Description

AD82128B is a digital audio amplifier capable of driving 32W (37W peak power) each to a pair of 8Ω load speaker (BTL) or 64W (74W peak power) to a 4Ω load speaker (PBTL) operating at 24V supply, that's no external heat-sink or fan requirement during music playing.

AD82128B provides advanced audio processing functions, such as volume control, 46 EQ bands, audio mixing, 3D surround sound and Dynamic Range Control (DRC). These are fully programmable via a simple I^2C control interface. Robust protection circuits are provided to protect AD82128B from damage due to accidental erroneous operating condition. The full digital circuit design of AD82128B is more tolerant to noise and PVT (Process, Voltage, and Temperature) variation than the analog class-AB or class-D audio amplifier counterpart implemented by analog circuit design. AD82128B is pop free during instantaneous power on/off or mute/shut down switching because of its robust built-in anti-pop circuit.

Pin Assignment



E-TSSOP-28L

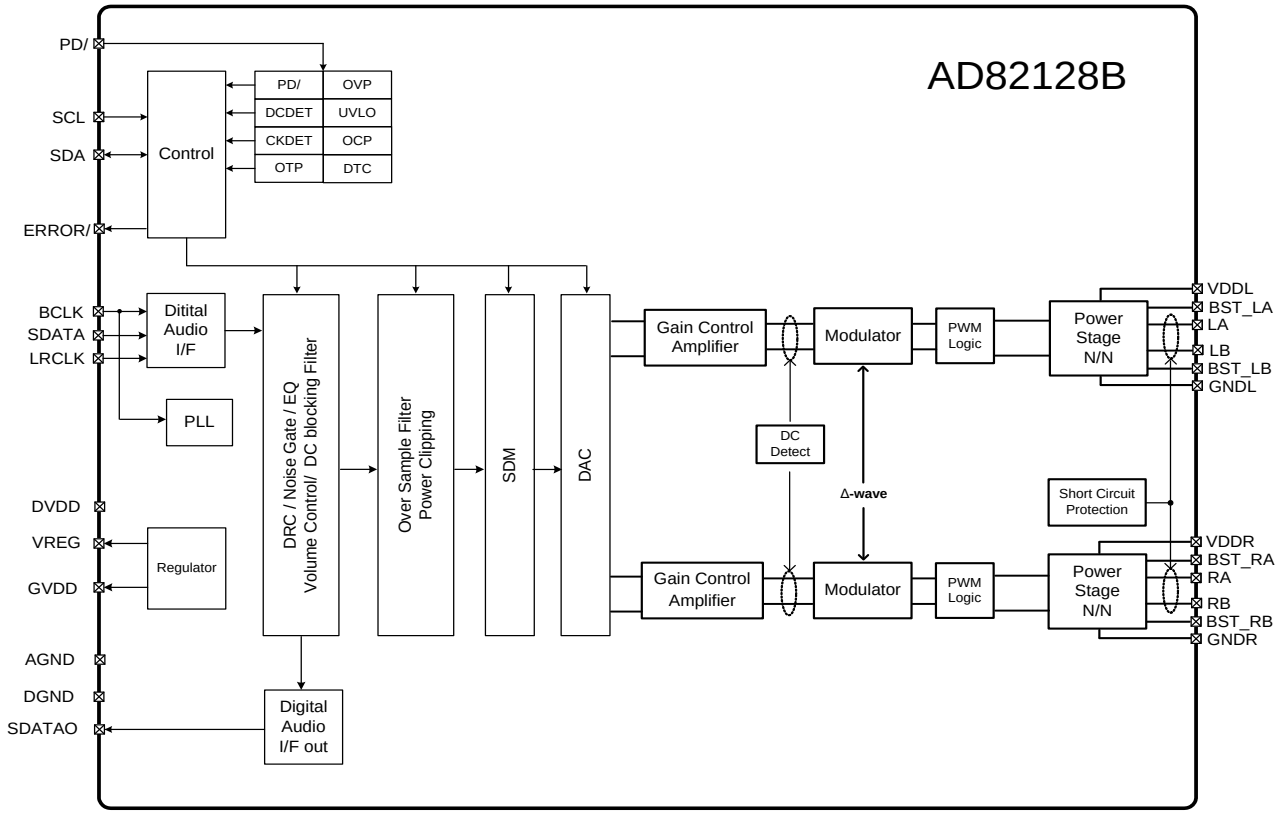
Pin Description

PIN	NAME	TYPE	DESCRIPTION	CHARACTERISTICS
1	DGND	P	Digital Ground.	
2	DVDD	P	Digital Power.	
3	$\overline{\text{ERROR}}$	AI/O	This pin is a dual function pin. One is I^2C address setting during power up initial. After power up, it is indicator for error status report (low active), it sets by register of A_SEL_FAULT at address 0x1C B[6] to enable it.	This pin is monitored on the rising edge of reset. It will determine the slave address of AD82128B and define in the device addressing part.
4	VREG	P	1.5V regulator voltage output, this pin must not be used to drive external devices.	
5	NC		Not connected.	
6	LRCIN	DI	Left/Right clock input (Fs).	Schmitt trigger TTL input buffer, internal pull Low with a 100Kohm resistor.
7	BCLK	DI	Bit clock input.	Schmitt trigger TTL input buffer, internal pull Low with a 100Kohm resistor.
8	SDATA	DI	Serial audio data input.	Schmitt trigger TTL input buffer.
9	SDATAO	DO	Serial audio data output.	Schmitt trigger TTL output buffer.
10	SDA	DI/O	I^2C bi-directional serial data.	Schmitt trigger TTL input/output buffer.

11	SCL	DI	I^2C serial clock input.	Schmitt trigger TTL input buffer.
12	$\overline{PD}$	AI	Power down, low active. Place the amplifier in Shutdown.	Schmitt trigger TTL input buffer, internal pull Low with a 100Kohm resistor.
13	GVDD	P	5V Regulator voltage output, this pin must not be used to drive external devices.	
14	AGND	P	Analog Ground.	
15	VDDR	P	Right channel supply.	
16	VDDR	P	Right channel supply.	
17	RA	O	Right channel output A.	
18	BST_RA	P	Bootstrap capacitor connect pin for right channel output A, it is used to create a power supply for the high-side gate drive for right channel output A.	
19	GNDR	P	Right channel ground.	
20	RB	O	Right channel output B.	
21	BST_RB	P	Bootstrap capacitor connect pin for right channel output B, it is used to create a power supply for the high-side gate drive for right channel output B.	
22	BST_LB	P	Bootstrap capacitor connect pin for left channel output B, it is used to create a power supply for the high-side gate drive for left channel output B.	
23	LB	O	Left channel output B.	
24	GNDL	P	Left channel ground.	
25	BST_LA	P	Bootstrap capacitor connect pin for left channel output A, it is used to create a power supply for the high-side gate drive for left channel output A.	
26	LA	O	Left channel output A.	
27	VDDL	P	Left channel supply.	
28	VDDL	P	Left channel supply.	
Thermal land			Connect to the system ground.	

Note: AI=Analog input; AO=Analog output; AI/O = Analog Bi-directional (input and output); DI=Digital Input; DO=Digital Output; DI/O = Digital Bi-directional (input and output); P=Power or Ground; O: PWM output

Functional Block Diagram



Ordering Information

Product ID	Package	Packing / MPQ	Comments
AD82128B-QG28NRR	E-TSSOP 28L	2500 Units / Reel 1 Reel / Small Box	Green

Available Package

Package Type	Device No.	θ_{JA}(℃/W)	θ_{JT}(℃/W)	Ψ_{JT}(℃/W)	Exposed Thermal Pad
E-TSSOP 28L	AD82128B	28	27.1	1.33	Yes (Note 1)

Note 1.1: The thermal pad is located at the bottom of the package. To optimize thermal performance, soldering the thermal pad to the PCB's ground plane is suggested.

Note 1.2: θ_{JA}, the junction-to-ambient thermal resistance is simulated on a room temperature (T_A=25℃), natural convection environment test board, which is constructed with a thermally efficient, 4-layers PCB (2S2P). The simulation is tested using the JESD51-5 thermal measurement standard.

Note 1.3: θ_{JT} represents the thermal resistance for the heat flow between the chip junction and the package's top surface. It's extracted from the simulation data with obtaining a cold plate on the package top.

Note 1.4: Ψ_{JT} represents the thermal parameter for the heat flow between the chip junction and the package's top surface center. It's extracted from the simulation data for obtainingθ_{JA}, using a procedure described in JESD51-2.

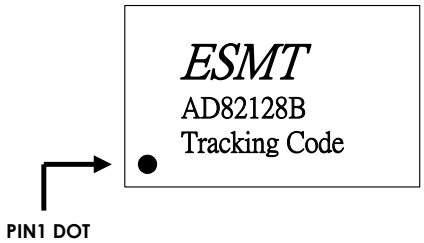
Marking Information

AD82128B

Line 1 : LOGO

Line 2 : Product no.

Line 3 : Tracking Code



Absolute Maximum Ratings (AMR)

Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device.

Symbol	Parameter		Min	Max	Units
DVDD	Supply for Digital Circuit		-0.3	3.6	V
PVDD	VDDL/R Supply for Driver Stage		-0.3	30	V
	Output Pin (LA, LB, RA and RB) to GND			32	V
V_i	Input Voltage		-0.3	3.6	V
T_{stg}	Storage Temperature		-65	150	^oC
T_J	Junction Operating Temperature		-40	150	^oC
ESD	Human Body Model			±2K	V
	Charged Device Model			±500	V
R_L	Minimum Load Resistance	BTL: 8V≦PVDD ≦16V	3.2		Ω
		BTL: 16V＜PVDD ≦24V	4.8		Ω
		PBTL: 8V≦PVDD ≦16V	1.6		Ω
		PBTL: 16V＜PVDD ≦24V	2.4		Ω

Recommended Operating Conditions

Symbol	Parameter	Typ	Units
DVDD	Supply for Digital Circuit for 1.8V	1.65~1.95	V
	Supply for Digital Circuit for 3.3V	3.0~3.6	
PVDD	VDDL/R Supply for Driver Stage	4.5~26	V
T_J	Junction Operating Temperature	-40~125	^oC
T_A	Ambient Operating Temperature	-40~85	^oC

General Electrical Characteristics

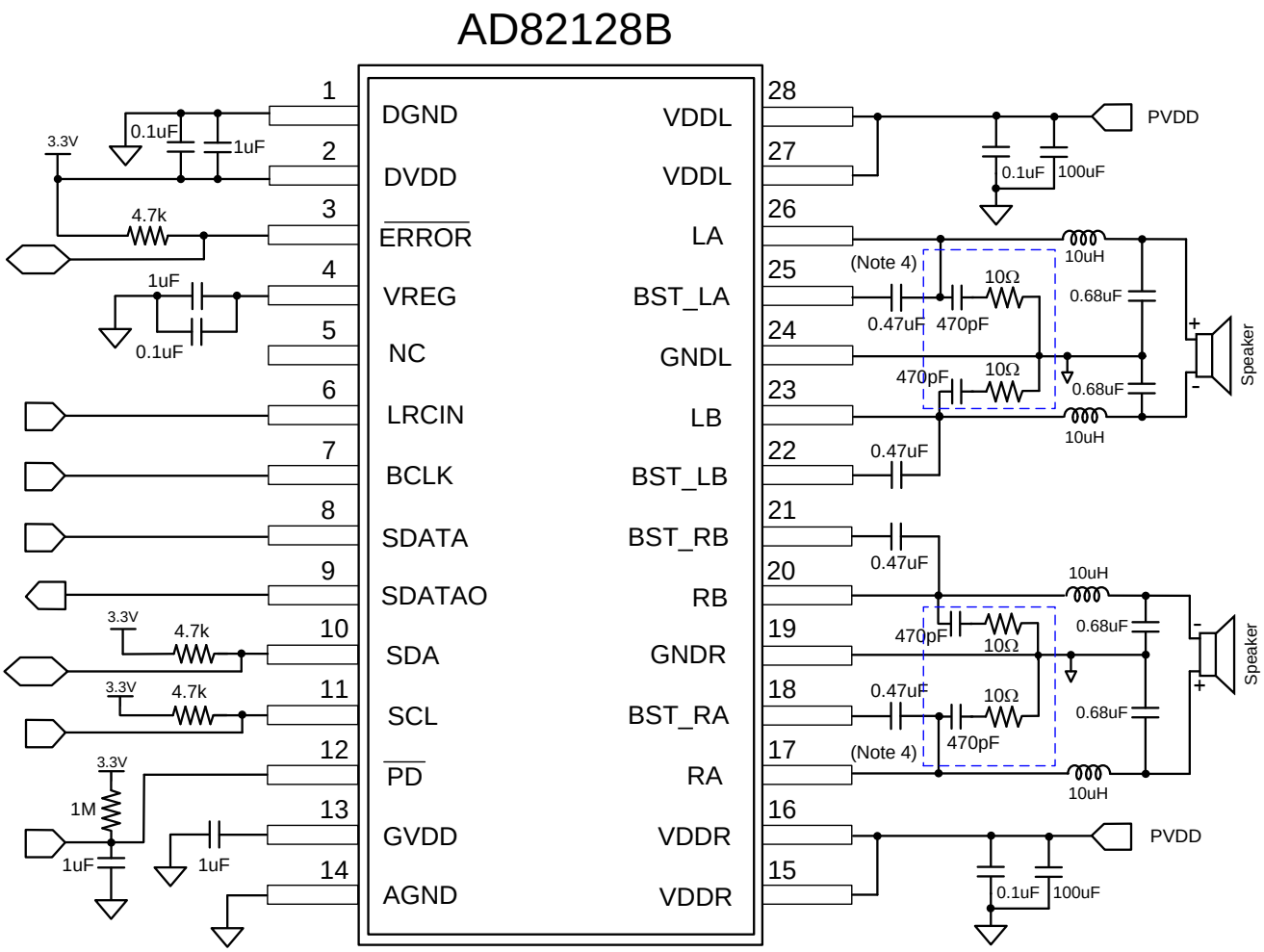
Condition: T_A=25 °C (unless otherwise specified).

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_Q(HV)	Quiescent current for PVDD (PWM in idle pulse after de-mute)	PVDD=24V		13		mA
I_{PD}(HV)	PVDD Supply Current during Shutdown	PVDD=24V		17		uA
I_Q(LV)	Quiescent current for DVDD (Un-mute)	DVDD=3.3V		15		mA
I_{PD}(LV)	DVDD Supply Current during Shutdown	DVDD=3.3V		2		mA
T_{SENSOR}	Junction Temperature for Driver Shutdown			165		°C
	Temperature Hysteresis for Recovery from Shutdown			35		°C
OV_H	VDDL/R Over Voltage Active			29		V
OV_L	VDDL/R Over Voltage Release			28.3		V
$R_{DS(on)}$	Static Drain-to-Source On-state Resistor, NMOS (Note 2)	PVDD=24V, Id=500mA		120		mΩ
I_{SC}	L(R) Channel Over-Current Protection (Note 3)	PVDD=24V		9		A
		PVDD=12V		8.5		A
	Mono Over-Current Protection (Note 3)	PVDD=24V		9		A
		PVDD=12V		8.5		A
V_{IH}	High-Level Input Voltage	DVDD=3.3V	2.0			V
		DVDD=1.8V	1.26			V
V_{IL}	Low-Level Input Voltage	DVDD=3.3V			0.8	V
		DVDD=1.8V			0.54	V
V_{OH}	High-Level Output Voltage	DVDD=3.3V	2.4			V
		DVDD=1.8V	1.44			V
V_{OL}	High-Level Output Voltage	DVDD=3.3V			0.4	V
		DVDD=1.8V			0.4	V
C_I	Input Capacitance			6.4		pF
f_{PWM}	PWM Frequency	FSW=00		384		KHz
		FSW=01		600		
		FSW=10		850		

Note 2: That's no bond-wire or pin resistance included in here.

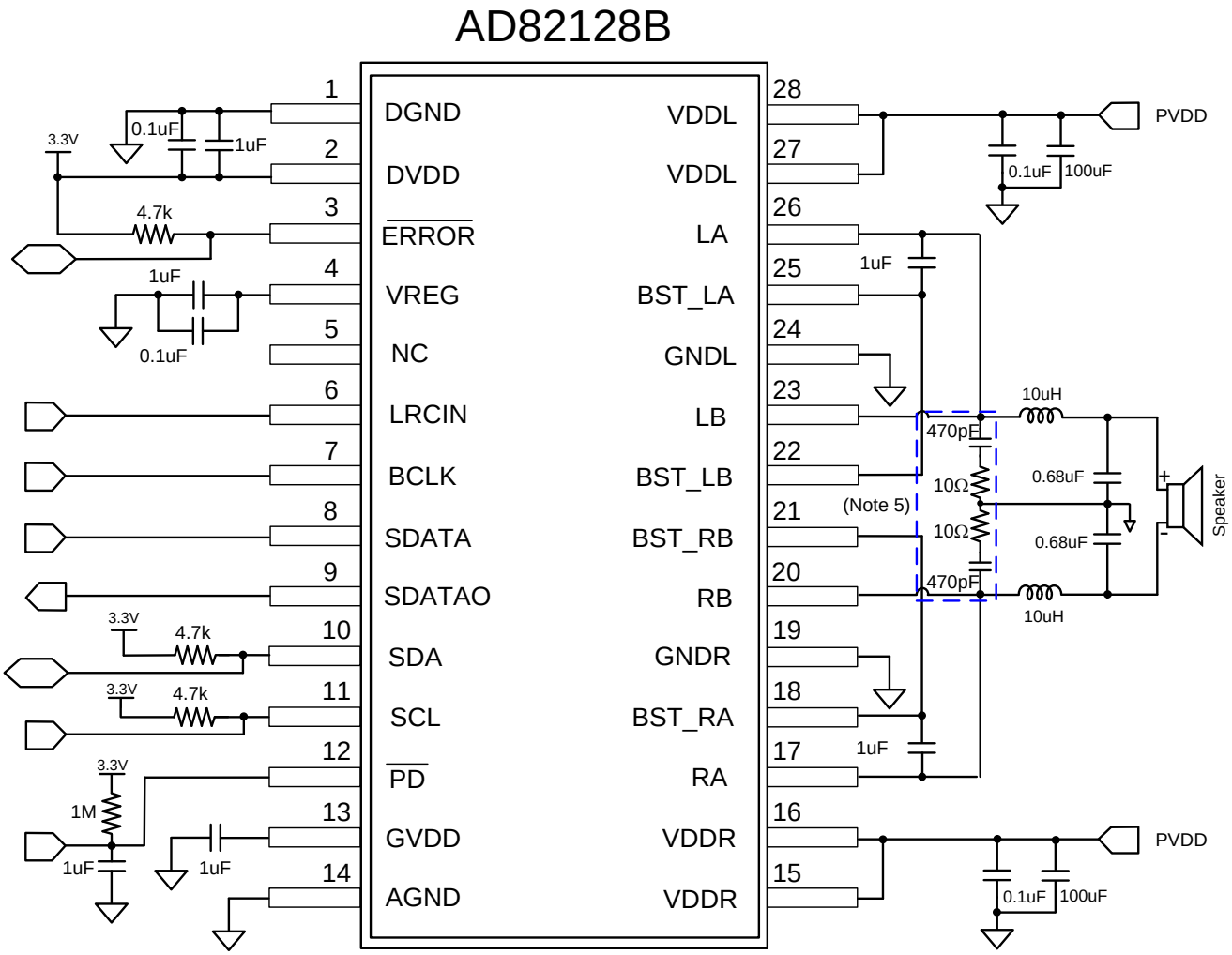
Note 3: Loudspeaker over-current protection is only effective when loudspeaker drivers are properly connected with external LC filters. Please refer to the application circuit example for recommended LC filter configuration.

Application Circuit Example for Stereo



Note 4: Option for EMI.

Application Circuit Example for Mono



Note 5: Option for EMI.

Electrical Characteristics and Specifications for Loudspeaker

- **BTL (Bridge-Tied-Load) output for Stereo**

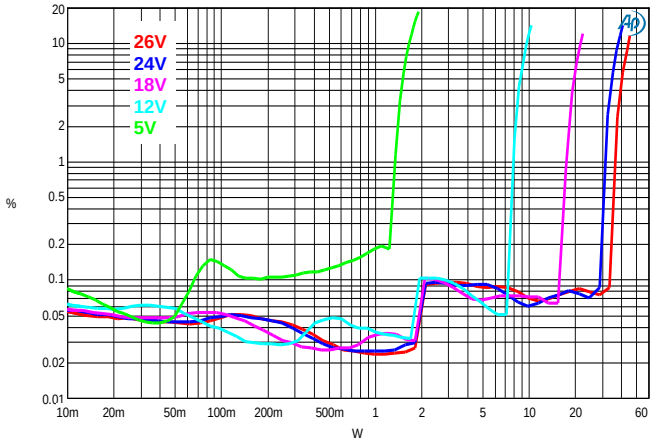
Condition: T_A=25°C, DVDD=3.3V, VDDL=VDDR=24V, F_S=48kHz, Load=8Ω with passive LC lowpass filter (L=10μ H with R_{DC}=25mΩ , C=680nF); Input is 1kHz sinewave. Volume is 0dB, f_{PWM}=384kHz unless otherwise specified.

Symbol	Parameter	Condition	Input Level	Min	Typ	Max	Units
P_O (Note 8)	RMS Output Power (THD+N=10%)	Instantaneous output power			37		W
	RMS Output Power (THD+N=2%)	Continuous output power			32		W
	RMS Output Power (THD+N=1%)				30		W
	RMS Output Power (THD+N=0.08%)				20		W
	RMS Output Power (THD+N=0.06%)				10		W
THD+N	Total Harmonic Distortion + Noise	P_O=1W			0.03		%
		P_O=15W			0.07		%
SNR	Signal to Noise Ratio (Note 9)	Maximum power at THD < 1% @1kHz			108		dB
DR	Dynamic Range (Note 9)		-60dB		112		dB
Vn	Output Noise (Note 9)	20Hz to 20kHz			45		uV
		20Hz to 20kHz @12V			40		
PSRR	Power Supply Rejection Ratio	V_{RIPPLE}=200mVpp noise injected at 1kHz			-74		dB
	Channel Separation	P_O=1W @1kHz			-97		dB

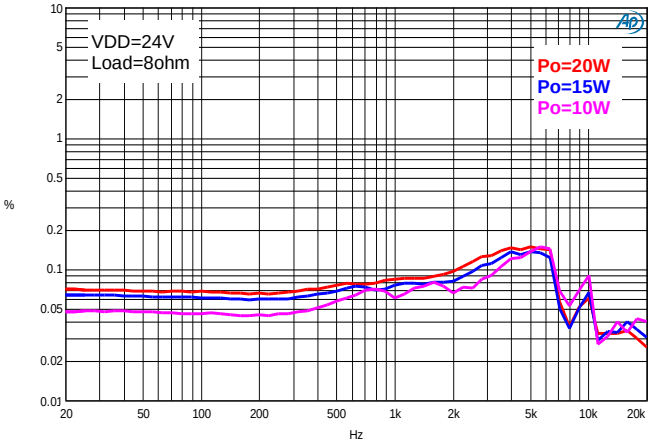
Note 8: Thermal dissipation is limited by package type and PCB design. The external heat-sink or system cooling method should be adopted to meet system thermal requirement.

Note 9: Measured with A-weighting filter.

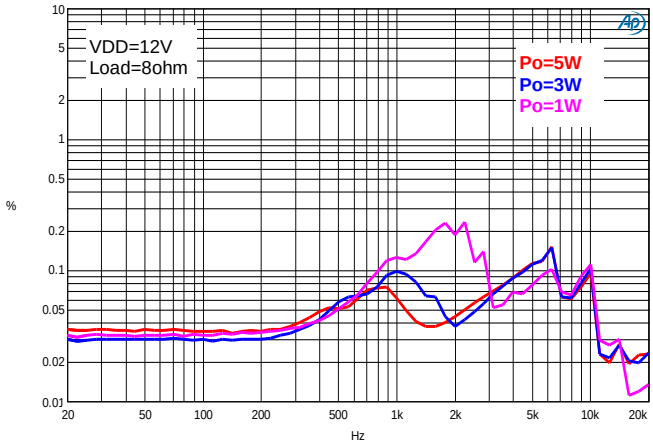
THD+N vs. Output Power, 8Ω load (BTL)



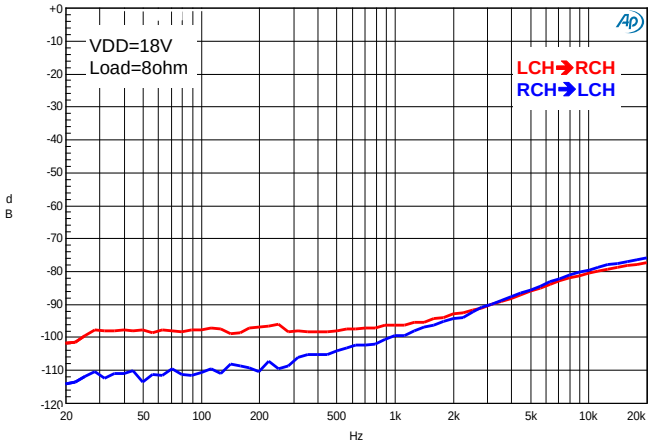
THD+N vs. Frequency, 8Ω load (BTL)



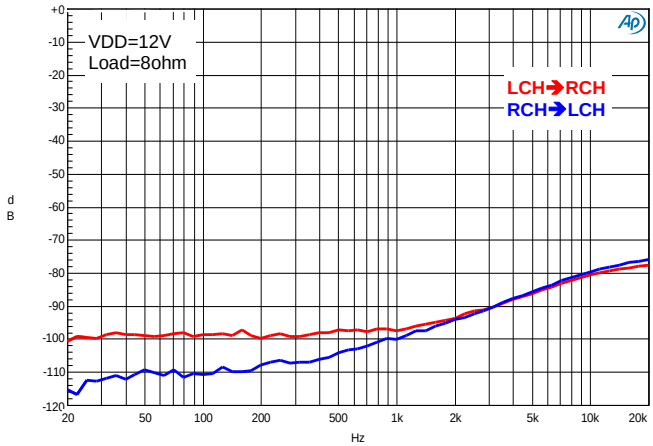
THD+N vs. Frequency, 8Ω load (BTL)



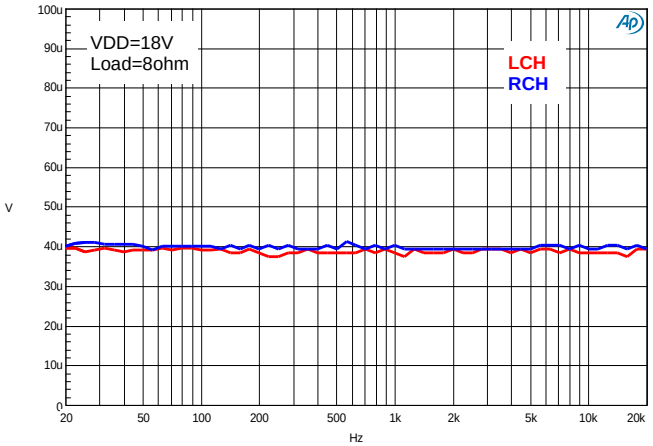
Crosstalk, 8Ω load (BTL)



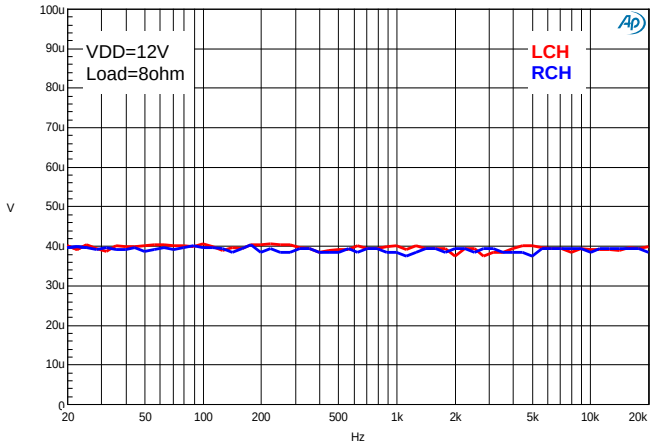
Crosstalk, 8Ω load (BTL)



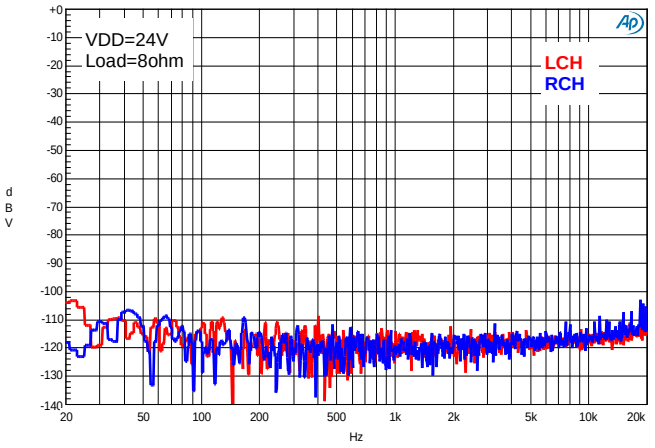
Noise, 8Ω load (BTL)



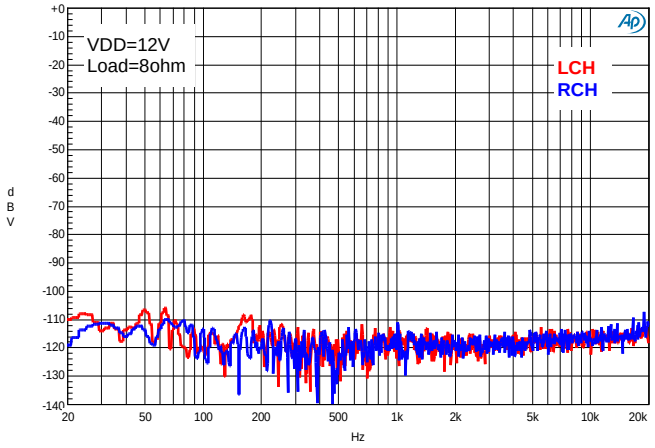
Noise, 8Ω load (BTL)



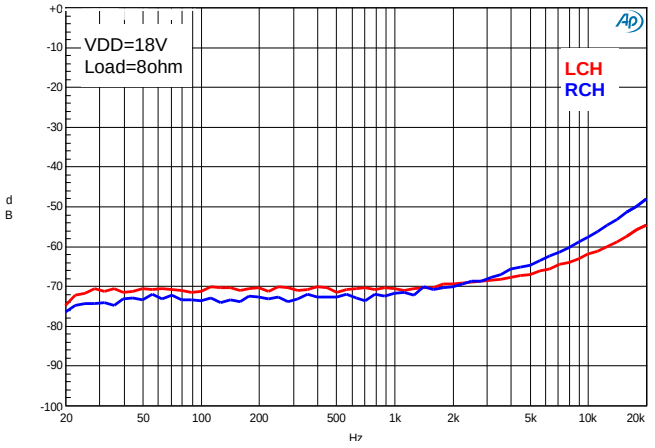
Noise FFT, 8Ω load (BTL)



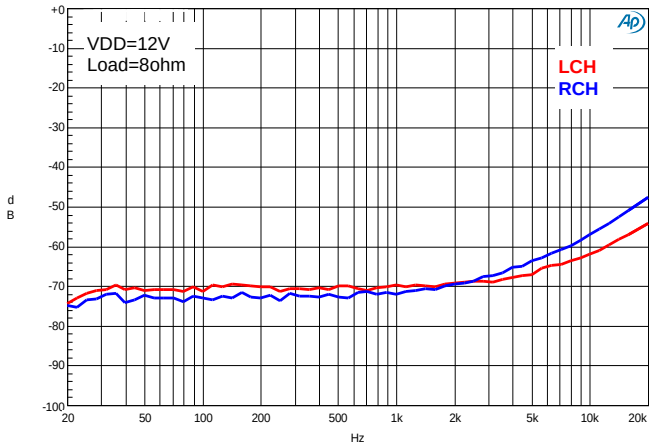
Noise FFT, 8Ω load (BTL)



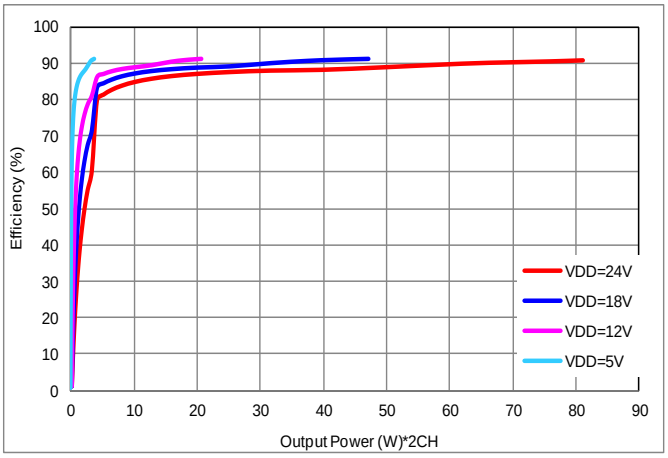
PSRR, 8Ω load (BTL)



PSRR, 8Ω load (BTL)



Efficiency, 8Ω load (BTL)



Electrical Characteristics and Specifications for Loudspeaker (cont.)

- **PBTL (Parallel-Bridge-Tied-Load) output for Mono**

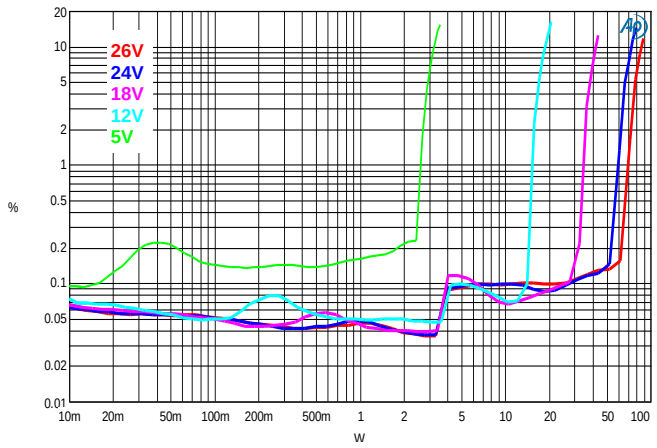
Condition: T_A=25°C, DVDD= 3.3V, VDDL=VDDR=24V, F_S=48kHz, Load=4Ω with passive LC lowpass filter (L=10μ H with R_{DC}=25mΩ , C=680nF); Input is 1kHz sinewave. Volume is 0dB, f_{PWM}=384kHz unless otherwise specified.

Symbol	Parameter	Condition	Input Level	Min	Typ	Max	Units
P_O (Note 10)	RMS Output Power (THD+N=10%)	Instantaneous output power			74		W
	RMS Output Power (THD+N=3%)	Continuous output power			64		W
	RMS Output Power (THD+N=1%)				60		W
	RMS Output Power (THD+N=0.14%)				50		W
	RMS Output Power (THD+N=0.12%)				40		W
THD+N	Total Harmonic Distortion + Noise	P_O=1W			0.05		%
		P_O=30W			0.1		%
SNR	Signal to Noise Ratio (Note 11)	Maximum power at THD < 1% @1kHz			108		dB
DR	Dynamic Range (Note 11)		-60dB		112		dB
Vn	Output Noise (Note 11)	20Hz to 20kHz			45		uV
		20Hz to 20kHz @12V			42		

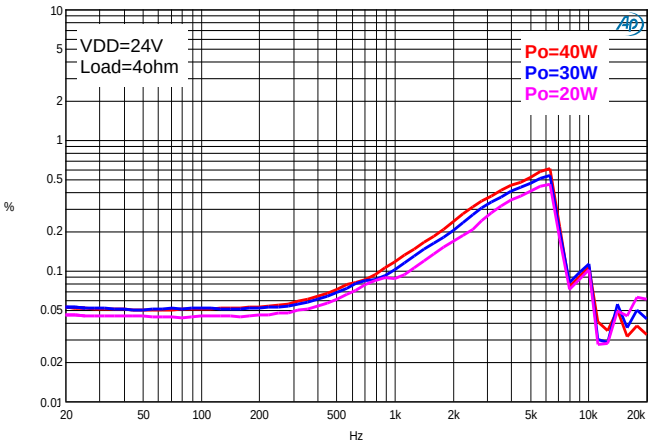
Note 10: Thermal dissipation is limited by package type and PCB design. The external heat-sink or system cooling method should be adopted for to meet system thermal requirement.

Note 11: Measured with A-weighting filter.

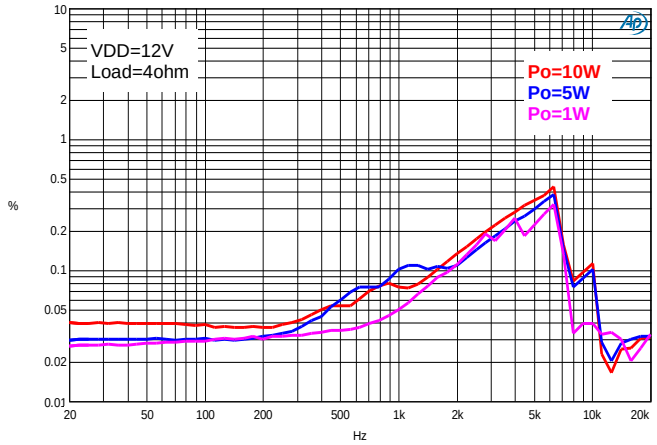
THD+N vs. Output Power, 4Ω load (PBTL)



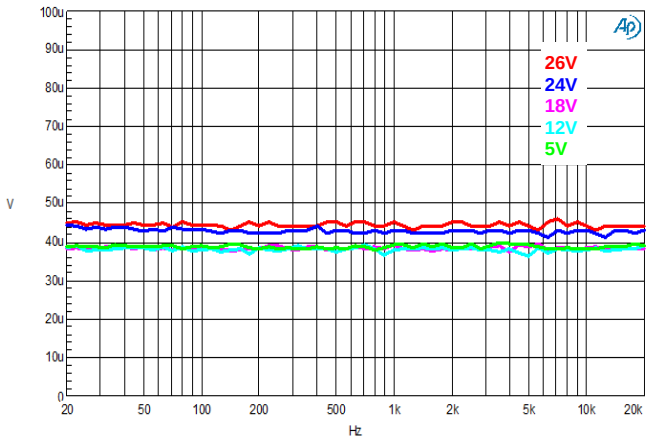
THD+N vs. Frequency, 4Ω load (PBTL)



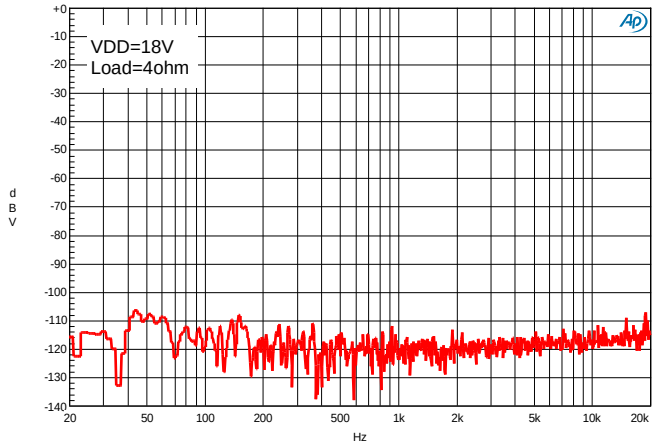
THD+N vs. Frequency, 4Ω load (PBTL)



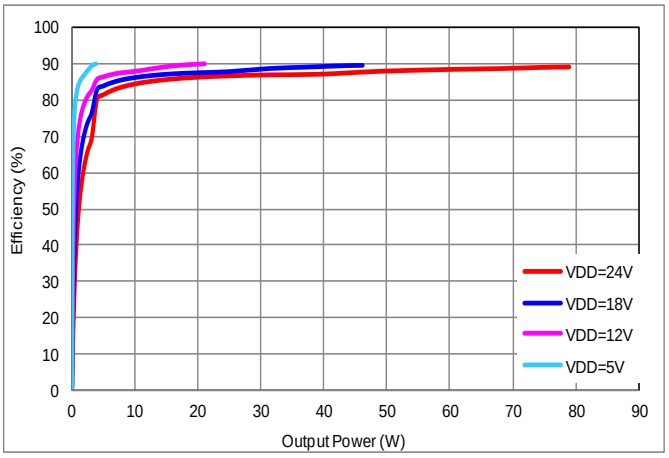
Noise, 4Ω load (PBTL)



Noise FFT, 4Ω load (PBTL)

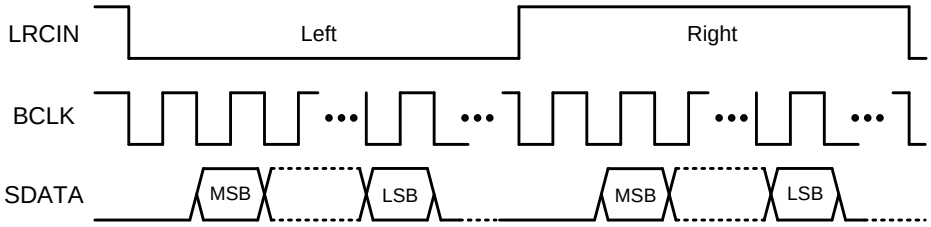


Efficiency, 4Ω load (PBTL)

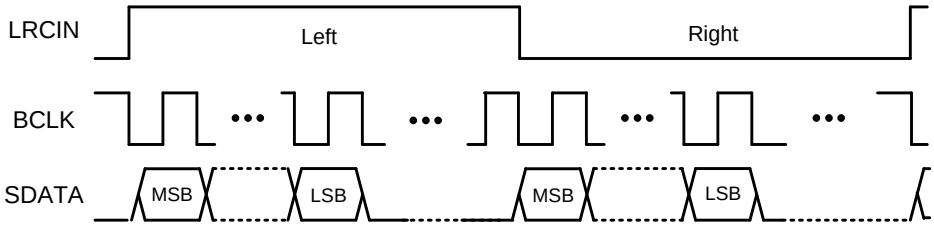


Interface configuration

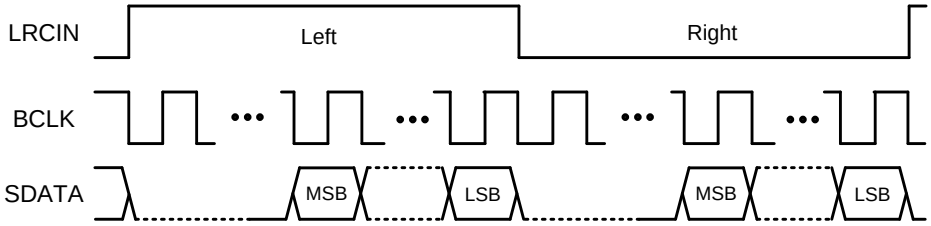
- I^2S



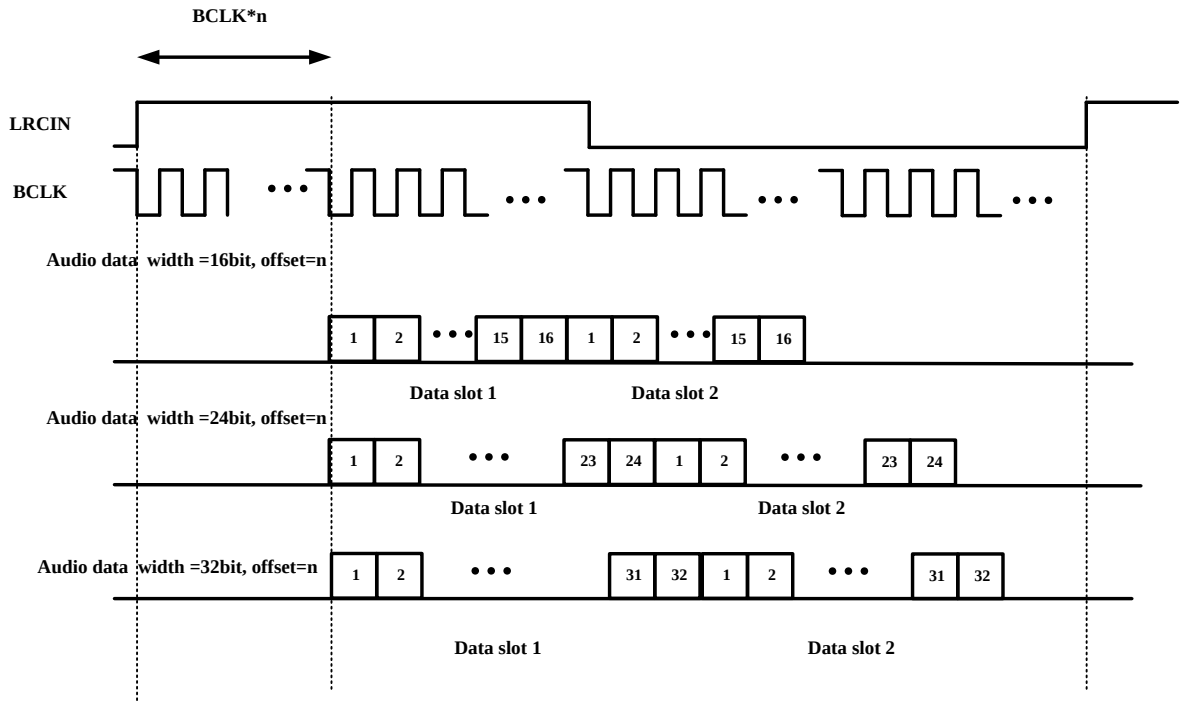
- Left-Alignment



- Right-Alignment



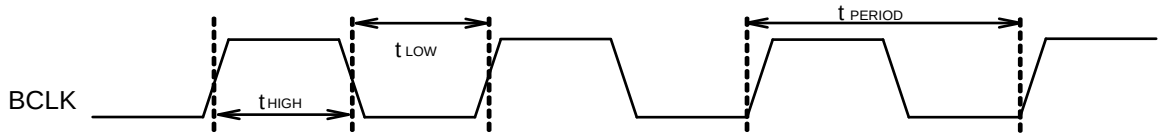
- TDM



AD82128B device audio data formats, bit depths, clock rates, and channel numbers (BCLK system)

Format	Data Bits	LRCIN Frequency (KHz)	BCLK Rate (FS)	Channel numbers
I^2S/LJ/RJ	32, 24, 16	16, 48, 96	64x, 48x, 32x	2
	32, 16	8	64x, 32x	2
TDM	32, 24, 16	8	64x, 128x, 192x ,256x for 32 data bits 96x, 192x for 24 data bits 32x, 64x, 96x ,128x, 256x for 16 data bits	2, 4, 6, 8 channels for 32 data bits 4,8 channels for 24 data bits 2,4,6,8,16 channels for 16 data bits
	32, 24, 16	16	64x 128x 192x and 256x for 32 data bits 48x,96x, 192x for 24 data bits 32x, 64x,128x, 256x for 16 data bits	2, 4, 6, 8 channels for 32 data bits 2, 4, 8 channels for 24 data bits 2,4,6,8,16 channel for 16 data bits
	32, 24, 16	48, 96	64x, 128x, 192x, 256x for 32 data bits 48x,96x, 192x for 24 data bits 32x, 64x,128x, 256x for 16 data bits	2, 4, 6, 8 channels for 32 data bits 2, 4, 8 channels for 24 data bits 2, 4, 6, 8,16 channels for 16 data bits

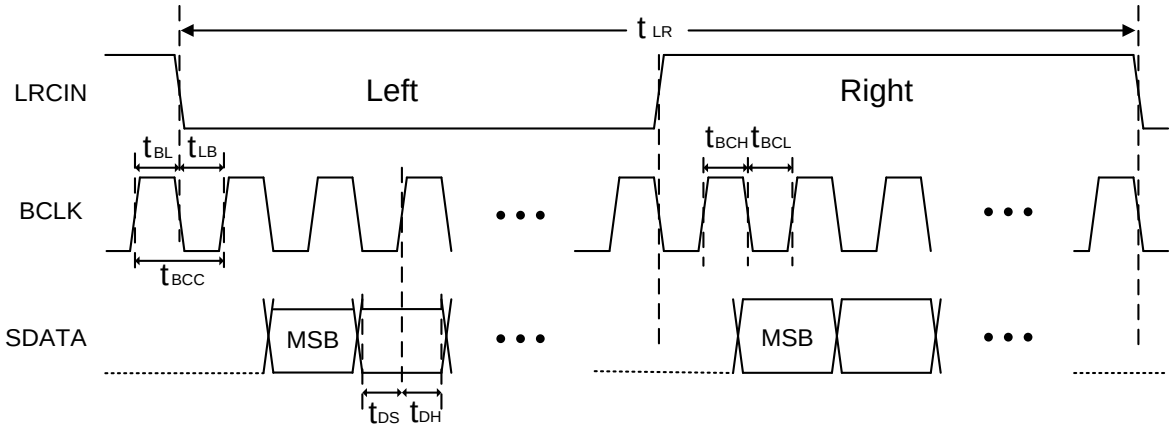
- System Clock Timing



t_{HIGH} ≧ 162.7 ns , t_{LOW} ≧ 162.7 ns , t_{PERIOD} ≧ 325.4 ns

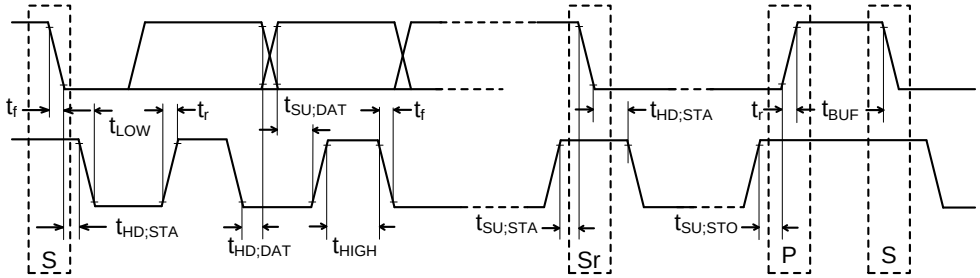
Default setting,PLL is enable
BCLK system

- Timing Relationship (Using I^2S format as an example)



Symbol	Parameter	Min	Typ	Max	Units
t_{LR}	LRCIN Period ($1/F_S$)	10.4		31.25	μs
t_{BL}	BCLK Rising Edge to LRCIN Edge	12.5			ns
t_{LB}	LRCIN Edge to BCLK Rising Edge	12.5			ns
t_{BCC}	BCLK Period (Min. is for 96k with 1/256Fs, Max. is for 32k with 1/64 Fs)	40.69		488.3	ns
t_{BCH}	BCLK Pulse Width High	20.35		244	ns
t_{BCL}	BCLK Pulse Width Low	20.35		244	ns
t_{DS}	SDATA Set-Up Time	12.5			ns
t_{DH}	SDATA Hold Time	12.5			ns

- I^2C Timing



Parameter	Symbol	Standard Mode		Fast Mode		Unit
		MIN.	MAX.	MIN.	MAX.	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Hold time for repeated START condition	$t_{HD,STA}$	4.0	---	0.6	---	μs
LOW period of the SCL clock	t_{LOW}	4.7	---	1.3	---	μs
HIGH period of the SCL clock	t_{HIGH}	4.0	---	0.6	---	μs
Setup time for repeated START condition	$t_{SU;STA}$	4.7	---	0.6	---	μs
Hold time for I^2C bus data	$t_{HD;DAT}$	0	3.45	0	0.9	μs
Setup time for I^2C bus data	$t_{SU;DAT}$	250	---	100	---	ns
Rise time of both SDA and SCL signals	t_r	---	1000	---	300	ns
Fall time of both SDA and SCL signals	t_f	---	300	---	300	ns
Setup time for STOP condition	$t_{SU;STO}$	4.0	---	0.6	---	μs
Bus free time between STOP and the next START condition	t_{BUF}	4.7	---	1.3	---	μs
Capacitive load for each bus line	C_b		400		400	pF

Operation Description

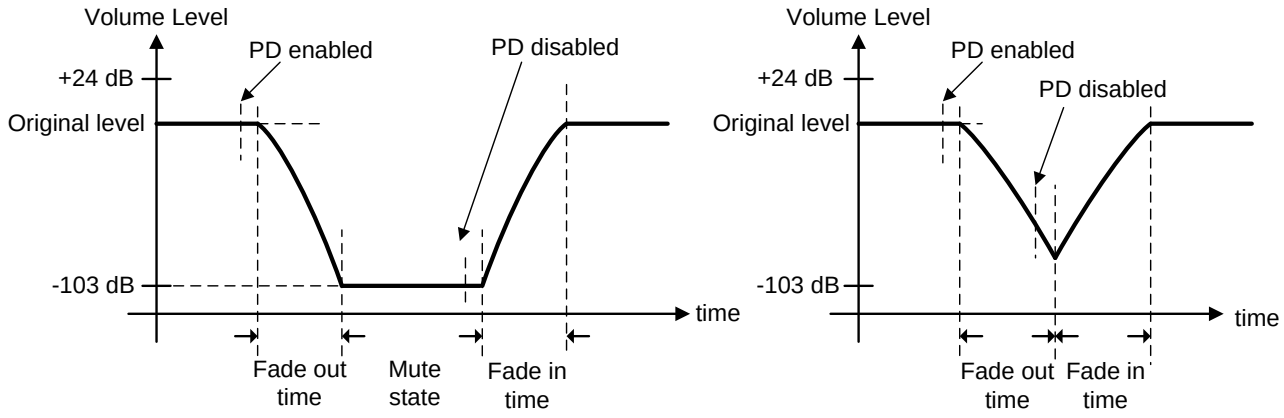
The default volume of AD82128B is muted. AD82128B will be activated while the de-mute command via I^2C is programmed.

- Internal PLL

  AD82128B has a built-in PLL internally, the BCLK/FS ratio, which is selected by I^2C control interface. The clock inputted into the BCLK pin becomes the frequency of multiple edge evaluation in chip internally.

- Power down control

  AD82128B has a built-in volume fade-in/fade-out design for PD/Mute function. The relative PD timing diagrams for loudspeakers are shown below.



$$(10^{\frac{target(dB)}{20}} - 10^{\frac{original(dB)}{20}}) x 128 x (1/96K)$$

(Note: Address 0x1C B[3:2]=0)

The volume level will be decreased to -∞dB in several LRCIN cycles. Once the fade-out procedure is finished, AD82128B will turn off the power stages, clock signals (for digital circuits) and current (for analog circuits). After PD/ pin is pulled low, AD82128B requires T_{fade} to finish the forementioned work before entering power down state. User can not program AD82128B during power down state. Also, all settings in the registers will remain intact unless DVDD is removed.

If the PD signal is removed during the fade-out procedure (above, right figure), AD82128B will still execute the fade-in procedure. In addition, AD82128B will establish the analog circuits' bias current and send the clock signals to digital circuits. Afterwards, AD82128B will return to its normal status.

- Self-protection circuits

AD82128B has built-in protection circuits including thermal, short-circuit, under-voltage detection, and over voltage circuits.

(i) When the internal junction temperature is higher than 165℃, power stages will be turned off and AD82128B will return to normal operation once the temperature drops to 130℃. The temperature values may vary around 10%.

(ii) The short-circuit protection circuit protects the output stage when the wires connected to loudspeakers are shorted to each other or GND/VDD. For normal 18V operations, the current flowing through the power stage will be less than 9A for stereo configuration. Otherwise, the short-circuit detectors may pull the $\overline{\text{ERROR}}$ pin to DGND, disabling the output stages. When the over-temperature or short-circuit condition occurs, the open-drain $\overline{\text{ERROR}}$ pin will be pulled low and latched into ERROR state.

Once short-circuit condition is removed, AD82128B will exit ERROR state when one of the following conditions is met: (1) $\overline{\text{PD}}$ pin is pulled low, (2) Master mute is enabled through the I^2C interface.

(iii) Once the DVDD voltage is lower than 1.35V, AD82128B will turn off its loudspeaker and reset power stages. When DVDD becomes higher than 1.5V, AD82128B will return to normal operation.

(iv) Once the PVDD voltage is higher than 29V, AD82128B will turn off its loudspeaker power stages. When PVDD becomes lower than 28.3V, AD82128B will return to normal operation.

(v) Once the PVDD voltage is lower than 4.0V, AD82128B will turn off its loudspeaker power stages. When PVDD becomes higher than 4.2V, AD82128B will return to normal operation.

- Clock detection

AD82128B has clock error handling that uses the built-in oscillator clock to quickly detect changes / errors. Once the system detects the clock change / error, it will turn off the output and then force the oscillator clock as the reference clock of PLL. If the clocks are stable, the system will detect automatically and the system will revert to normal operation. During this process, AD82128B will fade in to the current volume setting.

- Anti-pop design

AD82128B will generate appropriate control signals to suppress pop sounds during initial power on/off, power down/up, mute, and volume level changes.

- 3D surround sound

AD82128B provides the virtual surround sound technology with greater separation and depth voice quality for stereo signals.

- Error indicator

$\overline{\text{ERROR}}$ is a protection indicator when A_SEL_FAULT(0X1C, B[6]) register is setting high. If OVP/OCP/OTP occur, ERROR pin will be low.

- I^2C chip select

2 address mode (register 0X1C B[5], DEV_NUM=0), $\overline{\text{ERROR}}$ pin is an input pin during power. It can be pulled high (15-kΩ pull up) or low (15-kΩ pull down) for I2C address selection. Low indicates an I^2C address of 0x68, and high an address of 0x69.

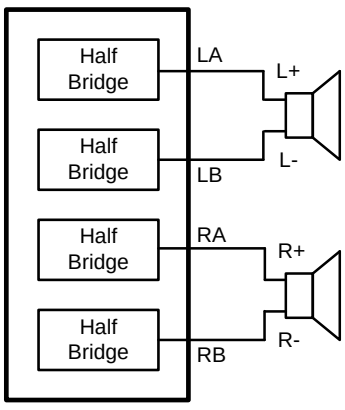
4 address mode (register 0X1C B[5], DEV_NUM=1), AD82128B slave address can be selected by $\overline{\text{ERROR}}$ in the following table.

ERROR pin configuration	MSBs				User Define			LSB
4.7k Ω to DVDD	1	1	0	1	0	0	0	R/W
15k Ω to DVDD	1	1	0	1	0	0	1	R/W
47kΩ to DVDD	1	1	0	1	1	0	0	R/W
120kΩ to DVDD	1	1	0	1	1	0	1	R/W

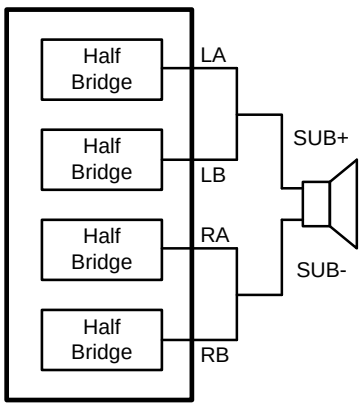
- Output configuration

AD82128B can be configured to mono (PBTL) via I^2C control, set register MONO_EN=1 (register 0X1A, B[6]) and MONO_KEY=3006(HEX) (register 0X5B & 0X5C) to entry PBTL configuration.

Configuration figures:



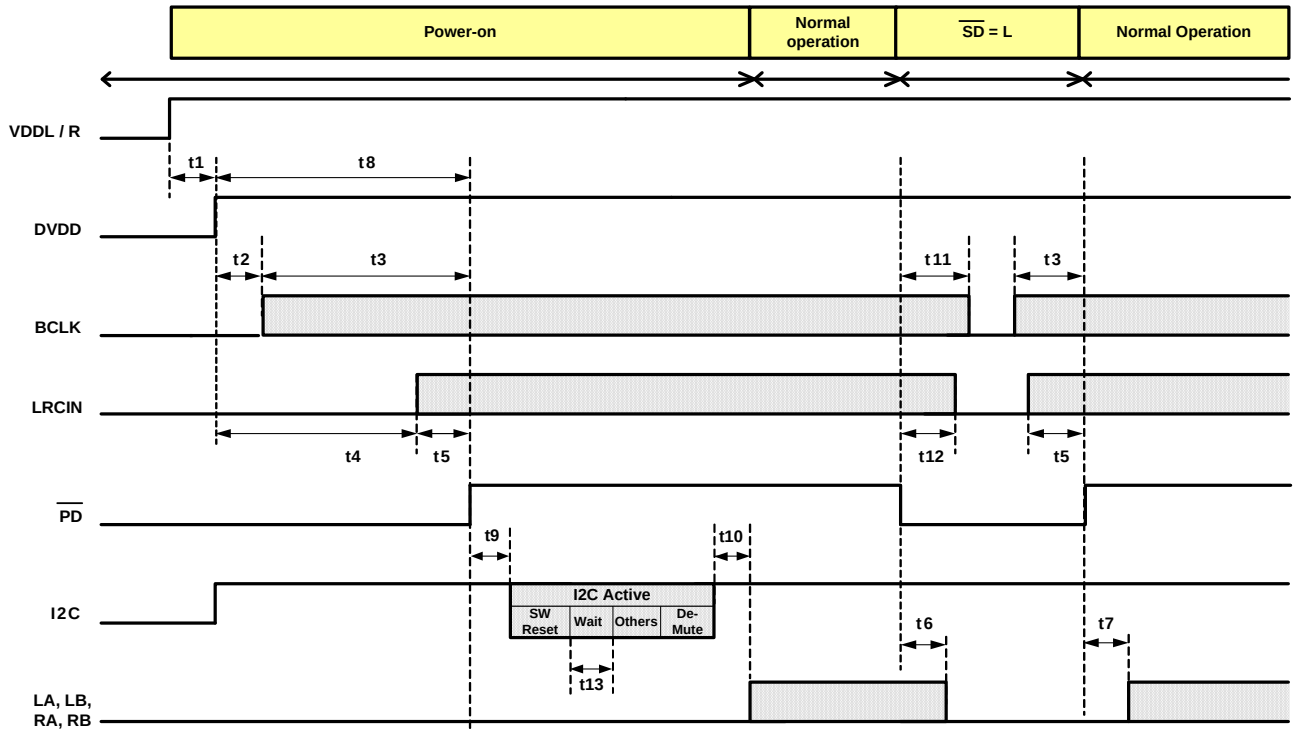
STEREO



MONO

- Power on sequence

  Hereunder is AD82128B's power on sequence. Give a de-mute command via I^2C when the whole system is stable.



Note 8:

Please be noted below sequence shall be followed up with "I2C Active" processing,

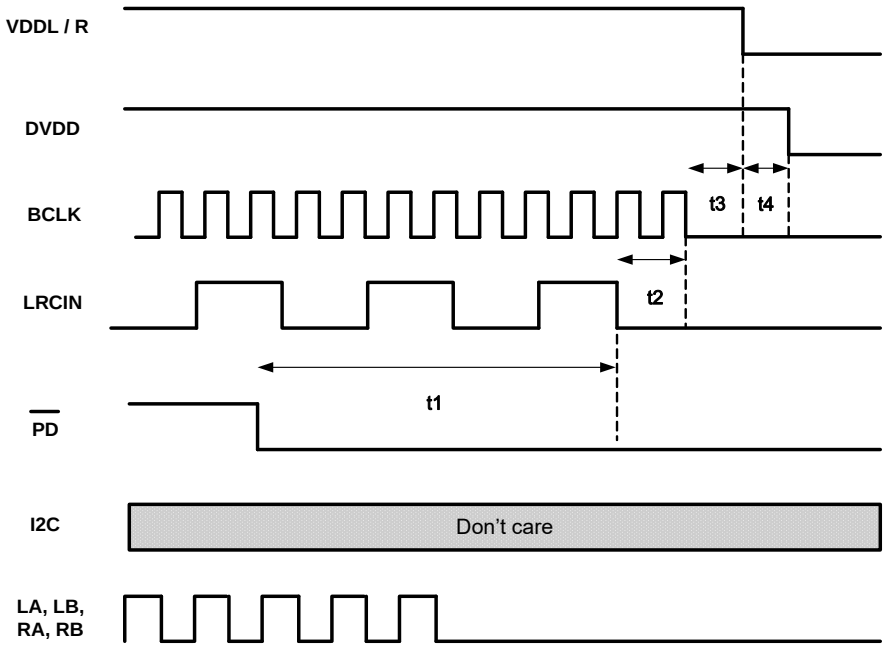
(1) Set S/W reset bit (0X1A B[5]) = 0 → (2) Delay 5ms → (3) Set S/W reset bit (0X1A B[5]) = 1 → (4) Delay 20ms → (5) Set all channels = mute (setting address 0X02 B[6] = 1) → (6) Set other registers (except setting address 0X02 B[6] and 0X1A B[5]) → (7) Set all channels = de-mute (setting address 0X02 B[6] = 0)

Symbol	Condition	Min	Max	Units
t1		0	-	msec
t2		0	-	msec
t3		10	-	msec
t4		0	-	msec
t5		10	-	msec
t6		-	22	msec
t7		-	45	msec
t8		10	-	msec
t9		45	-	msec
t10		-	0.1	msec

t11		25	-	msec
t12		25	-	msec
t13		20	-	msec

- Power off sequence

Hereunder is AD82128B's power off sequence.



Symbol	Condition	Min	Max	Units
t1		35(Note 9)	-	msec
t2		0	-	msec
t3		1(Note 10)	-	msec
t4		1(Note 10)	-	msec

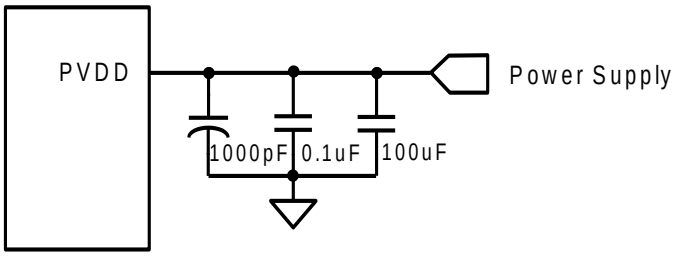
Note 9: t1 min 35ms refer to FADE_SPEED register=0(address: 0X1C, B[3:2]). If the FADE_SPEED=1, t1 should change to 280ms.

Note10: Don't care it if the PVDD or DVDD power supports continuously during the system off.

Application information

- Power supply decoupling capacitor (Cs)

  Because of the power loss on the trace between the device and decoupling capacitor, the decoupling capacitor should be placed close to PVDD and PGND to reduce any parasitic resistor or inductor. A low ESR ceramic capacitor, typically 1000pF, is suggested for high frequency noise rejection. For mid-frequency noise filtering, place a capacitor typically 0.1uF or 1uF as close as possible to the device PVDD leads works best. For low frequency noise filtering, a 100uF or greater capacitor (tantalum or electrolytic type) is suggested.



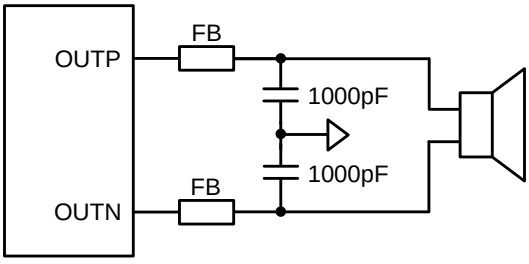
Recommended Power Supply Decoupling Capacitors.

- Boot-strap Capacitor

  The output stage of the AD82128B uses a high-side NMOS driver. To generate the gate driver voltage for the high-side NMOS, a boot-strap capacitor for each output terminal acts as a floating power supply for the switching cycle. Use 0.47uF capacitors to connect the appropriate output pin to the boot-strap pin in stereo application and use 1uF boot-strap capacitor in mono application.

- Ferrite Bead selection

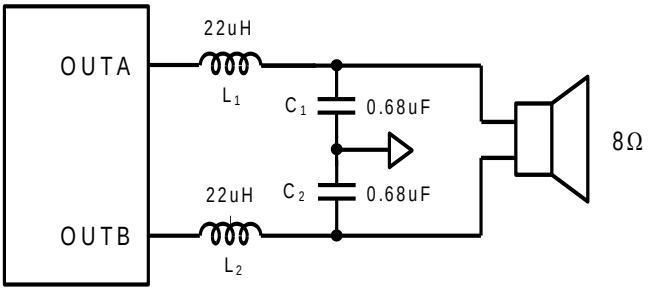
  If the traces from the AD82128B to speaker are short, the ferrite bead filters can reduce the high frequency emissions to meet FCC requirements. A ferrite bead that has very low impedance at low frequency and high impedance at high frequency (above 1MHz) is recommended. The impedance of the ferrite bead can be used along with a small capacitor with a value around 1000pF to reduce the frequency spectrum of the signal to an acceptable level.



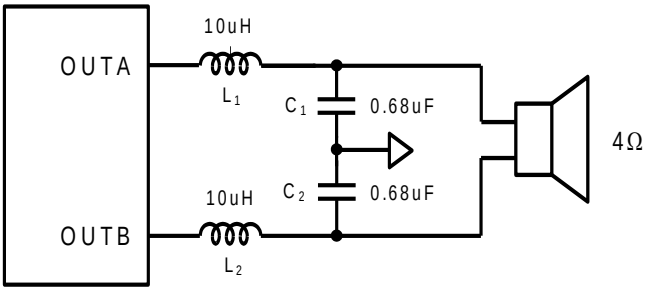
Typical output filter for Filter-less application

- Output LC Filter

If the traces from the AD82128B to speaker are not short, it is recommended to add the output LC filter to eliminate the high frequency emissions. Below figure shows the typical output filter for 8Ω speaker with a cut-off frequency of 41KHz and 4Ω speaker with a cut-off frequency of 61KHz.



Typical LC output filter for 8Ω speaker



Typical LC output filter for 4Ω speaker

AD82128B switching frequency can be adjusted by 384KHz, 600KHz or 850KHz. Higher switching frequency means smaller inductor value needed.

- With 850KHz switching frequency, designers can select 10uH+0.68uF or 4.7uH+0.68uF as the output filter, this will help to save the inductor size with the same rated current during the inductor selection. With 4.7uH+0.68uF filter, make sure PVDD voltage lower enough to avoid the large ripple current to trigger the OC threshold.

PVDD (V)	Speaker Load (Ω)	Recommended Minimum Inductance (uH) for LC filter design
≦18	8	4.7uH+0.68uF
≦12	4	

- With 384KHz switching frequency, designers can select 22uH+0.68uF or 15uH+0.68uF or 10uH+0.68uF as the output filter, this will help to save power dissipation for some battery power supply application.

- Inductor Selection

The inductance vs. current profile for the inductor used in the output LC filter of a class-D amplifier can significantly impact the total harmonic distortion (THD) performance. The inductors always have decreasing inductance with increasing operating current. The inductance falls off severely, which induce inductor distortion is higher during lower-impedance loads. The effective inductance at the peak current is required to be at least 80% of the inductance value

In addition, it is required that the peak current is smaller than the OCP trigger threshold. Same PVDD and switching frequency, larger inductance means smaller idle current for lower power dissipation. The inductor's saturation current Isat > the amplifier's operating peak current is necessary. To operating safe considering, the inductor's saturation current >1.35 times of the peak current of maximum output power is suggested.

$$Inductor\_Ipeak\_selection \geq \sqrt{2 \times \frac{Maximum\_output\_power}{Rload}} \times 1.35$$

I²C-Bus Transfer Protocol

- Introduction

AD82128B employs I²C-bus transfer protocol. Two wires, serial data and serial clock carry information between the devices connected to the bus. Each device is recognized by a unique 7-bit address and can operate as either a transmitter or a receiver. The master device initiates a data transfer and provides the serial clock on the bus. AD82128B is always an I²C slave device.

- Protocol

  - START and STOP condition

START is identified by a high to low transition of the SDA signal. A START condition must precede any command for data transfer. A STOP is identified by a low to high transition of the SDA signal. A STOP condition terminates communication between AD82128B and the master device on the bus. In both START and STOP, the SCL is stable in the high state.

  - Data validity

The SDA signal must be stable during the high period of the clock. The high or low change of SDA only occurs when SCL signal is low. AD82128B samples the SDA signal at the rising edge of SCL signal.

  - Device addressing

The master generates 7-bit address to recognize slave devices. If DEV_NUM=1 (register 0X1C, B[5]), AD82128B slave address can be selected by $\overline{\text{ERROR}}$ in the following table.

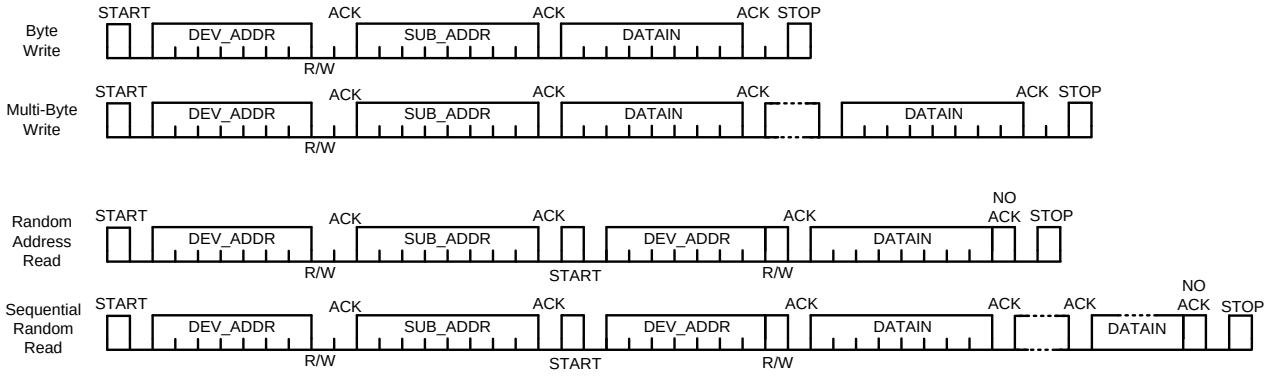
I²C slave address configuration when DEV_NUM is 1.

ERROR pin configuration	MSBs				User Define			LSB
4.7k Ω to DVDD	1	1	0	1	0	0	0	R/W
15k Ω to DVDD	1	1	0	1	0	0	1	R/W
47kΩ to DVDD	1	1	0	1	1	0	0	R/W
120kΩ to DVDD	1	1	0	1	1	0	1	R/W

If DEV_NUM=0, AD82128B receives 7-bit address matched with 1101000 (0x68) or 1101001 (0x69) depend on $\overline{\text{ERROR}}$ pin state during power up ($\overline{\text{ERROR}}$ pin state before changing A_SEL_FAULT=1). AD82128B will acknowledge at the 9th bit (the 8th bit is for R/W bit). The bytes following the device identification address are for AD82128B internal sub-addresses.

■ Data transferring

Each byte of SDA signaling must consist of 8 consecutive bits, and the byte is followed by an acknowledge bit. Data is transferred with MSB first, as shown in the figure below. In both write and read operations, AD82128B supports both single-byte and multi-byte transfers. Refer to the figure below for detailed data-transferring protocol.



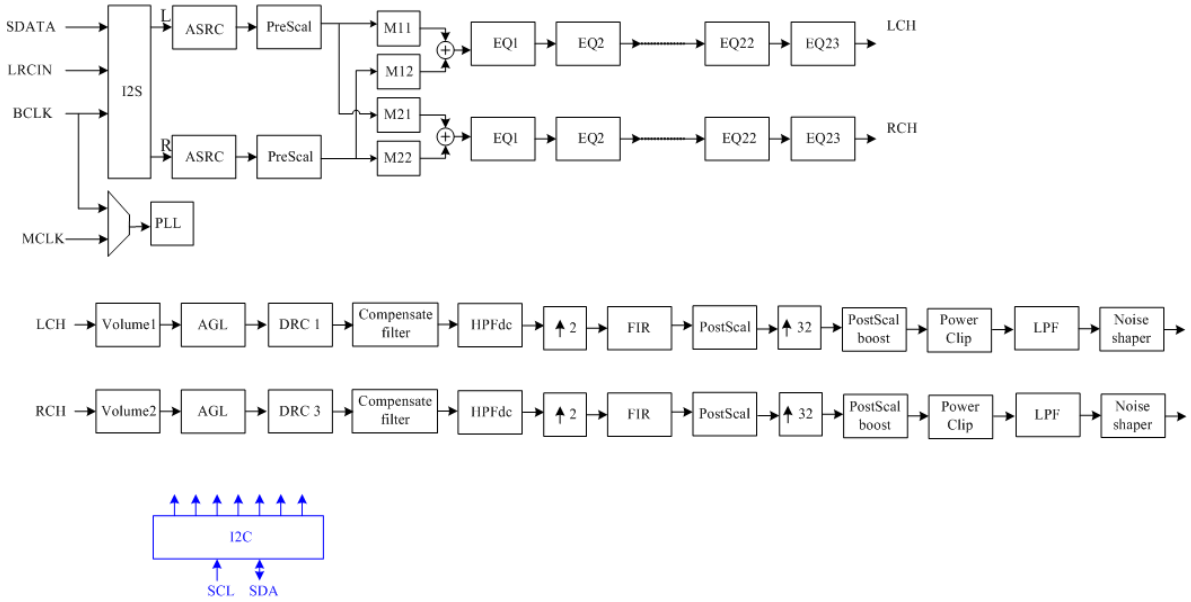
Process Flows

The AD82128B's audio signal processing data flow is shown as the following figures. User can control these functions by programming appropriate settings in the register table. The processing features of each process flow showed as below,

Processing	DRC Band	EQ Per Channel	SRS	EQ of SRS	DPEQ	EQ of DPEQ
1	1	23	No	N/A	No	N/A
2		21	Yes	22~23	No	N/A
3		17	No	N/A	Yes	18~23
4	3	13	No	N/A	No	N/A
5		9	No	N/A	Yes	10~15

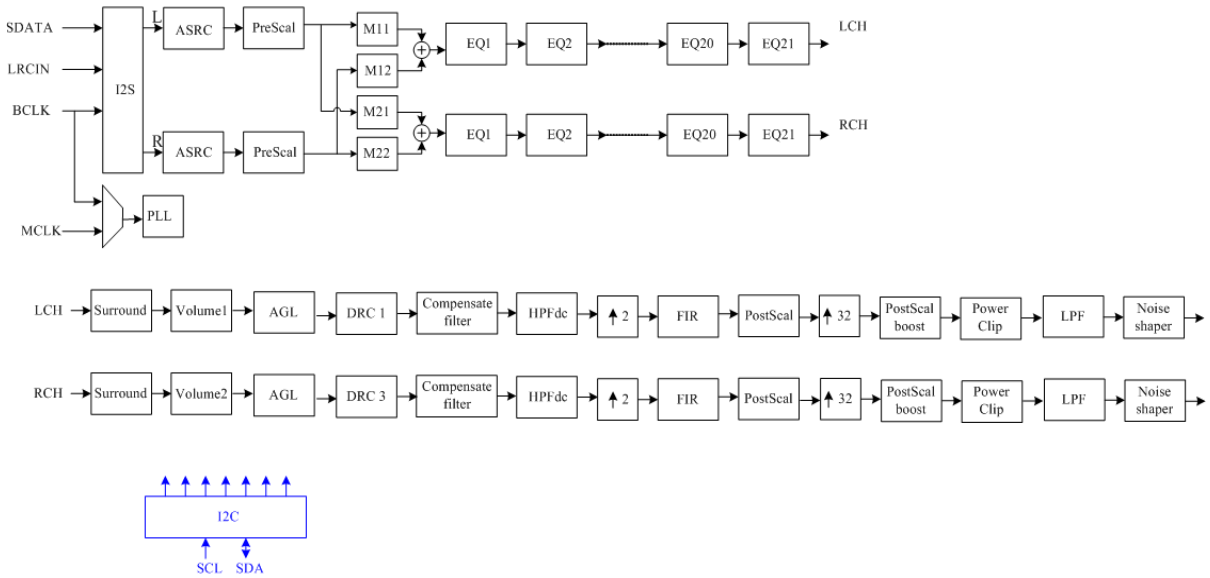
Processing 1:

One band DRC



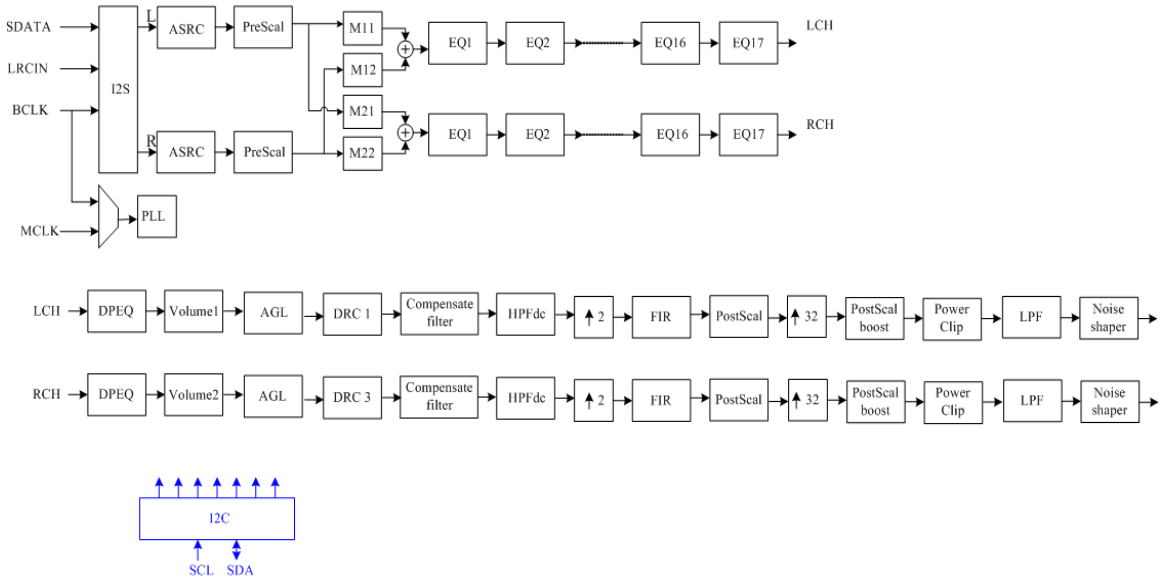
Processing 2:

One band DRC with SRS



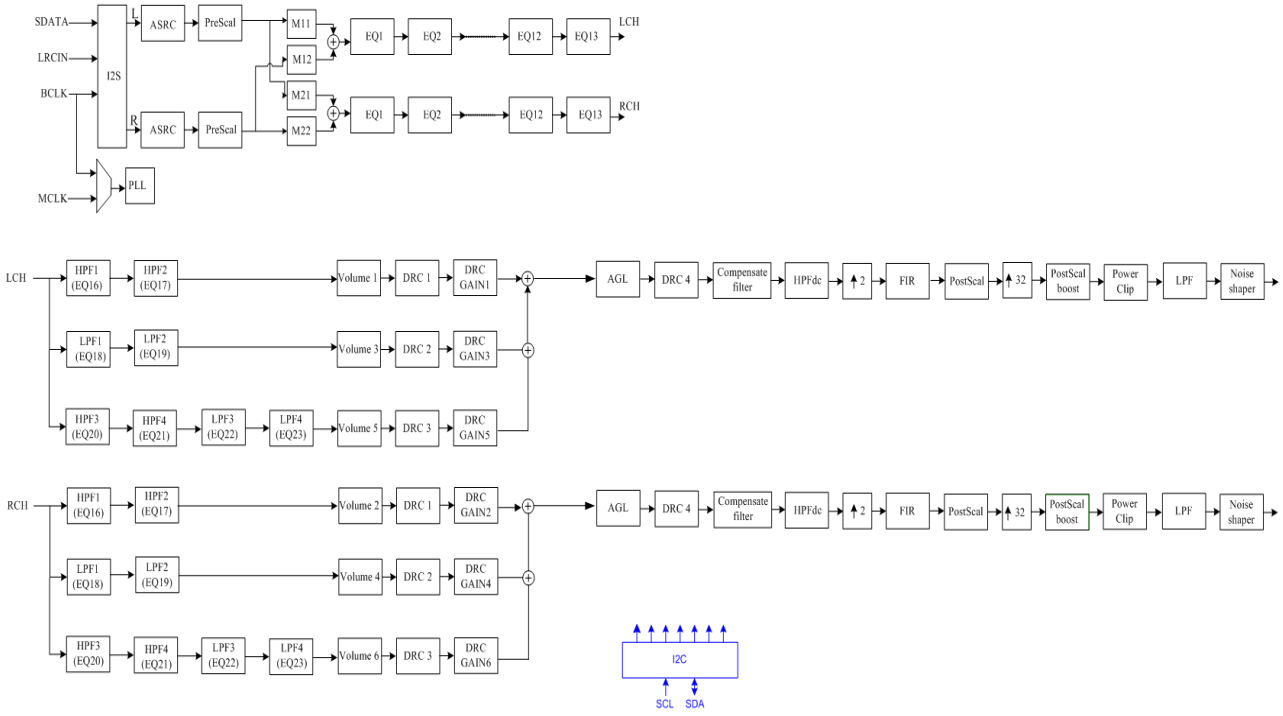
Processing 3:

One band DRC with DPEQ



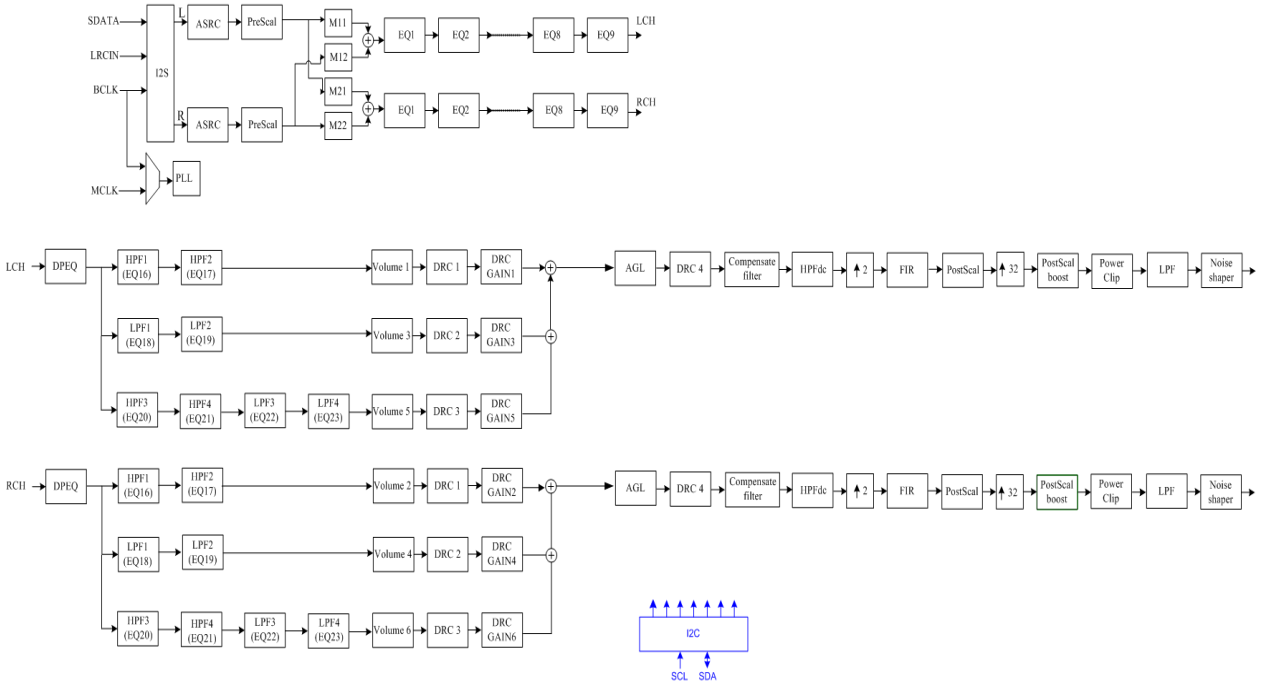
Processing 4:

Three band DRC



Processing 5:

Three band DRC with DPEQ



Register Table

In this section, the register table is summarized first. The definition of each register follows in the next section.

Address	Name	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]
0X00	SCTL1	IF[2]	IF[1]	IF[0]	Reserved	L_INVERSE	R_INVERSE	LV_UVSEL	LREXC
0X01	SCTL2	BCLK_SEL	FS[1]	FS[0]	Reserved	PMF[3]	PMF[2]	PMF[1]	PMF[0]
0X02	SCTL3	Reserved	MUTE	CM1	CM2	CM3	CM4	CM5	CM6
0X03	MVOL	MV[7]	MV[6]	MV[5]	MV[4]	MV[3]	MV[2]	MV[1]	MV[0]
0X04	C1VOL	C1V[7]	C1V[6]	C1V[5]	C1V[4]	C1V[3]	C1V[2]	C1V[1]	C1V[0]
0X05	C2VOL	C2V[7]	C2V[6]	C2V[5]	C2V[4]	C2V[3]	C2V[2]	C2V[1]	C2V[0]
0X06	C3VOL	C3V[7]	C3V[6]	C3V[5]	C3V[4]	C3V[3]	C3V[2]	C3V[1]	C3V[0]
0X07	C4VOL	C4V[7]	C4V[6]	C4V[5]	C4V[4]	C4V[3]	C4V[2]	C4V[1]	C4V[0]
0X08	C5VOL	C5V[7]	C5V[6]	C5V[5]	C5V[4]	C5V[3]	C5V[2]	C5V[1]	C5V[0]
0X09	C6VOL	C6V[7]	C6V[6]	C6V[5]	C6V[4]	C6V[3]	C6V[2]	C6V[1]	C6V[0]
0X0A	DTC	DTC_EN	DTC_TH[1]	DTC_TH[0]	DTC_A_R_rate[1]	DTC_A_R_rate[0]	Reserved	Reserved	Reserved
0X0B	Reserved	Reserved							
0X0C	SCTL4	SRBP	SRS_DLY	COMPEN_EN	NGE	EQL	PSL	CHIP_SYNC_EN	HPB
0X0D	C1CFG	C1DRCGS[1]	C1DRCGS[0]	Reserved		C1PCBP	C1DRCBP	Reserved	C1VBP
0X0E	C2CFG	C2DRCGS[1]	C2DRCGS[0]	Reserved		C2PCBP	C2DRCBP	Reserved	C2VBP
0X0F	C3CFG	C3DRCGS[1]	C3DRCGS[0]	Reserved			C3DRCBP	Reserved	C3VBP
0X10	C4CFG	C4DRCGS[1]	C4DRCGS[0]	Reserved			C4DRCBP	Reserved	C4VBP
0X11	C5CFG	C5DRCGS[1]	C5DRCGS[0]	Reserved			C5DRCBP	Reserved	C5VBP
0X12	C6CFG	C6DRCGS[1]	C6DRCGS[0]	Reserved			C6DRCBP	Reserved	C6VBP
0X13	C7CFG	C7DRCGS[1]	C7DRCGS[0]	Reserved			C7DRCBP	Reserved	
0X14	C8CFG	C8DRCGS[1]	C8DRCGS[0]	Reserved			C8DRCBP	Reserved	
0X15	Reserved	Reserved							
0X16	Reserved	Reserved							
0X17	Reserved	Reserved							
0X18	Reserved	Reserved							
0X19	QT	QT_EN	MODE_LSEL	MODE_RSEL	Reserved				
0X1A	SCTL5	Reserved	MONO_EN	SW_RSTB	LVUV_FADE	DIS_OV_FADE	CKDET_FADE	BSUV_FADE	Reserved
0X1B	SCTL6	DIS_HVUV	Reserved	POST_BOOST	MTDMOC	Reserved	HV_UVSEL [2]	HV_UVSEL [1]	HV_UVSEL [0]
0X1C	SCTL7	PDB_DOPS	A_SEL_FAULT	DEV_NUM	DIS_NG_FADE	FADE_SPEED[1]	FADE_SPEED[0]	NG_GAIN[1]	NG_GAIN[0]
0X1D	CFADDR	CFA[7]	CFA[6]	CFA[5]	CFA[4]	CFA[3]	CFA[2]	CFA[1]	CFA[0]
0X1E	A1CF1	Reserved	Reserved	Reserved	Reserved]	C1B[27]	C1B[26]	C1B[25]	C1B[24]
0X1F	A1CF2	C1B[23]	C1B[22]	C1B[21]	C1B[20]	C1B[19]	C1B[18]	C1B[17]	C1B[16]

0X20	A1CF3	C1B[15]	C1B[14]	C1B[13]	C1B[12]	C1B[11]	C1B[10]	C1B[9]	C1B[8]
0X21	A1CF4	C1B[7]	C1B[6]	C1B[5]	C1B[4]	C1B[3]	C1B[2]	C1B[1]	C1B[0]
0X22	A2CF1	Reserved	Reserved	Reserved	Reserved]	C2B[27]	C2B[26]	C2B[25]	C2B[24]
0X23	A2CF2	C2B[23]	C2B[22]	C2B[21]	C2B[20]	C2B[19]	C2B[18]	C2B[17]	C2B[16]
0X24	A2CF3	C2B[15]	C2B[14]	C2B[13]	C2B[12]	C2B[11]	C2B[10]	C2B[9]	C2B[8]
0X25	A2CF4	C2B[7]	C2B[6]	C2B[5]	C2B[4]	C2B[3]	C2B[2]	C2B[1]	C2B[0]
0X26	B1CF1	Reserved	Reserved	Reserved	Reserved]	C3B[27]	C3B[26]	C3B[25]	C3B[24]
0X27	B1CF2	C3B[23]	C3B[22]	C3B[21]	C3B[20]	C3B[19]	C3B[18]	C3B[17]	C3B[16]
0X28	B1CF3	C3B[15]	C3B[14]	C3B[13]	C3B[12]	C3B[11]	C3B[10]	C3B[9]	C3B[8]
0X29	B1CF4	C3B[7]	C3B[6]	C3B[5]	C3B[4]	C3B[3]	C3B[2]	C3B[1]	C3B[0]
0X2A	B2CF1	Reserved	Reserved	Reserved	Reserved]	C4B[27]	C4B[26]	C4B[25]	C4B[24]
0X2B	B2CF2	C4B[23]	C4B[22]	C4B[21]	C4B[20]	C4B[19]	C4B[18]	C4B[17]	C4B[16]
0X2C	B2CF3	C4B[15]	C4B[14]	C4B[13]	C4B[12]	C4B[11]	C4B[10]	C4B[9]	C4B[8]
0X2D	B2CF4	C4B[7]	C4B[6]	C4B[5]	C4B[4]	C4B[3]	C4B[2]	C4B[1]	C4B[0]
0X2E	A0CF1	Reserved	Reserved	Reserved	Reserved]	C5B[27]	C5B[26]	C5B[25]	C5B[24]
0X2F	A0CF2	C5B[23]	C5B[22]	C5B[21]	C5B[20]	C5B[19]	C5B[18]	C5B[17]	C5B[16]
0X30	A0CF3	C5B[15]	C5B[14]	C5B[13]	C5B[12]	C5B[11]	C5B[10]	C5B[9]	C5B[8]
0X31	A0CF4	C5B[7]	C5B[6]	C5B[5]	C5B[4]	C5B[3]	C5B[2]	C5B[1]	C5B[0]
0X32	CFRW	Reserved	RBS	R3	W3	RA	R1	WA	W1
0X33	SCTL8	Reserved				DRC_SEL	Reserved	DRC_LINK	DPEQE
0X34	SCTL9	Reserved							
0X35	VFT1	MV_FT[1]	MV_FT[0]	C1V_FT[1]	C1V_FT[0]	C2V_FT[1]	C2V_FT[0]	C3V_FT[1]	C3V_FT[0]
0X36	VFT2	C4V_FT[1]	C4V_FT[0]	C5V_FT[1]	C5V_FT[0]	C6V_FT[1]	C6V_FT[0]	Reserved	
0X37	ID	DN[3]	DN[2]	DN[1]	DN[0]	VN[3]	VN[2]	VN[1]	VN[0]
0X38	LMC	C1_CLR	C2_CLR	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0X39	PMC	C1_CLR_RMS	C2_CLR_RMS	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0X3A	1STC1LM	C1_LEVEL[31]	C1_LEVEL[30]	C1_LEVEL[29]	C1_LEVEL[28]	C1_LEVEL[27]	C1_LEVEL[26]	C1_LEVEL[25]	C1_LEVEL[24]
0X3B	2NDC1LM	C1_LEVEL[23]	C1_LEVEL[22]	C1_LEVEL[21]	C1_LEVEL[20]	C1_LEVEL[19]	C1_LEVEL[18]	C1_LEVEL[17]	C1_LEVEL[16]
0X3C	3RDC1LM	C1_LEVEL[15]	C1_LEVEL[14]	C1_LEVEL[13]	C1_LEVEL[12]	C1_LEVEL[11]	C1_LEVEL[10]	C1_LEVEL[9]	C1_LEVEL[8]
0X3D	4THC1LM	C1_LEVEL[7]	C1_LEVEL[6]	C1_LEVEL[5]	C1_LEVEL[4]	C1_LEVEL[3]	C1_LEVEL[2]	C1_LEVEL[1]	C1_LEVEL[0]
0X3E	1STC2LM	C2_LEVEL[31]	C2_LEVEL[30]	C2_LEVEL[29]	C2_LEVEL[28]	C2_LEVEL[27]	C2_LEVEL[26]	C2_LEVEL[25]	C2_LEVEL[24]
0X3F	2NDC2LM	C2_LEVEL[23]	C2_LEVEL[22]	C2_LEVEL[21]	C2_LEVEL[20]	C2_LEVEL[19]	C2_LEVEL[18]	C2_LEVEL[17]	C2_LEVEL[16]
0X40	3RDC2LM	C2_LEVEL[15]	C2_LEVEL[14]	C2_LEVEL[13]	C2_LEVEL[12]	C2_LEVEL[11]	C2_LEVEL[10]	C2_LEVEL[9]	C2_LEVEL[8]
0X41	4THC2LM	C2_LEVEL[7]	C2_LEVEL[6]	C2_LEVEL[5]	C2_LEVEL[4]	C2_LEVEL[3]	C2_LEVEL[2]	C2_LEVEL[1]	C2_LEVEL[0]
0X42	CHK_STAT	CHK_BEQ_F	CHK_ BEQ_AM	CHK_ BEQ _R	CHK_ BEQ _EN	Reserved			
0X43	CHS_BEQ_V	Reserved				CHS_ BEQ_V[27]	CHS_ BEQ_V[26]	CHS_ BEQ_V[25]	CHS_ BEQ_V[24]

0X44	CHS_BEQ_V	CHS_ BEQ_V[23]	CHS_ BEQ_V[22]	CHS_ BEQ_V[21]	CHS_ BEQ_V[20]	CHS_ BEQ_V[19]	CHS_ BEQ_V[18]	CHS_ BEQ_V[17]	CHS_ BEQ_V[16]
0X45	CHS_BEQ_V	CHS_ BEQ_V[15]	CHS_ BEQ_V[14]	CHS_ BEQ_V[13]	CHS_ BEQ_V[12]	CHS_ BEQ_V[11]	CHS_ BEQ_V[10]	CHS_ BEQ_V[9]	CHS_ BEQ_V[8]
0X46	CHS_BEQ_V	CHS_ BEQ_V[7]	CHS_ BEQ_V[6]	CHS_ BEQ_V[5]	CHS_ BEQ_V[4]	CHS_ BEQ_V[3]	CHS_ BEQ_V[2]	CHS_ BEQ_V[1]	CHS_ BEQ_V[0]
0X47	CHS_BEQ_R	Reserved				CHS_ BEQ_R[27]	CHS_ BEQ_R[26]	CHS_ BEQ_R[25]	CHS_ BEQ_R[24]
0X48	CHS_BEQ_R	CHS_ BEQ_R[23]	CHS_ BEQ_R[22]	CHS_ BEQ_R[21]	CHS_ BEQ_R[20]	CHS_ BEQ_R[19]	CHS_ BEQ_R[18]	CHS_ BEQ_R[17]	CHS_ BEQ_R[16]
0X49	CHS_BEQ_R	CHS_ BEQ_R[15]	CHS_ BEQ_R[14]	CHS_ BEQ_R[13]	CHS_ BEQ_R[12]	CHS_ BEQ_R[11]	CHS_ BEQ_R[10]	CHS_ BEQ_R[9]	CHS_ BEQ_R[8]
0X4A	CHS_BEQ_R	CHS_ BEQ_R[7]	CHS_ BEQ_R[6]	CHS_ BEQ_R[5]	CHS_ BEQ_R[4]	CHS_ BEQ_R[3]	CHS_ BEQ_R[2]	CHS_ BEQ_R[1]	CHS_ BEQ_V[0]
0X4B	DCD_CTRL	DC_JUDGE_BYP	DC_ACTIVE_TIME[2]	DC_ACTIVE_TIME[1]	DC_ACTIVE_TIME[0]	Reserved			
0X4C	DC_JUDGE_TH	DC_JUDGE_TH[7]	DC_JUDGE_TH[6]	DC_JUDGE_TH[5]	DC_JUDGE_TH[4]	DC_JUDGE_TH[3]	DC_JUDGE_TH[2]	DC_JUDGE_TH[1]	DC_JUDGE_TH[0]
0X4D	ERR_REG	A_OCP_N	A_OTP_N	A_UV_N	A_DCD_N	A_BSUV_N	A_CKERR_N	A_OVP_N	D_CKERR_N
0X4E	ERR_LATCH	A_OCP_N_LATCH	A_OTP_N__LATCH	A_UV_N__LATCH	A_DCD_N_LATCH	A_BSUV_N_LATCH	A_CKERR_N_LATCH	A_OVP_N_LATCH	D_CKERR_N_LATCH
0X4F	ERR_CLEAR	A_OCP_N_CLEAR	A_OTP_N_CLEAR	A_UV_N_CLEAR	A_DCD_N_CLEAR	A_BSUV_N_CLEAR	A_CKERR_N_CLEAR	A_OVP_N_CLEAR	D_CKERR_CLEAR
0X50	ERR2_REG	Reserved							D_DCD_N
0X51	ERR2_LATCH	Reserved							D_DCD_N_LATCH
0X52	ERR2_CLEAR	Reserved							D_DCD_N_CLEAR
0X53	Reserved	Reserved							
0X54	Reserved	Reserved							
0X55	CK_FS_DET	ASR_ERR	BCLK_FS_RATIO_ERR	MCLK_FS_RATIO_ERR	Reserved				
0X56	CLK_DET	ASR_DET	BCLK_FS_RATIO_DET	MCLK_FS_RATIO_DET	D_CKDET _EN	FS_PMF_AUTO_EN	A_CKDET _EN	CKDET_SEL	RECOUNT_EN
0X57	TDM_W	Reserved						WORD_WIDTH_SEL[1]	WORD_WIDTH_SEL[0]
0X58	TDM_O	TDM_OFFSET[7]	TDM_OFFSET[6]	TDM_OFFSET[5]	TDM_OFFSET[4]	TDM_OFFSET[3]	TDM_OFFSET[2]	TDM_OFFSET[1]	TDM_OFFSET[0]
0X59	I2S_OUT	Reserved				SDATAO_CTRL	I2S_DO_SEL[2]	I2S_DO_SEL[2]	I2S_DO_SEL[2]
0X5A	PWMFREQ	Reserved				SS[1]	SS[0]	FSW[1]	FSW[0]
0X5B	MKHB	MK_HBYTE[7]	MK_HBYTE[6]	MK_HBYTE[5]	MK_HBYTE[4]	MK_HBYTE[3]	MK_HBYTE[2]	MK_HBYTE[1]	MK_HBYTE[0]
0X5C	MKLB	MK_LBYTE[7]	MK_LBYTE[6]	MK_LBYTE[5]	MK_LBYTE[4]	MK_LBYTE[3]	MK_LBYTE[2]	MK_LBYTE[1]	MK_LBYTE[0]
0X5D	HI_RES	Reserved							FIR2_EN
0X5E	ANA_GAIN	Reserved					ANA_GAIN[2]	ANA_GAIN[1]	ANA_GAIN[0]
0X5F	AGL	CH1_AGLEN	CH2_AGLEN	CH1_AGL_SHIFT[1]	CH1_AGL_SHIFT[0]	CH2_AGL_SHIFT[1]	CH2_AGL_SHIFT[0]	Reserved	
0X60	CH1_EQ_BYP1	CH1_EQ1_BYP	CH1_EQ2_BYP	CH1_EQ3_BYP	CH1_EQ4_BYP	CH1_EQ5_BYP	CH1_EQ6_BYP	CH1_EQ7_BYP	CH1_EQ8_BYP
0X61	CH1_EQ_BYP2	CH1_EQ9_BYP	CH1_EQ10_BYP	CH1_EQ11_BYP	CH1_EQ12_BYP	CH1_EQ13_BYP	CH1_EQ14_BYP	CH1_EQ15_BYP	CH1_EQ16_BYP
0X62	CH1_EQ_BYP3	CH1_EQ17_BYP	CH1_EQ18_BYP	CH1_EQ19_BYP	CH1_EQ20_BYP	CH1_EQ21_BYP	CH1_EQ22_BYP	CH1_EQ23_BYP	Reserved
0X63	CH2_EQ_BYP1	CH2_EQ1_BYP	CH2_EQ2_BYP	CH2_EQ3_BYP	CH2_EQ4_BYP	CH2_EQ5_BYP	CH2_EQ6_BYP	CH2_EQ7_BYP	CH2_EQ8_BYP
0X64	CH2_EQ_BYP2	CH2_EQ9_BYP	CH2_EQ10_BYP	CH2_EQ11_BYP	CH2_EQ12_BYP	CH2_EQ13_BYP	CH2_EQ14_BYP	CH2_EQ15_BYP	CH2_EQ16_BYP
0X65	CH2_EQ_BYP3	CH2_EQ17_BYP	CH2_EQ18_BYP	CH2_EQ19_BYP	CH2_EQ20_BYP	CH2_EQ21_BYP	CH2_EQ22_BYP	CH2_EQ23_BYP	Reserved

Detail Description for Register

Note that the highlighted columns are default values of these tables. If there is no highlighted value, the default setting of this bit is determined by the external pin.

- Address 0X00 : State control 1

  AD82128B supports multiple serial data input formats including I^2S, Left-alignment and Right-alignment. These formats are selected by user via bit7~bit5 of address 0X00. The left/right channels can be exchanged to each other by programming to bit0, LREXC.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:5]	IF[2:0]	Input Format	000	I^2S 16-24 bits
			001	Left-alignment 16-24 bits
			010	Right-alignment 16 bits
			011	Right-alignment 18 bits
			100	Right-alignment 20 bits
			101	Right-alignment 24 bits
			110	TDM
B[4]		Reserved		
B[3]	L_INVERSE	L channel signal inverse	0	Normal
			1	Inverse
B[2]	R_INVERSE	R channel signal inverse	0	Normal
			1	Inverse
B[1]	LV_UVSEL	LV under voltage selection	0	1.35V
			1	2.7V
B[0]	LREXC	Left/Right (L/R) Channel exchanged	0	No exchanged
			1	L/R exchanged

- Address 0X01 : State control 2

AD82128B has a built-in PLL and supports multiple BCLK/Fs ratios.

AD82128B can support different sample rate via bit6~5.

Detail setting is shown in the following table.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	BCLK_SEL	MCLK-less (BCLK system)	0	Prohibited
			1	Enable
B[6:5]	FS[1:0]	Sampling Frequency	00	32/44.1/48kHz
			01	64/88.2/96kHz
			10	8kHz
			11	16kHz
B[4]	Reserved	Reserved		

Multiple BCLK/FS in BCLK system ratio setting table,

BIT	NAME	DESCRIPTION	VALUE	B[6:5]=00	B[6:5]=01	B[6:5]=10	B[6:5]=11
B[3:0]	PMF[3:0]	BCLK/Fs Setup	0000	32X	32X	32X	32X
			0001	48X	48X	Reserved	48X
			0010	64X	64X	64X	64X
			0011	96X	96X	96X	96X
			0100	128X	128X	128X	128X
			0101	192X	192X	192X	192X
			0110	256X	256X	256X	256X
			0111	384X	384X	384X	384X
			1000	512X	512X	512X	512X

- Address 0X02 : State control 3

AD82128B has mute function including master mute and channel mute.

In one band DRC, master, channel 1, and channel 2 mute will active.

When master mute is enabled, all 2 processing channels are muted. User can mute these 2 channels individually by channel mute. When the mute function is enabled or disabled, the fade-out or fade-in process will be initiated.

In three bands DRC, master, channel 1 to channel 6 mute will active.

When master mute is enabled, all 6 processing channels are muted. User can mute these 6 channels individually by channel mute. When the mute function is enabled or disabled, the fade-out or fade-in process will be initiated.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	Reserved	Reserved		
B[6]	MMUTE	Master Mute	0	All channel not muted
			1	All channel muted
B[5]	CM1	Channel 1 Mute	0	Ch1 not muted
			1	Only Ch1 muted
B[4]	CM2	Channel 2 Mute	0	Ch2 not muted
			1	Only Ch2 muted
B[3]	CM3	Channel 3 Mute	0	Ch3 not muted
			1	Only Ch3 muted
B[2]	CM4	Channel 4 Mute	0	Ch4 not muted
			1	Only Ch4 muted
B[1]	CM5	Channel 5 Mute	0	Ch5 not muted
			1	Only Ch5 muted
B[0]	CM6	Channel 6 Mute	0	Ch6 not muted
			1	Only Ch6 muted

- Address 0X03 : Master volume control

AD82128B supports both master-volume (Address 0X03) and channel-volume control (Address 0X04, 0X05, 0X06, 0X07, 0X08, 0X09) modes. Both volume control settings range from +12dB ~ -103dB and 0.5dB per step. Note that the master volume control is added to the individual channel volume control as the total volume control. For example, if the master volume level is set at, Level A (in dB unit) and the channel volume level is set at Level B (in dB unit), the total volume control setting is equal to Level A plus with Level B.

-103dB ≦ Total volume (Level A + Level B) ≦ +24dB.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
BIT[7:0]	MV[7:0]	Master Volume	00000000	+12.0dB
			00000001	+11.5dB
			00000010	+11.0dB
			:	:
			00010111	+0.5dB
			00011000	0.0dB
			00011001	-0.5dB
			:	:
			11100110	-103.0dB
			11100111	-∞dB
			:	:
			11111111	-∞dB

- Address 0X04 : Channel 1 volume

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
BIT[7:0]	C1V[7:0]	Channel1 Volume	00000000	+12.0dB
			00000001	+11.5dB
			:	:
			00010100	+2dB
			:	:
			00011000	0.0dB
			00011001	-0.5dB
			:	:
			11100110	-103.0dB
			11100111	-∞dB
			:	:
			11111111	-∞dB

- Address 0X05 : Channel 2 volume

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
BIT[7:0]	C2V[7:0]	Channel2 Volume	00000000	+12.0dB
			00000001	+11.5dB
			:	:
			00010100	+2dB
			:	:
			00011000	0.0dB
			00011001	-0.5dB
			:	:
			11100110	-103.0dB
			11100111	-∞dB
			:	:
			11111111	-∞dB

- Address 0X06 : Channel 3 volume

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
BIT[7:0]	C3V[7:0]	Channel3 Volume	00000000	+12.0dB
			00000001	+11.5dB
			:	:
			00010100	+2dB
			:	:
			00011000	0.0dB
			00011001	-0.5dB
			:	:
			11100110	-103.0dB
			11100111	-∞dB
			:	:
			11111111	-∞dB

- Address 0X07 : Channel 4 volume

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
BIT[7:0]	C4V[7:0]	Channel 4 Volume	00000000	+12.0dB
			00000001	+11.5dB
			:	:
			00010100	+2dB
			:	:
			00011000	0.0dB
			00011001	-0.5dB
			:	:
			11100110	-103.0dB
			11100111	-∞dB
			:	:
			11111111	-∞dB

- Address 0X08 : Channel 5 volume

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
BIT[7:0]	C5V[7:0]	Channel 5 Volume	00000000	+12.0dB
			00000001	+11.5dB
			:	:
			00010100	+2dB
			:	:
			00011000	0.0dB
			00011001	-0.5dB
			:	:
			11100110	-103.0dB
			11100111	-∞dB
			:	:
			11111111	-∞dB

- Address 0X09 : Channel 6 volume

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
BIT[7:0]	C6V[7:0]	Channel 6 Volume	00000000	+12.0dB
			00000001	+11.5dB
			:	:
			00010100	+2dB
			:	:
			00011000	0.0dB
			00011001	-0.5dB
			:	:
			11100110	-103.0dB
			11100111	-∞dB
			:	:
			11111111	-∞dB

- Address 0X0A : DTC setting

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	DTC_EN	DTC enable	0	Disable
			1	Enable
B[6:5]	DTC_TH	DTC threshold	00	110℃
			01	120℃
			10	130℃
			11	140℃
B[4:3]	DTC_A_R_rate	DTC attack and release rate	00	1db/sec
			01	0.5db/sec
			10	0.33db/sec
			11	0.25dB/sec
B[2:0]	Reserved	Reserved		

- Address 0X0C : State control 4

The AD82128B provides several DSP setting as following.

Due the DSP processing bandwidth limitation, surround sound effect doesn't support in 88.2K/96K sample rate.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	SRBP	Surround bypass	0	Surround enable
			1	Surround bypass
B[6]	SRS_dly	Surround Delay	0	No delay
			1	Delay 1 DSP sample point(1/96K)
B[5]	COMPEN_EN	Compensate filter enable	0	Disable
			1	Enable
B[4]	NGE	Noise gate enable	0	Noise gate disable
			1	Noise gate enable
B[3]	EQL	EQ Link	0	Each channel uses individual EQ
			1	Channel-2 uses channel-1 EQ
B[2]	PSL	Post-scale link	0	Each channel uses individual post-scale
			1	Use channel-1 post-scale
B[1]	DSP_SYNC_EN	DSP SYNC enable	0	No SYNC
			1	SYNC
B[0]	HPB	DC blocking HPF bypass	0	HPF dc enable
			1	HPF dc bypass

- Address 0X0D, 0X0E ,0X0F,0X10,0X11,0X12, 0X13,0X14 : Channel configuration registers

  AD82128B can configure each channel to enable or bypass DRC and channel volume and select the limiter set.

Address 0X0D and 0X0E; where x=1 or 2

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:6]	CXDRCGS	Channel X DRC gain step	00	DRC gain step =0.5dB
			01	DRC gain step =0.25dB
			1x	DRC gain step =0.125dB
B[5:4]		Reserved		
B[3]	CxPCBP	Channel x Power Clipping bypass	0	Channel x PC enable
			1	Channel x PC bypass
B[2]	CxDRCBP	Channel x DRC bypass	0	Channel x DRC enable
			1	Channel x DRC bypass
B[1]		Reserved		
B[0]	CxVBP	Channel x Volume bypass	0	Channel x's master volume operation
			1	Channel x's master volume bypass

Address 0X0F, 0X10, 0X11, and 0X12; where x=3, 4, 5, 6

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:6]	CXDRCGS	Channel X DRC gain step	00	DRC gain step =0.5dB
			01	DRC gain step =0.25dB
			1x	DRC gain step =0.125dB
B[5:3]		Reserved		
B[2]	CxDRCBP	Channel x DRC bypass	0	Channel x DRC enable
			1	Channel x DRC bypass
B[1]		Reserved		
B[0]	CxVBP	Channel x Volume bypass	0	Channel x volume operation
			1	Channel x volume bypass

Address 0X13, and 0X14; where x=7 or 8

C7DRCBP/C8DRCBP use to control L/R post DRC.

The gains are internally setting and they can't be changed via I2C control.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:6]	CXDRCGS	Channel X DRC gain step	00	DRC gain step =0.5dB
			01	DRC gain step =0.25dB
			1x	DRC gain step =0.125dB
B[5:3]		Reserved		
B[2]	CxDRCBP	Channel x DRC bypass	0	Channel x DRC enable
			1	Channel x DRC bypass
B[1:0]		Reserved		

- Address 0X19 : QTSEL

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	QT_SEL	Power saving mode	0	Disable
			1	Enable
B[6]	MODE_LSEL	L channel Q and T mode selection	0	Qua-ternary
			1	Ternary
B[5]	MODE_RSEL	R channel Q and T mode selection	0	Qua-ternary
			1	Ternary
B[4:0]	Reserved	Reserved		

- Address 0X1A : State control 5

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	Reserved	Reserved		
B[6]	MONO_EN	MONO enable register	0	Stereo
			1	MONO_EN=1 and MONO_KEY=3006(hex) Output will become mono
B[5]	SW_RSTB	Software reset	0	Reset
			1	Normal operation
B[4]	LVUV_FADE	Low Under Voltage Fade	0	No Fade
			1	Fade
B[3]	DIS_OV_FADE	Disable over voltage fade	0	Fade
			1	No fade
B[2]	CKDET_FADE	CKDET fade setting	0	Direct off
			1	Fade when no clock
B[1]	BSUV_FADE	Fade when boost strap under voltage occur	0	No fade
			1	Fade
B[0]		Reserved		

- Address 0X1B : State control 6

AD82128B can disable HV under voltage detection via bit 7.

AD82128B support multi-level HV under voltage detection via bit2~ bit0, using this function, AD82128B will fade out signal to avoid pop sounds if high voltage supply disappear before low voltage supply.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	DIS_HVUV	Disable HV under voltage selection	0	Enable
			1	Disable
B[6]		Reserved		
B[5]	POST_BOOST	POST boost +48dB	0	0dB
			1	+48dB
B[4]	MTDMOC	Multi TDM Output Connection	0	Disable
			1	Enable
B[3]		Reserved		
B[2:0]	HV_UV SEL	UV detection level	000	4V
			001	8.2V
			010	9.7 V
			011	13.2V
			100	15.5 V
			101	19.5 V
			Others	7.2V

- Address 0X1C: State control 7

The $\overline{\text{ERROR}}$ pin of AD82128B is a dual function pin. It is treated as a I^2C device address selection input when B[6] is set as low. It will become as an ERROR output pin when B[6] is set as high.

AD82128B supports 2 device address and 4 device address selection via bit 5. AD82128B provide 4 kind of fade in/out speed via bit 3~2.

AD82128B provide noise gate function if receiving 2048 signal sample points smaller than noise gate attack level. User can change noise gate gain via bit1~ bit0. When noise gate function occurs, input signal will multiply noise gate gain (x1/8, x1/4 x1/2, x0). User can select fade out or not via bit 4.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	PDB_DOPS	PDB Direct Off Power stage	0	Fade out when PD
			1	Power stage direct off when PD
B[6]	A_SEL_FAULT	I^2C address selection or ERROR output	0	I^2C device address selection
			1	ERROR output
B[5]	DEV_NUM	Device address number for I^2C	0	2 address
			1	4 address
B[4]	DIS_NG_FADE	Disable noise gate fade	0	Fade
			1	No fade
B[3:2]	FADE_SPEED	Fade in/out speed selection	00	1.25ms
			01	5ms
			10	10ms
			11	20ms
B[1:0]	NG_GAIN[1:0]	Noise gate gain	00	x1/8
			01	x1/4
			10	x1/2
			11	Mute

- Address 0X1D ~0X32 : User-defined coefficients registers

An on-chip RAM in AD82128B stores user-defined EQ, mixing, pre-scale, post-scale coefficients…etc. The content of this coefficient RAM is indirectly accessed via coefficient registers, which consist of one base address register (address 0X1D), five sets of registers (address 0X1E to 0X31) of four consecutive 8-bit entries for each 28-bit coefficient, and one control register (address 0X32) to control access of the coefficients in the RAM..

Address 0X1D

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	CFA[7:0]	Coefficient RAM base address	00000000	

Address 0X1E, A1cf1

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:4]		Reserved		
B[3:0]	C1B[27:24]	First 4-bits of coefficients A1		

Address 0X1F, A1cf2

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C1B[23:16]	Second byte of coefficients A1		

Address 0X20, A1cf3

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C1B[15:8]	Third byte of coefficients A1		

Address 0X21, A1cf4

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C1B[7:0]	Fourth byte of coefficients A1		

Address 0X22, A2cf1

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:4]		Reserved		
B[3:0]	C2B[27:24]	First 4-bits of coefficients A2		

Address 0X23, A2cf2

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C2B[23:16]	Second byte of coefficients A2		

Address 0X24, A2cf3

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C2B[15:8]	Third byte of coefficients A2		

Address 0X25, A2cf4

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C2B[7:0]	Fourth byte of coefficients A2		

Address 0X26, B1cf1

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:4]		Reserved		
B[3:0]	C3B[27:24]	First 4-bits of coefficients B1		

Address 0X27, B1cf2

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C3B[23:16]	Second byte of coefficients B1		

Address 0X28, B1cf3

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C3B[15:8]	Third byte of coefficients B1		

Address 0X29, B1cf4

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C3B[7:0]	Fourth byte of coefficients B1		

Address 0X2A, B2cf1

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:4]		Reserved		
B[3:0]	C4B[27:24]	First 4-bits of coefficients B2		

Address 0X2B, B2cf2

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C4B[23:16]	Second byte of coefficients B2		

Address 0X2C, B2cf3

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C4B[15:8]	Third byte of coefficients B2		

Address 0X2D, B2cf4

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C4B[7:0]	Fourth byte of coefficients B2		

Address 0X2E, A0cf1

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:4]		Reserved		
B[3:0]	C5B[27:24]	First 4-bits of coefficients A0		

Address 0X2F, A0cf2

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C5B[23:16]	Second byte of coefficients A0		

Address 0X30, A0cf3

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C5B[15:8]	Third byte of coefficients A0		

Address 0X31, A0cf4

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C5B[7:0]	Fourth byte of coefficients A0		

Address 0X32, CfRW

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]		Reserved		
B[6]	RBS	RAM bank selection	0	Select RAM bank 0
			1	Select RAM bank 1
B[5]	R3	Enable of reading three coefficients from RAM	0	Read complete
			1	Read enable
B[4]	W3	Enable of writing three coefficients to RAM	0	Write complete
			1	Write enable
B[3]	RA	Enable of reading a set of coefficients from RAM	0	Read complete
			1	Read enable
B[2]	R1	Enable of reading a single coefficients from RAM	0	Read complete
			1	Read enable
B[1]	WA	Enable of writing a set of coefficients to RAM	0	Write complete
			1	Write enable
B[0]	W1	Enable of writing a single coefficient to RAM	0	Write complete
			1	Write enable

- Address 0X33 : State control 8

AD82128B can support one band and three band DRC selection via bit3.

In one band DRC mode, CH1 and CH2 DRC threshold are the same via setting bit1, DRC_LINK as 1, and CH1 and CH2 can have different DRC threshold via setting bit1 as 0.

DPEQ (Dynamic Parametric Equalizer), is an audio processing technique that employs two distinct signal paths for audio mixing: a low-level path and a high-level path. Each of these paths is subjected to separate equalization settings. Additionally, a third path analyzes the incoming audio, determining thresholds and blending characteristics to mix between the low and high-level paths.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:4]		Reserved		
B[3]	DRC_SEL	DRC mode selection	0	One band DRC
			1	Three band DRC
B[2]		Reserved		
B[1]	DRC_LINK	One band DRC link	0	1.1 application
			1	Stereo application
B[0]	DPEQE	DPEQ enable	0	Disable
			1	Enable

- Address 0X35/0X36: Volume fine tune

AD82128B supports both master-volume fine tune and channel-volume control fine tune modes. Both volume control settings range from 0dB ~ -0.375dB and 0.125dB per step. Note that the master volume fine tune is added to the individual channel volume fine tune as the total volume fine tune.

Address 0X35

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:6]	MV_FT	Master Volume Fine Tune	00	0dB
			01	-0.125dB
			10	-0.25dB
			11	-0.375dB
B[5:4]	C1V_FT	Channel 1 Volume Fine Tune	00	0dB
			01	-0.125dB
			10	-0.25dB
			11	-0.375dB
B[3:2]	C2V_FT	Channel 2 Volume Fine Tune	00	0dB
			01	-0.125dB
			10	-0.25dB
			11	-0.375dB
B[1:0]	C3V_FT	Channel 3 Volume Fine Tune	00	0dB
			01	-0.125dB
			10	-0.25dB
			11	-0.375dB

Address 0X36

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:6]	C4V_FT	Channel 4 Volume Fine Tune	00	0dB
			01	-0.125dB
			10	-0.25dB
			11	-0.375dB
B[5:4]	C5V_FT	Channel 5 Volume Fine Tune	00	0dB
			01	-0.125dB
			10	-0.25dB
			11	-0.375dB
B[3:2]	C6V_FT	Channel 6 Volume Fine Tune	00	0dB
			01	-0.125dB
			10	-0.25dB
			11	-0.375dB
B[1:0]		Reserved		

- Address 0X37 : Device number and Version number

  Device number and version number are the ID for the device.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:4]	DN	Device number	1010	Identification code
B[3:0]	VN	Version number	0000	Identification code

- Address 0X38 : level meter clear

  AD82128B has 2 set of level meter which hold the maximum absolute value.

  Each level meter has its own level meter clear.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	C1_CLR	Clear CH1 level meter	0	No clear
			1	Clear
B[6]	C2_CLR	Clear CH2 level meter	0	No clear
			1	Clear
B[5:0]		Reserved		

- Address 0X39 : Power meter clear

  AD82128B has 2 set of power meter which continue update peak value.

  Each power meter has its own power meter clear.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	C1_CLR_RMS	Clear CH1 power meter	0	No clear
			1	Clear
B[6]	C2_CLR_RMS	Clear CH2 power meter	0	No clear
			1	Clear
B[5:0]		Reserved		

- Address 0X3A : First byte of C1 level meter

  In one band DRC, channel-1 level meter is used for L channel.

  In three bands DRC, channel-1 level meter is all frequency path of L channel.

  The addresses to show channel-1 level meter are 0X3A, 0X3B, 0X3C, and 0X3D.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C1_LEVEL[31:24]	First byte of channel 1 level meter	0000000	Reset value
			X	Read out

- Address 0X3B : Second byte of C1 level meter

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C1_LEVEL[23:16]	Second byte of channel 1 level meter	0000000	Reset value
			X	Read out

- Address 0X3C : Third byte of C1 level meter

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C1_LEVEL[15:8]	Third byte of channel 1 level meter	0000000	Reset value
			X	Read out

- Address 0X3D : Fourth byte of C1 level meter

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C1_LEVEL[7:0]	Fourth byte of channel 1 level meter	0000000	Reset value
			X	Read out

- Address 0X3E : First byte of C2 level meter

  In one band DRC, channel-2 level meter is used for R channel.

  In three bands DRC, channel-2 level meter is high frequency path of R channel.

  The addresses to show channel-2 level meter are 0X3E, 0X3F, 0X40, and 0X41.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C2_LEVEL[31:24]	First byte of channel 2 level meter	0000000	Reset value
			X	Read out

- Address 0X3F : Second byte of C2 level meter

  In one band DRC, channel-2 level meter is used for R channel.

  In two/three bands DRC, channel-2 level meter is high frequency path of R channel.

  The addresses to show channel-2 level meter are 0X47, 0X48, and 0X49.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C2_LEVEL[23:16]	Second byte of channel 2 level meter	0000000	Reset value
			X	Read out

- Address 0X40 : Third byte of C2 level meter

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C2_LEVEL[15:8]	Third byte of channel 2 level meter	0000000	Reset value
			X	Read out

- Address 0X41 : Fourth byte of C2 level meter

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C2_LEVEL[7:0]	Fourth byte of channel 2 level meter	0000000	Reset value
			X	Read out

- Address 0X42 : CHK_stat

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	CHK_BEQ_F	FAULT link BEQ_CHK	0	No link
			1	Fault link
B[6]	CHK_BEQ_AM	Auto MUTE BEQ_CHK	0	Disable
			1	Enable
B[5]	CHK_BEQ_R	Result BEQ_CHK	0	No error
			1	Error occurred
B[4]	CHK_BEQ_EN	Enable BEQ_CHK	0	Disable
			1	Enable
B[3:0]	Reserved	Reserved		

- Address 0X43 : First 4 bits of BEQ_CHK set value

The addresses to show BEQ_CHK set value are 0X43, 0X44, 0X45, and 0X46

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:4]	Reserved	Reserved		
B[3:0]	CHS_BEQ_V[27:24]	First 4-bits of BEQ_CHK set value	0000000	Initial value
			X	Set value

- Address 0X44 : Second byte of BEQ_CHK set value

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	CHS_BEQ_V [23:16]	Second byte of BEQ_CHK set value	0000000	Initial value
			X	Set value

- Address 0X45 : Third byte of BEQ_CHK set value

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	CHS_BEQ_V [15:8]	Third byte of BEQ_CHK set value	0000000	Initial value
			X	Set value

- Address 0X46 : Fourth byte of BEQ_CHK set value

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	CHS_BEQ_V [8:0]	Fourth byte of BEQ_CHK set value	0000000	Initial value
			X	Set value

- Address 0X47 : First 4 bits of BEQ_CHK result

The addresses to show BEQ_CHK result are 0X47, 0X48, 0X49, and 0X4A

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:4]	Reserved	Reserved		
B[3:0]	CHS_BEQ_R[27:24]	First 4-bits of BEQ_CHK result	0000000	Initial value
			X	Set value

- Address 0X48 : Second byte of BEQ_CHK result

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	CHS_BEQ_R [23:16]	Second byte of BEQ_CHK result	0000000	Initial value
			X	Set value

- Address 0X49 : Third byte of BEQ_CHK result

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:4]	Reserved	Reserved		
B[3:0]	CHS_BEQ_R[15:8]	First 4-bits of BEQ_CHK result	0000000	Initial value
			X	Set value

- Address 0X4A : Fourth byte of BEQ_CHK result

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	CHS_BEQ_R [7:0]	Second byte of BEQ_CHK result	0000000	Initial value
			X	Set value

- Address 0X4B: digital DC control

AD82128B has dc detection circuit to protect the speakers from DC current which might from input signal. The detection circuit detects from the amplifier output stage, when both differential output voltage higher than the threshold voltage more than active time, the DC detector will alarm and report to $\overline{\text{ERROR}}$ pin.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	DC_JUDGE_BYP	DC judge bypass	0	Enable
			1	Bypass
B[6:4]	DC_ACTIVE_TIME	DC detectionactive time	000	167.8ms
			001	335.6ms
			010	503.4ms
			011	671.2ms
			100	839ms
			101	1006.8ms
			110	1174.6ms
			111	1174.6ms
B[3:0]	Reserved	Reserved		

- Address 0X4C: digital DC judge threshold

The DC threshold voltage is can be programmed, the threshold voltage is PVDD*DUTY.

DUTY=10^{[20*log(DC_JUGDE_TH/256)+2.5]/20}

Default duty=10^{[20*(32/256)+2.5]/20}=0.167

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[6:4]	DC_JUDGE_TH	DC judge threshold	00000000	167.8ms
			00000001	335.6ms
			00000010	503.4ms
			00000011	671.2ms
			…	…
			00100000	-18dB (PVDD=18V,DC=3V)
			…	…
			11111100	-0.13dB
			11111101	-0.1dB
			11111110	-0.06dB
			11111111	-0.03dB

- Address 0X4D : Protection register

The protection registers will show what kind of protection occurs.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	A_OCP_N	OCP register	0	OC occur
			1	Normal
B[6]	A_OTP_N	OTP register	0	OT occur
			1	Normal
B[5]	A_UV_N	UV register	0	UV occur
			1	Normal
B[4]	A_DCD_N	DCD register	0	DCD occur
			1	Normal
B[3]	A_BSUV_N	BSUV register	0	BSUV occur
			1	Normal
B[2]	A_CKERR_N	CKERR register	0	CKERR occur
			1	Normal
B[1]	A_OVP_N	OVP register	0	OV occur
			1	Normal

B[0]	D_CKERR_N	CKERR register	0	Digital CKERR occur
			1	Normal

- Address 0X4E : Protection latch register

The protection registers will show what kind of protection ever occurred.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	A_OCP_N_LATCH	OCP latch register	0	OC ever occur
			1	Normal
B[6]	A_OTP_N_LATCH	OTP latch register	0	OT ever occur
			1	Normal
B[5]	A_UV_N_LATCH	UV latch register	0	UV ever occur
			1	Normal
B[4]	A_DCD_N_LATCH	DCD latch register	0	DCD ever occur
			1	Normal
B[3]	A_BSUV_N_LATCH	BSUV latch register	0	BSUV ever occur
			1	Normal
B[2]	A_CKERR_N_LATCH	CKERR latch register	0	CKERR ever occur
			1	Normal
B[1]	A_OVP_N_LATCH	OVP latch register	0	OV ever occur
			1	Normal
B[0]	D_CKERR_N_LATCH	Digital CKERR latch register	0	Digital CKERR ever occur
			1	Normal

- Address 0X4F : Protection latch clear register

The protection latch clear registers will show what kind of protection ever occurred.

Using the protection latch clear registers can clear the corresponding protection latch registers.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	A_OCP_N_CLEAR	OCP latch clear register	0	No clear
			1	Clear
B[6]	A_OTP_N_CLEAR	OTP latch clear register	0	No clear
			1	Clear
B[5]	A_UV_N_CLEAR	UV latch clear register	0	No clear
			1	Clear
B[4]	A_ DCD_N _CLEAR	DCD latch clear register	0	No clear
			1	Clear
B[3]	A_ BSUV _N _CLEAR	BSUV latch clear register	0	No clear
			1	Clear
B[2]	A_CKERR_N_CLEAR	CKERR latch clear register	0	No clear
			1	Clear
B[1]	A_OVP_N_CLEAR	OVP latch clear register	0	No clear
			1	Clear
B[0]	D_CKERR_CLEAR	Digital CLCOK ERROR latch clear register	0	No clear
			1	Clear

- Address 0X50 : Protection register 2

The protection registers will show what kind of protection occurs.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:1]	reserved	reserved		
B[0]	D_DCD_N	D_DCD register	0	Digital DC occur
			1	Normal

- Address 0X51 : Protection latch register 2

The protection registers will show what kind of protection ever occurred.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:1]	reserved	reserved		
B[0]	D_DCD_N_LATCH	Digital DC detection latch register	0	Digital DC ever occur
			1	Normal

- Address 0X52 : Protection latch clear register 2

The protection latch clear registers will show what kind of protection ever occurred.

Using the protection latch clear registers can clear the corresponding protection latch registers.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:1]	reserved	reserved		
B[0]	D_DCD_N_CLEAR	Digital DC detection latch clear register	0	No clear
			1	Clear

- Address 0X55 : clock and FS detection

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	ASR_ERR	Auto sample rate detection error	0	Normal
			1	FS ERROR
B[6]	BCLK_FS_RATIO_ERR	BCLK/FS ratio error	0	Normal
			1	BCLK/FS ratio ERROR
B[5]	MCLK_FS_RATIO_ERR	MCLK/FS ratio error	0	Normal
			1	MCLK/FS ratio ERROR
B[4:0]	Reserved	Reserved		

- Address 0X56 : CLK_DET

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	ASR_DET	Auto sample rate detection	0	Disable
			1	Enable
B[6]	BCLK_FS_RATIO_DET	Bit Clock/FS Ratio detection	0	Disable
			1	Enable
B[5]	MCLK_FS_RATIO_DET	Master Clock/FS Ratio detection	0	Disable
			1	Enable
B[4]	D_CKDET _EN	Digital Clock detection	0	Disable
			1	Enable
B[3]	FS_PMF_AUTO_EN	sample rate and PMF auto change enable	0	Disable
			1	Enable
B[2]	A_CKDET _EN	Analog Clock detection	0	Disable
			1	Enable
B[1]	CKDET_SEL	Select A_CKDET or D_CKDET	0	D_CKDET
			1	A_CKDET
B[0]	RECOUNT_EN	ASRC RECOUNT EN	0	Disable
			1	Enable

- Address 0X57 : TDM word length selection

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:2]		Reserved		
B[1:0]	WORD_WIDTH_SEL	TDM word length selection	00	32 bits
			01	24 bits
			10	20 bits
			11	16 bits

- Address 0X58 : TDM offset

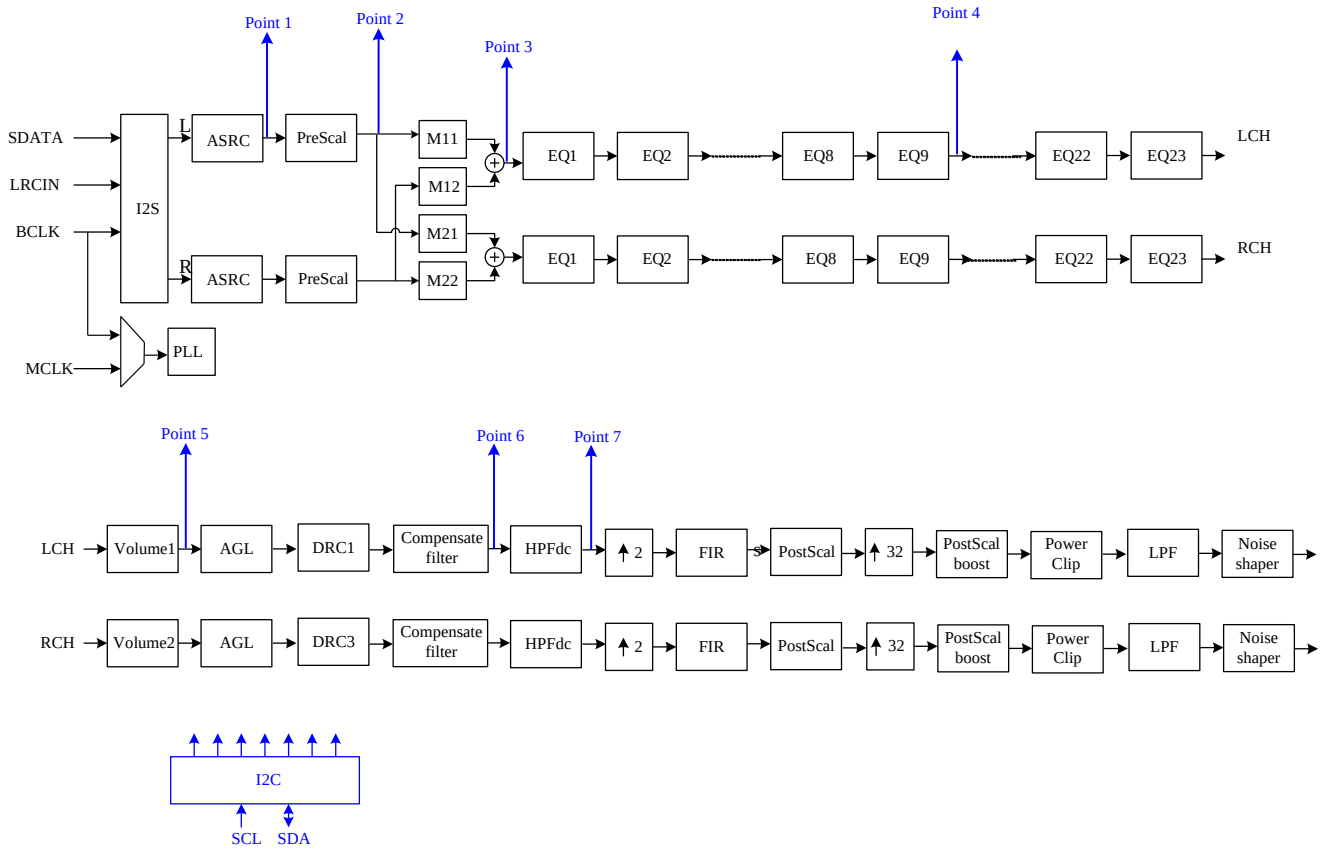
These bits control the offset of audio data in the audio frame for both input and output. The offset is defined as the number of BCLK from the starting (MSB) of audio frame to the starting of the desired audio sample

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	TDM_OFFSET	TDM offset bits	00000000	Offset is 0 BCLK
			00000001	Offset is 1 BCLK
			00000010	Offset is 2 BCLK
			…	
			11111101	Offset is 253 BCLK
			11111110	Offset is 254 BCLK
			11111111	Offset is 255 BCLK

- Address 0X59 : I^2S output selection

AD82128B provide I^2S output function and the output point.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:4]		Reserved		
B[3]	SDATAO_CTRL	SDTATO pin control	0	GND
			1	SDATAO
B[2:0]	I2S_DO_SEL	I2S DATA OUTPUT selection	000	ASRC output (Point1)
			001	Pre-scale output (Point2)
			010	Mixer output (Point3)
			011	EQ9 output (Point4)
			100	Volume output (Point5)
			101	Compensate filter output (Point6)
			110	DC blocking HPF output (Point7)
			111	Reserved



- Address 0X5A : Filter-less selection and PWM frequency selection

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:4]		Reserved		
B[3:2]	Filterless_SEL	EMI enhancement	00	Disabled
			01	Prohibited
			10	Enable
			11	Prohibited
B[1:0]	FSW	PWM frequency selection	00	384KHZ
			01	600KHZ
			10	850KHz
			11	Reserved

- Address 0X5B : MONO_KEY high byte

  AD82128B doesn't have PBTL pin. It needs to set MONO_EN=1 & MONO_KEY=3006 (hex) to configure MONO type.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	MK_HBYTE	MONO KEY high byte	others	Stereo
			00110000	Mono

- Address 0X5C : MONO_KEY low byte

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	MK_LBYTE	MONO KEY low byte	others	Stereo
			00000110	Mono

- Address 0X5D : Wide Band Setting Register

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:1]		Reserved		
B[0]	FIR2_EN	Enable FIR2	0	Disabled
			1	Enable

- Address 0X5E : Analog gain

AD82128B provide several analog gain for different voltage application.

For 18V application, setting +13dB is suggested.

For 15V application, setting +11.5dB is suggested.

For 12V application, setting +9.5dB is suggested.

For 10V application, setting +8dB is suggested.

For 8V application, setting +6dB is suggested.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:3]		Reserved		
B[2:0]	ANA_GAIN	Analog gain control	000	X6(+15.5dB)
			001	X5(+14dB)
			010	X4.5(+13dB)
			011	X3.75(+11.5dB)
			100	X3(+9.5dB)
			101	X2.5(+8dB)
			110	X2(+6dB)
			111	X1.15(1.21dB)

- Address 0X5F : AGL control

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	CH1_AGLEN	Channel 1 AGL enable	0	Disable
			1	Enable
B[6]	CH2_AGLEN	Channel 2 AGL enable	0	Disable
			1	Enable
B[5:4]	CH1_AGL_SHIFT	Channel 1 AGL shift	00	0.125dB
			01	0.25dB
			10	0.5dB
			11	1dB
B[3:2]	CH2_AGL_SHIFT	Channel 2 AGL shift	00	0.125dB
			01	0.25dB
			10	0.5dB
			11	1dB
B[1:0]		Reserved		

- Address 0X60 : Channel1 EQ bypass byte 1

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	CH1_EQ1_BYP	Channel 1 EQ1 Bypass	0	Enable
			1	Bypass
B[6]	CH1_EQ2_BYP	Channel 1 EQ2 Bypass	0	Enable
			1	Bypass
B[5]	CH1_EQ3_BYP	Channel 1 EQ3 Bypass	0	Enable
			1	Bypass
B[4]	CH1_EQ4_BYP	Channel 1 EQ4 Bypass	0	Enable
			1	Bypass
B[3]	CH1_EQ5_BYP	Channel 1 EQ5 Bypass	0	Enable
			1	Bypass
B[2]	CH1_EQ6_BYP	Channel 1 EQ6 Bypass	0	Enable
			1	Bypass
B[1]	CH1_EQ7_BYP	Channel 1 EQ7 Bypass	0	Enable
			1	Bypass
B[0]	CH1_EQ8_BYP	Channel 1 EQ8 Bypass	0	Enable
			1	Bypass

- Address 0X61 : Channel1 EQ bypass byte 2

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	CH1_EQ9_BYP	Channel 1 EQ9 Bypass	0	Enable
			1	Bypass
B[6]	CH1_EQ10_BYP	Channel 1 EQ10 Bypass	0	Enable
			1	Bypass
B[5]	CH1_EQ11_BYP	Channel 1 EQ11 Bypass	0	Enable
			1	Bypass
B[4]	CH1_EQ12_BYP	Channel 1 EQ12 Bypass	0	Enable
			1	Bypass
B[3]	CH1_EQ13_BYP	Channel 1 EQ13 Bypass	0	Enable
			1	Bypass
B[2]	CH1_EQ14_BYP	Channel 1 EQ14 Bypass	0	Enable
			1	Bypass
B[1]	CH1_EQ15_BYP	Channel 1 EQ15 Bypass	0	Enable
			1	Bypass

B[0]	CH1_EQ16_BYP	Channel 1 EQ16 Bypass	0	Enable
			1	Bypass

- Address 0X62 : Channel1 EQ bypass byte 3

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	CH1_EQ17_BYP	Channel 1 EQ17 Bypass	0	Enable
			1	Bypass
B[6]	CH1_EQ18_BYP	Channel 1 EQ18 Bypass	0	Enable
			1	Bypass
B[5]	CH1_EQ19_BYP	Channel 1 EQ19 Bypass	0	Enable
			1	Bypass
B[4]	CH1_EQ20_BYP	Channel 1 EQ20 Bypass	0	Enable
			1	Bypass
B[3]	CH1_EQ21_BYP	Channel 1 EQ21 Bypass	0	Enable
			1	Bypass
B[2]	CH1_EQ22_BYP	Channel 1 EQ22 Bypass	0	Enable
			1	Bypass
B[1]	CH1_EQ23_BYP	Channel 1 EQ23 Bypass	0	Enable
			1	Bypass
B[0]	Reserved	Reserved		

- Address 0X63 : Channel2 EQ bypass byte 1

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	CH2_EQ1_BYP	Channel 2 EQ1 Bypass	0	Enable
			1	Bypass
B[6]	CH2_EQ2_BYP	Channel 2 EQ2 Bypass	0	Enable
			1	Bypass
B[5]	CH2_EQ3_BYP	Channel 2 EQ3 Bypass	0	Enable
			1	Bypass
B[4]	CH2_EQ4_BYP	Channel 2 EQ4 Bypass	0	Enable
			1	Bypass
B[3]	CH2_EQ5_BYP	Channel 2 EQ5 Bypass	0	Enable
			1	Bypass
B[2]	CH2_EQ6_BYP	Channel 2 EQ6 Bypass	0	Enable
			1	Bypass

B[1]	CH2_EQ7_BYP	Channel 2 EQ7 Bypass	0	Enable
			1	Bypass
B[0]	CH2_EQ8_BYP	Channel 2 EQ8 Bypass	0	Enable
			1	Bypass

- Address 0X64 : Channel2 EQ bypass byte 2

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	CH2_EQ9_BYP	Channel 2 EQ9 Bypass	0	Enable
			1	Bypass
B[6]	CH2_EQ10_BYP	Channel 2 EQ10 Bypass	0	Enable
			1	Bypass
B[5]	CH2_EQ11_BYP	Channel 2 EQ11 Bypass	0	Enable
			1	Bypass
B[4]	CH2_EQ12_BYP	Channel 2 EQ12 Bypass	0	Enable
			1	Bypass
B[3]	CH2_EQ13_BYP	Channel 2 EQ13 Bypass	0	Enable
			1	Bypass
B[2]	CH2_EQ14_BYP	Channel 2 EQ14 Bypass	0	Enable
			1	Bypass
B[1]	CH2_EQ15_BYP	Channel 2 EQ15 Bypass	0	Enable
			1	Bypass
B[0]	CH2_EQ16_BYP	Channel 2 EQ16 Bypass	0	Enable
			1	Bypass

- Address 0X65 : Channel2 EQ bypass byte 3

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	CH2_EQ17_BYP	Channel 2 EQ17 Bypass	0	Enable
			1	Bypass
B[6]	CH2_EQ18_BYP	Channel 2 EQ18 Bypass	0	Enable
			1	Bypass
B[5]	CH2_EQ19_BYP	Channel 2 EQ19 Bypass	0	Enable
			1	Bypass
B[4]	CH2_EQ20_BYP	Channel 2 EQ20 Bypass	0	Enable
			1	Bypass
B[3]	CH2_EQ21_BYP	Channel 2 EQ21 Bypass	0	Enable

			1	Bypass
B[2]	CH2_EQ22_BYP	Channel 2 EQ22 Bypass	0	Enable
			1	Bypass
B[1]	CH2_EQ23_BYP	Channel 2 EQ23 Bypass	0	Enable
			1	Bypass
B[0]	Reserved	Reserved		

RAM access

The procedure to read/write coefficient(s) from/to RAM is as followings:

Read a single coefficient from RAM:

1. Write 7-bis of address to I^2C address-0X1D
2. Write 1 to R1 bit and write 1/0 to RBS in address-0X32
3. Read first byte of coefficient in I^2C address-0X1E
4. Read second byte of coefficient in I^2C address-0X1F
5. Read third byte of coefficient in I^2C address-0X20
6. Read fourth byte of coefficient in I^2C address-0X20

Read a set of coefficients from RAM:

1. Write 7-bits of address to I^2C address-0X1D
2. Write 1 to RA bit and write 1/0 to RBS in address-0X32
3. Read first byte of coefficient A1 in I^2C address-0X1E
4. Read second byte of coefficient A1in I^2C address-0X1F
5. Read third byte of coefficient A1 in I^2C address-0X20
6. Read fourth byte of coefficient A1 in I^2C address-0X21
7. Read first byte of coefficient A2 in I^2C address-0X22
8. Read second byte of coefficient A2 in I^2C address-0X23
9. Read third byte of coefficient A2 in I^2C address-0X24
10. Read fourth byte of coefficient A2 in I^2C address-0X25
11. Read first byte of coefficient B1 in I^2C address-0X26
12. Read second byte of coefficient B1 in I^2C address-0X27
13. Read third byte of coefficient B1 in I^2C address-0X28
14. Read fourth byte of coefficient B1 in I^2C address-0X29
15. Read first byte of coefficient B2 in I^2C address-0X2A
16. Read second byte of coefficient B2 in I^2C address-0X2B
17. Read third byte of coefficient B2 in I^2C address-0X2C
18. Read fourth byte of coefficient B2 in I^2C address-0X2D
19. Read first byte of coefficient A0 in I^2C address-0X2E
20. Read second byte of coefficient A0 in I^2C address-0X2F
21. Read third byte of coefficient A0 in I^2C address-0X30
22. Read fourth byte of coefficient A0 in I^2C address-0X31

Write a single coefficient from RAM:

1. Write 7-bis of address to I^2C address-0X1D
2. Write first byte of coefficient in I^2C address-0X1E
3. Write second byte of coefficient in I^2C address-0X1F
4. Write third byte of coefficient in I^2C address-0X20
5. Write fourth byte of coefficient in I^2C address-0X21
6. Write 1 to W1 bit and write 1/0 to RBS in address-0X32

Write a set of coefficients from RAM:

1. Write 7-bits of address to I^2C address-0X1D
2. Write first byte of coefficient A1 in I^2C address-0X1E
3. Write second byte of coefficient A1 in I^2C address-0X1F
4. Write third byte of coefficient A1 in I^2C address-0X20
5. Write fourth byte of coefficient A1 in I^2C address-0X21
6. Write first byte of coefficient A2 in I^2C address-0X22
7. Write second byte of coefficient A2 in I^2C address-0X23
8. Write third byte of coefficient A2 in I^2C address-0X24
9. Write fourth byte of coefficient A2 in I^2C address-0X25
10. Write first byte of coefficient B1 in I^2C address-0X26
11. Write second byte of coefficient B1 in I^2C address-0X27
12. Write third byte of coefficient B1 in I^2C address-0X28
13. Write fourth byte of coefficient B1 in I^2C address-0X29
14. Write first byte of coefficient B2 in I^2C address-0X2A
15. Write second byte of coefficient B2 in I^2C address-0X2B
16. Write third byte of coefficient B2 in I^2C address-0X2C
17. Write fourth byte of coefficient B2 in I^2C address-0X2D
18. Write first byte of coefficient A0 in I^2C address-0X2E
19. Write second byte of coefficient A0 in I^2C address-0X2F
20. Write third byte of coefficient A0 in I^2C address-0X30
21. Write fourth byte of coefficient A0 in I^2C address-0X31
22. Write 1 to WA bit and write 1/0 to RBS in address-0X32

Note that: the read and write operation on RAM coefficients works only if LRCIN switching on rising edge. And, before each writing operation, it is necessary to read the address-0X32 to confirm whether RAM is writable current in first. If the logic of W1 or WA is high, the coefficient writing is prohibited.

- User-defined equalizer

The AD82128B provides 46 parametric Equalizer (EQ). User can program suitable coefficients via I^2C control interface to program the required audio band frequency response for every EQ. The transfer function

$$H(z) = \frac{A_0 + A_1 z^{-1} + A_2 z^{-2}}{1 + B_1 z^{-1} + B_2 z^{-2}}$$

The data format of 2's complement binary code for EQ coefficient is 3.25. i.e., 3-bits for integer (MSB is the sign bit) and 25-bits for mantissa. Each coefficient range is from 0x8000000 (-4) to 0x7FFFFFF (+3.99999997). These coefficients are stored in User Defined RAM and are referenced in following manner:

$$CHxEQyA0 = A0$$
$$CHxEQyA1 = A1$$
$$CHxEQyA2 = A2$$
$$CHxEQyB1 = -B1$$
$$CHxEQyB2 = -B2$$

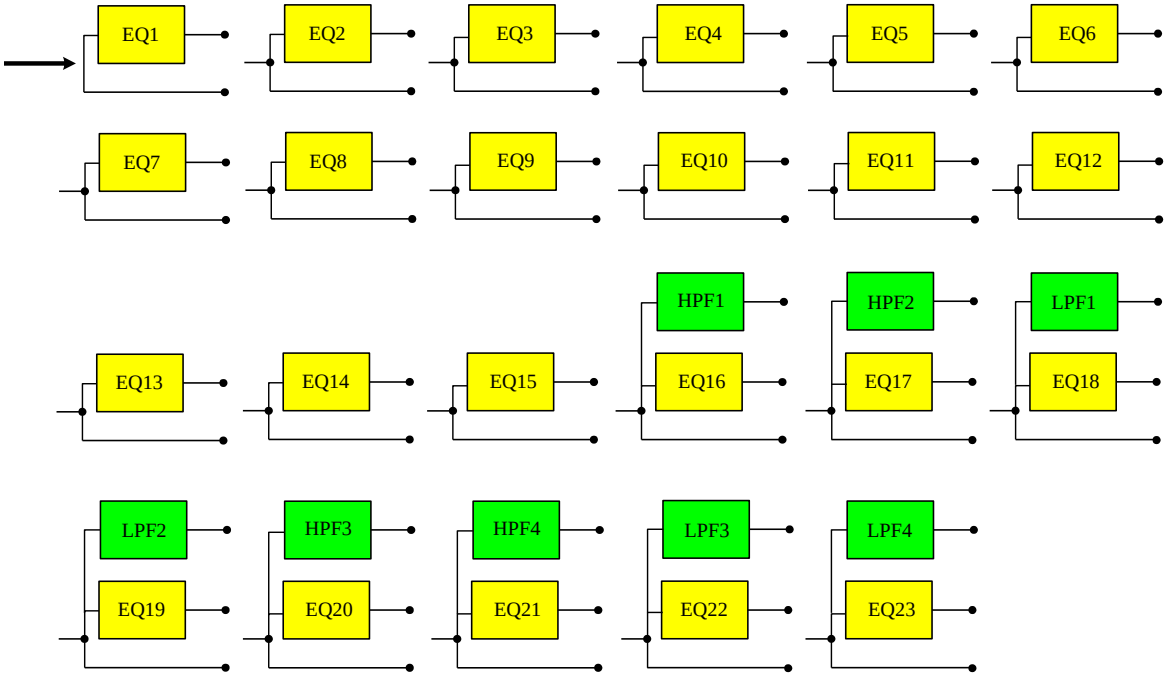
Where *x* and *y* represents the number of channel and the band number of EQ biquard.

All user-defined filters are path-through, where all coefficients are defaulted to 0 after being powered up, except the A0 that is set to 0x2000000 which represents 1.

- EQ arrangement

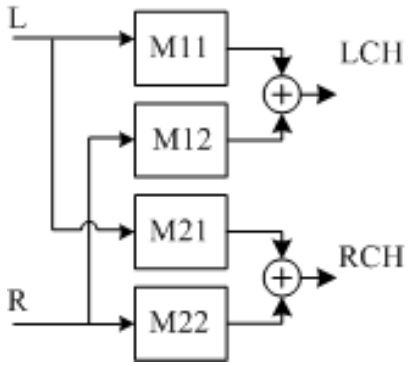
AD82128B provide 23 EQ per channel.

In Audio processing4, EQ-16, EQ-17, EQ-18, EQ-19, EQ-20, EQ-21, EQ-22, and EQ-23 will perform as HPF1, HPF2, LPF1, LPF2, HPF3, HPF4, LPF3, and LPF4 respectively.



- Mixer

The AD82128B provides mixers to generate the extra audio source from the input left and right channels. The coefficients of mixers are defined in range from 0x8000000 (-1) to 0x7FFFFFF (0.99999999). The function block diagram is as following:



- Pre-scale

For each audio channel, AD82128B can scale input signal level prior to EQ processing which is realized by a 28-bit signed fractional multiplier. The pre-scale factor, ranging from -16 (0x8000000) to 15.99999988 (0x7FFFFFF), for this multiplier, can be loaded into RAM. The default values of the pre-scaling factors are set to 0x07e88e0. Programming of RAM is described in RAM access.

- Post-scale

The AD82128B provides an additional multiplication after equalizing and before interpolation stage, which is realized by a 28-bit signed fractional multiplier. The post-scaling factor, ranging from -4 (0x8000000) to 3.99999997 (0x7FFFFFF), for this multiplier, can be loaded into RAM. The default values of the post-scaling factors are set to 0x2000000. All channels can use the channel-1 post-scale factor by setting the post-scale link. Programming of RAM is described in RAM access.

- Power Clipping

The AD82128B provides power clipping function to avoid excessive signal that may destroy loud speaker. 3. The power clipping level is defined by 28-bit representation and is stored in RAM address 0X77 of RAM bank 0. The following table shows the power clipping level's numerical representation.

GAIN=5*ANA_GAIN (Note. ANA_GAIN, please refer the setting to address 0X5E)

Sample calculation for power clipping

Max amplitude	dB	Linear	Decimal	Hex (3.25 format)
GAIN	0	1	33554432	2000000
GAIN *0.707	-3	0.707	23722976	169FBE0
GAIN *0.5	-6	0.5	16777216	1000000
GAIN *L	x	$L=10^{(x/20)}$	D=33554432xL	H=dec2hex(D)

- DRC threshold

The AD82128B provides DRC function. When the input RMS exceeds the programmable DRC threshold value, the output power will be limited by this threshold power level via gradual gain reduction. Four sets of DRC are provided. DRC1 is used for high frequency path in three bands DRC and used for L/R channel in one band DRC. DRC2 is used for low frequency path in three bands DRC. DRC3 is used for band pass frequency path in three bands DRC. DRC4 is used for the post DRC.

After AD82128B has reached the DRC threshold, its output power will be limited to that level. The output power level will be gradually adjusted to the programmable DRC threshold level. DRC threshold is defined by 28-bit presentation and is stored in RAM address 0X85, 0x89, 0X8D, 0X91 of RAM bank 0.

The following table shows the DRC threshold's numerical representation. "T" is the threshold of DRC.

The equation is

$$T_{dB} = (T - 24) / 6.0206(dB)$$

Ex: T=-6 db, TdB=(-6-24)/6.0206=-4.982892(dB)

T_{Dec}=-41799528

T_{Hex}=0XD823098

Vp=5*ANA_GAIN*[10^((T+4)/20)] (Note. ANA_GAIN, please refer the setting to address 0X5E)

Sample calculation for DRC threshold

Power	T	TdB	Decimal	Hex (5.23 format)
(Vp^2)/2R	-4	-4.65	-39012893	DACB5E3
	-7	-5.149	-43192845	D6CEDF3
	X	(x-24)/6.0206	D=2^23*TdB	H=dec2hex(D)

- DRC slope

The AD82128B DRC provides limiter and compressor. Using slope to decide compression factor. The relationship between the ratio R and the slope S is

$$S = 1 - \frac{1}{R}$$

$$R = \frac{1}{1-S} = \frac{x - Threshold(dB)}{y - Threshold(dB)}$$

DRC slope is defined by 28bit and is stored in RAM address 0x86, 0x8A, 0x8E, 0x92

Ex: Setting DRC is limiter, S=1 (R=∞).

S_DEC=1*2^25 = 33554432

S_HEX = 0X2000000

- Noise Gate Attack Level

When both left and right signals have 2048 consecutive sample points less than the programmable noise gate attack level, the audio signal will multiply noise gate gain, which can be set at x1/8, x1/4, x1/2, or zero if the noise gate function is enabled. Noise gate attack level is defined by 28-bit representation and is stored in RAM address 0X78 of RAM bank 0.

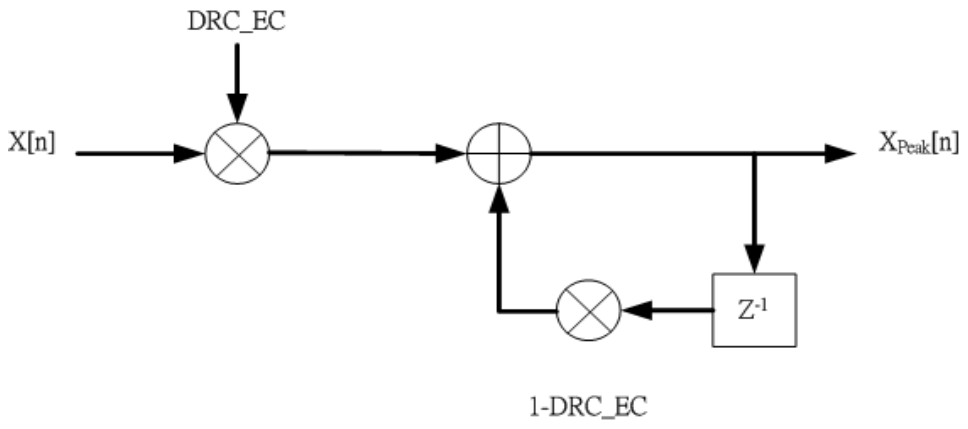
- Noise Gate Release Level

After entering the noise gating status, the noise gain will be removed whenever AD82128B receives any input signal that is more than the noise gate release level. Noise gate release level is defined by 28-bit representation and is stored in RAM address 0X79 of RAM bank 0. The following table shows the noise gate attack and release threshold level's numerical representation.

Sample calculation for noise gate attack and release level

Input amplitude (dB)	Linear	Decimal	Hex (1.27 format)
0	1	134217712	7FFFFF0
-100	10^{-5}	1328	530
-110	$10^{-5.5}$	416	1A0
x	$L=10^{(x/20)}$	D=134217712xL	H=dec2hex(D)

- DRC Energy Coefficient



The above figure illustrates the digital processing of calculating Peak signal average. In this processing, a DRC energy coefficient is required, which can be programmed for different frequency range. Four sets of energy coefficients are provided and used for respective DRC. Energy coefficient is defined by 28-bit representation and is stored in RAM address 0X7A, 0X7B, 0X7C, and 0X7D of RAM bank 0. The following table shows the DRC energy coefficient numerical representation.

Sample calculation for DRC energy coefficient

DRC energy coefficient	dB	Linear	Decimal	Hex (1.27 format)
1	0	1	134217712	7FFFFF0
1/256	-48.2	1/256	524288	80000
1/1024	-60.2	1/1024	131072	20000
L	x	$L=10^{(x/20)}$	D=134217712xL	H=dec2hex(D)

The user defined RAM

The contents of user defined RAM is represented in following table.

Ram Bank selection = 0

Address	NAME	Coefficient	Default	Format
0x00	1st SET Channel-1 EQ1	CH1EQ1A1	0x0000000	3.25
0x01		CH1EQ1A2	0x0000000	3.25
0x02		CH1EQ1B1	0x0000000	3.25
0x03		CH1EQ1B2	0x0000000	3.25
0x04		CH1EQ1A0	0x2000000	3.25
0x05	1st SET Channel-1 EQ2	CH1EQ2A1	0x0000000	3.25
0x06		CH1EQ2A2	0x0000000	3.25
0x07		CH1EQ2B1	0x0000000	3.25
0x08		CH1EQ2B2	0x0000000	3.25
0x09		CH1EQ2A0	0x2000000	3.25
0x0A	1st SET Channel-1 EQ3	CH1EQ3A1	0x0000000	3.25
0x0B		CH1EQ3A2	0x0000000	3.25
0x0C		CH1EQ3B1	0x0000000	3.25
0x0D		CH1EQ3B2	0x0000000	3.25
0x0E		CH1EQ3A0	0x2000000	3.25
0x0F	1st SET Channel-1 EQ4	CH1EQ4A1	0x0000000	3.25
0x10		CH1EQ4A2	0x0000000	3.25
0x11		CH1EQ4B1	0x0000000	3.25
0x12		CH1EQ4B2	0x0000000	3.25
0x13		CH1EQ4A0	0x2000000	3.25
0x14	1st SET Channel-1 EQ5	CH1EQ5A1	0x0000000	3.25
0x15		CH1EQ5A2	0x0000000	3.25
0x16		CH1EQ5B1	0x0000000	3.25

0x17		CH1EQ5B2	0x0000000	3.25
0x18		CH1EQ5A0	0x2000000	3.25
0x19	1st SET Channel-1 EQ6	CH1EQ6A1	0x0000000	3.25
0x1A		CH1EQ6A2	0x0000000	3.25
0x1B		CH1EQ6B1	0x0000000	3.25
0x1C		CH1EQ6B2	0x0000000	3.25
0x1D		CH1EQ6A0	0x2000000	3.25
0x1E	1st SET Channel-1 EQ7	CH1EQ7A1	0x0000000	3.25
0x1F		CH1EQ7A2	0x0000000	3.25
0x20		CH1EQ7B1	0x0000000	3.25
0x21		CH1EQ7B2	0x0000000	3.25
0x22		CH1EQ7A0	0x2000000	3.25
0x23	1st SET Channel-1 EQ8	CH1EQ8A1	0x0000000	3.25
0x24		CH1EQ8A2	0x0000000	3.25
0x25		CH1EQ8B1	0x0000000	3.25
0x26		CH1EQ8B2	0x0000000	3.25
0x27		CH1EQ8A0	0x2000000	3.25
0x28	1st SET Channel-1 EQ9	CH1EQ9A1	0x0000000	3.25
0x29		CH1EQ9A2	0x0000000	3.25
0x2A		CH1EQ9B1	0x0000000	3.25
0x2B		CH1EQ9B2	0x0000000	3.25
0x2C		CH1EQ9A0	0x2000000	3.25
0x2D	1st SET Channel-1 EQ10	CH1EQ10A1	0x0000000	3.25
0x2E		CH1EQ10A2	0x0000000	3.25
0x2F		CH1EQ10B1	0x0000000	3.25
0x30		CH1EQ10B2	0x0000000	3.25
0x31		CH1EQ10A0	0x2000000	3.25
0x32	1st SET Channel-1 EQ11	CH1EQ11A1	0x0000000	3.25
0x33		CH1EQ11A2	0x0000000	3.25
0x34		CH1EQ11B1	0x0000000	3.25
0x35		CH1EQ11B2	0x0000000	3.25
0x36		CH1EQ11A0	0x2000000	3.25
0x37	1st SET Channel-1 EQ12	CH1EQ12A1	0x0000000	3.25
0x38		CH1EQ12A2	0x0000000	3.25
0x39		CH1EQ12B1	0x0000000	3.25
0x3A		CH1EQ12B2	0x0000000	3.25
0x3B		CH1EQ12A0	0x2000000	3.25

0x3C	1st SET Channel-1 EQ13	CH1EQ13A1	0x0000000	3.25
0x3D		CH1EQ13A2	0x0000000	3.25
0x3E		CH1EQ13B1	0x0000000	3.25
0x3F		CH1EQ13B2	0x0000000	3.25
0x40		CH1EQ13A0	0x2000000	3.25
0x41	1st SET Channel-1 EQ14	CH1EQ14A1	0x0000000	3.25
0x42		CH1EQ14A2	0x0000000	3.25
0x43		CH1EQ14B1	0x0000000	3.25
0x44		CH1EQ14B2	0x0000000	3.25
0x45		CH1EQ14A0	0x2000000	3.25
0x46	1st SET Channel-1 EQ15	CH1EQ15A1	0x0000000	3.25
0x47		CH1EQ15A2	0x0000000	3.25
0x48		CH1EQ15B1	0x0000000	3.25
0x49		CH1EQ15B2	0x0000000	3.25
0x4A		CH1EQ15A0	0x2000000	3.25
0x4B	1st SET Channel-1 EQ16	CH1EQ16A1	0x0000000	3.25
0x4C		CH1EQ16A2	0x0000000	3.25
0x4D		CH1EQ16B1	0x0000000	3.25
0x4E		CH1EQ16B2	0x0000000	3.25
0x4F		CH1EQ16A0	0x2000000	3.25
0x50	1st SET Channel-1 EQ17	CH1EQ17A1	0x0000000	3.25
0x51		CH1EQ17A2	0x0000000	3.25
0x52		CH1EQ17B1	0x0000000	3.25
0x53		CH1EQ17B2	0x0000000	3.25
0x54		CH1EQ17A0	0x2000000	3.25
0x55	1st SET Channel-1 EQ18	CH1EQ18A1	0x0000000	3.25
0x56		CH1EQ18A2	0x0000000	3.25
0x57		CH1EQ18B1	0x0000000	3.25
0x58		CH1EQ18B2	0x0000000	3.25
0x59		CH1EQ18A0	0x2000000	3.25
0x5A	1st SET Channel-1 EQ19	CH1EQ19A1	0x0000000	3.25
0x5B		CH1EQ19A2	0x0000000	3.25
0x5C		CH1EQ19B1	0x0000000	3.25
0x5D		CH1EQ19B2	0x0000000	3.25
0x5E		CH1EQ19A0	0x2000000	3.25
0x5F	1st SET Channel-1 EQ20	CH1EQ20A1	0x0000000	3.25
0x60		CH1EQ20A2	0x0000000	3.25

0x61		CH1EQ20B1	0x0000000	3.25
0x62		CH1EQ20B2	0x0000000	3.25
0x63		CH1EQ20A0	0x2000000	3.25
0x64	1st SET Channel-1 EQ21	CH1EQ20A1	0x0000000	3.25
0x65		CH1EQ20A2	0x0000000	3.25
0x66		CH1EQ20B1	0x0000000	3.25
0x67		CH1EQ20B2	0x0000000	3.25
0x68		CH1EQ20A0	0x2000000	3.25
0x69	1st SET Channel-1 EQ22	CH1EQ20A1	0x0000000	3.25
0x6A		CH1EQ20A2	0x0000000	3.25
0x6B		CH1EQ20B1	0x0000000	3.25
0x6C		CH1EQ20B2	0x0000000	3.25
0x6D		CH1EQ20A0	0x2000000	3.25
0x6E	1st SET Channel-1 EQ23	CH1EQ20A1	0x0000000	3.25
0x6F		CH1EQ20A2	0x0000000	3.25
0x70		CH1EQ20B1	0x0000000	3.25
0x71		CH1EQ20B2	0x0000000	3.25
0x72		CH1EQ20A0	0x2000000	3.25
0x73	Channel-1 Mixer1	M11	0x7FFFFFF	1.27
0x74	Channel-1 Mixer2	M12	0x0000000	1.27
0x75	Channel-1 Prescale	C1PRS	0x07E88E0	5.23
0x76	Channel-1 Postscale	C1POS	0x2000000	3.25
0x77	CH1.2 Power Clipping	PC1	0x2000000	3.25(last 1byte no used)
0x78	Noise Gate Attack Level	NGAL	0x00001A0	1.27(last 1byte no used)
0x79	Noise Gate Release Level	NGRL	0x0000530	1.27(last 1byte no used)
0x7A	DRC1 Energy Coefficient	DRC1_EC	0x10000	1.27
0x7B	DRC2 Energy Coefficient	DRC2_EC	0x10000	1.27
0x7C	DRC3 Energy Coefficient	DRC3_EC	0x10000	1.27
0x7D	DRC4 Energy Coefficient	DRC4_EC	0x10000	1.27
0x7E	DRC1 Power Meter	C1_RMS	Read only	5.23
0x7F	DRC3 Power Meter	C3_RMS	Read only	5.23
0x80	DRC5 Power Meter	C5_RMS	Read only	5.23
0x81	DRC7 Power Meter	C7_RMS	Read only	5.23
0x82	Channel-1 DRC GAIN1	CH1DRCGAIN1	0x2000000	3.25

0x83	Channel-1 DRC GAIN2	CH1DRCGAIN2	0x2000000	3.25
0x84	Channel-1 DRC GAIN3	CH1DRCGAIN3	0x2000000	3.25
0x85	DRC1 FF threshold	DRC1TH	0xE01C070	5.23
0x86	DRC1 FF Slope	DRC1_Slope	0X2000000	3.25
0x87	DRC1 FF aa	DRC1_AA	0X0004000	3.25
0x88	DRC1 FF da	DRC1_DA	0X0004000	3.25
0x89	DRC2 FF threshold	DRC2TH	0xE01C070	5.23
0x8A	DRC2 FF Slope	DRC2_Slope	0X2000000	3.25
0x8B	DRC2 FF aa	DRC2_AA	0X0004000	3.25
0x8C	DRC2 FF da	DRC2_DA	0X0004000	3.25
0x8D	DRC3 FF threshold	DRC3TH	0xE01C070	5.23
0x8E	DRC3 FF Slope	DRC3_Slope	0X2000000	3.25
0x8F	DRC3 FF aa	DRC3_AA	0X0004000	3.25
0x90	DRC3 FF da	DRC3_DA	0X0004000	3.25
0x91	DRC4 FF threshold	DRC4TH	0xE01C070	5.23
0x92	DRC4 FF Slope	DRC4_Slope	0X2000000	3.25
0x93	DRC4 FF aa	DRC4_AA	0X0004000	3.25
0x94	DRC4 FF da	DRC4_DA	0X0004000	3.25
0x95	Reserved			
0x96	Reserved			
0x97	Reserved			
0x98	Reserved			
0x99	I2SO LCH GAIN	I2SO_L_GAIN	0X0800000	5.23
0x9A	SRS GAIN	SRS GAIN	0X2000000	3.25
0x9B	Comp filter of A0	comp_A0	0X1D7E6E0	3.25
0x9C	Comp filter of A1	comp_A1	0X02E7740	3.25
0x9D	Comp filter of B1	comp_B1	0XFF9A1E0	3.25
0x9E	QT AT	QT_AT	0X1912BE0	1.27
0x9F	QT_RT	QT_RT	0x11B5AB9	1.27
0xA0	QT_REGION_T	QT_REGION_T	0x05FCACA	1.27
0xA1	QT_REGION_B	QT_REGION_B	0x0000000	1.27

Ram Bank selection = 1

Address	NAME	Coefficient	Default	Format
0x00	1st SET Channel-2 EQ1	CH2EQ1A1	0x0000000	3.25
0x01		CH2EQ1A2	0x0000000	3.25
0x02		CH2EQ1B1	0x0000000	3.25

0x03		CH2EQ1B2	0x0000000	3.25
0x04		CH2EQ1A0	0x2000000	3.25
0x05	1st SET Channel-2 EQ2	CH2EQ2A1	0x0000000	3.25
0x06		CH2EQ2A2	0x0000000	3.25
0x07		CH2EQ2B1	0x0000000	3.25
0x08		CH2EQ2B2	0x0000000	3.25
0x09		CH2EQ2A0	0x2000000	3.25
0x0A	1st SET Channel-2 EQ3	CH2EQ3A1	0x0000000	3.25
0x0B		CH2EQ3A2	0x0000000	3.25
0x0C		CH2EQ3B1	0x0000000	3.25
0x0D		CH2EQ3B2	0x0000000	3.25
0x0E		CH2EQ3A0	0x2000000	3.25
0x0F	1st SET Channel-2 EQ4	CH2EQ4A1	0x0000000	3.25
0x10		CH2EQ4A2	0x0000000	3.25
0x11		CH2EQ4B1	0x0000000	3.25
0x12		CH2EQ4B2	0x0000000	3.25
0x13		CH2EQ4A0	0x2000000	3.25
0x14	1st SET Channel-2 EQ5	CH2EQ5A1	0x0000000	3.25
0x15		CH2EQ5A2	0x0000000	3.25
0x16		CH2EQ5B1	0x0000000	3.25
0x17		CH2EQ5B2	0x0000000	3.25
0x18		CH2EQ5A0	0x2000000	3.25
0x19	1st SET Channel-2 EQ6	CH2EQ6A1	0x0000000	3.25
0x1A		CH2EQ6A2	0x0000000	3.25
0x1B		CH2EQ6B1	0x0000000	3.25
0x1C		CH2EQ6B2	0x0000000	3.25
0x1D		CH2EQ6A0	0x2000000	3.25
0x1E	1st SET Channel-2 EQ7	CH2EQ7A1	0x0000000	3.25
0x1F		CH2EQ7A2	0x0000000	3.25
0x20		CH2EQ7B1	0x0000000	3.25
0x21		CH2EQ7B2	0x0000000	3.25
0x22		CH2EQ7A0	0x2000000	3.25
0x23	1st SET Channel-2 EQ8	CH2EQ8A1	0x0000000	3.25
0x24		CH2EQ8A2	0x0000000	3.25
0x25		CH2EQ8B1	0x0000000	3.25
0x26		CH2EQ8B2	0x0000000	3.25
0x27		CH2EQ8A0	0x2000000	3.25

0x28	1st SET Channel-2 EQ9	CH2EQ9A1	0x0000000	3.25
0x29		CH2EQ9A2	0x0000000	3.25
0x2A		CH2EQ9B1	0x0000000	3.25
0x2B		CH2EQ9B2	0x0000000	3.25
0x2C		CH2EQ9A0	0x2000000	3.25
0x2D	1st SET Channel-2 EQ10	CH2EQ10A1	0x0000000	3.25
0x2E		CH2EQ10A2	0x0000000	3.25
0x2F		CH2EQ10B1	0x0000000	3.25
0x30		CH2EQ10B2	0x0000000	3.25
0x31		CH2EQ10A0	0x2000000	3.25
0x32	1st SET Channel-2 EQ11	CH2EQ11A1	0x0000000	3.25
0x33		CH2EQ11A2	0x0000000	3.25
0x34		CH2EQ11B1	0x0000000	3.25
0x35		CH2EQ11B2	0x0000000	3.25
0x36		CH2EQ11A0	0x2000000	3.25
0x37	1st SET Channel-2 EQ12	CH2EQ12A1	0x0000000	3.25
0x38		CH2EQ12A2	0x0000000	3.25
0x39		CH2EQ12B1	0x0000000	3.25
0x3A		CH2EQ12B2	0x0000000	3.25
0x3B		CH2EQ12A0	0x2000000	3.25
0x3C	1st SET Channel-2 EQ13	CH2EQ13A1	0x0000000	3.25
0x3D		CH2EQ13A2	0x0000000	3.25
0x3E		CH2EQ13B1	0x0000000	3.25
0x3F		CH2EQ13B2	0x0000000	3.25
0x40		CH2EQ13A0	0x2000000	3.25
0x41	1st SET Channel-2 EQ14	CH2EQ14A1	0x0000000	3.25
0x42		CH2EQ14A2	0x0000000	3.25
0x43		CH2EQ14B1	0x0000000	3.25
0x44		CH2EQ14B2	0x0000000	3.25
0x45		CH2EQ14A0	0x2000000	3.25
0x46	1st SET Channel-2 EQ15	CH2EQ15A1	0x0000000	3.25
0x47		CH2EQ15A2	0x0000000	3.25
0x48		CH2EQ15B1	0x0000000	3.25
0x49		CH2EQ15B2	0x0000000	3.25
0x4A		CH2EQ15A0	0x2000000	3.25
0x4B	1st SET Channel-2 EQ16	CH2EQ16A1	0x0000000	3.25
0x4C		CH2EQ16A2	0x0000000	3.25

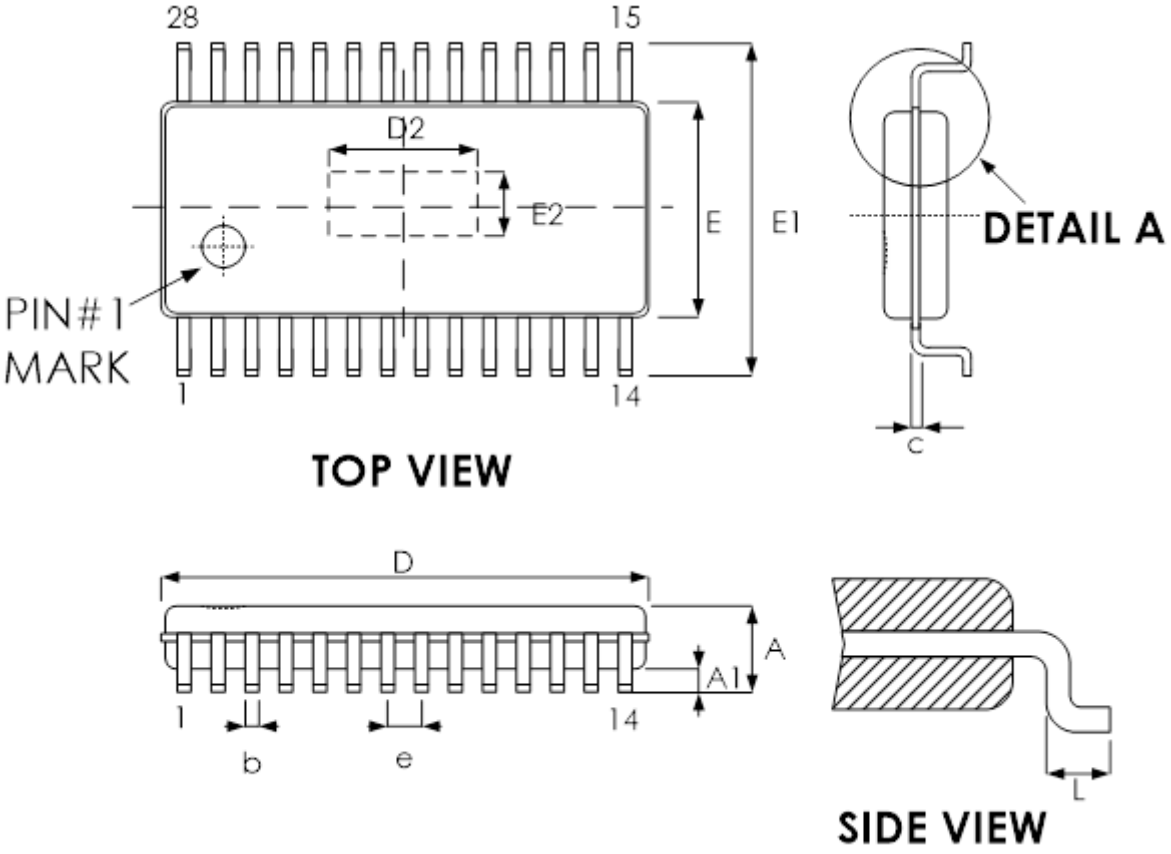
0x4D		CH2EQ16B1	0x0000000	3.25
0x4E		CH2EQ16B2	0x0000000	3.25
0x4F		CH2EQ16A0	0x2000000	3.25
0x50	1st SET Channel-2 EQ17	CH2EQ17A1	0x0000000	3.25
0x51		CH2EQ17A2	0x0000000	3.25
0x52		CH2EQ17B1	0x0000000	3.25
0x53		CH2EQ17B2	0x0000000	3.25
0x54		CH2EQ17A0	0x2000000	3.25
0x55	1st SET Channel-2 EQ18	CH2EQ18A1	0x0000000	3.25
0x56		CH2EQ18A2	0x0000000	3.25
0x57		CH2EQ18B1	0x0000000	3.25
0x58		CH2EQ18B2	0x0000000	3.25
0x59		CH2EQ18A0	0x2000000	3.25
0x5A	1st SET Channel-2 EQ19	CH2EQ19A1	0x0000000	3.25
0x5B		CH2EQ19A2	0x0000000	3.25
0x5C		CH2EQ19B1	0x0000000	3.25
0x5D		CH2EQ19B2	0x0000000	3.25
0x5E		CH2EQ19A0	0x2000000	3.25
0x5F	1st SET Channel-2 EQ20	CH2EQ20A1	0x0000000	3.25
0x60		CH2EQ20A2	0x0000000	3.25
0x61		CH2EQ20B1	0x0000000	3.25
0x62		CH2EQ20B2	0x0000000	3.25
0x63		CH2EQ20A0	0x2000000	3.25
0x64	1st SET Channel-2 EQ21	CH2EQ20A1	0x0000000	3.25
0x65		CH2EQ20A2	0x0000000	3.25
0x66		CH2EQ20B1	0x0000000	3.25
0x67		CH2EQ20B2	0x0000000	3.25
0x68		CH2EQ20A0	0x2000000	3.25
0x69	1st SET Channel-2 EQ22	CH1EQ20A1	0x0000000	3.25
0x6A		CH1EQ20A2	0x0000000	3.25
0x6B		CH1EQ20B1	0x0000000	3.25
0x6C		CH1EQ20B2	0x0000000	3.25
0x6D		CH1EQ20A0	0x2000000	3.25
0x6E	1st SET Channel-2 EQ23	CH1EQ20A1	0x0000000	3.25
0x6F		CH1EQ20A2	0x0000000	3.25
0x70		CH1EQ20B1	0x0000000	3.25
0x71		CH1EQ20B2	0x0000000	3.25

0x72		CH1EQ20A0	0x2000000	3.25
0x73	Channel-2 Mixer1	M21	0x000000	1.27
0x74	Channel-2 Mixer2	M22	0x7FFFFF	1.27
0x75	Channel-2 Prescale	C2PRS	0x07E88E0	5.23
0x76	Channel-2 Postscale	C2POS	0x2000000	3.25
0x77	Reserved			
0x78	Reserved			
0x79	Reserved			
0x7A	Reserved			
0x7B	Reserved			
0x7C	Reserved			
0x7D	Reserved			
0x7E	DRC2 Power Meter	C2_RMS	Read only	5.23
0x7F	DRC4 Power Meter	C4_RMS	Read only	5.23
0x80	DRC6 Power Meter	C6_RMS	Read only	5.23
0x81	DRC8 Power Meter	C8_RMS	Read only	5.23
0x82	Channel-2 DRC GAIN1	CH2DRCGAIN1	0x2000000	3.25
0x83	Channel-2 DRC GAIN2	CH2DRCGAIN2	0x2000000	3.25
0x84	Channel-2 DRC GAIN3	CH2DRCGAIN3	0x2000000	3.25
0x85	DPEQ Energy Coefficient	DPEQ_EC	0x0020000	1.27
0x86	DBE upper mix threshold	DBE_UMTH	0xD2D2600	5.23
0x87	DBE lower mix threshold	DBE_LMTH	0xB83F110	5.23
0x88	DBE 1/(Upper-Lower)	DBE_U_L	0x02687F0	5.23
0x89	Reserved			
0x8A	Reserved			
0x8B	Reserved			
0x8C	Reserved			
0x8D	Reserved			
0x8E	Reserved			
0x8F	Reserved			
0x90	Reserved			
0x91	Reserved			
0x92	Reserved			
0x93	Reserved			

0x94	Reserved			
0x95	Reserved			
0x96	Reserved			
0x97	Reserved			
0x98	Reserved			
0x99	I2SO RCH GAIN	I2SO_R_GAIN	0X0800000	5.23
0x9A	AGL Attack threshold	AGL ATH	0X05A9DF0	5.23
0x9B	AGL Release threshold	AGL RTH	0X047FAD0	5.23
0x9C	AGL Attack Rate / Release Rate	AGL AR / AGL RR	0X0000864	No use (6 bit) + AR (11 bit) + RR(11 bit)
0x9D	Reserved			
0x9E	AGL_EC	AGL_EC	0x0040000	3.25

Package Dimensions

- **TSSOP-28 (173 mil)**



Symbol	Dimension in mm	
	Min	Max
A	--	1.20
A1	0.05	0.15
b	0.19	0.30
c	0.09	0.20
D	9.60	9.80
E	4.30	4.50
E1	6.30	6.50
e	0.65 BSC	
L	0.45	0.75

Exposed pad

	Dimension in mm	
	Min	Max
D2	5.00	6.40
E2	2.50	2.90

Revision History

Revision	Date	Description
0.1	2023.12.29	Initial version.

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