2x20W Stereo / 1x 40W Mono Digital Audio Amplifier

Features

- 16/18/20/24-bits input with I^2S, Left-alignment, Right-alignment and TDM data format
- PSNR & DR (A-weighting)
  Loudspeaker: 104dB (PSNR), 108dB (DR) @ 24V
- Multiple sampling frequencies (Fs)
  8kHz, 16kHz, 32kHz / 44.1kHz / 48kHz
  and 88.2kHz / 96kHz
- BCLK = 32x, 48x, 64x, 96x,128x, 192x, 256x Fs
- Supply voltage
  3.3V for digital circuit
  4.5V ~ 26V for loudspeaker driver
- Supports 2.0CH/Mono configuration
- Loudspeaker output power @ 12V for stereo
  7W x 2CH into 8Ω < 1% THD+N
  10W x 2CH into 4Ω < 1% THD+N
- Loudspeaker output power @ 18V for stereo
  15W x 2CH into 8Ω < 1% THD+N
- Loudspeaker output power @ 24V for stereo
  20W x 2CH into 8Ω < 1% THD+N
- Sound processing including：
  Volume control (+24dB ~ -103dB, 0.125dB / step)
  Dynamic range control
  Power Clipping
  Channel mixing
  User programmed compensated filter
  Noise gate with hysteresis window
  Pre-scale/post-scale
  DC-blocking high-pass filter
  I2S output with user programmed gain
  (+24dB ~ mute)
- Anti-pop design
- I^2S output with selectable Audio DSP point
- Short circuit and over-temperature protection
- Supports I^2C control without clock
- I^2C control interface with selectable device address
- Dynamic temperature control
- Support software reset
- Internal PLL
- LV Under-voltage shutdown and HV Under-voltage detection
- Over voltage protection
- Power saving mode

Applications

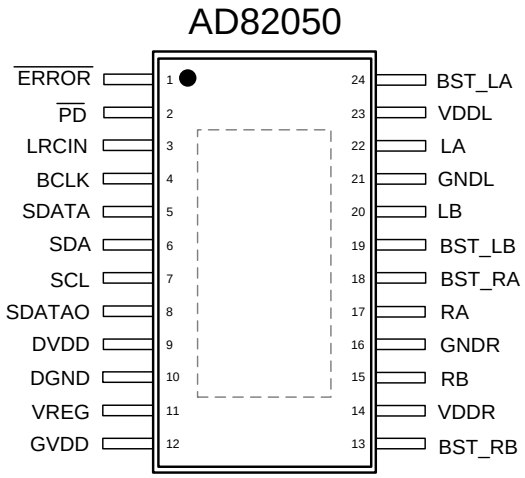
- TV audio
- Boom-box, CD and DVD receiver, docking system
- Powered speaker
- Wireless audio

Description

AD82050 is a digital audio amplifier capable of driving 20W (BTL) each to a pair of 8Ω load speaker and 40W (PBTL) to a 4Ω load speaker operating at 24V supply without external heat-sink or fan requirement with play music.

AD82050 can provide advanced audio processing functions, such as volume control, audio mixing, and Dynamic Range Control (DRC). These are fully programmable via a simple I^2C control interface. Robust protection circuits are provided to protect AD82050 from damage due to accidental erroneous operating condition. The full digital circuit design of AD82050 is more tolerant to noise and PVT (Process, Voltage, and Temperature) variation than the analog class-AB or class-D audio amplifier counterpart implemented by analog circuit design. AD82050 is pop free during instantaneous powered on/off or mute/shut down switching because of its robust built-in anti-pop circuit.

Pin Assignment



E-TSSOP-24L

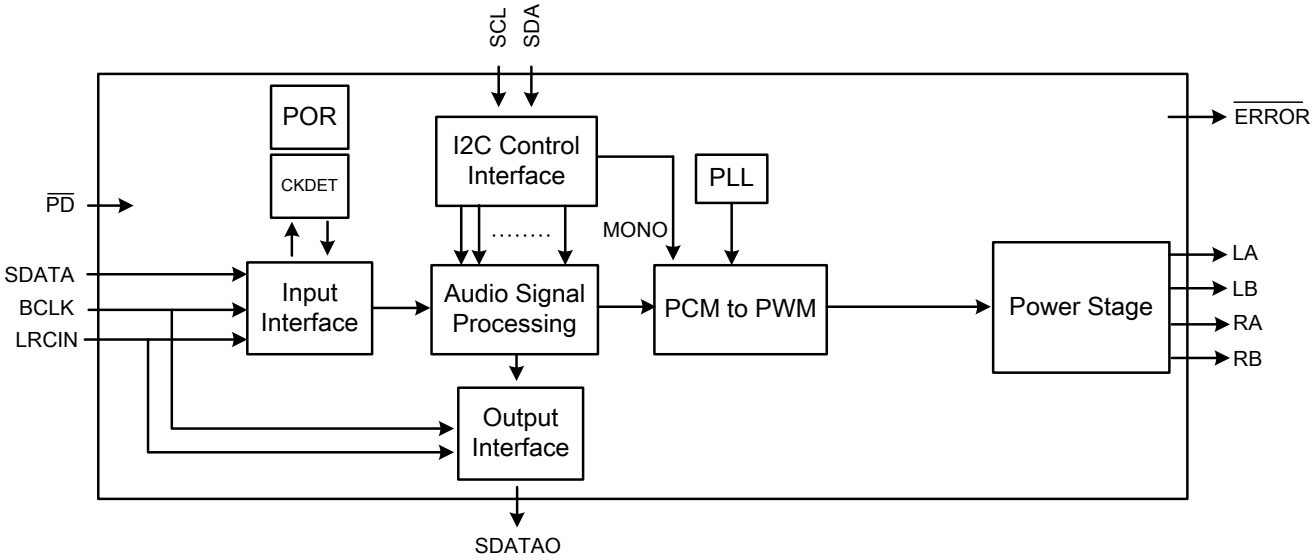
Pin Description (E-TSSOP 24L)

PIN	NAME	TYPE	DESCRIPTION	CHARACTERISTICS
1	$\overline{\text{ERROR}}$	AI/O	$\overline{\text{ERROR}}$ pin is a dual function pin. One is I^2C address setting during power up. The other one is error status report (low active), It sets by register of A_SEL_FAULT at address 0x02 B[7] to enable it.	This pin is monitored on the rising edge of reset. A value of Low (15-kΩ pull down) sets the I^2C device address to 0x30 and a value of High (15-kΩ pull up) sets it to 0x34.
2	$\overline{\text{PD}}$	DI	Power down, low active.	Schmitt trigger TTL input buffer, internal pull High with a 330Kohm resistor.
3	LRCIN	DI	Left/Right clock input (Fs).	Schmitt trigger TTL input buffer, internal pull Low with a 100Kohm resistor.
4	BCLK	DI	Bit clock input (64Fs).	Schmitt trigger TTL input buffer, internal pull Low with a 100Kohm resistor.
5	SDATA	DI	Serial audio data input.	Schmitt trigger TTL input buffer
6	SDA	DI/O	I^2C bi-directional serial data.	Schmitt trigger TTL input buffer
7	SCL	DI	I^2C serial clock input.	Schmitt trigger TTL input buffer
8	SDATAO	DO	Serial audio data output.	Schmitt trigger TTL input buffer
9	DVDD	P	Digital Power.	
10	DGND	P	Digital Ground.	
11	VREG	P	1.8V Regulator voltage output.	

12	GVDD	P	5V Regulator voltage output. This pin must not be used to drive external devices.	
13	BST_RB	P	Bootstrap supply for right channel output B.	
14	VDDR	P	Right channel supply.	
15	RB	O	Right channel output B.	
16	GNDR	P	Right channel ground.	
17	RA	O	Right channel output A.	
18	BST_RA	P	Bootstrap supply for right channel output A.	
19	BST_LB	P	Bootstrap supply for left channel output B.	
20	LB	O	Left channel output B.	
21	GNDL	P	Left channel ground.	
22	LA	O	Left channel output A.	
23	VDDL	P	Left channel supply.	
24	BST_LA	P	Bootstrap supply for left channel output A.	

Note: AI=Analog input; AO=Analog output; AI/O = Analog Bi-directional (input and output); DI=Digital Input; DO=Digital Output; DI/O = Digital Bi-directional (input and output); P=Power or Ground; O: PWM output

Functional Block Diagram



Ordering Information

Product ID	Package	Packing/MPQ	Comments
AD82050-QG24NRR	E-TSSOP 24L	2.5K Units / Reel 1 Reel / Small box	Green

Available Package

Package Type	Device No.	θ_{ja}(℃/W)	Ψ_{jt}(℃/W)	θ_{jt}(℃/W)	Exposed Thermal Pad
E-TSSOP 24L	AD82050	30.9	0.5	29.6	Yes (Note1)

Note 1.1: The thermal pad is located at the bottom of the package. To optimize thermal performance, soldering the thermal pad to the PCB's ground plane is suggested.

Note 1.2: θ_{ja}, the junction-to-ambient thermal resistance is simulated on a room temperature (T_A=25℃), natural convection environment test board, which is constructed with a thermally efficient, 4-layers PCB (2S2P). The simulation is tested using the JESD51-5 thermal measurement standard.

Note 1.3: Ψ_{jt} represents the thermal parameter for the heat flow between the chip junction and the package's top surface center. It's extracted from the simulation data for obtainingθ_{ja}, using a procedure described in JESD51-2.

Note 1.4: θ_{jt} represents the thermal resistance for the heat flow between the chip junction and the package's top surface. It's extracted from the simulation data with obtaining a cold plate on the package top.

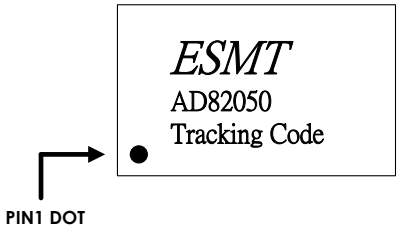
Marking Information

AD82050

Line 1 : LOGO

Line 2 : Product no.

Line 3 : Tracking Code



Absolute Maximum Ratings

Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device.

Symbol	Parameter	Min	Max	Units
DVDD	Supply for Digital Circuit	-0.3	3.6	V
VDDL / R	Supply for Driver Stage	-0.3	30	V
V_i	Input Voltage	-0.3	3.6	V
T_{stg}	Storage Temperature	-65	150	°C
T_J	Junction Operating Temperature	-40	150	°C
ESD	Human Body Model		±2K	V
	Charged Device Model		±750	V

Recommended Operating Conditions

Symbol	Parameter	Typ	Units
DVDD	Supply for Digital Circuit	3.0 ~ 3.6	V
VDDL / R	Supply for Driver Stage	4.5 ~ 26	V
T_J	Junction Operating Temperature	-40 ~ 125	^oC
T_A	Ambient Operating Temperature	-40 ~ 85	^oC

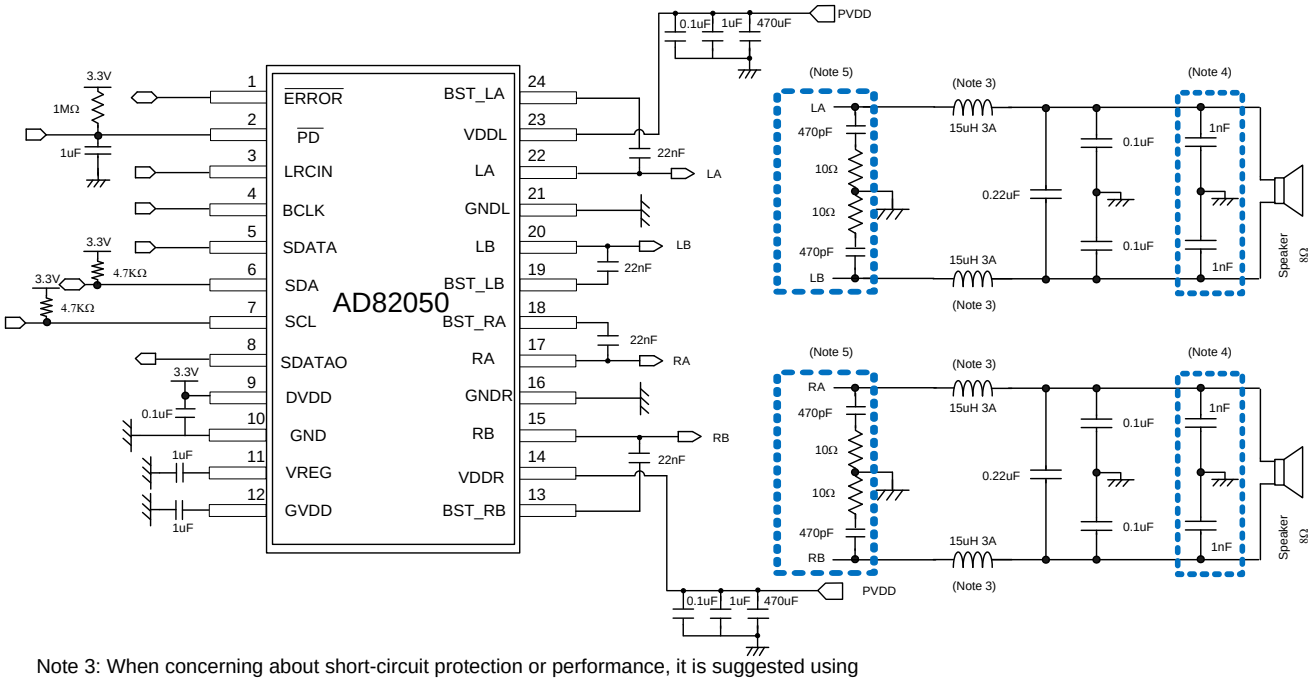
General Electrical Characteristics

Condition: T_A=25 ^oC (unless otherwise specified).

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{PD}(HV)	PVDD Supply Current during Power Down	PVDD=24V		19		uA
I_{PD}(LV)	DVDD Supply Current during Power Down	DVDD=3.3V		1.6		mA
I_Q(HV)	Quiescent current for PVDD	PVDD=24V		7.6		mA
I_Q(LV)	Quiescent current for DVDD (Un-mute)	DVDD=3.3V		11.7		mA
T_{SENSOR}	Junction Temperature for Driver Shutdown			155		^oC
	Temperature Hysteresis for Recovery from Shutdown			35		^oC
UV_H	Under Voltage Disabled (For DVDD)			3		V
UV_L	Under Voltage Enabled (For DVDD)			2.8		V
	Static Drain-to-Source On-state Resistor, NMOS			210		mΩ
I_{SC}	L(R) Channel Over-Current Protection (Note 2)	PVDD=24V		8		A
	Mono Channel Over-Circuit Protection (Note 2)	PVDD=24V		14		A
V_{IH}	High-Level Input Voltage	DVDD=3.3V	2.0			V
V_{IL}	Low-Level Input Voltage	DVDD=3.3V			0.8	V
V_{OH}	High-Level Output Voltage	DVDD=3.3V	2.4			V
V_{OL}	Low-Level Output Voltage	DVDD=3.3V			0.4	V
C_I	Input Capacitance			6.4		pF

Note 2: Loudspeaker over-current protection is only effective when loudspeaker drivers are properly connected with external LC filters. Please refer to the application circuit example for recommended LC filter configuration.

Application Circuit Example for Stereo



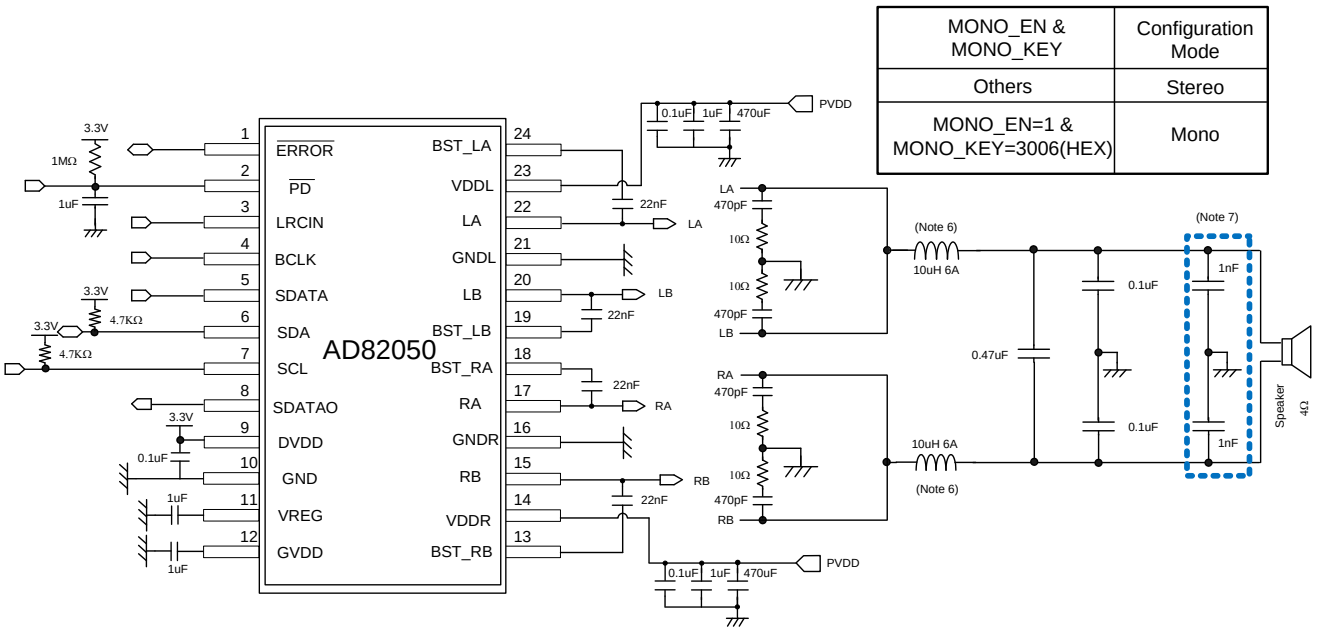
Note 3: When concerning about short-circuit protection or performance, it is suggested using the choke with its I_{DC} larger than I_{SC}.

Note 4: These capacitors should be placed as close to speaker jack as possible, and their values should be determined according to EMI test results.

Note 5: The snubber circuit is used to suppress overshoot voltage on output pin, and it is also helpful with EMI suppression.

Application Circuit Example for Mono

MONO_EN & MONO_KEY	Configuration Mode
Others	Stereo
MONO_EN=1 & MONO_KEY=3006(HEX)	Mono



Note 6: When concerning about short-circuit protection or performance, it is suggested using the choke with its I_{DC} larger than I_{SC}.

Note 7: These capacitors should be placed as close to speaker jack as possible, and their values should be determined according to EMI test results.

Electrical Characteristics and Specifications for Loudspeaker

- **BTL (Bridge-Tied-Load) output for Stereo**

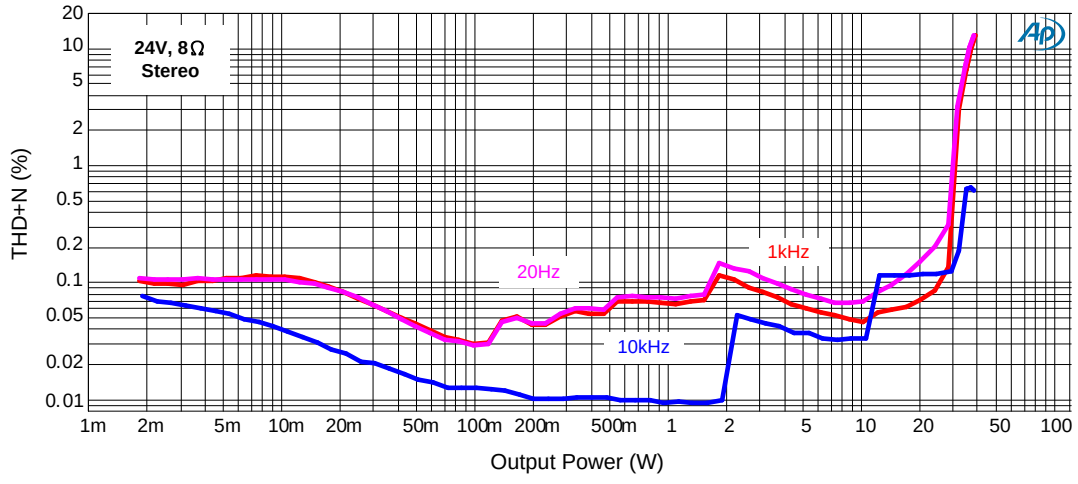
Condition: T_A = 25 °C, DVDD = 3.3V, VDDL = VDDR = 24V, F_S = 48kHz, Load = 8Ω with passive LC lowpass filter (L = 15μ H with R_{DC} = 63mΩ , Cdiff. = 220nF, Ccom. = 100nF); Input is 1kHz sinewave. Volume is 0dB unless otherwise specified.

Symbol	Parameter	Condition	Input Level	Min	Typ	Max	Units
P_O (Note 9)	RMS Output Power (THD+N = 0.07%)				20		W
	RMS Output Power (THD+N = 0.06%)				15		W
	RMS Output Power (THD+N = 0.05%)				10		W
THD+N	Total Harmonic Distortion + Noise	P_O = 7.5W			0.06		%
SNR	Signal to Noise Ratio (Note 8)	Maximum power at THD < 1% @ 1kHz	-1dB		104		dB
DR	Dynamic Range (Note 8)		-60dB		108		dB
Vn	Output Noise (Note 8)	20Hz to 20kHz			80		uV
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = $1V_{RMS}$ @ 1kHz			-72		dB
	Channel Separation	1W @ 1kHz			-73		dB

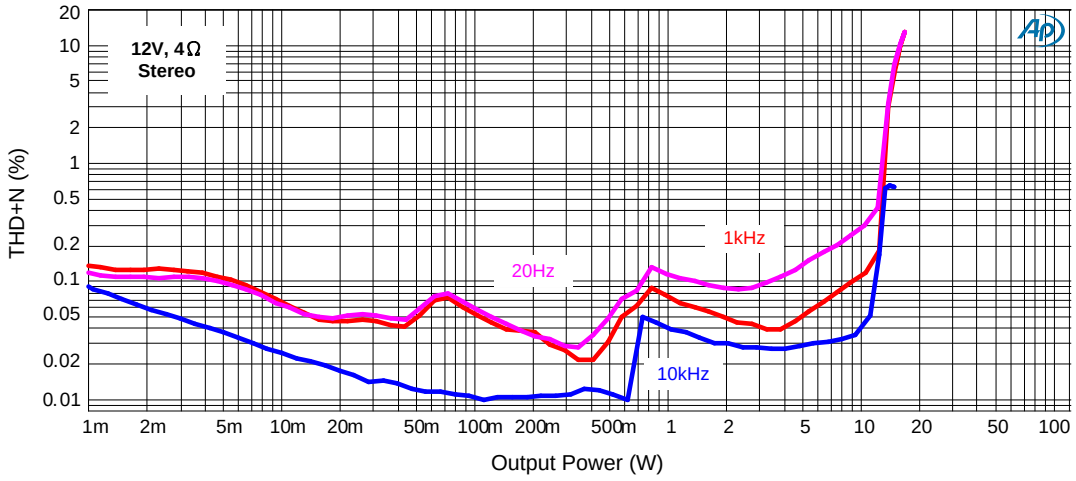
Note 8: Measured with A-weighting filter.

Note 9: Thermal dissipation is limited by package type and PCB design. The external heat-sink or system cooling method should be adopted for maximum power output.

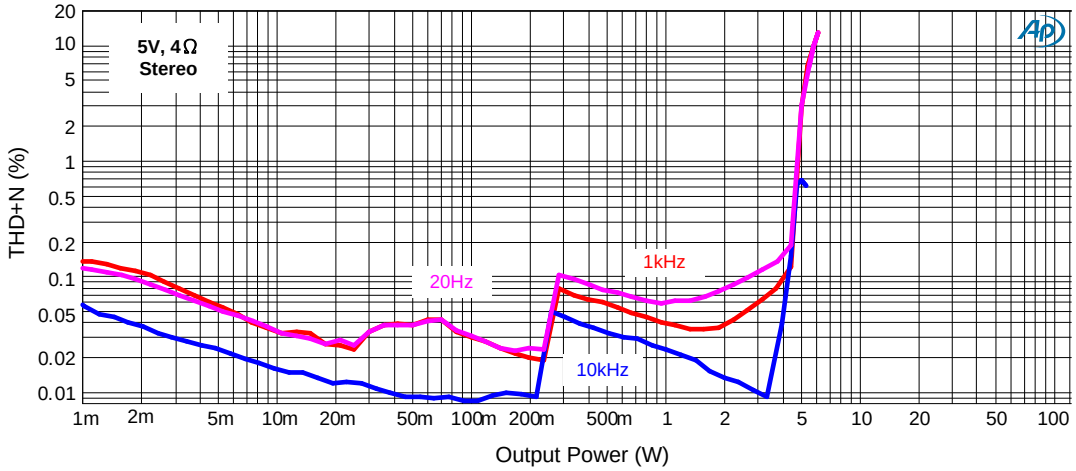
Total Harmonic Distortion + Noise vs. Output Power (BTL)



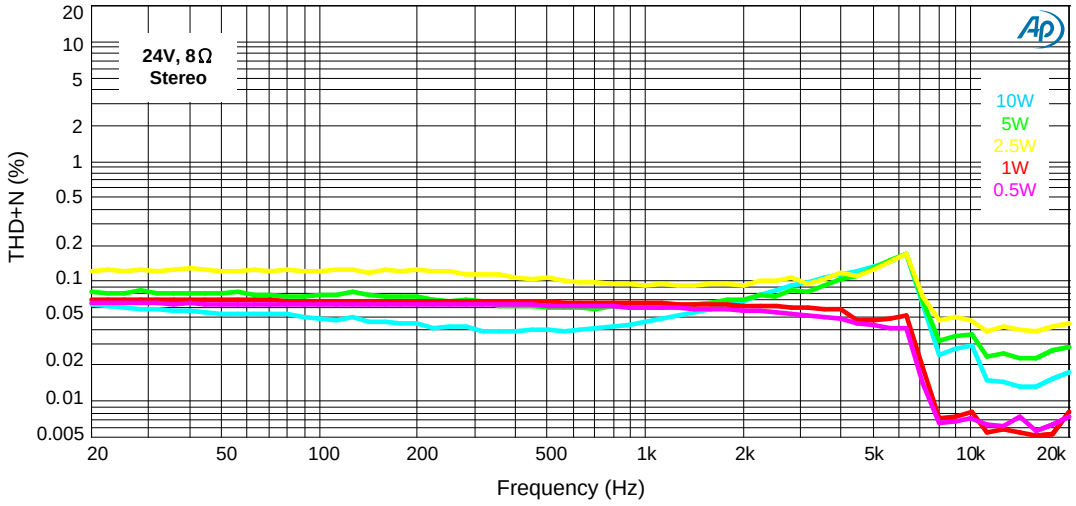
Total Harmonic Distortion + Noise vs. Output Power (BTL)



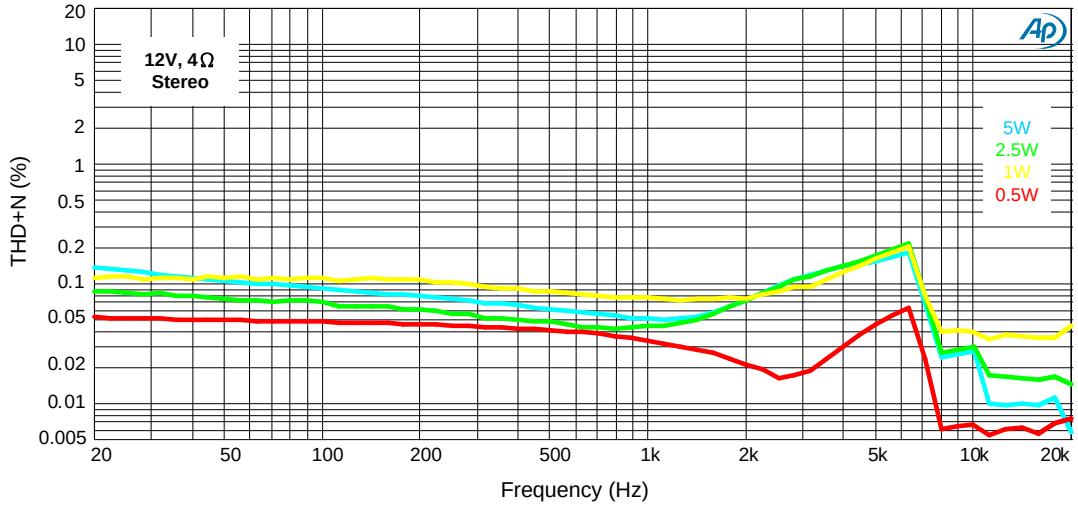
Total Harmonic Distortion + Noise vs. Output Power (BTL)



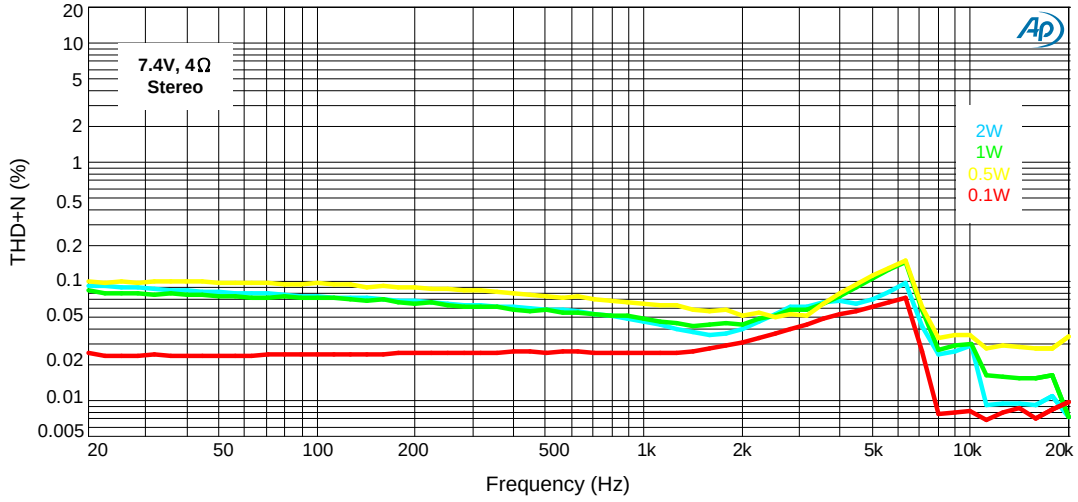
Total Harmonic Distortion + Noise vs. Frequency (BTL)



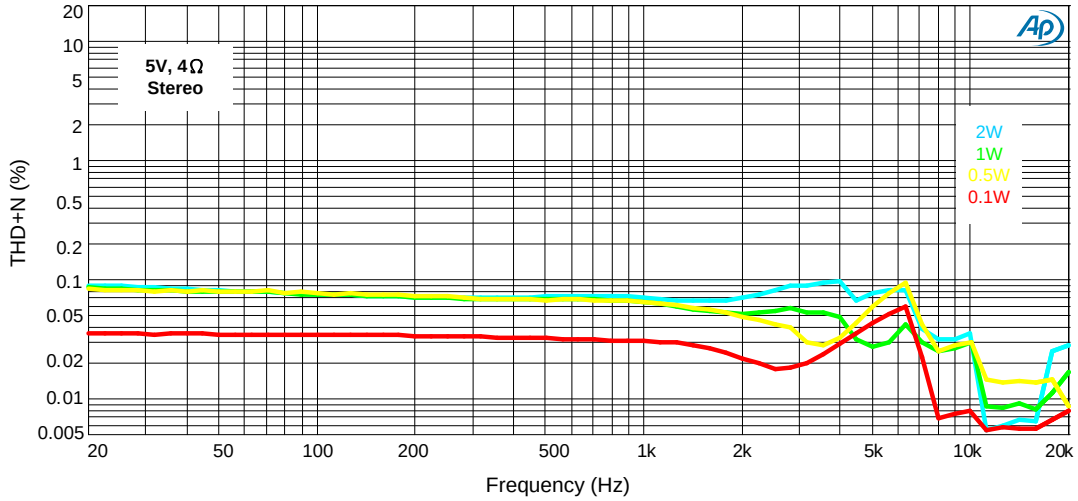
Total Harmonic Distortion + Noise vs. Frequency (BTL)



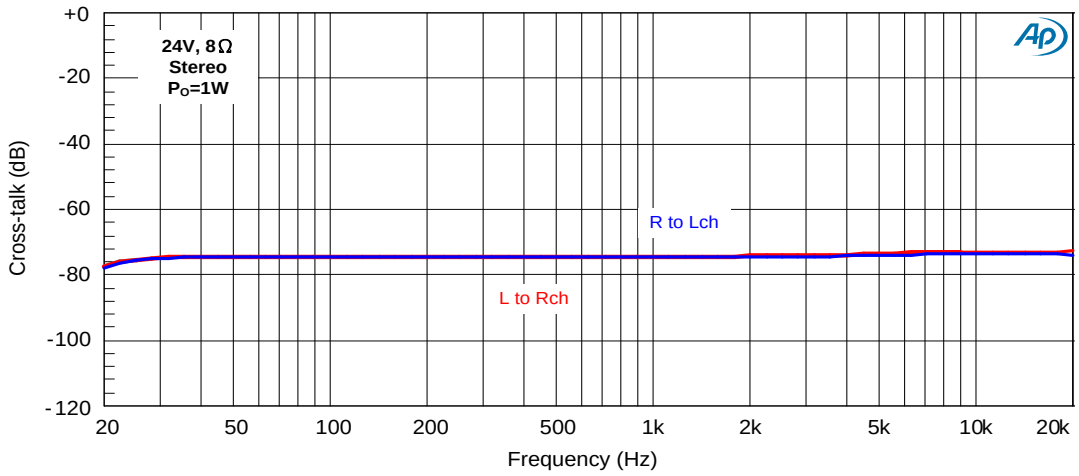
Total Harmonic Distortion + Noise vs. Frequency (BTL)



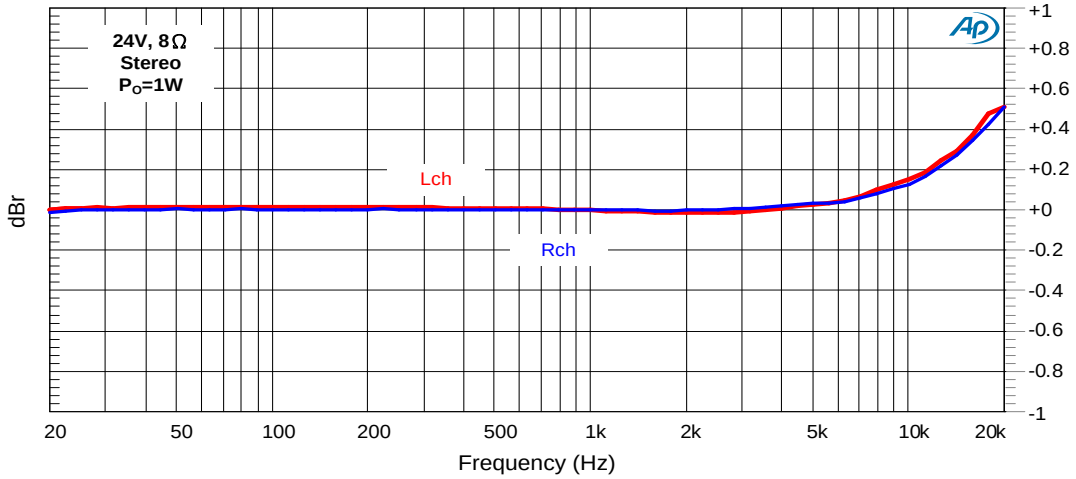
Total Harmonic Distortion + Noise vs. Frequency (BTL)



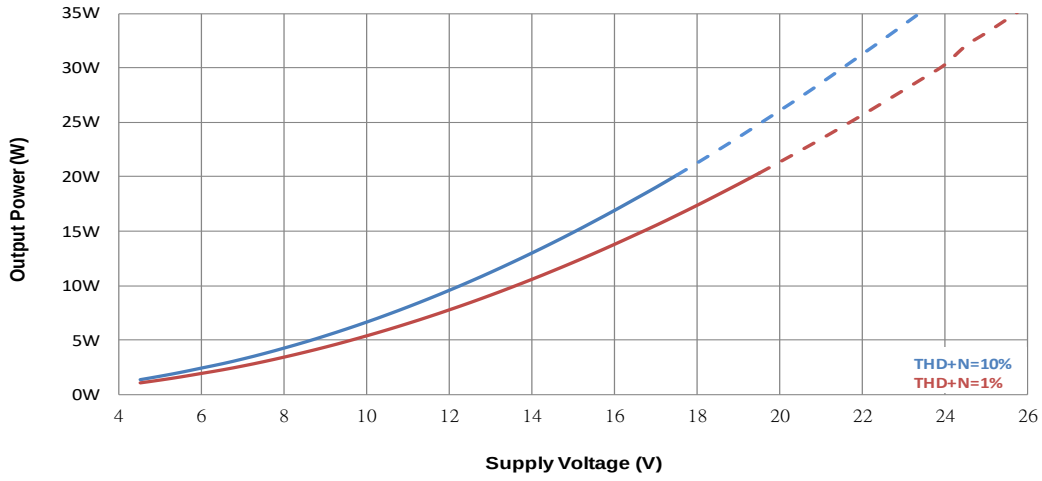
Cross-talk (Stereo, BTL)



Frequency Response (BTL)

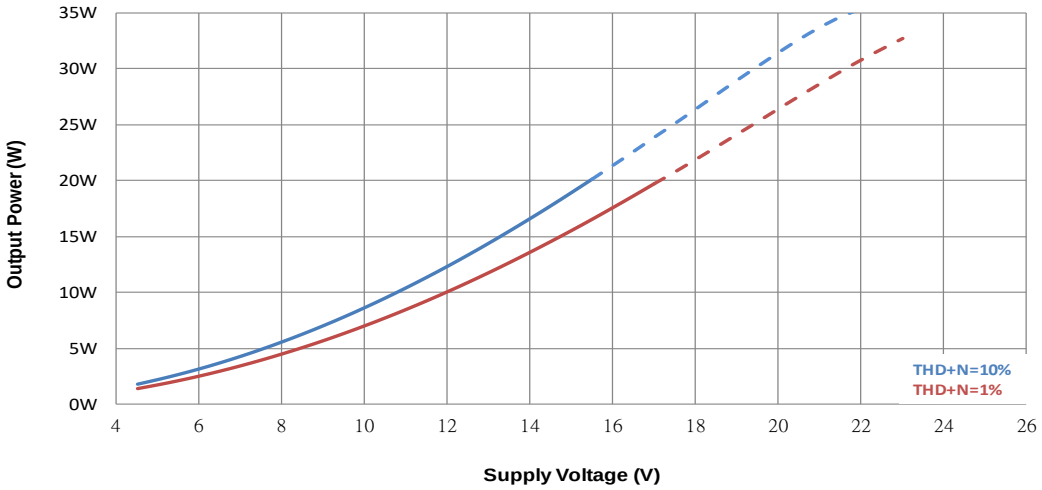


Output Power vs. Supply Voltage (BTL, 8ohm)



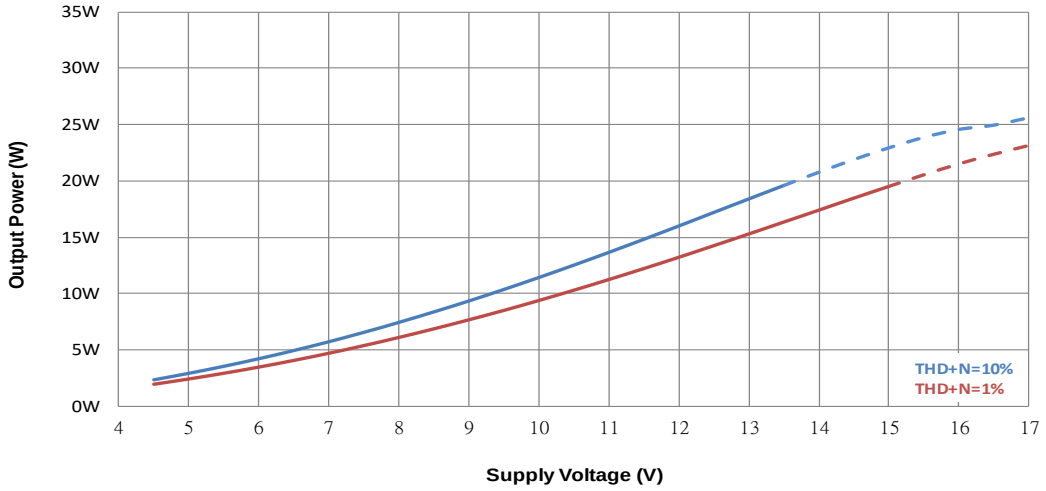
Note: Dashed Line represent thermally limited regions.

Output Power vs. Supply Voltage (BTL, 6ohm)



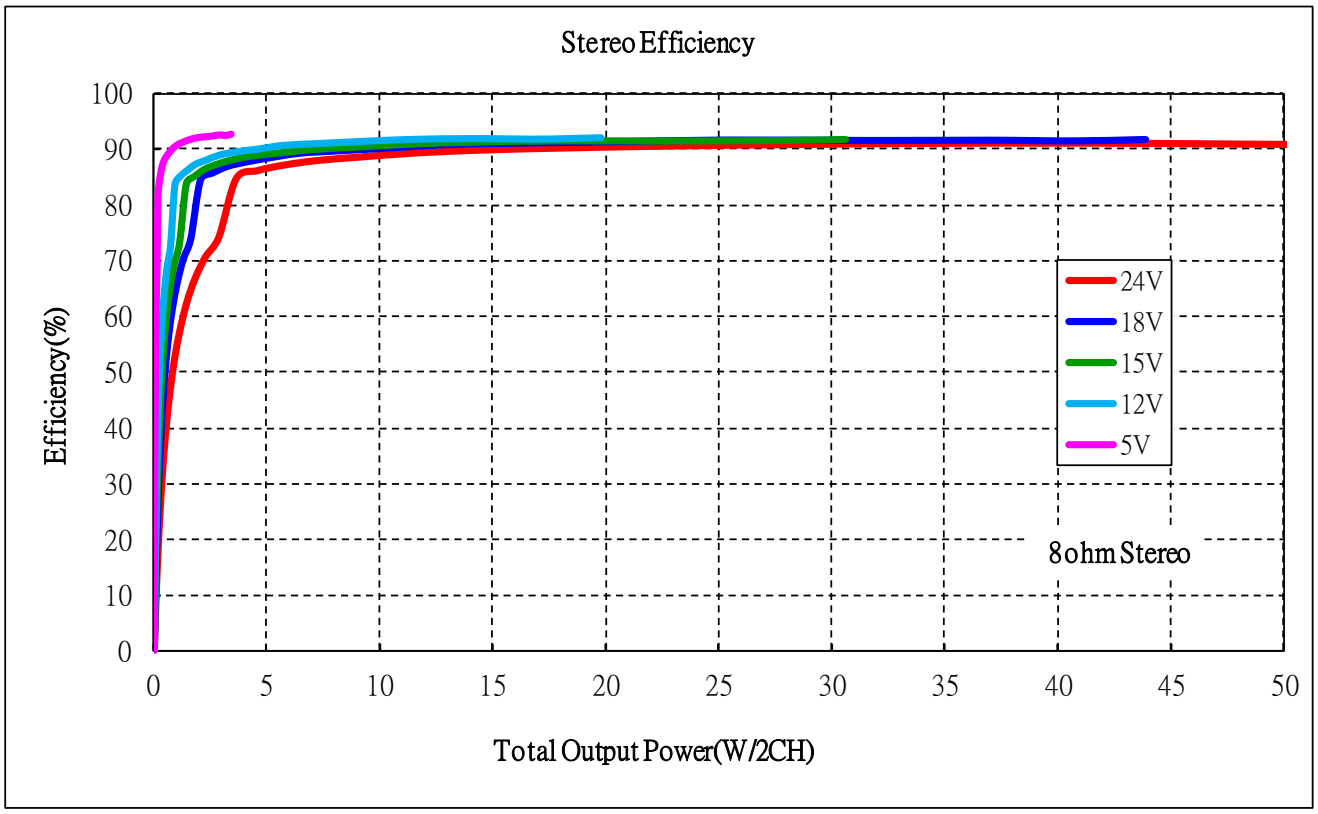
Note: Dashed Line represent thermally limited regions.

Output Power vs. Supply Voltage (BTL, 4ohm)

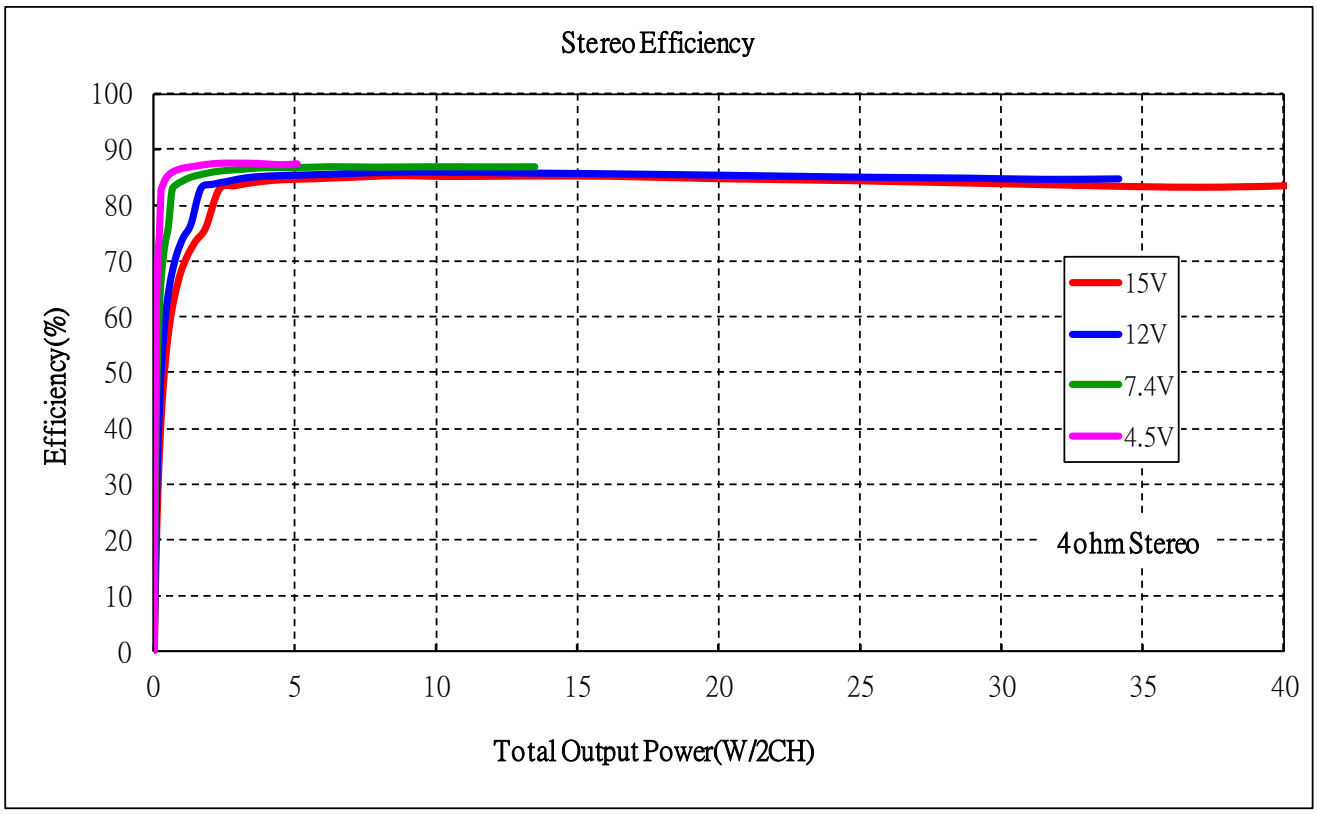


Note: Dashed Line represent thermally limited regions.

Efficiency (Stereo, BTL) with Advanced Quaternary during Power Saving Mode



Efficiency (Stereo, BTL) with Advanced Quaternary during Power Saving Mode



Electrical Characteristics and Specifications for Loudspeaker (cont.)

- **PBTL (Parallel-Bridge-Tied-Load) output for Mono**

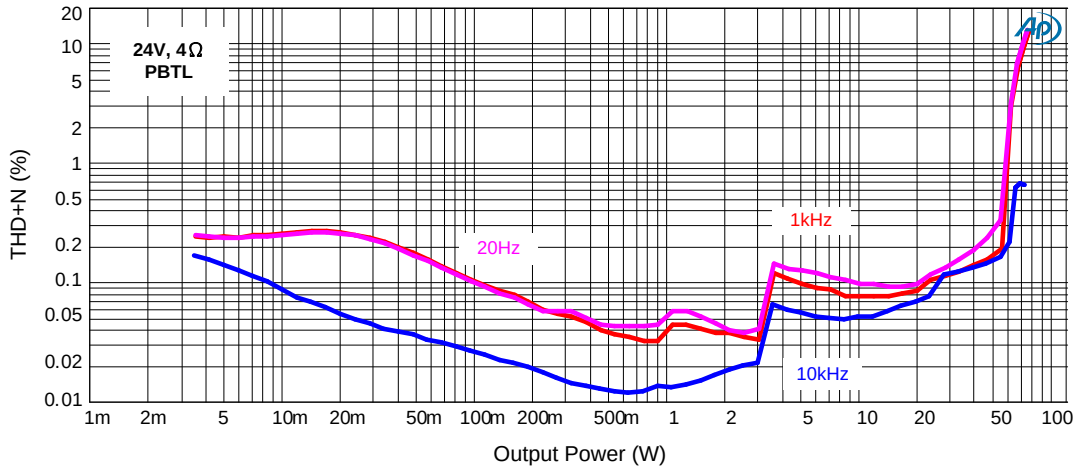
Condition: T_A = 25 °C, DVDD = 3.3V, VDDL = VDDR = 24V, F_S = 48kHz, Load = 4Ω with passive LC lowpass filter (L = 10μ H with R_{DC} = 27mΩ , Cdiff. = 470nF, Ccom. = 100nF); Input is 1kHz sinewave.

Symbol	Parameter	Condition	Input Level	Min	Typ	Max	Units
P_O (Note 9)	RMS Output Power (THD + N = 0.18%)				40		W
	RMS Output Power (THD + N = 0.15%)				30		W
	RMS Output Power (THD + N = 0.09%)				20		W
THD+N	Total Harmonic Distortion + Noise	P_o = 15W			0.08		%
SNR	Signal to Noise Ratio (Note 8)	Maximum power at THD < 1% @ 1kHz			102		dB
DR	Dynamic Range (Note 8)		-60dB		106		dB
Vn	Output Noise (Note 8)	20Hz to 20kHz			110		uV
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = $1V_{RMS}$ @ 1kHz			-72		dB

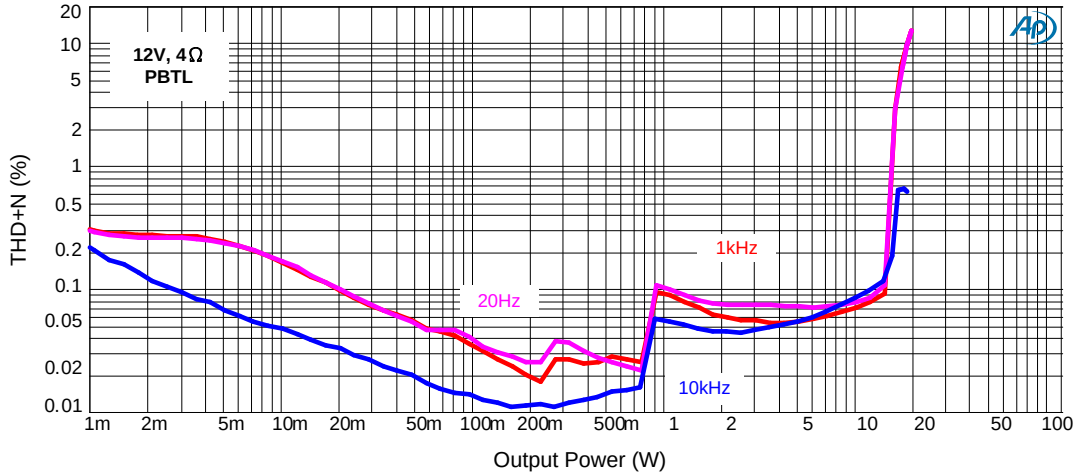
Note 8: Measured with A-weighting filter.

Note 9: Thermal dissipation is limited by package type and PCB design. The external heat-sink or system cooling method should be adopted for maximum power output.

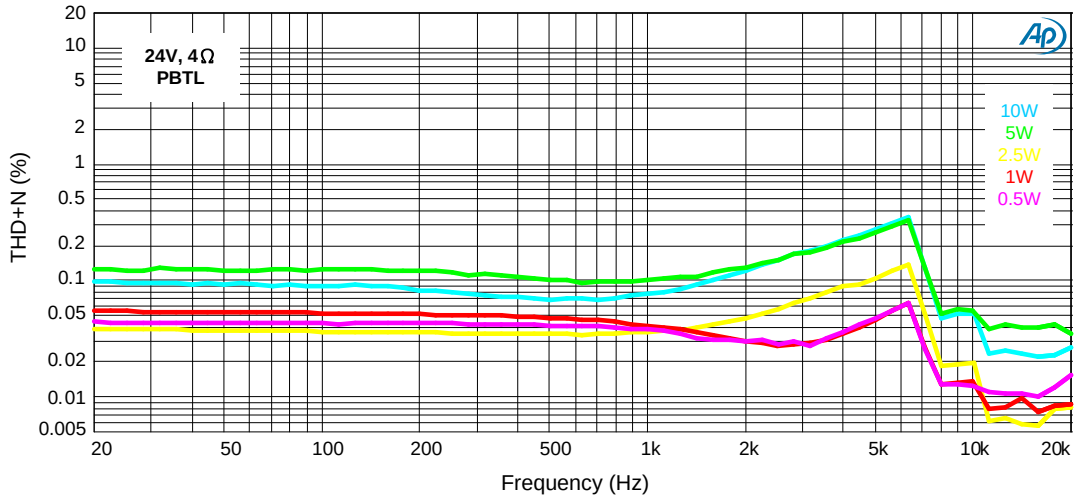
Total Harmonic Distortion + Noise vs. Output Power (PBTL)



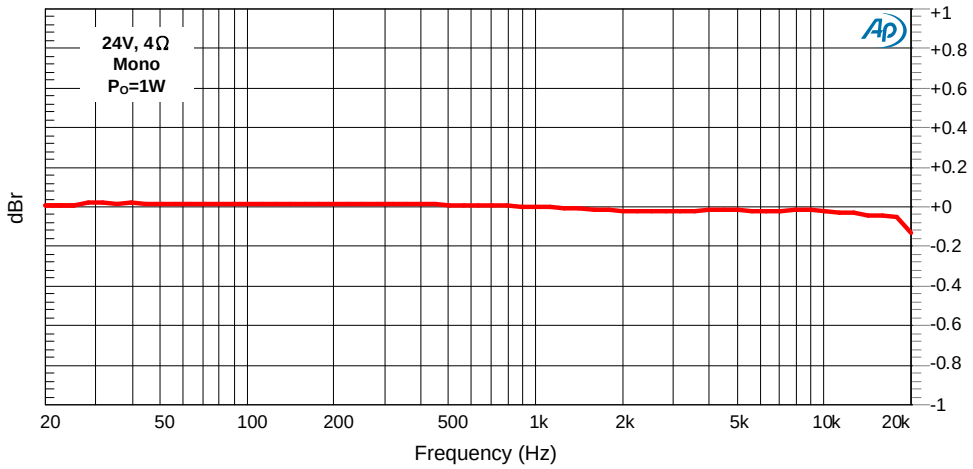
Total Harmonic Distortion + Noise vs. Output Power (PBTL)



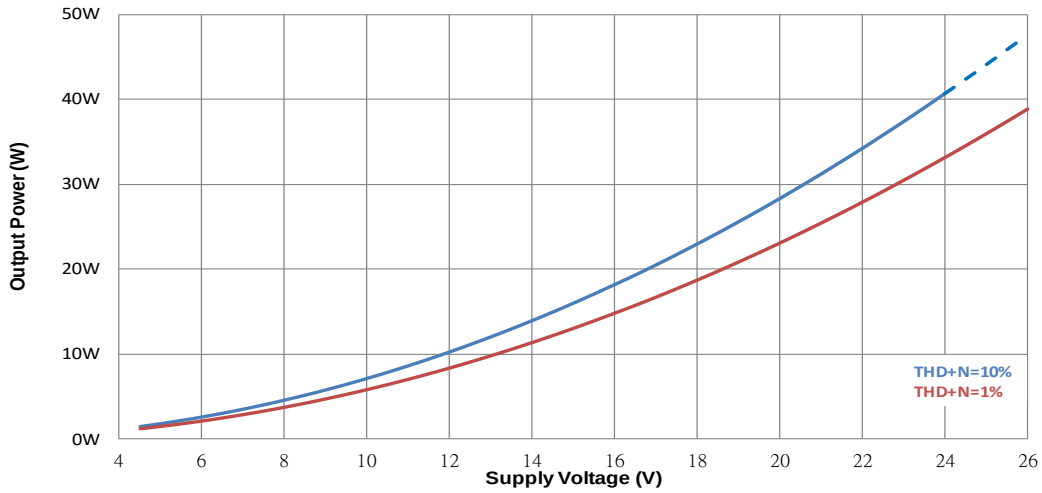
Total Harmonic Distortion + Noise vs. Frequency (PBTL)



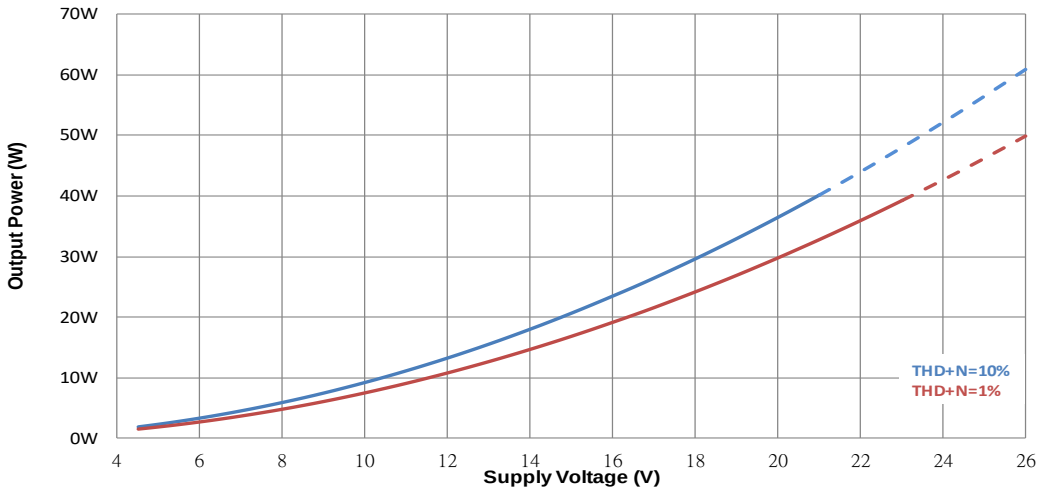
Frequency Response (PBTL)



Output Power vs. Supply Voltage (PBTL, 8ohm)

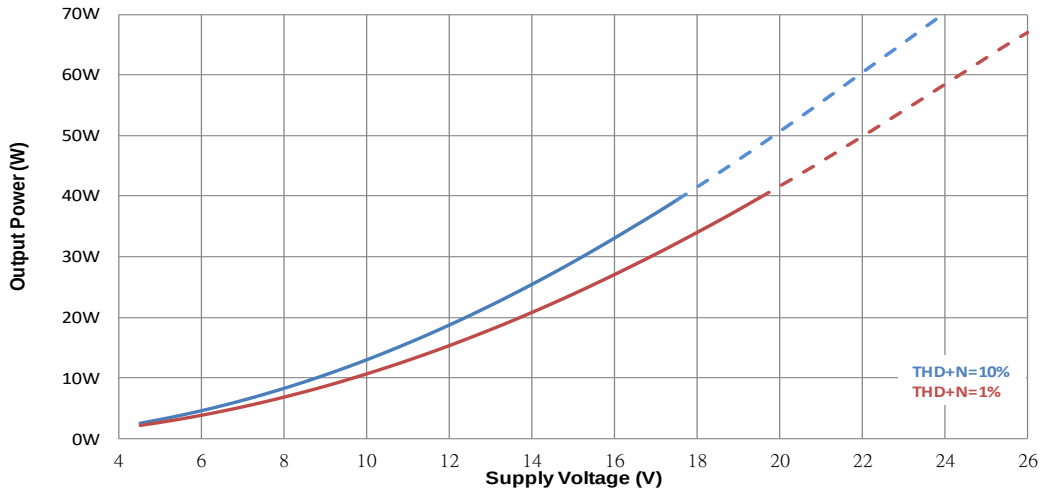


Output Power vs. Supply Voltage (PBTL, 6ohm)



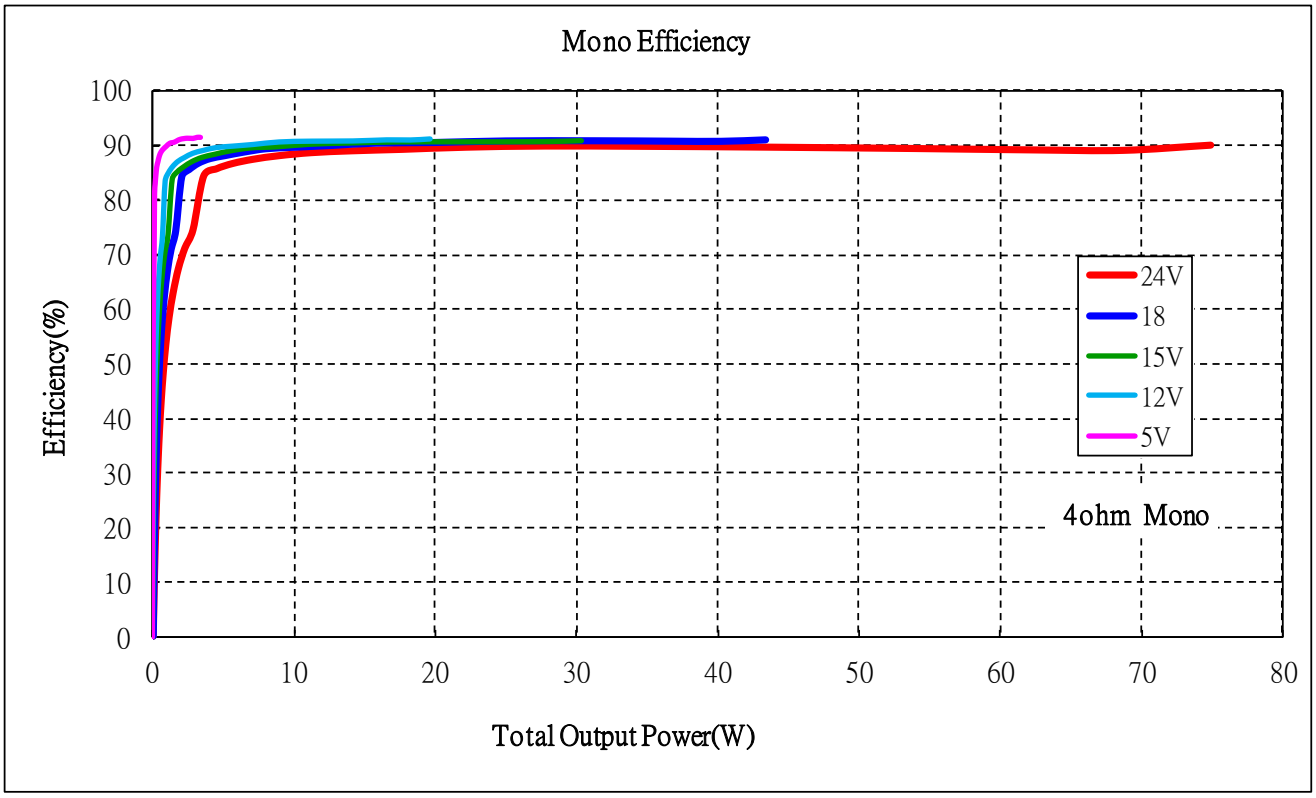
Note: Dashed Line represent thermally limited regions.

Output Power vs. Supply Voltage (PBTL, 4ohm)



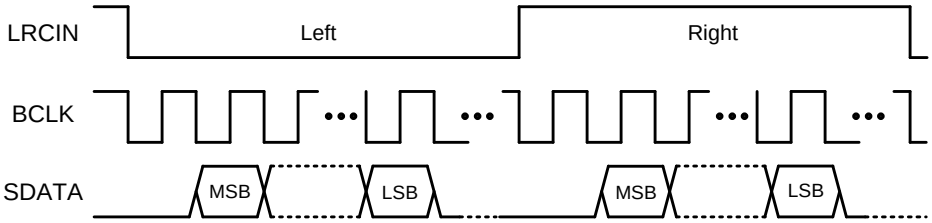
Note: Dashed Line represent thermally limited regions.

Efficiency (Mono, PBTL) with Advanced Quaternary during Power Saving Mode

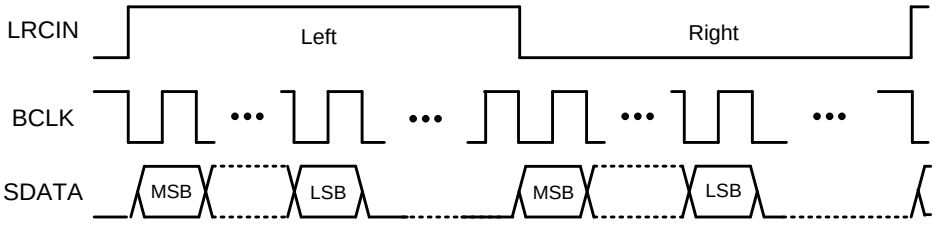


Interface configuration

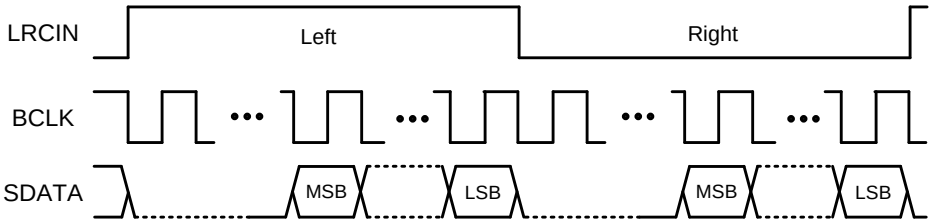
- I^2S



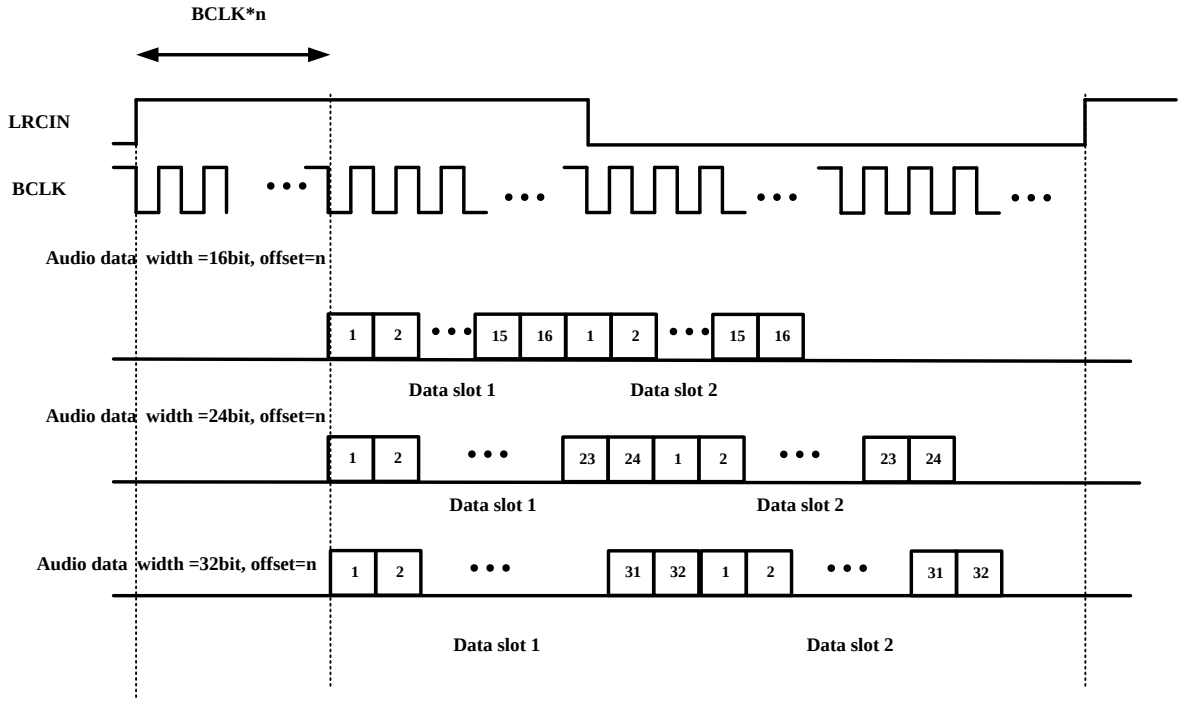
- Left-Alignment



- Right-Alignment



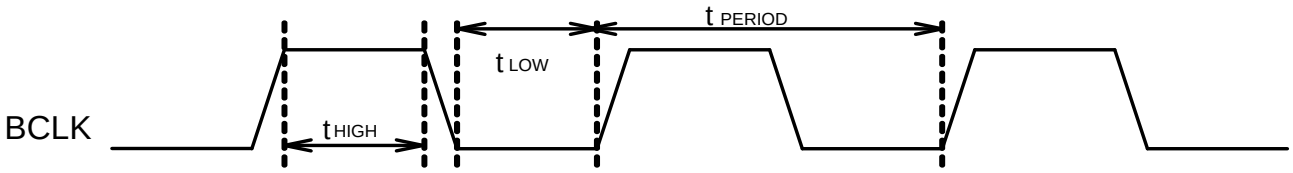
- TDM



AD82050 device audio data formats, bit depths, clock rates, and channel numbers
Table 1

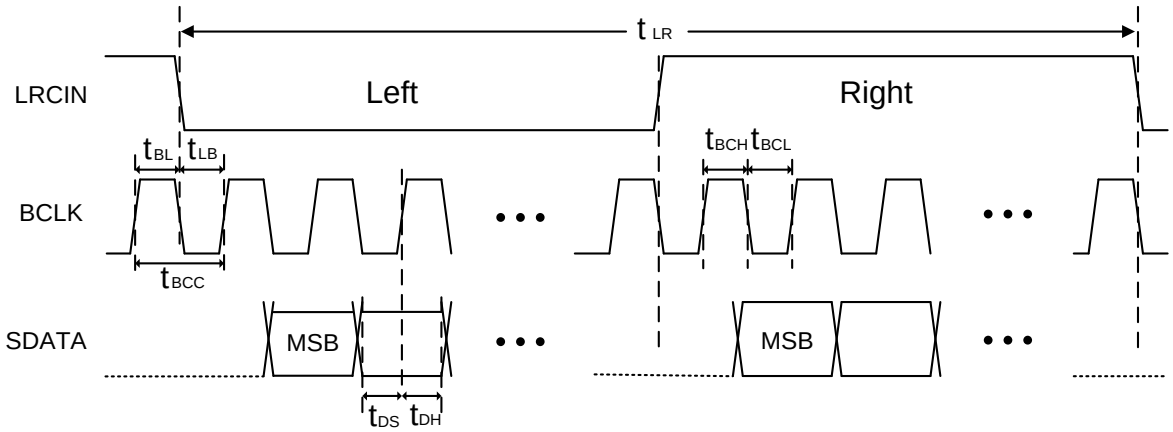
Format	Data Bits	LRCIN Frequency (kHz)	BCLK Rate (FS)	Channel Numbers
I^2S/LJ/RJ	32, 24, 16	48, 96	32x, 48x, 64x	2
	32, 24, 16	16	32x,48x, 64x	2
	32, 16	8	32x, 64x	2
TDM	32, 24,16	48, 96	64x, 128x, 192x, and 256x for 32 data bits	2, 4, 8 channels for 32 data bits
			48x,96x,and 192X for 24 data bits	2, 4, 8 channels for 24 data bits
			32x,64x,96x,128x,192x and 256x for 16 data bits	2, 4, 6, 8,12,16 channels for 16 data bits
	32, 24, 16	16	64x, 128x,192x, and 256x for 32 data bits	2, 4, 6, 8 channels for 32 data bits
			48x, 96x,and 192X for 24 data bits	2, 4, 8 channels for 24 data bits
			32X, 64x,96x, and 128x for 16 data bits	2,4, 6, 8 channel for 16 data bits
	32, 24,16	8	64x, 128x, 192x, and 256x for 32 data bits	2, 4, 8 channels for 32 data bits
			96x,and 192X for 24 data bits	4, 8 channels for 24 data bits
			32x,64x,96x,128x,192x and 256x for 16 data bits	2, 4, 6, 8,12,16 channels for 16 data bits

- System Clock Timing



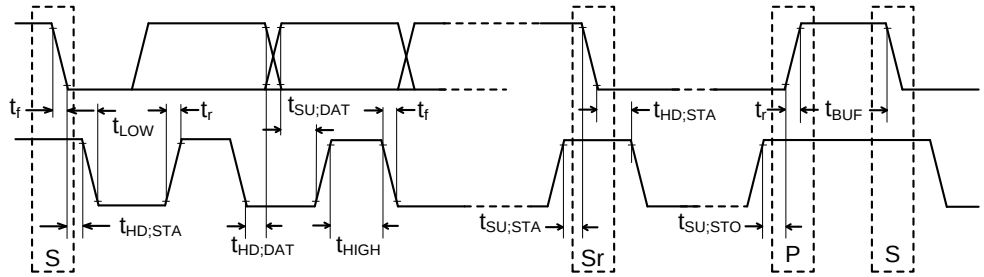
t_{HIGH} ≧ 81.83 ns , t_{LOW} ≧ 81.83 ns , t_{PERIOD} ≧ 162.7 ns Default setting,PLL is enable

- Timing Relationship (Using I^2S format as an example)



Symbol	Parameter	Min	Typ	Max	Units
t_{LR}	LRCIN Period ($1/F_S$)	10.4		31.25	μs
t_{BL}	BCLK Rising Edge to LRCIN Edge	12.5			ns
t_{LB}	LRCIN Edge to BCLK Rising Edge	12.5			ns
t_{BCC}	BCLK Period (Min. is for 96k with 1/256Fs, Max. is for 16k with 1/64 Fs)	40.69		1302	ns
t_{BCH}	BCLK Pulse Width High	20.35		651	ns
t_{BCL}	BCLK Pulse Width Low	20.35		651	ns
t_{DS}	SDATA Set-Up Time	12.5			ns
t_{DH}	SDATA Hold Time	12.5			ns

- I^2C Timing



Parameter	Symbol	Standard Mode		Fast Mode		Unit
		MIN.	MAX.	MIN.	MAX.	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Hold time for repeated START condition	$t_{HD,STA}$	4.0	---	0.6	---	μs
LOW period of the SCL clock	t_{LOW}	4.7	---	1.3	---	μs
HIGH period of the SCL clock	t_{HIGH}	4.0	---	0.6	---	μs
Setup time for repeated START condition	$t_{SU;STA}$	4.7	---	0.6	---	μs
Hold time for I^2C bus data	$t_{HD;DAT}$	0	3.45	0	0.9	μs
Setup time for I^2C bus data	$t_{SU;DAT}$	250	---	100	---	ns
Rise time of both SDA and SCL signals	t_r	---	1000	---	300	ns
Fall time of both SDA and SCL signals	t_f	---	300	---	300	ns
Setup time for STOP condition	$t_{SU;STO}$	4.0	---	0.6	---	μs
Bus free time between STOP and the next START condition	t_{BUF}	4.7	---	1.3	---	μs
Capacitive load for each bus line	C_b		400		400	pF

Operation Description

AD82050 has a built-in PLL internally, the default volume is muted. AD82050 will activate while the de-mute command via I^2C is programmed.

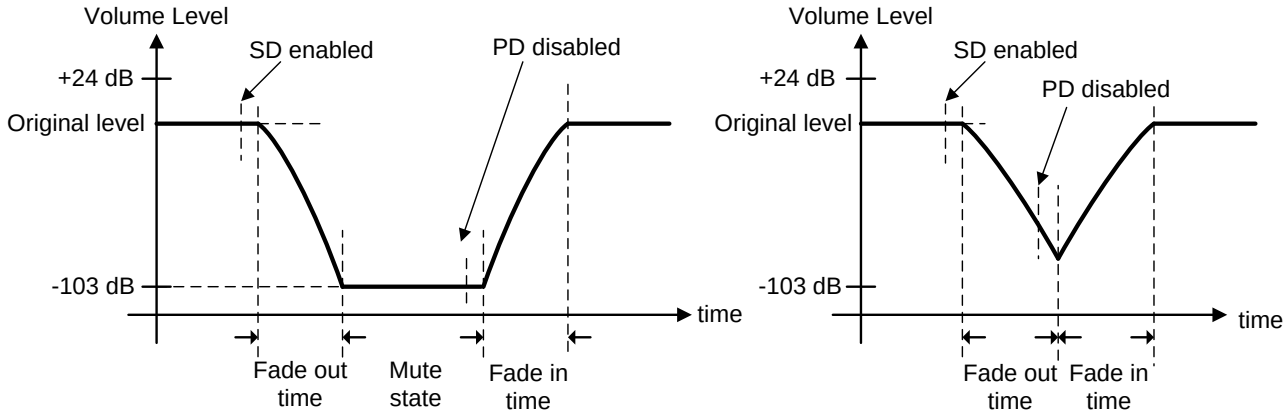
- Internal PLL

  AD82050 has a built-in PLL internally, the BCLK / FS ratio, which is selected by I^2C control interface. The clock inputted into the BCLK pin becomes the frequency of multiple edge evaluation in chip internally.

Fs	BCLK / FS Setting Ratio for PLL	BCLK Frequency	Multiple edge evaluation for bit clock	PWM Career Frequency
96kHz	64x	6.144MHz	32x	384kHz
48kHz	64x	3.072MHz	64x	384kHz
44.1kHz	64x	2.8224MHz	64x	352.8kHz
32kHz	64x	2.048MHz	64x	256kHz
16kHz	64x	1.024MHz	128x	256kHz
8kHz	64x	0.512MHz	256x	256kHz

- Power down control

  AD82050 has a built-in volume fade-in / fade-out design for PD / Mute function. The relative PD timing diagrams for loudspeakers are shown below.



$$(10^{\frac{target(dB)}{20}} - 10^{\frac{original(dB)}{20}}) x128x(1/96K)$$

(Note: Address 0x18 B[3:2] = 00)

The volume level will be decreased to -∞dB in several LRCIN cycles. Once the fade-out procedure is finished, AD82050 will turn off the power stages, clock signals (for digital circuits) and current (for analog circuits). After $\overline{PD}$ pin is pulled low, AD82050 requires T_{fade} to finish the forementioned work before entering power down state. User can not program AD82050 during power down state. Also, all settings in the registers will remain intact unless DVDD is removed.

If the PD signal is removed during the fade-out procedure (above, right figure), AD82050 will still execute the fade-in procedure. In addition, AD82050 will establish the analog circuits' bias current and send the clock signals to digital circuits. Afterwards, AD82050 will return to its normal status.

- Self-protection circuits

AD82050 has built-in protection circuits including thermal, short-circuit and under-voltage detection circuits.

(i) When the internal junction temperature is higher than 155℃, power stages will be turned off and AD82050 will return to normal operation once the temperature drops to 120℃. The temperature values may vary around 10%.

(ii) The short-circuit protection circuit protects the output stage when the wires connected to loudspeakers are shorted to each other or GND / VDD. For normal 24V operations, the current flowing through the power stage will be less than 8A for stereo configuration or less than 14A for mono configuration. Otherwise, the short-circuit detectors may pull the $\overline{ERROR}$ pin to DGND, disabling the output stages. When the over-temperature or short-circuit condition occurs, the open-drain $\overline{ERROR}$ pin will be pulled low and latched into ERROR state..

Once short-circuit condition is removed, AD82050 will exit ERROR state when one of the following conditions is met: (1) $\overline{PD}$ pin is pulled low, (2) Master mute is enabled through the I^2C interface.

(iii) Once the DVDD voltage is lower than 2.8V, AD82050 will turn off its loudspeaker power stages. When DVDD becomes higher than 3V, AD82050 will return to normal operation.

(iv) Once the PVDD voltage is higher than 29.4V, AD82050 will turn off its loudspeaker power stages. When PVDD becomes lower than 28.4V, AD82050 will return to normal operation.

(v) Once the PVDD voltage is lower than 3.9V, AD82050 will turn off its loudspeaker power stages. When PVDD becomes higher than 4.25V, AD82050 will return to normal operation.

- Anti-pop design

  AD82050 will generate appropriate control signals to suppress pop sounds during initial power on/off, power down/up, mute, and volume level changes.

- I^2C Chip Select

  $\overline{\text{ERROR}}$ is an input pin during power up. It can be pulled High (15-kΩ pull up) or Low (15-kΩ pull down). Low indicates an I^2C address of 0x30, and high an address of 0x34.

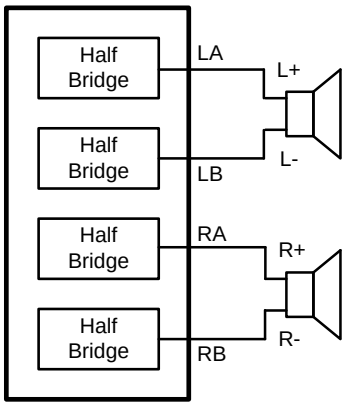
- Output configuration

  AD82050 can be configured to mono (PBTL) via I^2C control, set register MONO_EN=1 (register 0X07, B[3]) and MONO_KEY = 3006 (HEX) (register 0X12 & 0X13) to entry PBTL configuration.

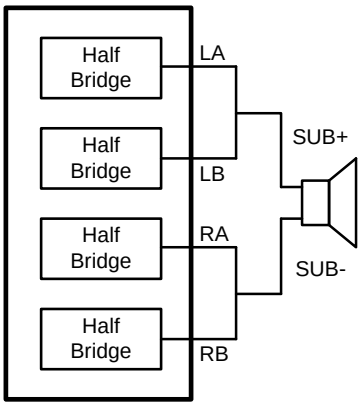
Table 2

MONO_EN & MONO_KEY	Configuration Mode
Others	Stereo
Mono via I^2C control (MONO_EN=1 and MONO_KEY=3006(HEX))	Mono

Configuration figures:



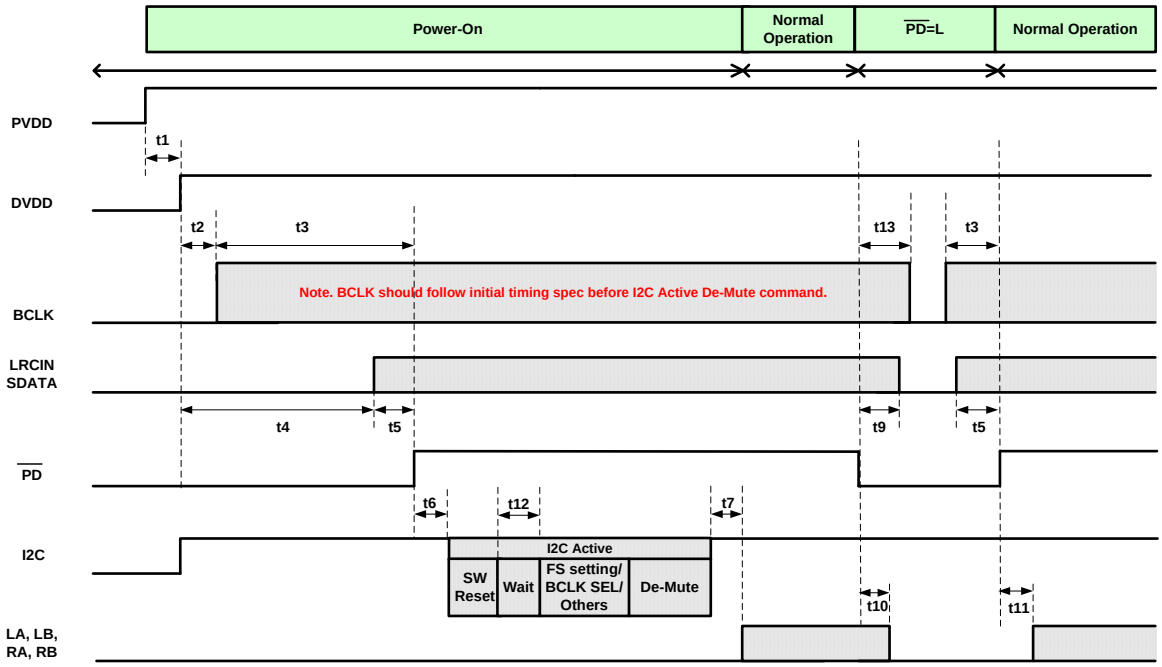
STEREO



MONO

- Power on sequence

Hereunder is AD82050's power on sequence. Give a de-mute command via I^2C when the whole system is stable.



Note:

Please be noted below sequence shall be follow up with "I2C Active" processing,

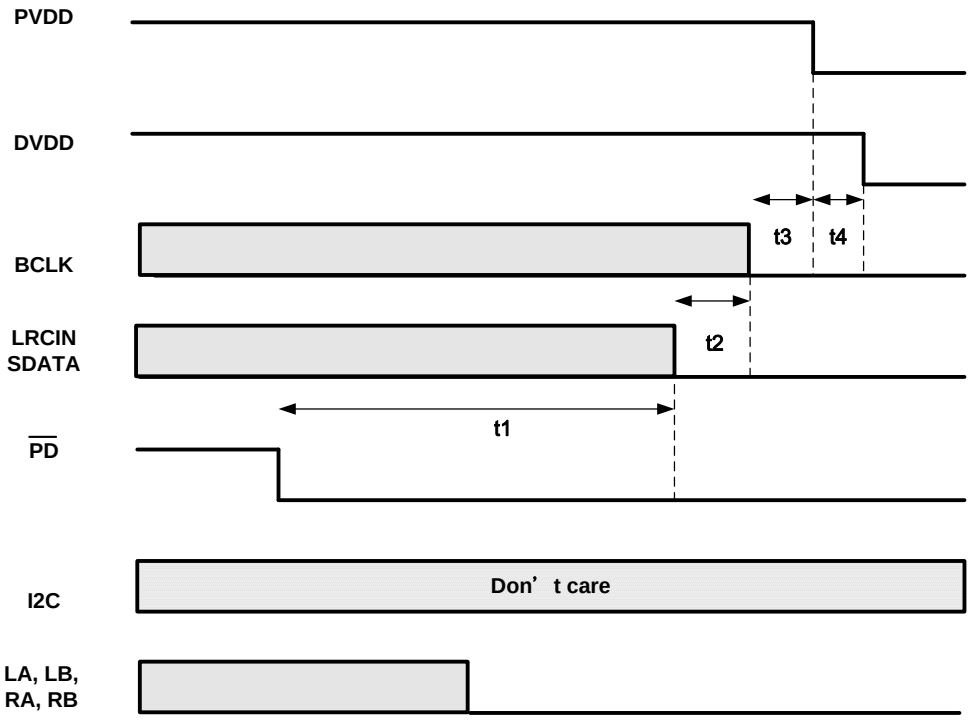
(1) Set S/W reset bit (0X02 B[4]) = 0 → (2) Delay 5ms → (3) Set S/W reset bit (0X02 B[4]) = 1 → (4) Delay 20ms → (5) Set all channels = mute (setting address 0X02 B[3] = 1) → (6) Set sampling frequency and other registers (except setting address 0X02 B[4:3]) → (7) Set all channels = de-mute (setting address 0X02 B[3]= 0)

Symbol	Condition	Min	Max	Units
t1		0	-	msec
t2		0	-	msec
t3		10	-	msec
t4		0	-	msec
t5		10	-	msec
t6		10	-	msec
t7		-	0.1	msec
t8		25	-	msec
t9		35 (FADE_SPEED = 00) 70 (FADE_SPEED = 01) 140 (FADE_SPEED = 10) 280 (FADE_SPEED = 11)	-	msec

t10		-	35 (FADE_SPEED = 00) 70 (FADE_SPEED = 01) 140 (FADE_SPEED = 10) 280 (FADE_SPEED = 11)	msec
t11		-	20	msec
t12		20		msec
t13		35 (FADE_SPEED = 00) 70 (FADE_SPEED = 01) 140 (FADE_SPEED = 10) 280 (FADE_SPEED = 11)		msec

- Power off sequence

Hereunder is AD82050's power off sequence.



Symbol	Condition	Min	Max	Units
t1		35 (FADE_SPEED = 00) 70 (FADE_SPEED = 01) 140 (FADE_SPEED = 10) 280 (FADE_SPEED = 11)	-	msec
t2		0	-	msec
t3		1	-	msec
t4		1	-	msec

I²C-Bus Transfer Protocol

- Introduction

AD82050 employs I²C-bus transfer protocol. Two wires, serial data and serial clock carry information between the devices connected to the bus. Each device is recognized by a unique 7-bit address and can operate as either a transmitter or a receiver. The master device initiates a data transfer and provides the serial clock on the bus. AD82050 is always an I²C slave device.

- Protocol

  - START and STOP condition

START is identified by a high to low transition of the SDA signal. A START condition must precede any command for data transfer. A STOP is identified by a low to high transition of the SDA signal. A STOP condition terminates communication between AD82050 and the master device on the bus. In both START and STOP, the SCL is stable in the high state.

  - Data validity

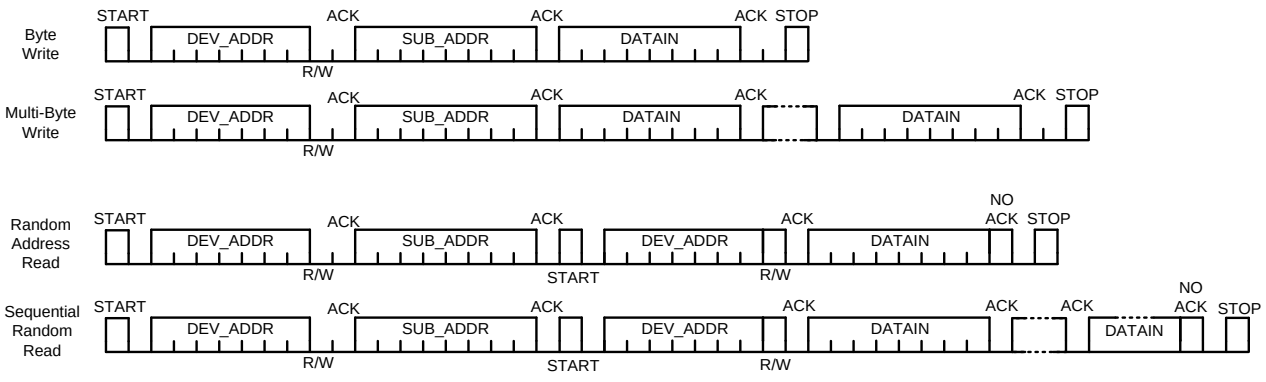
The SDA signal must be stable during the high period of the clock. The high or low change of SDA only occurs when SCL signal is low. AD82050 samples the SDA signal at the rising edge of SCL signal.

  - Device addressing

The master generates 7-bit address to recognize slave devices. When AD82050 receives 7-bit address matched with 0110000 or 0110100 ($\overline{\text{ERROR}}$ pin state during power up), AD82050 will acknowledge at the 9th bit (the 8th bit is for R/W bit). The bytes following the device identification address are for AD82050 internal sub-addresses.

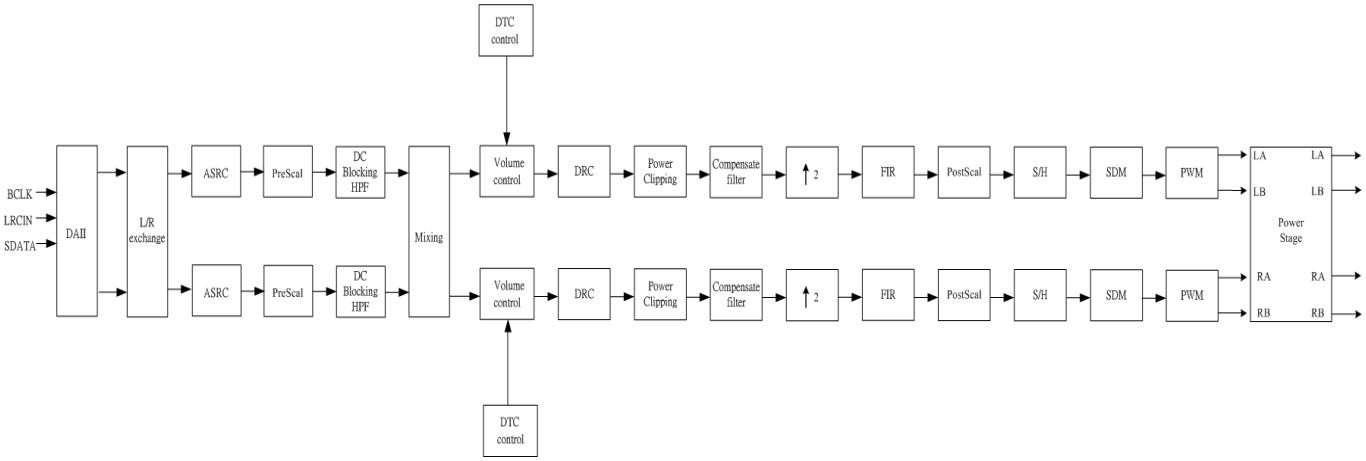
  - Data transferring

Each byte of SDA signaling must consist of 8 consecutive bits, and the byte is followed by an acknowledge bit. Data is transferred with MSB first, as shown in the figure below. In both write and read operations, AD82050 supports both single-byte and multi-byte transfers. Refer to the figure below for detailed data-transferring protocol.



Register Table

The AD82050's audio signal processing data flow is shown below. Users can control these functions by programming appropriate settings in the register table. In this section, the register table is summarized first. The definition of each register follows in the next section.



Address	Register	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]
0X00	SCTL1	IF[2]	IF[1]	IF[0]	LREXC	PWML_X	PWMR_X	Reserved	NG_EN
0X01	SCTL 2	Reserved		FS[1]	FS[0]	PMF[3]	PMF[2]	PMF[1]	PMF[0]
0X02	SCTL 3	A_SEL_FAULT	DC_HPB	LV_UVSEL	SW_RSTB	MUTE	CM1	CM2	CompSDMEn
0X03	MVOL	MV[7]	MV[6]	MV[5]	MV[4]	MV[3]	MV[2]	MV[1]	MV[0]
0X04	C1VOL	C1V[7]	C1V[6]	C1V[5]	C1V[4]	C1V[3]	C1V[2]	C1V[1]	C1V[0]
0X05	C2VOL	C2V[7]	C2V[6]	C2V[5]	C2V[4]	C2V[3]	C2V[2]	C2V[1]	C2V[0]
0X06	HVUV	DIS_HVUV	DIS_LVUV_FADE	DIS_OV_FADE	Reserved		HVUVSEL[2]	HVUVSEL[1]	HVUVSEL[0]
0X07	SCTL 4	C1MX_EN	C2MX_EN	PC1_EN	PL1_EN	MONO_EN	PC2_EN	PL2_EN	Reserved
0X08	PWM	PSM_EN	QD_EN	AQ_EN	D_MOD	PWM_SEL	Reserved		
0X09	QT_SW_LEVEL	QT_SW_WINDOW[2]	QT_SW_WINDOW[1]	QT_SW_WINDOW[0]	QT_SW_LEVEL[4]	QT_SW_LEVEL[3]	QT_SW_LEVEL[2]	QT_SW_LEVEL[1]	QT_SW_LEVEL[0]
0X0A	PWM_DUTY	Q_DUTY[7]	Q_DUTY[6]	Q_DUTY[5]	Q_DUTY[4]	Q_DUTY[3]	Q_DUTY[2]	Q_DUTY[1]	Q_DUTY[0]
0X0B	Reserved	Reserved							
0X0C	PRST	PRST[7]	PRST[6]	PRST[5]	PRST[4]	PRST[3]	PRST[2]	PRST[1]	PRST[0]
0X0D	PRSM	PRSM[7]	PRSM[6]	PRSM[5]	PRSM[4]	PRSM[3]	PRSM[2]	PRSM[1]	PRSM[0]
0X0E	PRSB	PRSB[7]	PRSB[6]	PRSB[5]	PRSB[4]	PRSB[3]	PRSB[2]	PRSB[1]	PRSB[0]
0X0F	POST	POST[7]	POST[6]	POST[5]	POST[4]	POST[3]	POST[2]	POST[1]	POST[0]
0X10	POSM	POSM[7]	POSM[6]	POSM[5]	POSM[4]	POSM[3]	POSM[2]	POSM[1]	POSM[0]
0X11	POSB	POSB[7]	POSB[6]	POSB[5]	POSB[4]	POSB[3]	POSB[2]	POSB[1]	POSB[0]
0X12	MK_HBYTE	MK_HBYTE[7]	MK_HBYTE[6]	MK_HBYTE[5]	MK_HBYTE[4]	MK_HBYTE[3]	MK_HBYTE[2]	MK_HBYTE[1]	MK_HBYTE[0]

0X13	MK_LBYTE	MK_LBYTE[7]	MK_LBYTE[6]	MK_LBYTE[5]	MK_LBYTE[4]	MK_LBYTE[3]	MK_LBYTE[2]	MK_LBYTE[1]	MK_LBYTE[0]
0X14	ID	DN[3]	DN[2]	DN[1]	DN[0]	VN[3]	VN[2]	VN[1]	VN[0]
0X15	PCT	PCT[7]	PCT[6]	PCT[5]	PCT[4]	PCT[3]	PCT[2]	PCT[1]	PCT[0]
0X16	PCM	PCM[7]	PCM[6]	PCM[5]	PCM[4]	PCM[3]	PCM[2]	PCM[1]	PCM[0]
0X17	PCB	PCB[7]	PCB[6]	PCB[5]	PCB [4]	PCB [3]	PCB [2]	PCB [1]	PCB [0]
0X18	NGR	NG_CNT_SEL[1]	NG_CNT_SEL[0]	Reserved	DIS_NG_FADE	FADE_SPEED[1]	FADE_SPEED[0]	NG_GAIN[1]	NG_GAIN[0]
0X19	VFT	MV_FT[1]	MV_FT[0]	C1V_FT[1]	C1V_FT[0]	C2V_FT[1]	C2V_FT[0]	Reserved	
0X1A	NGALT	NGALT[7]	NGALT[6]	NGALT[5]	NGALT[4]	NGALT[3]	NGALT[2]	NGALT[1]	NGALT[0]
0X1B	NGALM	NGALM[7]	NGALM[6]	NGALM[5]	NGALM[4]	NGALM[3]	NGALM[2]	NGALM[1]	NGALM[0]
0X1C	NGALB	NGALB[7]	NGALB [6]	NGALB [5]	NGALB [4]	NGALB [3]	NGALB [2]	NGALB [1]	NGALB [0]
0X1D	NGRLT	NGRLT[7]	NGRLT[6]	NGRLT[5]	NGRLT[4]	NGRLT[3]	NGRLT[2]	NGRLT[1]	NGRLT[0]
0X1E	NGRLM	NGRLM[7]	NGRLM[6]	NGRLM[5]	NGRLM[4]	NGRLM[3]	NGRLM[2]	NGRLM[1]	NGRLM[0]
0X1F	NGRLB	NGRLB[7]	NGRLB [6]	NGRLB[5]	NGRLB[4]	NGRLB [3]	NGRLB [2]	NGRLB [1]	NGRLB [0]
0X20	DRC_ECT	DRC_ECT[7]	DRC_ECT[6]	DRC_ECT[5]	DRC_ECT[4]	DRC_ECT[3]	DRC_ECT[2]	DRC_ECT[1]	DRC_ECT[0]
0X21	DRC_ECB	DRC_ECB[7]	DRC_ECB[6]	DRC_ECB[5]	DRC_ECB[4]	DRC_ECB[3]	DRC_ECB[2]	DRC_ECB[1]	DRC_ECB[0]
0X22	COMP_A0T	COMP_A0T[7]	COMP_A0T[6]	COMP_A0T[5]	COMP_A0T[4]	COMP_A0T[3]	COMP_A0T[2]	COMP_A0T[1]	COMP_A0T[0]
0X23	COMP_A0M	COMP_A0M[7]	COMP_A0M[6]	COMP_ A0M[5]	COMP_A0M[4]	COMP_A0M[3]	COMP_A0M[2]	COMP_A0M[1]	COMP_A0M[0]
0X24	COMP_A0B	COMP_A0B[7]	COMP_A0B[6]	COMP_A0B[5]	COMP_A0B[4]	COMP_A0B[3]	COMP_A0B[2]	COMP_A0B[1]	COMP_A0B[0]
0X25	COMP_A1T	COMP_A1T[7]	COMP_A1T[6]	COMP_A1T[5]	COMP_A1T[4]	COMP_A1T[3]	COMP_A1T[2]	COMP_A1T[1]	COMP_A1T[0]
0X26	COMP_A1M	COMP_A1M[7]	COMP_A1M[6]	COMP_A1M[5]	COMP_A1M[4]	COMP_A1M[3]	COMP_A1M[2]	COMP_A1M[1]	COMP_A1M[0]
0X27	COMP_A1B	COMP_A1B[7]	COMP_A1B[6]	COMP_A1B[5]	COMP_A1B[4]	COMP_A1B[3]	COMP_A1B[2]	COMP_A1B[2]	COMP_A1B[0]
0X28	COMB_B1T	COMP_B1T[7]	COMP_B1T[6]	COMP_B1T[5]	COMP_B1T[4]	COMP_B1T[3]	COMP_B1T[2]	COMP_B1T[1]	COMP_B1T[0]
0X29	COMB_B1M	COMP_B1M[7]	COMP_B1M[6]	COMP_B1M[5]	COMP_B1M[4]	COMP_B1M[3]	COMP_B1M[2]	COMP_B1M[1]	COMP_B1M[0]
0X2A	COMB_B1B	COMP_B1B[7]	COMP_B1B[6]	COMP_B1B[5]	COMP_B1B[4]	COMP_B1B[3]	COMP_B1B[2]	COMP_B1B[1]	COMP_B1B[0]
0X2B	SCTL 5	Reserved		WORD_WIDTH_SEL[1]	WORD_WIDTH_SEL[0]	SDATAO_CTRL	I2S_DO_SEL[2]	I2S_DO_SEL[1]	I2S_DO_SEL[0]
0X2C	TDM_O	TDM_O[7]	TDM_O[6]	TDM_O[5]	TDM_O[4]	TDM_O[3]	TDM_O[2]	TDM_O[2]	TDM_O[1]
0X2D	AAT	AAT[7]	AAT[6]	AAT[5]	AAT[4]	AAT[3]	AAT[2]	AAT[1]	AAT[0]
0X2E	AAM	AAM[7]	AAM[6]	AAM[5]	AAM[4]	AAM[3]	AAM[2]	AAM[1]	AAM[0]
0X2F	AAB	AAB[7]	AAB[6]	AAB[5]	AAB[4]	AAB[3]	AAB[2]	AAB[1]	AAB[0]
0X30	DAT	DAT[7]	DAT[6]	DAT[5]	DAT[4]	DAT[3]	DAT[2]	DAT[1]	DAT[0]
0X31	DAM	DAM[7]	DAM[6]	DAM[5]	DAM[4]	DAM[3]	DAM[2]	DAM[1]	DAM[0]
0X32	DAB	DAB[7]	DAB[6]	DAB[5]	DAB[4]	DAB[3]	DAB[2]	DAB[1]	DAB[0]
0X33	DRC_TH_T	DRC_TH_T[7]	DRC_TH_T[6]	DRC_TH_T[5]	DRC_TH_T[4]	DRC_TH_T[3]	DRC_TH_T[2]	DRC_TH_T[1]	DRC_TH_T[0]
0X34	DRC_TH_M	DRC_TH_M[7]	DRC_TH_M[6]	DRC_TH_M[5]	DRC_TH_M[4]	DRC_TH_M[3]	DRC_TH_M[2]	DRC_TH_M[1]	DRC_TH_M[0]
0X35	DRC_TH_B	DRC_TH_B[7]	DRC_TH_B[6]	DRC_TH_B[5]	DRC_TH_B[4]	DRC_TH_B[3]	DRC_TH_B[2]	DRC_TH_B[1]	DRC_TH_B[0]
0X36	SLT	SLT[7]	SLT[6]	SLT[5]	SLT[4]	SLT[3]	SLT[2]	SLT[1]	SLT[0]

0X37	SLM	SLM[7]	SLM[6]	SLM[5]	SLM[4]	SLM[3]	SLM[2]	SLM[1]	SLM[0]
0X38	SLB	SLB[7]	SLB[6]	SLB[5]	SLB[4]	SLB[3]	SLB[2]	SLB[1]	SLB[0]
0X39	I2SGT	I2SGT[7]	I2SGT[6]	I2SGT[5]	I2SGT[4]	I2SGT[3]	I2SGT[2]	I2SGT[1]	I2SGT[0]
0X3A	I2SGM	I2SGM[7]	I2SGM[6]	I2SGM[5]	I2SGM[4]	I2SGM[3]	I2SGM[2]	I2SGM[1]	I2SGM[0]
0X3B	I2SGB	I2SGB[7]	I2SGB[6]	I2SGB[5]	I2SGB[4]	I2SGB[3]	I2SGB[2]	I2SGB[1]	I2SGB[0]
0X3C	DTC	DTC_EN	DTC_TH[1]	DTC_TH[0]	DTC_RATE[1]	DTC_RATE[0]	Reserved		
0X3D	PWM SHIFT	Reserved							
0X3E	PMF_FS_R	Reserved							
0X3F	FIR2	Reserved							
0X40	MBIST	Prohibited							
0X41	MBIST_UPT_E	Prohibited							
0X42	MBIST_UPM_E	Prohibited							
0X43	MBIST_UPB_E	Prohibited							
0X44	MBIST_UPT_O	Prohibited							
0X45	MBIST_UPM_O	Prohibited							
0X46	MBIST_UPB_O	Prohibited							
0X47	TMR	Prohibited							
0X48	BS_UV_SEL	Prohibited							
0X49	OC	Prohibited							
0X4A	OCB	Prohibited							
0X4B	MDT	Prohibited							
0X4C	PLL_CTRL	Prohibited							
0X4D	PLL_TM	Prohibited							
0X4E	ERR_REG	A_OCP_N	A_OTP_N	A_UV_N	A_BSUV_N	A_BSOV_N	A_CKERR_N	A_OVP_N	A_GVDDUV_N
0X4F	ERR_RECORD	A_OCP_N_LATCH	A_OTP_N_LATCH	A_UV_N_LATCH	A_BSUV_N_LATCH	A_BSOV_ N_LATCH	A_CKERR_ N_LATCH	A_OVP_ N_LATCH	A_GVDDUV_ N_LATCH
0X50	ERR_CLEAR	A_OCP_N_CLEAR	A_OTP_N_CLEAR	A_UV_N_CLEAR	A_BSUV_ N_CLEAR	A_BSOV_ N_CLEAR	A_CKERR_ N_CLEAR	A_OVP_ N_CLEAR	A_GVDDUV_ N_CLEAR

Detail Description for Register

Note that the highlighted columns are default values of these tables. If there is no highlighted value, the default setting of this bit is determined by the external pin.

- Address 0X00 : State control 1

  AD82050 supports multiple serial data input formats including I^2S, Left-alignment and Right-alignment. These formats are selected by users via bit7 ~ bit5 of address 0X00. The left/right channels can be exchanged to each other by programming to address 0/bit0, LREXC.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:5]	IF[2:0]	Input Format	000	I^2S 16-24 bits
			001	Left-alignment 16-24 bits
			010	Right-alignment 16 bits
			011	Right-alignment 18 bits
			100	Right-alignment 20 bits
			101	Right-alignment 24 bits
			110	TDM
B[4]	LREXC	L/R Channel exchange	0	No exchanged
			1	L/R exchanged
B[3]	PWML_X	LA/LB exchange	0	No exchanged
			1	A/B exchanged
B[2]	PWMR_X	RA/RB exchange	0	A/B exchanged
			1	No exchanged
B[1]	X	Reserved		
B[0]	NG_EN	Noise gate enable	0	Disable
			1	Enable

- Address 0X01 : State control 2

AD82050 has a built-in PLL and supports multiple BCLK/Fs ratios.

Detail setting is shown in the following table.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:6]		Reserved		
B[5:4]	FS	Sampling Frequency	00	32/44.1/48kHz
			01	64/88.2/96kHz
			10	8kHz
			11	16kHz

Multiple BCLK/FS ratio setting table

BIT	NAME	DESCRIPTION	VALUE	B[5:4]=00	B[5:4]=01	B[5:4]=10	B[5:4]=11
B[3:0]	PMF[3:0]	BCLK/Fs setup	0000	32X	32X	Reserved	Reserved
			0001	48X	48X	Reserved	48X
			0010	64X	64X	Reserved	64X
			0011	96X	96X	Reserved	96X
			0100	128X	128X	Reserved	128X
			0101	192X	192X	Reserved	192X
			0110	256X	256X	Reserved	256X
			0111	Reserved	Reserved	Reserved	Reserved
			1000	Reserved	Reserved	Reserved	Reserved

- Address 0X02 : State control 3

AD82050 can set different device address of I2C.

$\overline{\text{ERROR}}$ is an input pin to decide device address when A_SEL_FAULT register is 0.

$\overline{\text{ERROR}}$ is an output pin to show the error status when A_SEL_FAULT register is 1.

To prevent the DC current from damaging the speaker, a high pass filter (3dB frequency = 1Hz) is built into the AD82050. It can be enabled or disabled by bit 6 of address 0x02.

AD82050 has a mute function which includes master mute and individual channel mute modes. When the master mute mode is enabled, both left and right processing channels are muted. On the other hand, either channel can be muted by using the channel mute mode. When the mute function is enabled or disabled, the fade-out or fade-in process will be initiated.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	A_SEL_FAULT	I2C address selection or ERROR output	0	I2C device address selection
			1	ERROR output
B[6]	DC_HPB	DC blocking High-Pass Filter	0	1Hz
			1	Disabled
B[5]	LV_UVSEL	Low under voltage selection	0	2.8V
			1	2.6V
B[4]	SW_RSTB	Software reset	0	Reset
			1	Normal operation
B[3]	MUTE	Master Mute	0	Un-Mute
			1	Mute
B[2]	CM1	Channel 1 Mute	0	Un-Mute
			1	Mute
B[1]	CM2	Channel 2 Mute	0	Un-Mute
			1	Mute
B[0]	CompSDMEn	Compensate SDM frequency response	0	Disabled
			1	Enabled

- Address 0X03 : Master volume

AD82050 supports both master-volume and channel-volume control for the stereo processing channels. Both master volume control (Address 0X03) and channel volume (Address 0X04 and 0X05) settings range from +12dB ~ -103dB. Given master volume level, say, Level A (in dB unit) and channel volume level, say Level B (in dB unit), the total volume equals to Level A plus with Level B and its range is from +24dB ~ -102dB, i.e., -103dB ≦ Total Volume (Level A + Level B) ≦ +24dB.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	MV[7:0]	Master Volume	00000000	+12dB
			00000001	+11.5dB
			00000010	+11dB
			:	:
			00010111	0.5dB
			00011000	0dB
			00011001	-0.5dB
			:	:
			11100110	-103dB
			11100111	-∞dB
			:	:
			11111111	-∞dB

- Address 0X04 : Channel1 volume

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C1V[7:0]	Channel 1 Volume	00000000	+12dB
			00000001	+11.5dB
			:	:
			00010100	2dB
			:	:
			00011000	0dB
			00011001	-0.5dB
			:	:
			11100110	-103dB
			11100111	-∞dB
			:	:
			1111111	-∞dB

- Address 0X05 : Channel2 volume

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C2V[7:0]	Channel 2 Volume	00000000	+12dB
			00000001	+11.5dB
			:	:
			00010100	2dB
			:	:
			00011000	0dB
			00011001	-0.5dB
			:	:
			11100110	-103dB
			11100111	-∞dB
			:	:
			1111111	-∞dB

- Address 0X06 : Under voltage selection for high voltage supply

AD82050 provides HV under voltage detection which can be enable or disable via bit 7. The under-voltage detection level is programmable via bit2 ~ bit0. Once the output stage voltage drops below the preset value (see table), AD82050 will fade out audio signals to turn off the speaker.

AD82050 also provide LVUV and OV fade function, User can select fade or not fade for LVUV and OV via bit 6 and bit5.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	DIS_HVUV	Disable HV Under Voltage Circuit	0	Enable
			1	Disable
B[6]	DIS_LVUV_FADE	Disable LVUV fade selection	0	Fade
			1	No fade
B[5]	DIS_OV_FADE	Disable over voltage fade	0	Fade
			1	No fade
B[4:3]	X	Reserved		
B[2:0]	HVUVSEL[2:0]	HV Under Voltage Selection	000	3.9V
			001	7.2V
			010	9.7V
			011	13.2V
			100	15.5V
			101	19.5V
			others	7.2V

- Address 0X07 : State control 4

AD82050 provides channel mix, power clipping, and dynamic range control (DRC) function. These functions can be enable or not as the following table.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	C1MX_EN	Channel1 Mixing Enable	0	Disable
			1	Enable
B[6]	C2MX_EN	Channel2 Mixing Enable	0	Disable
			1	Enable
B[5]	PC1_EN	CH1 Power Clipping enable	0	Disable
			1	Enable
B[4]	PL1_EN	CH1 Power limit enable	0	Disable
			1	Enable
B[3]	MONO_EN	MONO or Stereo Configure	0	Stereo
			1	MONO
B[2]	PC2_EN	CH2 Power Clipping enable	0	Disable
			1	Enable
B[1]	PL2_EN	CH2 Power limit enable	0	Disable
			1	Enable
B[0]	X	Reserved		

AD82050 also provides MONO configuration via register bit 3 of address 0X07. The output configuration (please refer to the page 6, Mono application circuit) shall be right connected before Mono configuration enable. That's possible to damage chips due to channel shoot-through if the wrong output configuration is connected.

- Address 0X08 : PWM control

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	PSM_EN	Power saving mode	0	Disable
			1	Enable
B[6]	QD_EN	Quaternary and delta quaternary switching	0	Disable
			1	Enable
B[5]	AQ_EN	Advanced Quaternary enable	0	Disable
			1	Enable
B[4]	D_MOD	Delta quaternary modulation	0	Disable
			1	Enable
B[3]	PWM_SEL	PWM modulation	0	Qua-ternary
			1	Ternary
B[2:0]	X	Reserved		

- Address 0X09 : Power saving mode switching level

If the PWM exceeds the programmed switching power level (default 40*20ns), the modulation algorithm will change from default modulation scheme into power saving mode scheme. It results in higher power efficiency during larger power output operations. If the PWM drops below the programmed switching power level - programmed switching window (default (40-10)*20ns), the modulation algorithm will change back to default modulation scheme.

Switching scheme is related to PSM_EN (address0X08, B[7]), and QD_EN(address0X08, B[6]), AQ_EN (address0X08, B[5]) , D_MOD(address0X08, B[4])). AD82050 has four type switching schemes and they share the same switching scheme. One time will only have one switching scheme.

Case1: PSM_EN=1, D_MOD=0, QD_EN=0, AQ_EN=0.The default modulation scheme is quaternary and power saving mode scheme is ternary.

Case2: PSM_EN=1, D_MOD=1, QD_EN=0, AQ _EN=0. The default modulation scheme is delta quaternary and power saving mode scheme is ternary.

Case3: PSM_EN=1, D_MOD=0, QD_EN=0, AQ _EN=1. The default modulation scheme is advanced quaternary and power saving mode scheme is ternary.

Case4: PSM_EN=0, D_MOD=0, QD_EN=1, AQ _EN=0. The default modulation scheme is quaternary and power saving mode scheme is delta quaternary

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:5]	SW_WINDOW	Power saving mode switching window	000	4
			001	6
			010	8
			011	10
			100	12
			101	14
			110	16
			111	18
B[4:0]	QT_SW_LEVEL	Power saving mode switching level	00000	8
			00001	8
			00010	8
			00011	12
			:	:
			01010	40
			01011	44
			01100	48
			:	:
			11110	120
			11111	124

- Address 0X0C : Top 8 bits of Pre scale Coefficient

For both audio channels, AD82050 can scale input signal level prior to DC blocking which is realized by a 24-bit signed fractional multiplier. The pre-scale factor, ranging from -4 (0x800000) to 3.999999523 (0x7FFFFF) and composed of registers controlled by I2C. The register addresses of Pre Scale Coefficient are 0X0C, 0X0D, and 0X0E.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	PRST[7:0]	Top 8 Bits of Pre scale coefficient	X	User programmed
			00011111	-0.1dB

- Address 0X0D : Middle 8 bits of Pre Scale Coefficient

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	PRSM[7:0]	Middle 8 Bits of Pre Scale Coefficient	X	User programmed
			10100010	-0.1dB

- Address 0X0E : Bottom 8 bits of Pre Scale Coefficient

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	PRSB[7:0]	Bottom 8 Bits of Pre Scale Coefficient	X	User programmed
			00111010	-0.1dB

- Address 0X0F : Top 8 bits of Post Scale Coefficient

The AD82050 provides an additional multiplication after interpolation stage which is realized by a 24-bit signed fractional multiplier. The post-scale factor, ranging from -4 (0x800000) to 3.999999523 (0x7FFFFF) and composed of registers controlled by I2C. The register addresses of Post Scale Coefficient are 0X0F, 0X10, and 0X11.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	POST[7:0]	Top 8 Bits of Post Scale Coefficient	X	User programmed
			00100000	0dB

- Address 0X10 : Middle 8 bits of Post Scale Coefficient

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	POSM[7:0]	Top 8 Bits of Post Scale Coefficient	X	User programmed
			00000000	0dB

- Address 0X11 : Bottom 8 bits of Post Scale Coefficient

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	POSB[7:0]	Bottom 8 Bits of Post Scale Coefficient	X	User programmed
			00000000	0dB

- Address 0X12 : Mono Key High Byte

AD82050 provide a protection method to enter mono mode. Besides setting MONO_EN register high, it needs to set address 0X12 value to 0X30 and address 0X13 value to 0X06 for mono application. Otherwise, AD82050 will be stereo.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	MK_HBYTE [7:0]	Mono key high byte	0000_0000	Stereo
			X	Stereo
			0011_0000	MONO

- Address 0X13 : Mono Key Low Byte

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	MK_LBYTE [7:0]	Mono key low byte	0000_0000	Stereo
			X	Stereo
			0000_0110	MONO

- Address 0X14 : Device number and Version number

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:4]	DN	Device number	0111	Identification code
B[3:0]	VN	Version number	0000	Identification code

- Address 0X15 : Top 8 bits of power clipping

The AD82050 provides power clipping function to avoid excessive signal that may destroy loud speaker. The power clipping level is defined by 24-bit representation composed of registers controlled by I2C. The register addresses of power clipping threshold are 0X15, 0X16, and 0X17.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	PCT[7:0]	Top 8 Bits of Power Clipping Level	X	User programmed
			00100000	0dB

- Address 0X16 : Middle 8 bits of power clipping

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	PCM[7:0]	Middle 8 Bits of Power Clipping Level	X	User programmed
			00000000	0dB

- Address 0X17 : Bottom 8 bits of power clipping level

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	PCB[7:0]	Bottom 8 Bits of Power Clipping Level	X	User programmed
			00000000	0dB

The following table shows the power clipping level's numerical representation.

Sample calculation for power clipping

Max amplitude	dB	Linear	Decimal	Hex (3.21 format)
PVDD	0	1	2097152	200000
PVDD*0.707	-3	0.707	1482680	169FB8
PVDD*0.5	-6	0.5	1048576	100000
PVDD*L	x	$L=10^{(x/20)}$	D=524288xL	H=dec2hex(D)

- Address 0X18 : Noise gate gain control

When receiving signal sample points less than noise gate attack level for the time more than noise gate count time, noise gate function will active. The noise gate count time can be programmed via bit [7:6]. User can change noise gate gain via bit1 ~ bit0. When noise gate function occurs, input signal will multiply noise gate gain (x1/8, x1/4 x1/2, x0). User can select fade out or not via bit 4.

AD82050 supports different fade speed, and user can select it via bit 3 ~ bit2.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:6]	NG_CNT_SEL	Noise gate count time selection	00	43ms @fs:48K
			01	86ms @fs:48K
			10	172ms @fs:48K
			11	344ms @fs:48K
B[5]	X	Reserved		
B[4]	DIS_NG_FADE	Disable Noise Gate Fade	0	Fade
			1	No fade
B[3:2]	FADE_SPEED	Fade in/out speed selection	00	1.25ms
			01	2.5ms
			10	5ms
			11	10ms
B[1:0]	NG_GAIN	Noise Gate Detection Gain	00	x1/8
			01	x1/4
			10	x1/2
			11	Mute

- Address 0X19 : Volume fine tune

AD82050 supports both master-volume fine tune and channel-volume control fine tune modes. Both volume control settings range from 0dB ~ -0.375dB and 0.125dB per step. Note that the master volume fine tune is added to the individual channel volume fine tune as the total volume fine tune.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:6]	MV_FT	Master Volume Fine Tune	00	0dB
			01	-0.125dB
			10	-0.25dB
			11	-0.375dB
B[5:4]	C1V_FT	Channel 1 Volume Fine Tune	00	0dB
			01	-0.125dB
			10	-0.25dB
			11	-0.375dB
B[3:2]	C2V_FT	Channel 2 Volume Fine Tune	00	0dB
			01	-0.125dB
			10	-0.25dB
			11	-0.375dB
B[1:0]	X	Reserved		

- Address 0X1A : Top 8 bits of noise gate attack level

When both left and right signals have 2048 consecutive sample points less than the programmable noise gate attack level, the audio signal will multiply noise gate gain, which can be set at x1/8, x1/4, x1/2, or zero if the noise gate function is enabled. Noise gate attack level is defined by 24-bit representation composed of registers controlled by I2C. The register addresses of noise gate attack level are 0X1A, 0X1B, and 0X1C

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	NGALT[7:0]	Top 8 Bits of Noise Gate Attack Level	X	User programmed
			00000000	-110dB

- Address 0X1B : Middle 8 bits of noise gate attack level

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	NGALM[7:0]	Middle 8 Bits of Noise Gate Attack Level	X	User programmed
			00000000	-110dB

- Address 0X1C : Bottom 8 bits of noise gate attack level

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	NGALB[7:0]	Bottom 8 Bits of Noise Gate Attack Level	X	User programmed
			00011010	-110dB

- Address 0X1D : Top 8 bits of noise gate release level

  After entering the noise gating status, the noise gain will be removed whenever AD82050 receives any input signal that is more than the noise gate release level. Noise gate release level is defined by 24-bit representation composed of registers controlled by I2C. The register addresses of noise gate release level are 0X1D, 0X1E, and 0X1F.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	NGRLT[7:0]	Top 8 Bits of Noise Gate Release Level	X	User programmed
			00000000	-100dB

- Address 0X1E : Middle 8 bits of noise gate release level

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	NGRLM[7:0]	Middle 8 Bits of Noise Gate Release Level	X	User programmed
			00000000	-100dB

- Address 0X1F : Bottom 8 bits of noise gate release level

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	NGRLB[7:0]	Bottom 8 Bits of Noise Gate Release Level	X	User programmed
			01010011	-100dB

The following table shows the noise gate attack and release threshold level's numerical representation.

Sample calculation for noise gate attack and release level

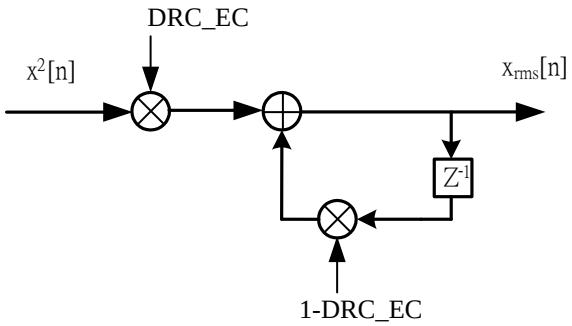
Input amplitude (dB)	Linear	Decimal	Hex (1.23 format)
0	1	8388607	7FFFFF
-100	10^{-5}	83	53
-110	$10^{-5.5}$	26	1A
X	$L=10^{(x/20)}$	D=8388607xL	H=dec2hex(D)

- Address 0X20 : Top 8 bits of DRC energy coefficient

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	DRC_ECT [7:0]	Top 8 Bits of DRC Energy Coefficient	X	User programmed
			00000000	1/2048

- Address 0X21 : Bottom 8 bits of DRC energy coefficient

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	DRC_ECB[7:0]	Bottom 8 Bits of DRC Energy Coefficient	X	User programmed
			00010000	1/2048



The above figure illustrates the digital processing of calculating RMS signal power. In this processing, a DRC energy coefficient is required, which can be programmed for different frequency range. Energy coefficient is defined by 16-bit representation composed of registers controlled by I2C. The register addresses of DRC energy coefficient are 0X20, and 0X21. The following table shows the DRC energy coefficient numerical representation.

Sample calculation for DRC energy coefficient

DRC energy coefficient	dB	Linear	Decimal	Hex {1,b0, DRC_ECT[6:0], DRC_ECB,8'b0} (1.23 format)
1	0	1	8388352	7FFF00
1/256	-48.2	1/256	32768	8000
1/2048	-66.2	1/2048	4096	1000
L	x	$L=10^{(x/20)}$	D=8388352xL	H=dec2hex(D)

- Address 0X22 : Top 8 bits of Compensate filter A0 Coefficient

The AD82050 provides user programmed compensate filter after power clipping. Compensate filter is defined by 24-bit representation composed of registers controlled by I2C. The register addresses of compensate filter are 0X22, 0X23, 0X24, 0X25, 0X26, 0X27, 0X28, 0X29, and 0X2A.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	COMB_A0T [7:0]	Top 8 Bits of Compensate A0 Coefficient	X	User programmed
			00001110	

- Address 0X23 : Middle 8 bits of Compensate filter A0 Coefficient

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	COMB_A0M [7:0]	Middle 8 Bits of Compensate A0 Coefficient	X	User programmed
			10111111	

- Address 0X24 : Bottom 8 bits of Compensate filter A0 Coefficient

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	COMB_A0B [7:0]	Bottom 8 Bits of Compensate A0 Coefficient	X	User programmed
			00110111	

- Address 0X25 : Top 8 bits of Compensate filter A1 Coefficient

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	COMB_A1T [7:0]	Top 8 Bits of Compensate A1 Coefficient	X	User programmed
			00000001	

- Address 0X26 : Middle 8 bits of Compensate filter A1 Coefficient

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	COMB_A0M [7:0]	Middle 8 Bits of Compensate A1 Coefficient	X	User programmed
			01110011	

- Address 0X27 : Bottom 8 bits of Compensate filter A1 Coefficient

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	COMB_A1B [7:0]	Bottom 8 Bits of Compensate A1 Coefficient	X	User programmed
			10111010	

- Address 0X28 : Top 8 bits of Compensate filter B1 Coefficient

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	COMB_B1T [7:0]	Top 8 Bits of Compensate B1 Coefficient	X	User programmed
			11111111	

- Address 0X29 : Middle 8 bits of Compensate filter B1 Coefficient

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	COMB_B1M [7:0]	Middle 8 Bits of Compensate B1 Coefficient	X	User programmed
			11001101	

- Address 0X2A : Bottom 8 bits of Compensate filter B1 Coefficient

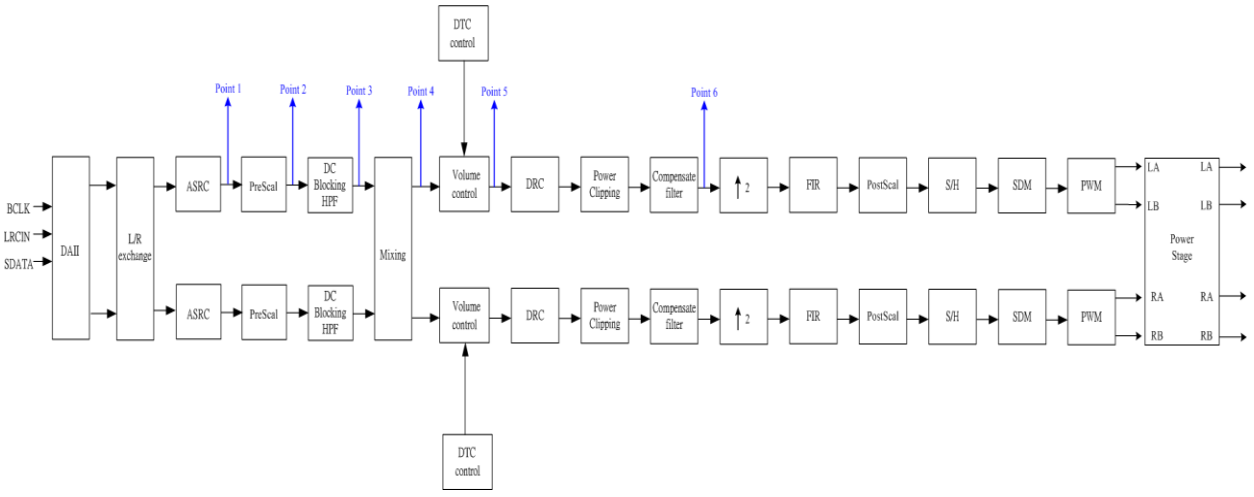
BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	COMB_B1B [7:0]	Bottom 8 Bits of Compensate B1 Coefficient	X	User programmed
			00001111	

- Address 0X2B : State control 5

AD82050 provides TDM word width selection. Please refer the table with device Audio Data Formats, Bit Depths, Clock Rates, and channel numbers.

AD82050 provide I^2S output function and the output point.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:6]	X	Reserved		
B[5:4]	WORD_WIDTH_SEL	TDM word width selection	00	32 bits
			01	24 bits
			10	20 bits
			11	16 bits
B[3]	SDATAO_CTRL	SDTATO pin control	0	GND
			1	SDATAO
B[2:0]	I2S_DO_SEL	I2S DATA OUTPUT selection	000	Ponit1 : DSP input
			001	Point2 : pre-scale output
			010	Point3 : DC blocking HPF output
			011	Point4 : Mixer output
			100	Point5 : volume output
			101	Point6 : compensate filter output
			others	Reserved



- Address 0X2C : TDM offset

These bits control the offset of audio data in the audio frame for both input and output. The offset is defined as the number of BCLK from the starting (MSB) of audio frame to the starting of the desired audio sample

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	TDM_OFFSET	TDM offset bits	00000000	Offset is 0 BCLK
			00000001	Offset is 1 BCLK
			00000010	Offset is 2 BCLK
			…	
			11111101	Offset is 253 BCLK
			11111110	Offset is 254 BCLK
			11111111	Offset is 255 BCLK

- Address 0X2D : Top 8 bits of DRC Attack Time

AD82050 can provide user programmed attack time and release when DRC is active.

The register addresses of attack time are 0X2D, 0X2E, and 0X2F.

The register addresses of release time are 0X30, 0X31, and 0X32.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	AAT[7:0]	Top 8-bits of DRC Attack Time	X	User programmed
			00000000	1/2048

- Address 0X2E : Middle 8 bits of DRC Attack Time

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	AAM[7:0]	Middle 8-bits of DRC Attack Time	X	User programmed
			00000100	1/2048

- Address 0X2F : Bottom 8 bits of DRC Attack Time

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	AAB[7:0]	Bottom 8-bits of DRC Attack Time	X	User programmed
			00000000	1/2048

- Address 0X30 : Top 8 bits of DRC Release Time

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	DAT[7:0]	Top 8-bits of DRC Release Time	X	User programmed
			00000000	1/8192

- Address 0X31 : Middle 8 bits of DRC Release Time

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	DAM[7:0]	Middle 8-bits of DRC Release Time	X	User programmed
			00000001	1/8192

- Address 0X32 : Bottom 8 bits of DRC Release Time

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	DAB[7:0]	Bottom 8-bits of DRC Release Time	X	User programmed
			00000000	1/8192

- Address 0X33 : Top 8 bits of DRC Threshold

The AD82050 provides DRC function. When the input RMS exceeds the programmable DRC threshold value, the output power will be limited by this threshold power level via gradual gain reduction. After AD82050 has reached the DRC threshold, its output power will be limited to that level. The output power level will be gradually adjusted to the programmable DRC threshold level. The register addresses of DRC threshold are 0X33, 0X34, and 0X35.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	DRC_TH_T[7:0]	Top 8-bits of DRC threshold	X	User programmed
			11110000	0dB

- Address 0X34 : Middle 8 bits of DRC Threshold

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	DRC_TH_M[7:0]	Middle 8-bits of DRC threshold	X	User programmed
			00001110	0dB

- Address 0X35 : Bottom 8 bits of DRC Threshold

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	DRC_TH_B[7:0]	Bottom 8-bits of DRC threshold	X	User programmed
			00000100	0dB

The equation is

$$T_{dB} = (T - 12) / 6.0206 (dB)$$

Ex: T=-6 db, TdB=(-6-12)/6.0206=-2.9897(dB)

T_{Dec}=-1567482

T_{Hex}=0XE81506

Sample calculation for DRC threshold

Power	T	TdB	Decimal	Hex (5.19 format)
(Vp^2)/2R	-4	-2.6575	-1393318	EABD5B
	-7	-3.1558	-1654565	E6C0DC
	X	(x-12)/6.0206	D=2^19*TdB	H=dec2hex(D)

- Address 0X36 : Top 8 bits of DRC Slope

The AD82050 DRC provides limiter and compressor. Use slope to decide compression factor. The relationship between the ratio R and the slope S is

$$S = 1 - \frac{1}{R}$$

$$R = \frac{1}{1-S} = \frac{x - Threshold(dB)}{y - Threshold(dB)}$$

DRC slope is defined by 24bit and the resister addresses are 0X36, 0X37, and 0X38

Ex: Setting DRC is limiter, S=1 (R=∞).

S_DEC=1*2^25 = 33554432

S_HEX = 0X2000000

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	SLT[7:0	Top 8-bits of DRC slope	X	User programmed
			00100000	slope=1

- Address 0X37 : Middle 8 bits of DRC Slope

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	SLM[7:0	Middle 8-bits of DRC slope	X	User programmed
			00000000	slope=1

- Address 0X38 : Bottom 8 bits of DRC Slope

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	SLM[7:0	Bottom 8-bits of DRC slope	X	User programmed
			00000000	slope=1

- Address 0X39: Top 8 bits of I^2S out gain coefficient

AD82050 can scale signal level before transmit the I^2S output. The range of I^2S out gain factor is from -16 (0x800000) to 15.999998(0x7FFFFF). The register addresses of I^2S out gain are 0X39, 0X3A, and 0X3B.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	I2SGT[7:0]	Top 8 Bits of I^2S Out Gain Coefficient	X	User programmed
			00001000	0dB

- Address 0X3A : Middle 8 bits of I^2S out gain coefficient

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	I2SGM[7:0]	Middle 8 Bits of I^2S Out Gain Coefficient	X	User programmed
			00000000	0dB

- Address 0X3B : Bottom 8 bits of I^2S out gain coefficient

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	I2SGB[7:0]	Bottom 8 Bits of I^2S Out Gain Coefficient	X	User programmed
			00000000	0dB

The following table shows the I^2S out gain numerical representation.

Sample calculation for I^2S out gain

Pre/post scale	dB	Linear	Decimal	Hex (5.19 format)
1	0	1	524288	80000
0.5	-6	0.5	262144	40000
0.25	-12	0.25	131072	20000
$L=10^{(x/20)}$	x	$L=10^{(x/20)}$	D=2097152xL	H=dec2hex(D)

- Address 0X3C : Dynamic Temperature Control (DTC)

AD82050 supports dynamic temperature control. The table describes the setting of DTC.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	DTC_EN	DTC Enable	0	Disable
			1	Enable
B[6:5]	DTC_TH	DTC Attack Threshold	00	110 °C
			01	120 °C
			10	130 °C
			11	140 °C
B[4:3]	DTC_RATE	DTC Attack and Release Rate	00	1dB/sec
			01	0.5dB/sec
			10	0.33dB/sec
			11	0.25dB/sec
B[2:0]	X	Reserved		

DTC release threshold is designed 10 °C lower than attack threshold.

For example:

DTC attack threshold =130 °C, the release threshold is 120 °C.

DTC attack threshold =120 °C, the release threshold is 110 °C.

If junction temperature (Tj) exceeds 130 °C, amplifier gain will be lowered to timing of 1dB/sec. If amplifier gain falls and junction temperature (Tj) turns into less than 130 °C and larger than 120 °C, the gain will not increase or decrease. If amplifier gain falls and junction temperature (Tj) turns into less than 120 °C, amplifier gain will be raised to timing of 1dB/sec.

- Address 0X4E, Protection Status Register

The protection registers will show what kind of protection occurs.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	A_OCP_N	Over current occur	0	Occurred
			1	Normal
B[6]	A_OTP_N	Over temperature occur	0	Occurred
			1	Normal
B[5]	A_UV_N	Under voltage occur	0	Occurred
			1	Normal
B[4]	A_BSUV_N	BSUV error	0	Occurred
			1	Normal
B[3]	A_BSOV_N	BSOV error	0	Occurred
			1	Normal
B[2]	A_CKERR_N	Clock detection error	0	Occurred
			1	Normal
B[1]	A_OVP_N	Over voltage occur	0	Occurred
			1	Normal
B[0]	A_GVDDUV_N	GVDDUV error	0	Occurred
			1	Normal

- Address 0X4F : Protection latch register

The protection registers will show what kind of protection ever occurred.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	A_OCP_N_LATCH	OCP latch register	0	OC ever occur
			1	Normal
B[6]	A_OTP_N_LATCH	OTP latch register	0	OT ever occur
			1	Normal
B[5]	A_UV_N_LATCH	UV latch register	0	UV ever occur
			1	Normal
B[4]	A_BSUV_N_LATCH	BSUV latch register	0	BSUV ever occur
			1	Normal
B[3]	A_BSOV_N_LATCH	BSOV latch register	0	BSOV ever occur
			1	Normal
B[2]	A_CKERR_N_LATCH	CKERR latch register	0	CKERR ever occur
			1	Normal
B[1]	A_OVP_N_LATCH	OVP latch register	0	OV ever occur
			1	Normal
B[0]	A_GVDDUV_N_LATCH	GVDDUV latch register	0	GVDDUV ever occur
			1	Normal

- Address 0X50 : Protection latch clear register

The protection latch registers will show what kind of protection ever occurred.

Using the protection clear registers can clear the corresponding protection latch registers.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	A_OCP_N_CLEAR	OCP latch clear register	0	No clear
			1	Clear
B[6]	A_OTP_N_CLEAR	OTP latch clear register	0	No clear
			1	Clear
B[5]	A_UV_N_CLEAR	UV latch clear register	0	No clear
			1	Clear
B[4]	A_BSUV_N_CLEAR	BSUV latch clear register	0	No clear
			1	Clear
B[3]	A_BSOV_N_CLEAR	BSUV latch clear register	0	No clear
			1	Clear
B[3]	A_CKERR_N_CLEAR	CKERR latch clear register	0	No clear
			1	Clear
B[2]	A_OVP_N_CLEAR	OVP latch clear register	0	No clear
			1	Clear
B[0]	A_GVDDUV_N_CLEAR	GVDDUV latch clear register	0	No clear
			1	Clear

Package Dimensions

E-TSSOP 24L (173mil)

錯誤! 尚未指定主題。

Symbol	Dimension in mm	
	Min	Max
A	1.00	1.20
A1	0.00	0.15
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	4.30	4.50
E1	6.30	6.50
e	0.65 BSC	
L	0.45	0.75

Exposed pad

	Dimension in mm	
Option 1	Min	Max
D2	3.95	4.75
E2	2.70	3.10

Revision History

Revision	Date	Description
0.1	2022.11.14	Original.
0.2	2022.12.07	1. Modify the minimum value of T_J in Absolute Maximum Ratings. 2. Modify Total Harmonic Distortion + Noise vs. Output Power for BTL and PBTL. 3. Modify Total Harmonic Distortion + Noise vs. Frequency for BTL and PBTL. 4. Add Efficiency (Stereo, PBTL) with Advanced Quaternary during Power Saving Mode. 5. Modify the value and function of Address 0X0C, 0X0D and 0X0E. 6. Modify the value of Address 0X14 and 0x2A. 7. Modify the function of Address 0X20 and 0X21. 8. Modify sample calculation fro DRC energy coefficient in Address 0X21.
1.0	2022.12.22	1.Remove” Preliminary”
1.1	2022.12.28	Modify a typo in Address 0x3C.

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