

3W/CH Stereo Filter-less Class-D Audio Amplifier

Features

- Supply voltage range: 3.0 V to 5.5 V
- 10mA static operation current
- <1uA shutdown current
- 64-step DC volume control from -60dB to +24dB
- Overload and thermal protection
- Loudspeaker output power @ 10% THD+N
 - 1.75W/CH into 8Ω loudspeaker
 - 3.0W/CH into 4Ω loudspeaker
- High efficiency
 - 91% @ 8Ω, Po,10% THD+N
 - 84% @ 4Ω, Po,10% THD+N

Applications

- Monitor audio
- Portable multimedia devices
- Mobile phone

Description

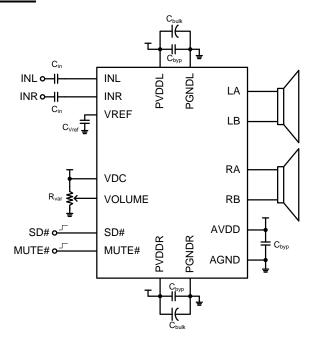
The AD52651C is a stereo, filter-less class-D audio amplifier and has a 64-step DC volume controller. Operating with 5.0V loudspeaker driver supply, it can deliver 3.0W/CH output power into 4 Ω loudspeaker within 10% THD+N.

The AD52651C is packaged as SSOP-24L (150mil) is a stereo audio amplifier with high efficiency, which leads to longer battery life, less heat sink requirement, smaller board size and lower system cost, and suitable for the notebook computer, and portable multimedia devices.

Ordering Information

Product ID	Package	Packing	Comments
AD52651C-ST24NAT	SSOP-24L	56 Units / Tube 100 Tubes / Small Box	Green

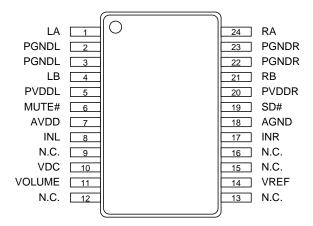
Typical Application Circuit



Publication Date :Dec. 2017 Revision: 1.0 1/19



Pin Assignments



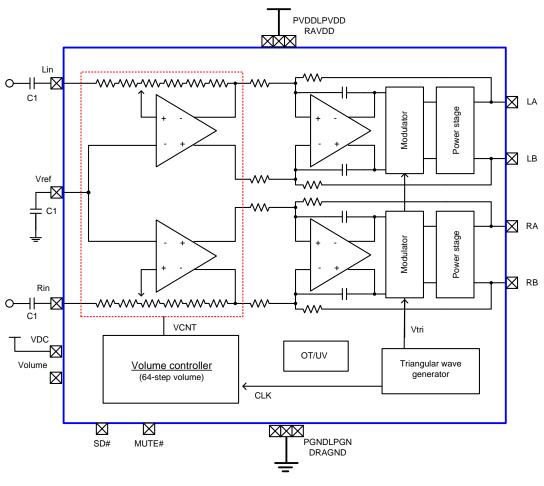
Pin Description

N	IAME	TYP	DESCRIPTION	CHARACTERISTIC
1	LA	0	Speaker driver_Left (+)	
2	PGNDL	G	Power ground_Left	
3	PGNDL	G	Power ground_Left	
4	LB	0	Speaker driver_Left (-)	
5	PVDDL	Р	Power supply_Left	
6	MUTE#	ı	Mute(low active)	Internal pull-up
7	AVDD	Р	Analog power supply	
8	INL	ı	Single-ended audio input_Left	
9	N.C.	Х	No connection	
10	VDC	I	Full scale level for gain control	Internal pull-up
			section	
11	VOLUME	I	DC voltage for gain setting	Internal pull-up
12	N.C.	Х	No connection	
13	N.C.	Х	No connection	
14	VREF	I	AVDD/2 reference voltage	
15	N.C.	х	No connection	
16	N.C.	Х	No connection	
17	INR	I	Single-ended audio input_Right	
18	AGND	G	Analog power ground	
19	SD#	ı	Shutdown(low active)	Internal pull-up
20	PVDDR	Р	Power supply_Right	
21	RB	0	Speaker driver_Right (-)	
22	PGNDR	G	Power ground_Right	
23	PGNDR	G	Power ground_Right	
24	RA	0	Speaker driver_Right (+)	

Publication Date :Dec. 2017 Revision: 1.0 2/19



Functional Block Diagram



Available Package

Package Type	ackage Type Device No. θ _{ja} (°C/W)		θ _{jc} (°C/W)
SSOP-24	AD52651C	90	17

Note 1: θ_{ja} is measured on a room temperature (T_A =25 $^{\circ}$ C), natural convection environment test board, which is constructed with a thermally efficient, 2-layers PCB. The measurement is tested using the JEDEC51-3 thermal measurement standard.

Note 2: θ_{jc} represents the heat resistance for the heat flow between the chip and the package's top surface.

Marking Information

AD52651C

Line 1: LOGO

Line 2 : Product no. Line 3 : Tracking Code

Line 4 : Date Code



Publication Date :Dec. 2017 Revision: 1.0 3/19



Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN	MAX	UNIT
AVDD	Power supply for lower power analog circuits	3.0	6.0	V
PVDDL(R)	Power supply for loudspeaker driver	3.0	6.0	V
	Input voltage	-0.3	AVDD	V
T _{stg}	Storage temperature	-65	150	°C
T _a	Ambient operating temperature	0	70	°C

Recommended Operating Conditions

SYMBOL	PARAMETER	TYP	UNIT
AVDD	Power supply for lower power analog cells	3.0~5.5	V
PVDDL(R)	Power supply for Driver Stage	3.0~5.5	V
V _{IH}	High-Level Input Voltage	1.2	V
V _{IL}	Low-Level Input Voltage	0.4	V
T _a	Ambient Operating Temperature	0~70	°C

General Electrical Characteristics

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
I _{SD}	Supply current during Shut-down mode	AVDD=PVDDR(L)=VDD VDD=5.0V SD#=0.4V			1	μА
I _{MUTE}	Supply current during MUTE mode	AVDD=PVDDR(L)=VDD VDD=5.0V SD#=VDD, MUTE#=0.4V		2.5	4	mA
ΙQ	Supply current during operating mode	AVDD=PVDDR(L)=VDD VDD=5.0V SD#=MUTE#=VDD, no load		10	15	mA
V _{offset}	Output offset voltage	Input ac grounded,		10	50	mV
	Junction temperature for driver shutdown			160		ο°
	Temperature hysteresis for recovery from shutdown			125		°C
f _{sw}	Switching frequency	AVDD=3.0V~5.0V	200	250	330	kHz
I _{sc}	Loudspeaker short-circuit detect resistance	PVDDR(L)=5.0V		2.2		A

Elite Semiconductor Microelectronics Technology Inc.

Publication Date :Dec. 2017 Revision: 1.0 4/19



Electrical Characteristics and Specifications of Loudspeaker Driver

● AVDD=PVDDL=PVDDR=VDD Gain=2 V/V, Load=8Ω, f_{in}=1 kHz, T_A=25°C (unless otherwise noted)

SYMBOL	PARAMETER	CONE	DITION	MIN	TYP	MAX	UNIT
		VDD=5.0V	THD+N = 10 %		1.75		W
		VDD=5.0V	THD+N = 1 %		1.4		W
Po	RMS Output Power per Channel	VDD=3.6V	THD+N = 10 %		0.9		W
F ₀	Kivis Output Fower per Channel	VDD=3.6V	THD+N = 1 %		0.7		W
		VDD=3.0V	THD+N = 10 %		0.6		W
		VDD=3.0V	THD+N = 1 %		0.45		W
	Total Harmania Distortion plus	VDD=5.0V, Po=1.0W			0.1		%
THD+N	Total Harmonic Distortion plus Noise	VDD=3.6V, Po=0.5W			0.2		%
	INUISE	VDD=3.0V, Po=0.3W			0.5		%
SNR	Signal to Noise Ratio	VDD=5.0V, Po=1.0W			96		dB
PSRR	Power Supply Rejection Ratio	VDD=5.0V, Gain=6dB, V _{ripple} =200mVpp, Inputs ac grounded with Ci=470nF f=1kHz			-55		dB
Crosstalk	Crosstalk	VDD=5.0V, f _{in} =1kHz			-100		dB
V _n	Output integrated noise (A-weighted)	VDD=5.0V f _{in} =20Hz ~ 20kHz			80		μV
η	Efficiency	VDD=5.0V, THD	VDD=5.0V, THD+N=10%		91		%

AVDD=PVDDL=PVDDR=VDD Gain=2 V/V, Load=4Ω, f_{in}=1 kHz, T_A=25°C (unless otherwise noted)

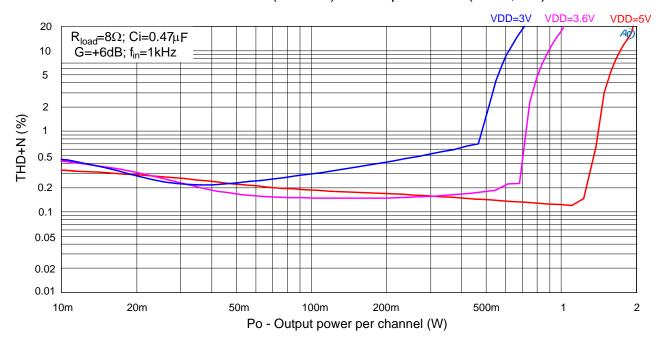
SYMBOL	PARAMETER	CONDITION		MIN	TYP	MAX	UNIT
		VDD=5.0V	THD+N = 10 %		3.0		W
		VDD=5.0V	THD+N = 1 %		2.45		W
D	PMS Output Dower per Channel	VDD=3.6V	THD+N = 10 %		1.5		W
Po	RMS Output Power per Channel	VDD=3.6V	THD+N = 1 %		1.2		W
		\/DD 2.0\/	THD+N = 10 %		1.0		W
		VDD=3.0V	THD+N = 1 %		0.8		W
	Total Harmania Distortion plus	VDD=5.0V, Po=2.0W			0.2		%
THD+N	Total Harmonic Distortion plus Noise	VDD=3.6V, Po=1.0W			0.3		%
	Noise	VDD=3.0V, Po=0.6W			0.6		%
SNR	Signal to Noise Ratio	VDD=5.0V, Po=1.8W			96		dB
PSRR	Power Supply Rejection Ratio	VDD=5.0V, Gain=6dB, V _{ripple} =200mVpp, Inputs ac grounded with Ci=470nF f=1kHz			-55		dB
Crosstalk	Crosstalk	VDD=5.0V, f _{in} =1kHz			-100		dB
V _n	Output integrated noise (A-weighted)	VDD=5.0V f _{in} =20Hz ~ 20kHz			80		μV
η	Efficiency	VDD=5.0V, THD	+N=10%		84		%

Publication Date :Dec. 2017 Revision: 1.0 5/19

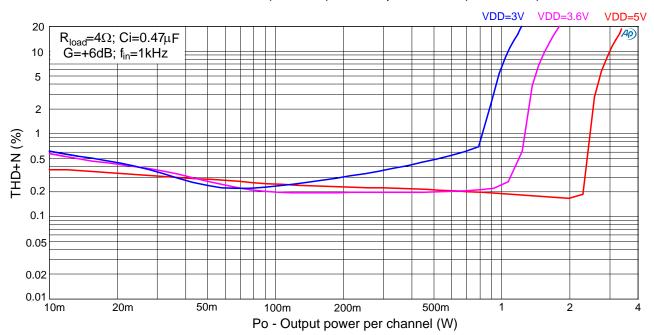


Typical Characteristics of Loudspeaker Driver

Total Harmonic Distortion + Noise (THD+N) vs. Output Power (+6dB, 8Ω)



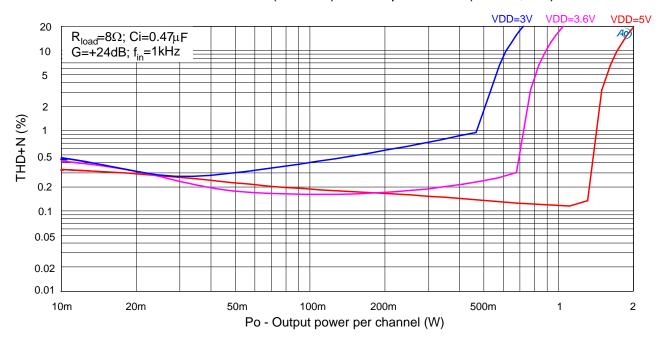
Total Harmonic Distortion + Noise (THD+N) vs. Output Power (+6dB, 4Ω)



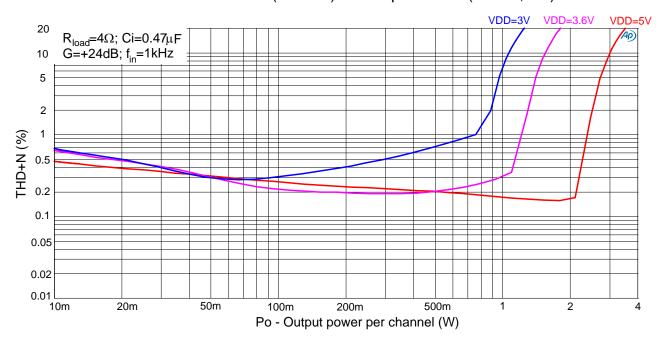
Publication Date :Dec. 2017 Revision: 1.0 6/19



• Total Harmonic Distortion + Noise (THD+N) vs. Output Power (+24dB, 8Ω)



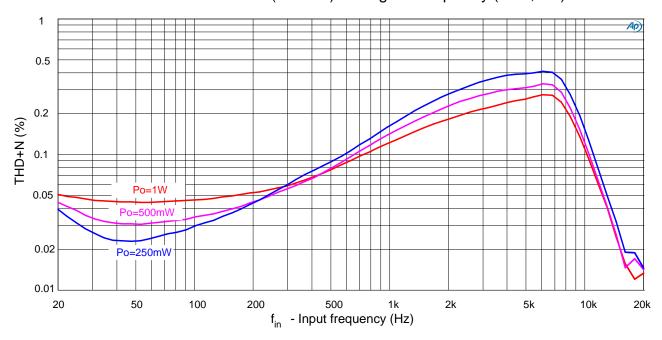
• Total Harmonic Distortion + Noise (THD+N) vs. Output Power (+24dB, 4Ω)



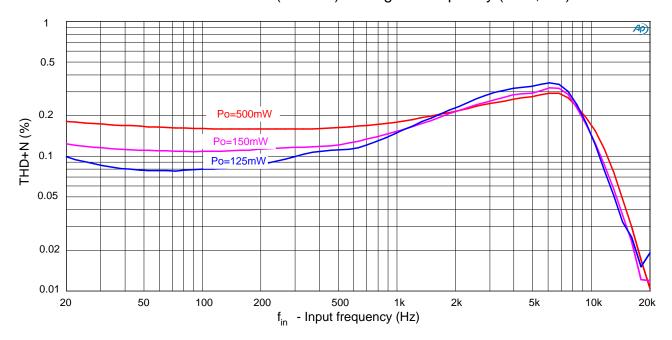
Publication Date :Dec. 2017 Revision: 1.0 7/19



• Total Harmonic Distortion + Noise (THD+N) vs. Signal Frequency (5.0V, 8Ω)



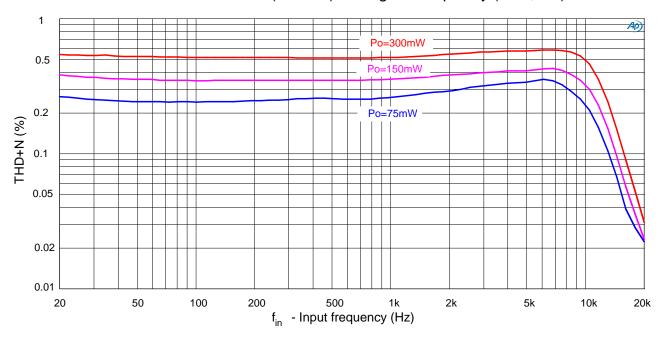
• Total Harmonic Distortion + Noise (THD+N) vs. Signal Frequency (3.6V, 8Ω)



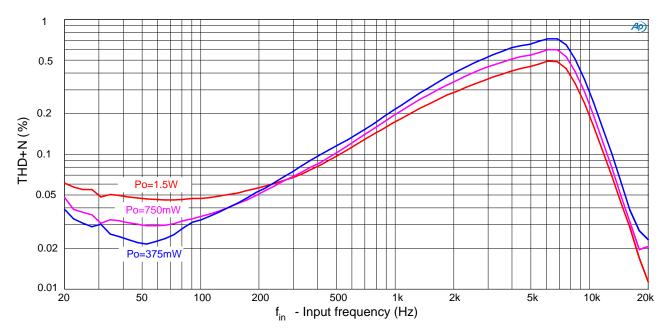
Publication Date :Dec. 2017 Revision: 1.0 **8/19**



• Total Harmonic Distortion + Noise (THD+N) vs. Signal Frequency (3.0V, 8Ω)



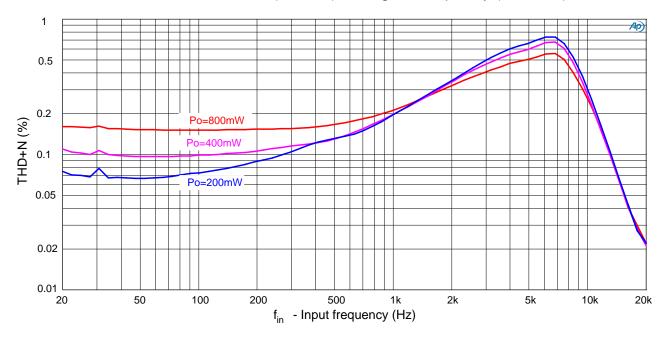
• Total Harmonic Distortion + Noise (THD+N) vs. Signal Frequency (5.0V, 4Ω)



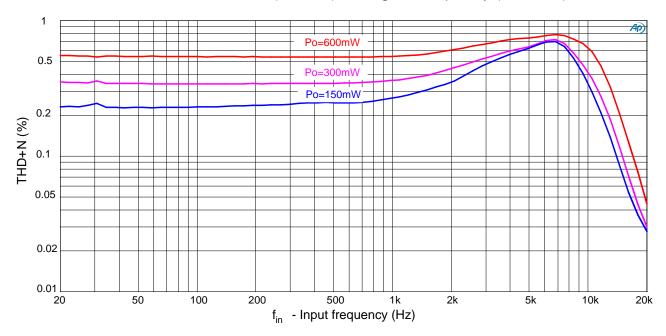
Publication Date :Dec. 2017 Revision: 1.0 9/19



• Total Harmonic Distortion + Noise (THD+N) vs. Signal Frequency (3.6V, 4Ω)



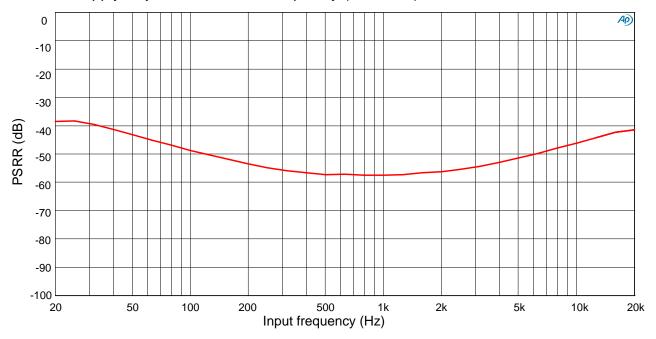
• Total Harmonic Distortion + Noise (THD+N) vs. Signal Frequency (3.0V, 4Ω)



Publication Date :Dec. 2017 Revision: 1.0 10/19



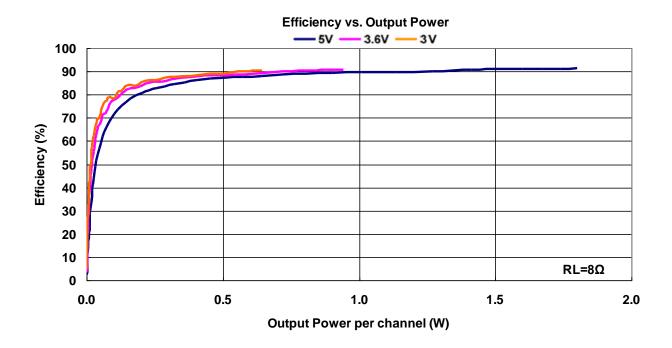
• Power Supply Rejection Ratio vs. Frequency (5V, +6dB)



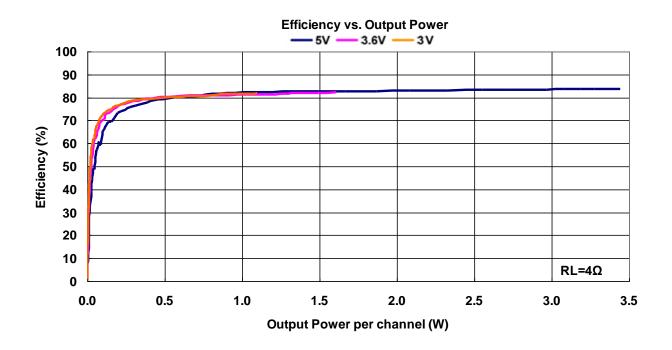
Publication Date :Dec. 2017 Revision: 1.0 11/19



• Efficiency vs. Output Power (8 Ω)



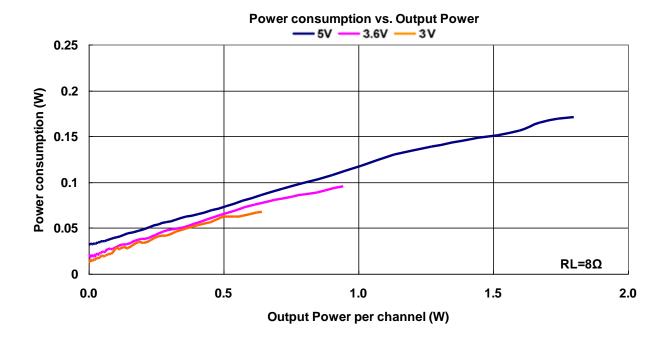
• Efficiency vs. Output Power (4Ω)



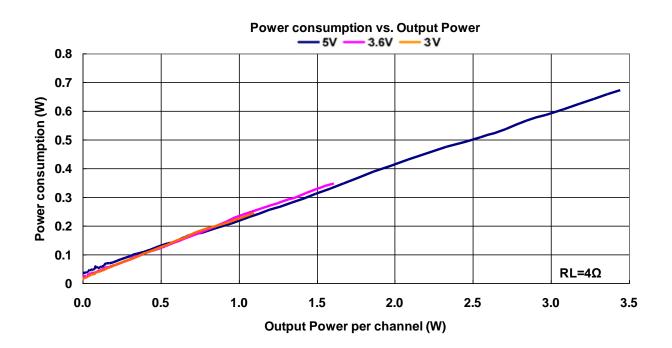
Publication Date :Dec. 2017 Revision: 1.0 12/19



Power Consumption vs. Output Power (8Ω)



• Power Consumption vs. Output Power (4 Ω)



Publication Date :Dec. 2017 Revision: 1.0 13/19

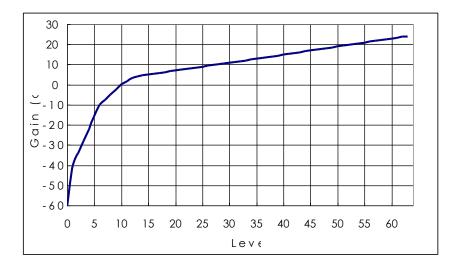


Operation Descriptions

Volume control

AD52651C has built-in a 64-steps DC volume controller, and the volume level is set by the VOLUME DC voltage to VDC ratio. To avoid volume level oscillation from one to adjacent one, the hysteresis voltage between the nearby volume levels is designed in AD52651C. For example, the volume level changes from LEVEL14 to LEVEL15 when DC voltage applied on VOLUME increases to 23.2% of VDC. And, the volume level drops from LEVEL15 to LEVEL14 when DC voltage applied on VOLUME decreases to 21.7% of VDC. The hysteresis voltage is about 70mV when VDC=5V. More volume levels, gains, and its DC voltage ratio applied on VOLUME are listed in following table.

Level	Gain (dB)	VOLUME (% of VDC)	Level	Gain (dB)	VOLUME (% of VDC)	Level	Gain (dB)	VOLUME (% of AVDD)
0	-60	0.0 ~ 2.8	22	7.8	32.2 ~ 33.6	43	16.1	61.6 ~ 63.2
1	-40	2.6 ~ 4.2	23	8.1	33.6 ~ 35.2	44	16.5	63.0 ~ 64.6
2	-34	4.0 ~ 5.6	24	8.5	35.2 ~ 36.4	45	16.9	64.6 ~ 65.8
3	-28	5.6 ~ 7.0	25	8.9	36.2 ~ 37.8	46	17.3	65.8 ~ 67.2
4	-22	6.8 ~ 8.4	26	9.3	37.8 ~ 39.2	47	17.7	67.2 ~ 68.8
5	-16	8.4 ~ 9.8	27	9.7	39.2 ~ 40.6	48	18.1	68.4 ~ 70.0
6	-10	9.8 ~ 11.0	28	10.1	40.6 ~ 42.0	49	18.5	70.0 ~ 71.4
7	-7.5	11.2 ~ 12.6	29	10.5	42.0 ~ 43.4	50	18.9	71.4 ~ 72.8
8	-4.9	12.4 ~ 14.0	30	10.8	43.2 ~ 45.0	51	19.3	72.8 ~ 74.4
9	-2.4	14.0 ~ 15.4	31	11.2	44.8 ~ 46.2	52	19.7	74.2 ~ 75.8
10	0.1	15.4 ~ 17.0	32	11.6	46.2 ~ 47.6	53	20.1	75.6 ~ 77.0
11	1.6	17.0 ~ 18.2	33	12.0	47.8 ~ 49.0	54	20.5	77.0 ~ 78.4
12	3.2	18.2 ~ 19.6	34	12.4	49.0 ~ 50.2	55	20.9	78.4 ~ 79.8
13	4.1	19.6 ~ 20.8	35	12.8	50.2 ~ 51.8	56	21.3	79.8 ~ 81.4
14	4.6	21.0 ~ 22.4	36	13.2	51.8 ~ 53.2	57	21.7	81.2 ~ 82.8
15	5.0	22.4 ~ 23.8	37	13.6	53.2 ~ 54.6	58	22.1	82.6 ~ 84.0
16	5.4	23.8 ~ 25.2	38	14.0	54.8 ~ 56.0	59	22.5	84.0 ~ 85.6
17	5.8	25.2 ~ 26.6	39	14.4	56.0 ~ 57.4	60	22.9	85.4 ~ 87.0
18	6.2	26.6 ~ 28.0	40	14.8	57.4 ~ 58.8	61	23.3	86.8 ~ 88.2
19	6.6	28.0 ~ 29.4	41	15.3	58.8 ~ 60.2	62	23.7	88.4 ~ 89.6
20	7.0	29.4 ~ 30.8	42	15.7	60.2 ~ 61.6	63	24.0	> 89.6
21	7.4	30.6 ~ 31.8			<u> </u>			<u> </u>



Publication Date :Dec. 2017 Revision: 1.0 14/19



Shut-down control (SD#)

During shutdown mode, means SD#=0, AD52651C ceases all internal circuits To avoid annoying pop during power on/off, well SD# control, like with a power ready signal, is suggested. And, due to its internal pull-up, there is no pop if let the SD# floating.

Mute control (MUTE#)

Like SD# mode, AD52651C ceases output driver, but keep part of internal circuit still working. That could provide quick disable and enable power amplifier.

- Self-protection circuits (Typical values are used below.)
 - AD52651C has built-in over-temperature, overload and voltage detectors.
 - (i) If the internal junction temperature is higher than 160°C, the outputs of loudspeaker drivers will be disabled and at low state. The temperature hysteresis for AD52651C to return to normal operation is about 35°C. The variation of protected temperature is around 10%.
 - (ii) AD52651C has built-in overload protection for both right and left channel. To protect loudspeaker drivers from over-current damage when the wires of loudspeaker are shorted to one another, GND or VDD, circuits for the detection of output loading are built in the AD52651C. For normal operation, loudspeaker resistance is larger than 3.2Ω is required. Otherwise, overload detectors may activate. Once one of right and left channel is overloaded, both loudspeaker drivers will be disabled. And, AD52651C will be recovery from overload fault by toggling SD# down to low and back to high after removing the short.

Application information

Input capacitors (C_{in})

The performance at low frequency (bass) is affected by the corner frequency (f_c) of the high-pass filter composed of input resistors (R_{in}) and input capacitors (C_{in}), determined in equation (a). And, the resistance of input resistors is different at different volume gain. But there is 20% variation in input resistance from 20% process variation in actual resistance of the input resistors. Typically, a $0.47\mu F$ or $1\mu F$ ceramic capacitor is suggested.

$$f_c = \frac{1}{2\pi R_{in}C_{in}} (Hz) \cdots (a)$$

G(dB)	Rin(Ω)
24	42k
18	73k
12	115k
6	160k

Elite Semiconductor Microelectronics Technology Inc.

Publication Date :Dec. 2017
Revision: 1.0 15/19



Capacitor on Vref (C_{Vref})

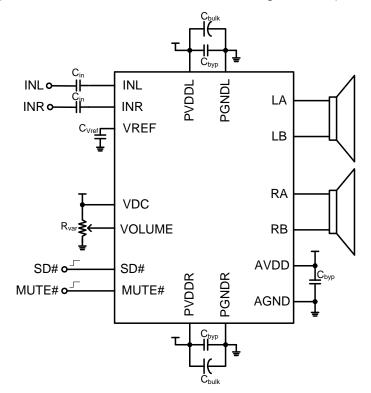
In order to reduce low-frequency noise produced by power supply, the capacitor (C_{Vref}) on Vref, which is the mid-rail voltage of AVDD, is necessary. It has a good help on PSRR. And, to have less annoying pop, the recommended C_{Vref} is the same with Cin.

Decoupling capacitor (C_{byp} and C_{bulk})

Because of the power loss on the trace, which is between the device and decoupling capacitor, the decoupling capacitor should be placed as close as to the device PVDDL (PVDDR) and PGNDL (PGNDR) to reduce any parasitic resistor or inductor between them. And, a low ESR ceramic capacitor (C_{byp}), typically $1\mu F$, is suggested for high frequency transients and as close to AD52651C as possible. For filtering audio band noise signal, a $10\mu F$ or greater capacitor (C_{bulk}) (tantalum or electrolytic type) is suggested.

Application Circuit

Application circuit (DC volume control with external voltage divider)

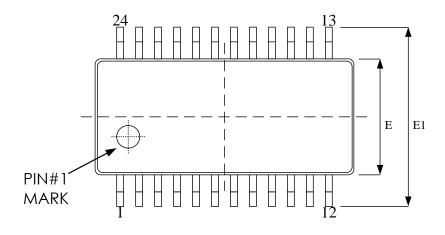


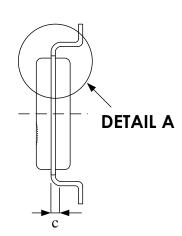
Publication Date :Dec. 2017 Revision: 1.0 16/19



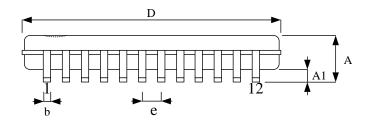
Package Dimensions

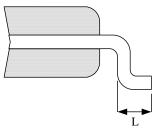
• SSOP 24 (150mil)





TOP VIEW





SIDE VIEW

DETAIL A

Cryss la o l	Dimension in mm			
Symbol	Min	Max		
А	1.35	1.75		
A1	0.10	0.25		
Ъ	0.20	0.31		
С	0.18	0.25		
D	8.53	8.74		
Е	3.80	4.00		
E1	5.80	6.20		
е	0.635 BSC			
L	0.38	1.27		

Publication Date :Dec. 2017 Revision: 1.0 17/19



Revision History

Revision	Date	Description
0.1	2012.05.25	Original
0.2	2012.07.04	Modifying the SD# characteristic of pin description
0.3	2013.12.10	Removing EMP logo. Modifying the Package Dimensions.
0.4	2014.11.27	Package Dimension update
0.5	2015.05.21	1) Change operating voltage from 3.0~5.0V to 3.0~5.5V. 2) Change AMR voltage from 5.5V to 6.0V
1.0	2017.12.29	Remove" Preliminary"and modify to V1.0

Publication Date :Dec. 2017 Revision: 1.0 18/19



Important Notice

All rights reserved.

No part of this document may be reproduced or duplicated in any form or by any means without the prior permission of ESMT.

The contents contained in this document are believed to be accurate at the time of publication. ESMT assumes no responsibility for any error in this document, and reserves the right to change the products or specification in this document without notice.

The information contained herein is presented only as a guide or examples for the application of our products. No responsibility is assumed by ESMT for any infringement of patents, copyrights, or other intellectual property rights of third parties which may result from its use. No license, either express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of ESMT or others.

Any semiconductor devices may have inherently a certain rate of failure. To minimize risks associated with customer's application, adequate design and operating safeguards against injury, damage, or loss from such failure, should be provided by the customer when making application designs.

ESMT's products are not authorized for use in critical applications such as, but not limited to, life support devices or system, where failure or abnormal operation may directly affect human lives or cause physical injury or property damage. If products described here are to be used for such kinds of application, purchaser must do its own quality assurance testing appropriate to such applications.

Publication Date :Dec. 2017 Revision: 1.0 19/19