

2x30W Stereo / 1x60W Mono Class-D Audio Amplifier With Power Limit

Features

- Single supply voltage
4.5V ~ 26V for loudspeaker driver
Built-in LDO output 5V for others
- Supports Multiple Output Configurations
BTL Mode: 30W/CH into 8Ω at 24 V
BTL Mode: 30W/CH into 4Ω at 18 V
PBTL Mode: 60W/CH into 4Ω at 24 V
PBTL Mode: 45W/CH into 4Ω at 18 V
PBTL Mode: 60W/CH into 2Ω at 18 V
- Loudspeaker performance
BTL Mode: 30W/CH into 8Ω <1% THD+N @24V
BTL Mode: 30W/CH into 4Ω <1% THD+N @18V
- >90% efficient Class-D operation eliminates need for heat sink
- Differential inputs
- Four selectable, fixed gain settings
- Internal oscillator
- Short-Circuit protection with auto recovery option
- Under-Voltage detection
- Over-Voltage protection
- Pop noise and click noise reduction
- Adjustable power limit function for speaker protection
- Output DC detection for speaker protection
- Over temperature protection with auto recovery

Applications

- TV audio
- Boom-Box
- Powered speaker
- Monitors
- Consumer Audio Equipment

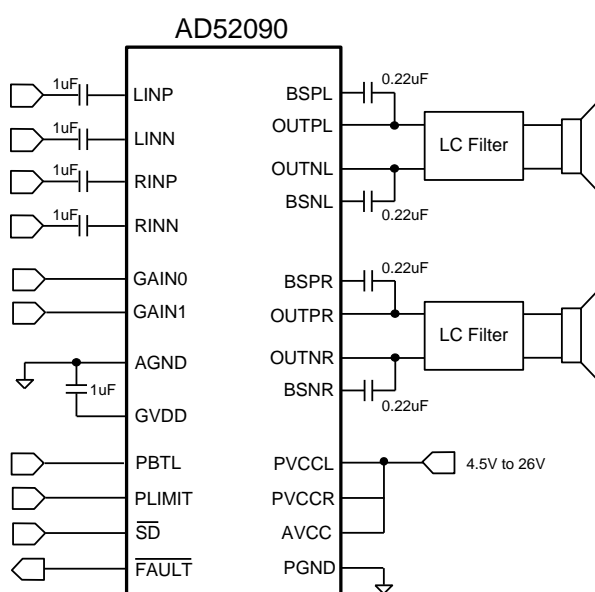
Description

The AD52090 is a high efficiency stereo class-D audio amplifier with adjustable power limit function. The loudspeaker driver operates from 4.5V~26V supply voltage and analog circuit operates at 5V supply voltage. It can deliver 30W/CH output power into 4Ω or 8Ω loudspeaker within 1% THD+N at 24V supply voltage.

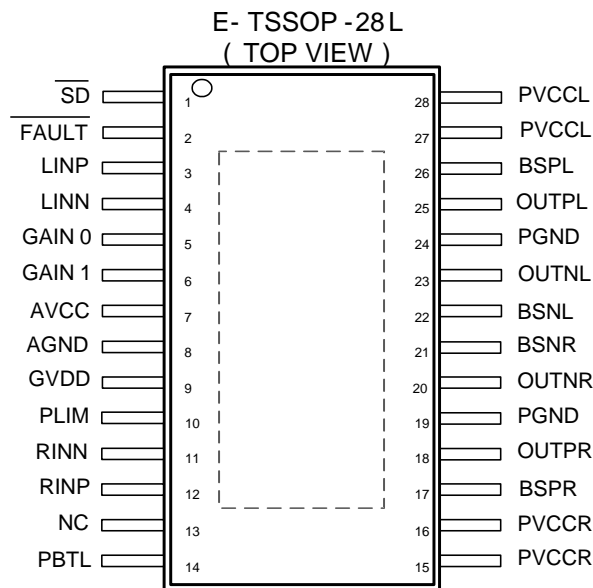
AD52090 provides parallel BTL (Mono) application, and it can deliver 60W into 4Ω loudspeaker at 24V supply voltage. The adjustable power limit function allows user to set a voltage rail lower than half of 5V to limit the amount of current through the speaker.

Output DC detection prevents speaker damage from long-time current stress. AD52090 output short circuit and over temperature protection include auto-recovery feature.

Simplified Application Circuit



Pin Assignments



Pin Description

| NAME | E-TSSOP -28L | TYP | DESCRIPTION |
|--------------------|--------------|-----|---|
| \overline{SD} | 1 | I | Shutdown signal for IC (low = disabled, high = operational). Voltage compliance to AVCC. |
| \overline{FAULT} | 2 | O | Open drain output used to display short circuit or dc detect fault. Voltage compliant to AVCC. Short circuit faults can be set to auto-recovery by connecting \overline{FAULT} pin to \overline{SD} pin. Otherwise, both short circuit faults and dc detect faults must be reset by cycling AVCC. |
| LINP | 3 | I | Positive audio input for left channel. |
| LINN | 4 | I | Negative audio input for left channel. |
| GAIN0 | 5 | I | Gain select least significant bit. Voltage compliance to AVCC. |
| GAIN1 | 6 | I | Gain select most significant bit. Voltage compliance to AVCC. |
| AVCC | 7 | P | Analog supply. |
| AGND | 8 | P | Analog signal ground. Connect to the thermal pad. |
| GVDD | 9 | O | 5V regulated output, also used as supply for PLIMIT function. |
| PLIMIT | 10 | I | Power limit level adjustment. Connect a resistor divider from GVDD to GND to set power limit. Give V(PLIMIT) <2.4V to set power limit level. Connect to GVDD (>2.4V) or GND to disable power limit function. |
| RINN | 11 | I | Negative audio input for right channel. |
| RINP | 12 | I | Positive audio input for right channel. |
| NC | 13 | NA | NC pin. |
| PBTL | 14 | I | Parallel BTL mode switch, high for parallel BTL output. Voltage compliance to AVCC. |

| | | | |
|-------------|-------|---|---|
| PVCCR | 15,16 | P | High-voltage power supply for right-channel. Right channel and left channel power supply inputs are connect internal. |
| BSPR | 17 | I | Bootstrap I/O for right channel, positive high side FET. |
| OUTPR | 18 | O | Class-D H-bridge positive output for right channel. |
| PGND | 19 | P | Power ground for the H-bridges. |
| OUTNR | 20 | O | Class-D H-bridge negative output for right channel. |
| BSNR | 21 | I | Bootstrap I/O for right channel, negative high side FET. |
| BSNL | 22 | I | Bootstrap I/O for left channel, negative high side FET. |
| OUTNL | 23 | O | Class-D H-bridge negative output for left channel. |
| PGND | 24 | P | Power ground for the H-bridges. |
| OUTPL | 25 | O | Class-D H-bridge positive output for left channel. |
| BSPL | 26 | I | Bootstrap I/O for left channel, positive high side FET. |
| PVCLL | 27,28 | P | High-voltage power supply for right-channel. Right channel and left channel power supply inputs are connect internal. |
| Thermal Pad | | P | Must be soldered to PCB's ground plane. |

Ordering Information

| Product ID | Package | Packing | Comments |
|-----------------|-------------|--|----------|
| AD52090-QG28NRR | E-TSSOP 28L | 2500 Units / Reel 1 Reels / Small Box | Green |

Available Package

| Package Type | Device No. | $\theta_{JA} (^{\circ}C/W)$ | $\theta_{JT} (^{\circ}C/W)$ | $\Psi_{JT} (^{\circ}C/W)$ | Exposed Thermal Pad |
|--------------|------------|-----------------------------|-----------------------------|---------------------------|---------------------|
| E-TSSOP 28L | AD52090 | 28 | 27.1 | 1.33 | Yes (Note 1) |

Note 1.1: The thermal pad is located at the bottom of the package. To optimize thermal performance, soldering the thermal pad to the PCB's ground plane is necessary.

Note 1.2: θ_{JA} is simulated on a room temperature ($T_A=25^{\circ}C$), natural convection environment test board, which is constructed with a thermally efficient, 4-layers PCB (2S2P). The measurement is simulated using the JEDEC51-5 thermal measurement standard.

Note 1.3: θ_{JT} represents the thermal resistance for the heat flow between the chip junction and the package's top surface. It's extracted from the simulation data with obtaining a cold plate on the package top.

Note 1.4: Ψ_{JT} represents the thermal parameter for the heat flow between the chip junction and the package's top surface center. It's extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-5.

Marking Information

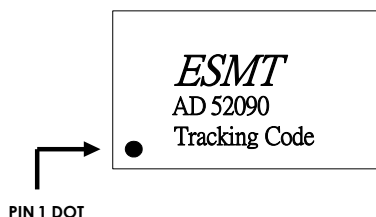
AD52090

- Marking Information

Line 1 : LOGO

Line 2 : Product No

Line 3 : Tracking Code



Absolute Maximum Ratings

Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device.

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN | MAX | UNIT |
|------------------|--------------------------------------|--|------|------|------|
| PVCC | Supply voltage | PVCCL, PVCCR, AVCC | -0.3 | 30 | V |
| V _I | Interface pin voltage | \overline{SD} , GAIN0, GAIN1, PBTL, \overline{FAULT} | -0.3 | 30 | V |
| | | PLIMIT | -0.3 | 5.5 | |
| T _A | Operating free-air temperature range | | -40 | 85 | °C |
| T _J | Operating junction temperature range | | -40 | 150 | °C |
| T _{stg} | Storage temperature range | | -65 | 150 | °C |
| R _L | Minimum Load Resistance | BTL (Stereo) | 3.2 | | Ω |
| | | PBTL (Mono) | 3.2 | | Ω |
| | | PBTL (Mono) ≤ 18V | 1.6 | | Ω |
| ESD | Human Body Model | | | ±2k | V |
| | Charged Device Model | | | ±500 | |

Recommended Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN | MAX | UNIT |
|-----------------|--------------------------|--|-----|-----|------|
| PVCC | Supply voltage | AVCC, PVCCL, PVCCR | 4.5 | 26 | V |
| V _{IH} | High-level input voltage | \overline{SD} , GAIN0, GAIN1, PBTL | 2 | | V |
| V _{IL} | Low-level input voltage | \overline{SD} , GAIN0, GAIN1, PBTL | | 0.8 | V |
| V _{OL} | Low-level output voltage | FAULT, R _{PULL-UP} =100k, PVCC=18V | | 0.8 | V |
| I _{IH} | High-level input current | \overline{SD} , GAIN0, GAIN1, PBTL, V _I =2V, PVCC=18V | | 50 | uA |
| I _{IL} | Low-level input current | \overline{SD} , GAIN0, GAIN1, PBTL, V _I =0.8V, PVCC=18V | | 5 | uA |
| T _A | Operating free-air | | -40 | 85 | °C |

General Electrical Characteristics

- PVCC=24V, R_L=8Ω, T_A=25°C (unless otherwise noted)

| SYMBOL | PARAMETER | CONDITION | | MIN | TYP | MAX | UNIT |
|---------------------|---|---|------------|------|------|------|------|
| I _{CC(q)} | Quiescent supply current | $\overline{SD}=2V$, no load, PVCC=12V | | | 20 | 35 | mA |
| I _{CC(SD)} | Quiescent supply current in shutdown mode | $\overline{SD}=0.8V$, no load, PVCC=12V | | | <12 | 25 | uA |
| R _{DS(on)} | Drain-source on-state resistance-High side NMOS | PVCC=12V, I _d =500mA, T _J =25°C | | | 90 | | mΩ |
| | Drain-source on-state resistance-Low side NMOS | | | | 90 | | mΩ |
| V _{OS} | Class-D output offset voltage (measured differential) | PVCC=12V V _I =0V, Gain=36dB | | | 1.5 | 15 | mV |
| t _{ON} | Turn-on time | $\overline{SD}=2V$ | | | 90 | | ms |
| t _{OFF} | Turn-off time | $\overline{SD}=0.8V$ | | | 2 | | us |
| I _{AVCC} | Operating current for AVCC | | | | 8.5 | 12.8 | mA |
| GVDD | Regulator output | IGVDD=0.1mA | | 4.75 | 5 | 5.25 | V |
| G | Gain | GAIN1=0.8V | GAIN0=0.8V | 17.5 | 18.5 | 19.5 | dB |
| | | | GAIN0=2V | 25 | 26 | 27 | |
| | | GAIN1=2V | GAIN0=0.8V | 31 | 32 | 33 | |
| | | | GAIN0=2V | 35 | 36 | 37 | |

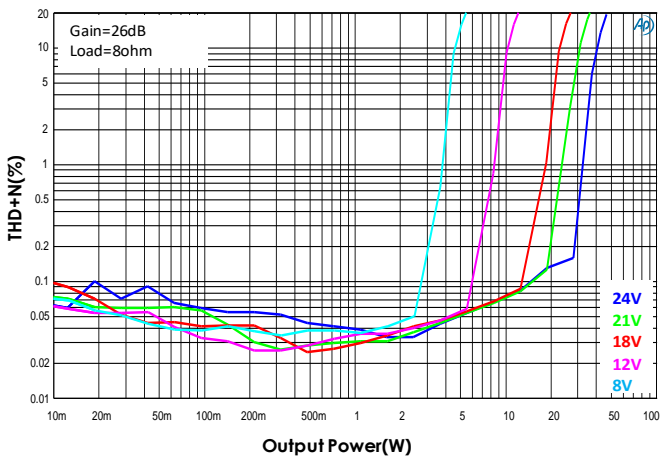
Electrical Characteristics and Specifications of Loudspeaker Driver

- PVCC=24V, R_L=8Ω with passive LC low-pass filterin ESMT EVB (unless otherwise noted).

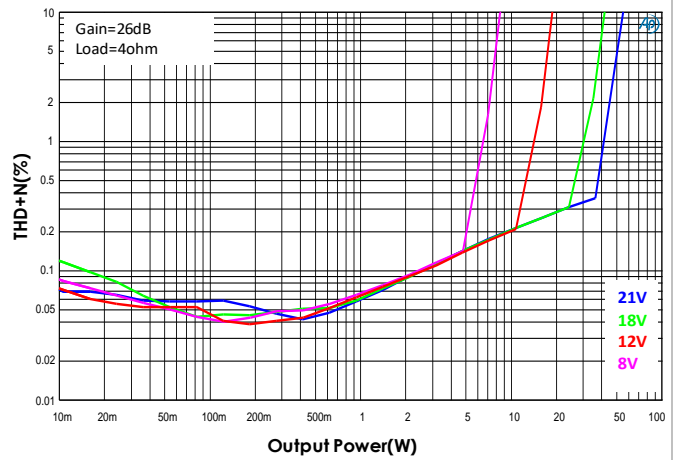
| SYMBOL | PARAMETER | CONDITION | MIN | TYP | MAX | UNIT |
|---------------------|--------------------------------------|--|-----|-------|-----|------|
| P _O | Output power (BTL) | THD+N=0.3%, f=1kHz, PVCC=24V | | 30 | | W |
| | | THD+N=10%, f=1kHz, PVCC=12V | | 10 | | |
| | | THD+N=0.35%,f=1kHz, VCC=21V, 4ohm | | 30 | | |
| | | THD+N=0.95%,f=1kHz, VCC=18V, 4ohm | | 30 | | |
| | | THD+N=10%,f=1kHz, PVCC=12V, 4ohm | | 19 | | |
| | | THD+N=10%,f=1kHz, PVCC=8V, 4ohm | | 8.5 | | |
| | Output power (PBTL) | THD+N=0.27%, f=1kHz, PVCC=24V, 4ohm | | 60 | | |
| | | THD+N=10%, f=1kHz, PVCC=18V, 4ohm | | 45 | | |
| | | THD+N=0.5%, f=1kHz, PVCC=18V, 2ohm | | 60 | | |
| THD+N | Total harmonic distortion plus noise | PVCC=24V, R _L =8Ω, f=1kHz, P _O =15W (half-power) | | 0.025 | | % |
| | | PVCC=12V, R _L =8Ω, f=1kHz, P _O =5W (half-power) | | 0.18 | | |
| SNR | Signal to noise ratio | Maximum output at THD+N<1%, f=1kHz, Gain=18.5dB, a-weighted | | 103 | | dB |
| V _n | Output integrated noise | F=20Hz ~ 20kHz, Gain=18.5dB, a-weighted filter, R _L =8Ω | | 75 | | uV |
| K _{SVR} | Power Supply Rejection Ratio | V _{ripple} =200mVpp at 1kHz, Gain=18.5dB, inputs ac-grounded | | -70 | | dB |
| X-talk | Crosstalk | F=1kHz, V _O =1Vrms, Gain=18.5dB | | -95 | | dB |
| f _{OSC} | Oscillator frequency | | 250 | 310 | 370 | kHz |
| T _{SENSOR} | Thermal trip point | | | 170 | | °C |
| | Thermal hysteresis | | | 35 | | °C |

Typical Characteristics

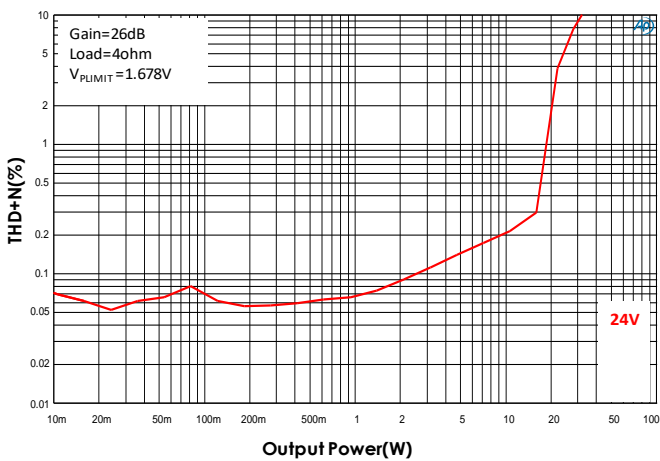
THD+N vs. Output Power, 8Ω load(BTL)



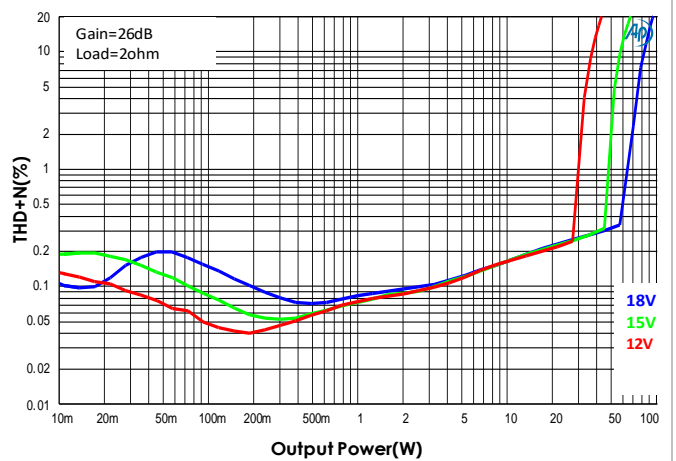
THD+N vs. Output Power, 4Ω load(BTL)



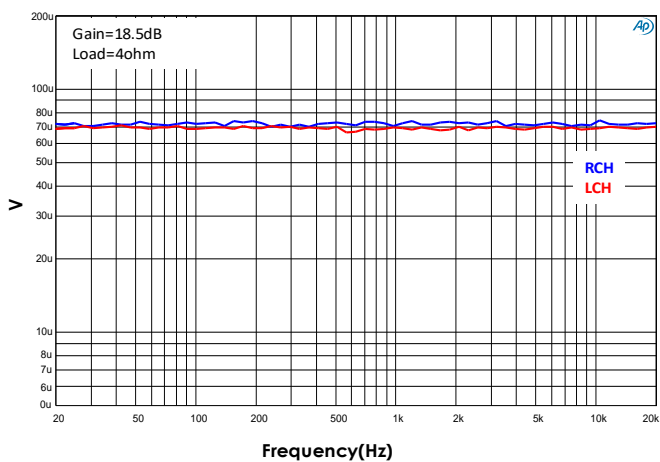
THD+N vs. Output Power, 4Ω load (BTL)



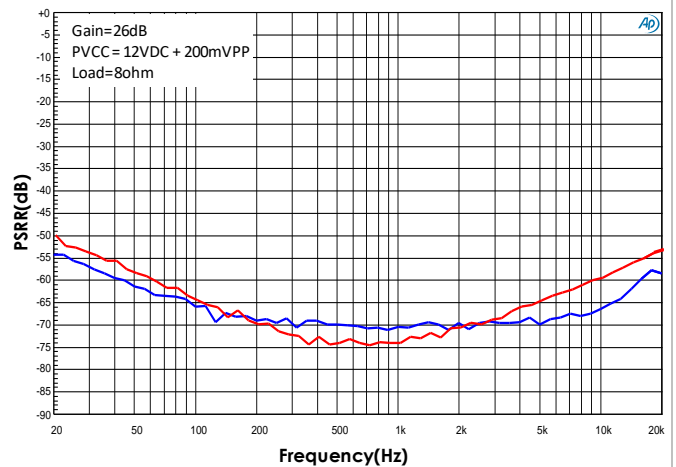
THD+N vs. Output Power, 2Ω load (PBTL)



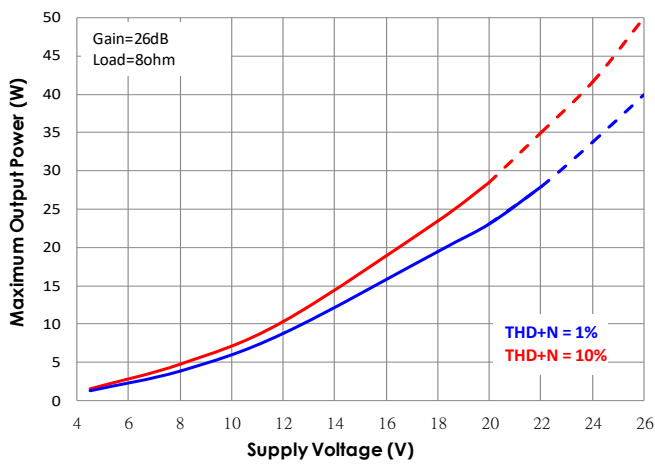
Noise, 24V, 4Ω load (BTL)



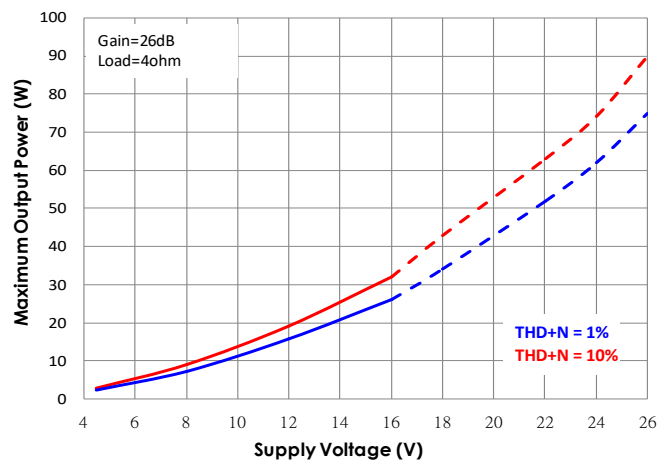
Supply Ripple Rejection Ratio vs Frequency (BTL)



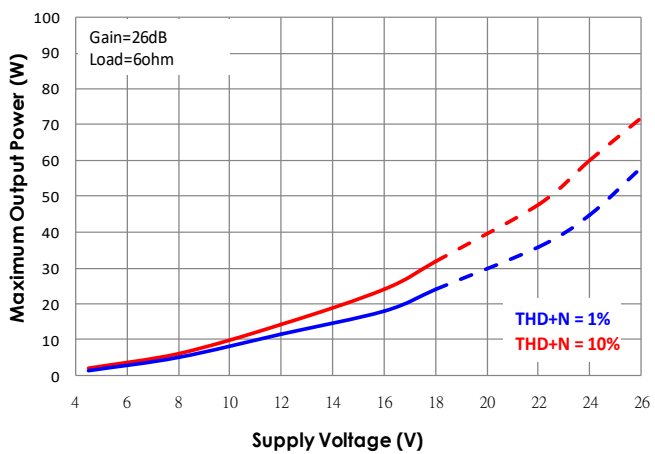
Maximum Output Power vs Supply Voltage (BTL)



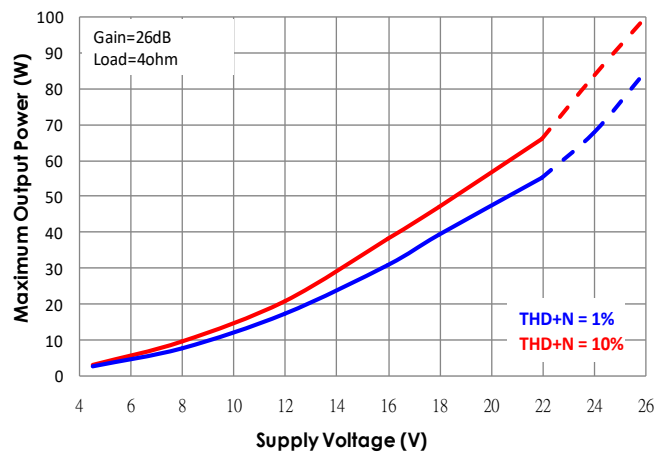
Maximum Output Power vs. Supply Voltage (BTL)



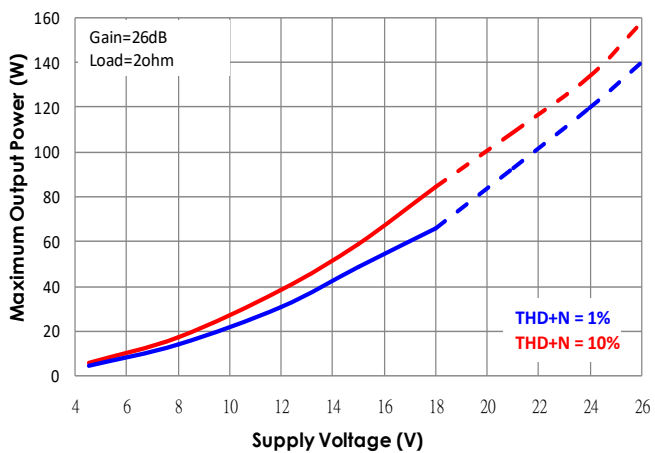
Maximum Output Power vs Supply Voltage (BTL)



Maximum Output Power vs Supply Voltage (PBTL)

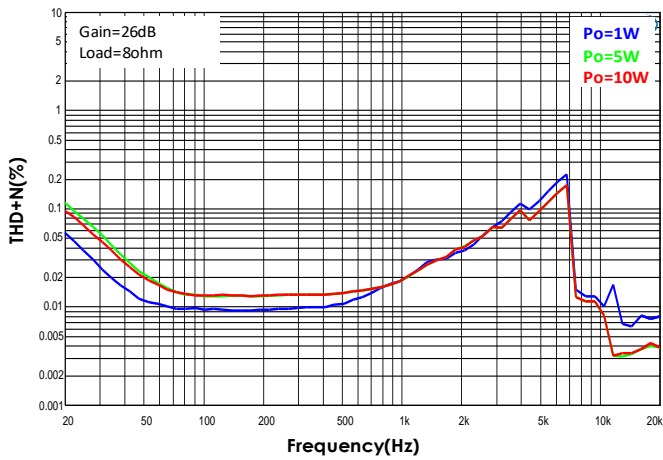


Maximum Output Power vs Supply Voltage (PBTL)

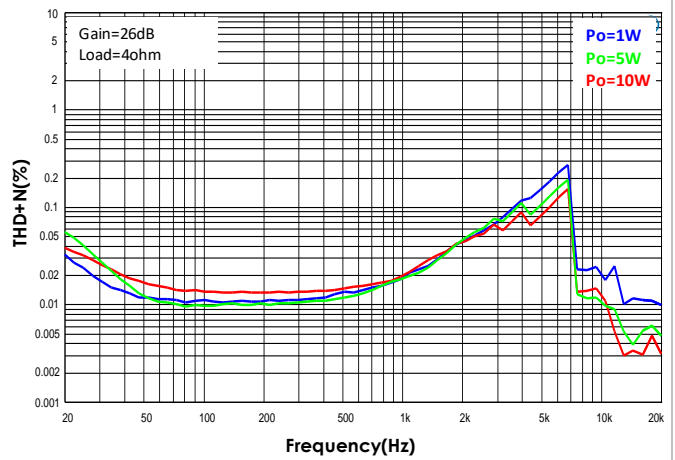


Note: Dashed Line represent thermally limited regions.

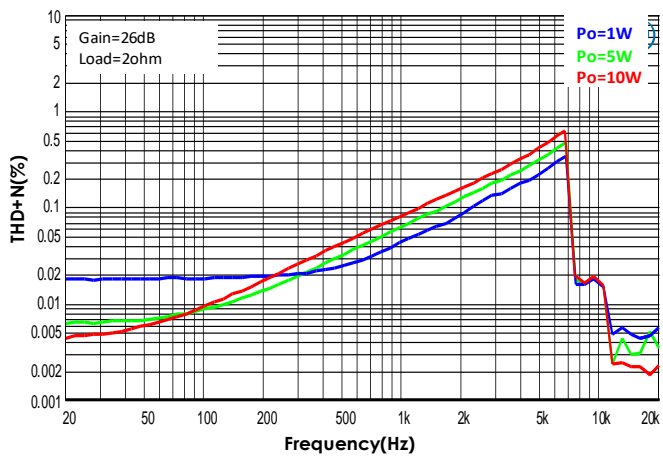
THD + N (%) vs. Frequency, 24V, 8Ω load (BTL)



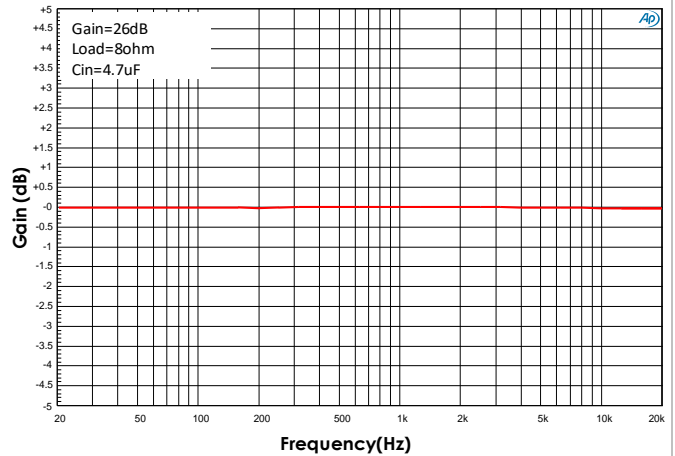
THD + N (%) vs. Frequency, 24V, 4Ω load (BTL)



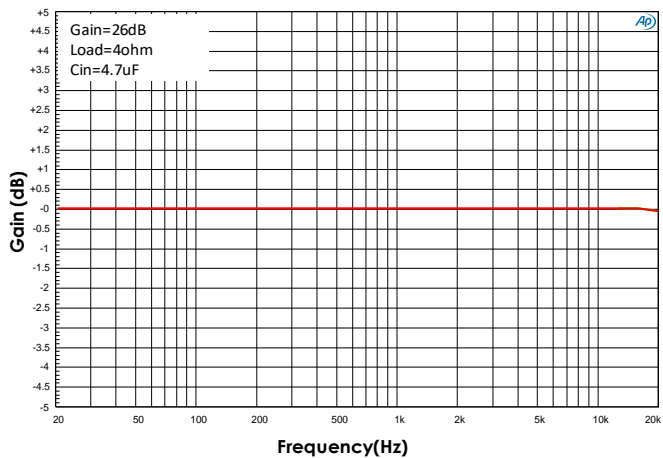
THD + N (%) vs. Frequency, 18V, 2Ω load (PBTL)



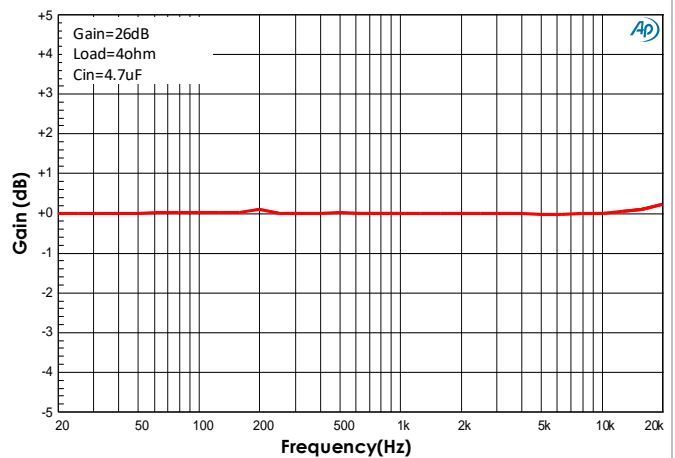
Gain vs. Frequency, 12V, 8Ω load (BTL)

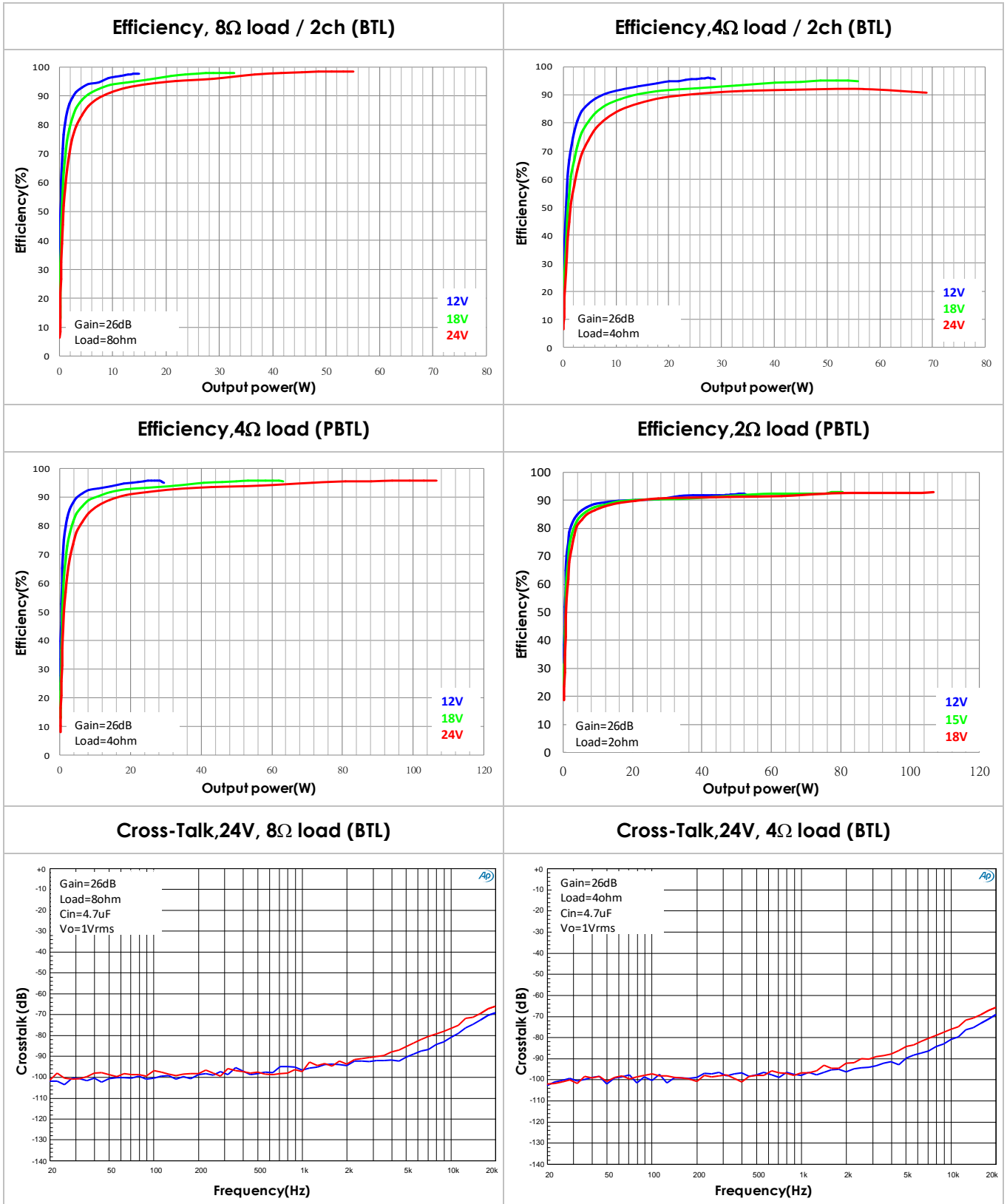


Gain vs. Frequency, 12V, 4Ω load (BTL)

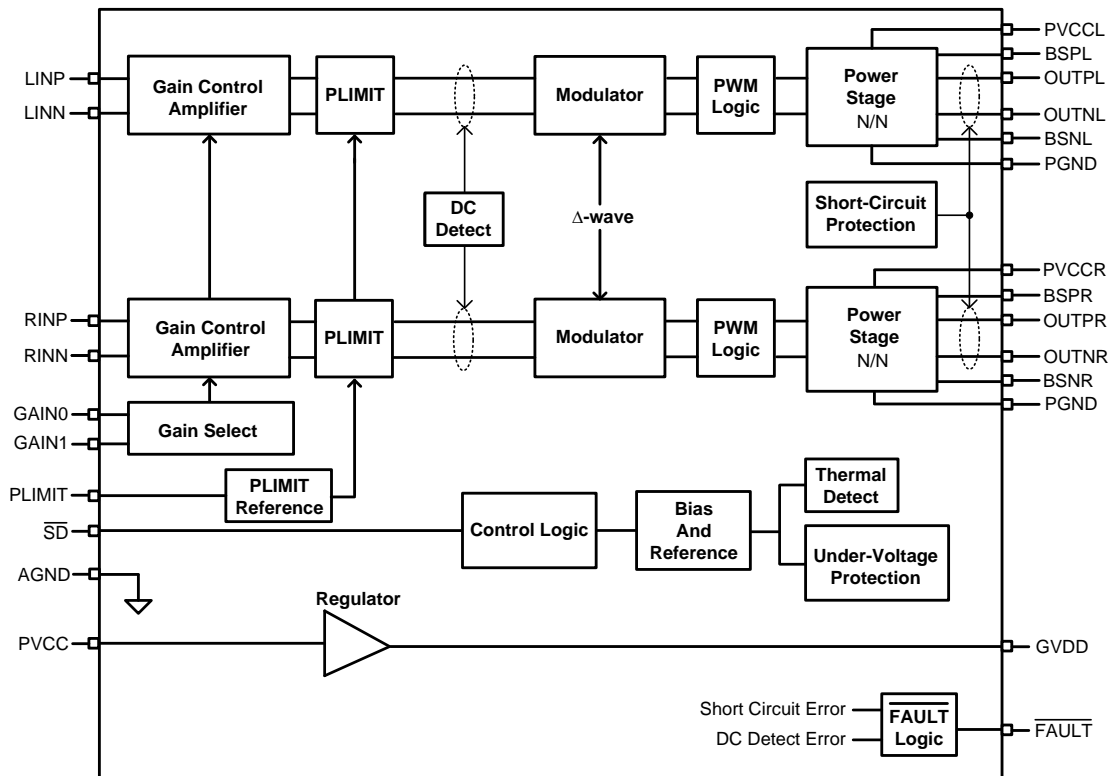


Gain vs. Frequency, 12V, 2Ω load (PBTL)





Functional Block Diagram



Operation Descriptions

- **Gain settings**

The gain of the AD52090 is set by two input pins, GAIN0 and GAIN1. By varying input resistance in AD52090, the various volume gains are achieved. The respective volume gain and input resistance are listed in Table 1. However, there is 20% variation in input resistance from production variation.

Table 1. Volume gain and input impedance

| GAIN1 | GAIN0 | Volume Gain (dB) | Input Resistance, R_{in} (k Ω) |
|-------|-------|------------------|--|
| 0 | 0 | 18.5 | 70.5 |
| 0 | 1 | 26 | 30 |
| 1 | 0 | 32 | 15 |
| 1 | 1 | 36 | 9 |

- **Shutdown (\overline{SD}) control**

Pulling \overline{SD} pin low will let AD52090 operate in low-current state for power conservation. The AD52090 outputs will enter mute once \overline{SD} pin is pulled low, and regulator will also disable to save power. If let \overline{SD} pin floating, the chip will enter shutdown mode because of the internal pull low resistor. For the best power-off performance, place the chip in the shutdown mode in advance of removing the power supply.

- **DC detection**

AD52090 has dc detection circuit to protect the speakers from DC current which might be occurred as input capacitor defect or inputs short on printed circuit board. The detection circuit detects first volume amplifier stage output, when both differential outputs' voltage become higher than a determined voltage or lower than a determined voltage for more than 420ms, the dc detect error will occur and report to \overline{FAULT} pin. At the same time, loudspeaker drivers of right/left channel will disable and enter Hi-Z. This fault can not be cleared by cycling \overline{SD} , it is necessary to cycle the PVCC supply.

The minimum differential input voltages required to trigger the DC detect function are shown in table2. The input voltage must keep above the voltage listed in the table for more than 420msec to trigger the DC detect fault. The equivalent class-D output duty of the DC detect threshold is listed in table3.

Table 2. DC Detect Threshold

| AV (dB) | V _{in} (mV, differential) |
|---------|------------------------------------|
| 18.5 | 286 |
| 26 | 136 |
| 32 | 64 |
| 36 | 44 |

Table 3. Output DC Detect Duty (for Either Channel)

| PVCC (V) | Output Duty Exceeds |
|----------|---------------------|
| 8 | 40 |
| 12 | 40 |
| 16 | 40 |

- **Thermal protection**

If the internal junction temperature is higher than 170°C, the outputs of loudspeaker drivers will be disabled and at low state. The temperature for AD52090 returning to normal operation is about 135°C. The variation of protected temperature is about 10%. Thermal protection faults are NOT reported on the $\overline{\text{FAULT}}$ pin.

- **Short-circuit protection**

To protect loudspeaker drivers from over-current damage, AD52090 has built-in short-circuit protection circuit. When the wires connected to loudspeakers are shorted to each other or shorted to VSS or to PVCC, overload detectors may activate. Once one of right and left channel overload detectors are active, the amplifier outputs will enter a Hi-Z state and the protection latch is engaged. The short protection fault is reported on $\overline{\text{FAULT}}$ pin as a low state. The latch can be cleared by reset $\overline{\text{SD}}$ or power supply cycling.

The short circuit protection latch can have auto-recovery function by connect the $\overline{\text{FAULT}}$ pin directly to $\overline{\text{SD}}$ pin. The latch state will be released after 420msec, and the short protection latch will re-cycle if output overload is detected again.

- **Under-voltage detection**

When the GVDD voltage is lower than 2.8V or the AVCC voltage is lower than 4V, loudspeaker drivers of right/left channel will be disabled and kept at low state. Otherwise, AD52090 return to normal operation.

● **Over-voltage protection**

When the AVCC voltage is higher than 29.5V, loudspeaker will be disabled kept at low state. The protection status will be released as AVCC lower than 29V.

● **Power limit function**

- The voltage at PLIMIT pin can used to limit the power of first gain control amplifier output. Add a resistor divider from GVDD to ground to set the voltage V_{PLIMIT} at the PLIMIT pin. The voltage V_{PLIMIT} sets a limit on the output peak-to-peak voltage. PLIMIT is adjustable from 1.33V~2.5V.

For normal BTL operation (Stereo) and PBTL (Mono) operation:

$$P_o @ 1\% = \frac{\left[\frac{2.5V - P_{LIMIT}}{2.1V + 0.81 \times P_{LIMIT}} \times 2 \times PVDD \times (1.22 - 0.0092 \times PVDD) \right]^2}{2 \times R_L}$$

$$P_o @ 10\% = (P_o @ 1\%) \times (1.21 + 0.021 \times PVDD)$$

Connect PLIMIT pin to ground or GVDD to disable power limit function. The output variation during power limit feature enable may have +-20% variation due to process window.

Table 4.1 PLIMIT Typical Operation I

| Test Conditions | Output P _O (W) | V _{PLIMIT} (V) @ THD+N=10% |
|-------------------|---------------------------|-------------------------------------|
| PVCC=24V RL=8Ω | 5 | 1.973 |
| | 8 | 1.851 |
| | 10 | 1.785 |
| | 12 | 1.727 |
| | 15 | 1.652 |
| | 20 | 1.545 |

Table 4.2 PLIMIT Typical Operation II

| Test Conditions | Output P _O (W) | V _{PLIMIT} (V) @ THD+N=10% |
|-------------------|---------------------------|-------------------------------------|
| PVCC=12V RL=8Ω | 3 | 1.744 |
| | 5 | 1.564 |
| | 8 | 1.371 |
| | 9 | 1.319 |

Table 4.3 PLIMIT Typical Operation III

| Test Conditions | Output P _O (W) | V _{PLIMIT} (V) @ THD+N=10% |
|-------------------|---------------------------|-------------------------------------|
| PVCC=24V RL=4Ω | 10 | 1.973 |
| | 15 | 1.869 |
| | 20 | 1.785 |
| | 30 | 1.651 |

Table 4.4 PLIMIT Typical Operation IV

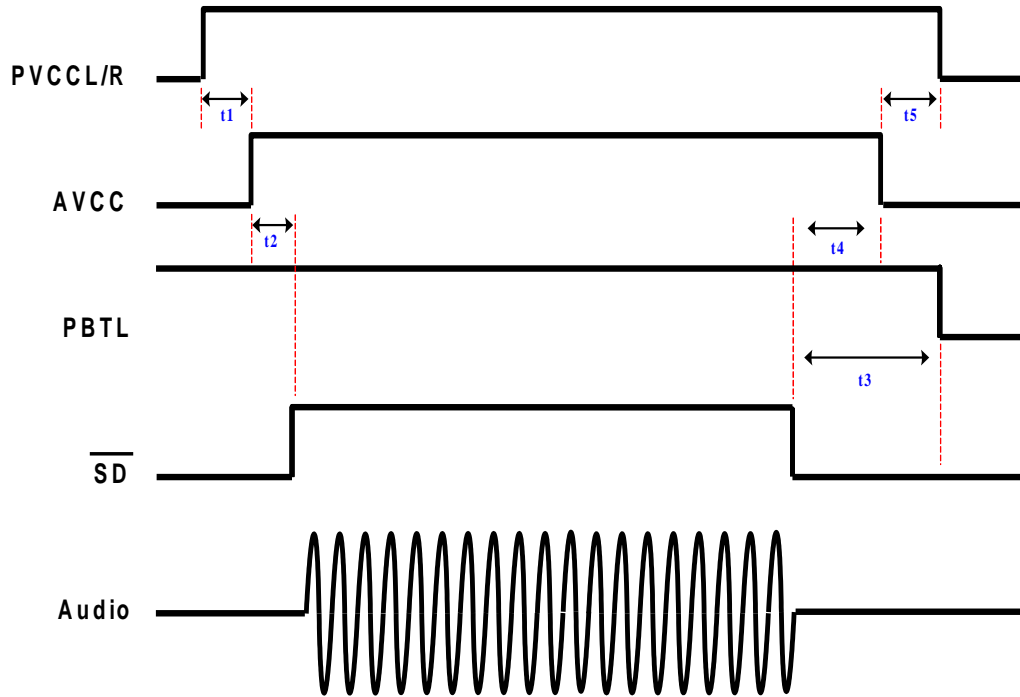
| Test Conditions | Output P _O (W) | V _{PLIMIT} (V) @ THD+N=10% |
|-------------------|---------------------------|-------------------------------------|
| PVCC=12V RL=4Ω | 5 | 1.8 |
| | 8 | 1.646 |
| | 10 | 1.564 |
| | 15 | 1.4 |

● **PBTL (Mono) function**

AD52090 provides the application of parallel BTL operation with two outputs of each channel connected directly. If the PBTL pin is tied high, the positive and negative outputs of left and right channel are synchronized and in phase. Apply the input signal to the RIGHT channel input in PBTL mode and let the LEFT channel input grounded, and place the speaker between the LEFT and RIGHT outputs. The output swing is doubled of that in normal mode. See the application circuit example for PBTL (Mono) mode operation. For normal BTL (Stereo) operation, connect the PBTL pin to ground.

- **Power On/Off sequence**

Hereunder is AD52090's power on/off sequence.



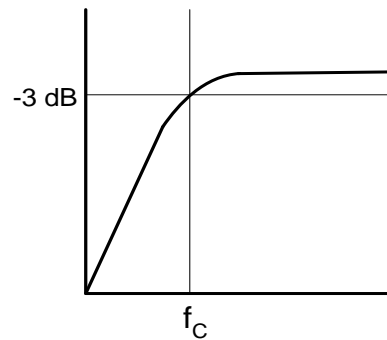
| Symbol | Min. (ms) | Typ. (ms) | Max. (ms) |
|--------|--|-----------|-----------|
| t1 | 0 | - | - |
| t2 | 0.1 | - | - |
| t3 | 0.2 (Don't care for PBTL=0 in stereo operating) | - | - |
| t4 | 0.1 | - | - |
| t5 | 0 | - | - |

Application information

● **Input capacitors (C_{in})**

The performance at low frequency (bass) is affected by the corner frequency (f_c) of the high-pass filter composed of input resistor (R_{in}) and input capacitor (C_{in}), determined in equation (2). Typically, a 0.1μF or 1μF ceramic capacitor is suggested for C_{in}. The resistance of input resistors is different at different gain setting. The respective gain and input resistance are listed in Table 1 (shown at GAIN SETTING). However, there is 20% variation in input resistance from production variation.

$$f_c = \frac{1}{2\pi R_{in} C_{in}} \text{ (Hz)} \dots\dots\dots (2)$$



● **Ferrite Bead selection**

If the traces from the AD52090 to speaker are short, the ferrite bead filters can reduce the high frequency emissions to meet FCC requirements. A ferrite bead that has very low impedance at low frequency and high impedance at high frequency (above 1MHz) is recommended. The impedance of the ferrite bead can be used along with a small capacitor with a value around 1000pF to reduce the frequency spectrum of the signal to an acceptable level.

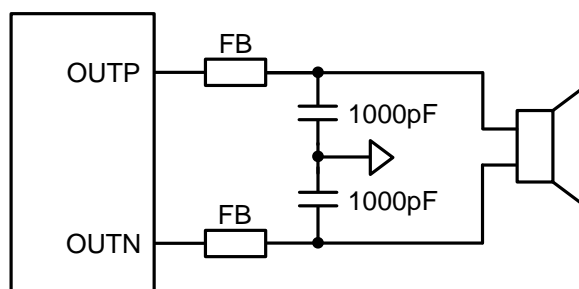


Figure 2. Typical Ferrite Bead Filter

● **Output LC Filter**

If the traces from the AD52090 to speaker are not short, it is recommended to add the output LC filter to eliminate the high frequency emissions. Figure 3 shows the typical output filter for 8Ω speaker with a cut-off frequency of 61 kHz and Figure 4 shows the typical output filter for 4Ω speaker with a cut-off frequency of 34 kHz.

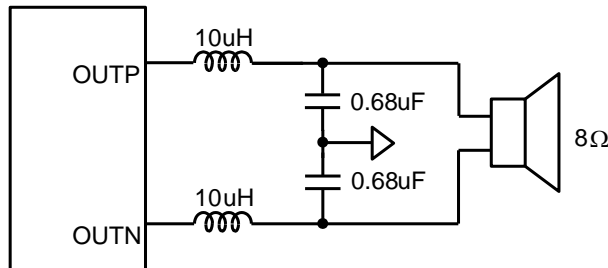


Figure 3. Typical LC Output Filter for 8Ω Speaker

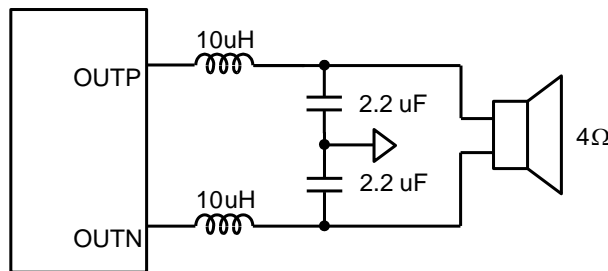


Figure 4. Typical LC Output Filter for 4Ω Speaker

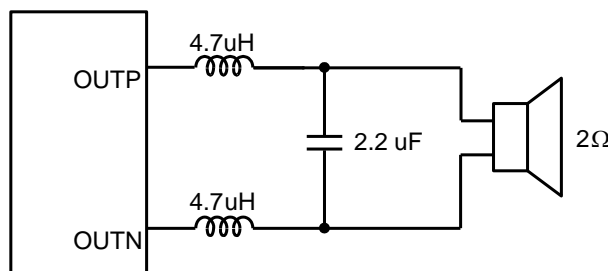


Figure 5. Typical LC Output Filter for 2Ω Speaker

- **Power supply decoupling capacitor (Cs)**

Because of the power loss on the trace between the device and decoupling capacitor, the decoupling capacitor should be placed close to PVCC and PGND to reduce any parasitic resistor or inductor. A low ESR ceramic capacitor, typically 1000pF, is suggested for high frequency noise rejection. For mid-frequency noise filtering, place a capacitor typically 0.1 μ F or 1 μ F as close as possible to the device PVCC leads works best. For low frequency noise filtering, a 100 μ F or greater capacitor (tantalum or electrolytic type) is suggested.

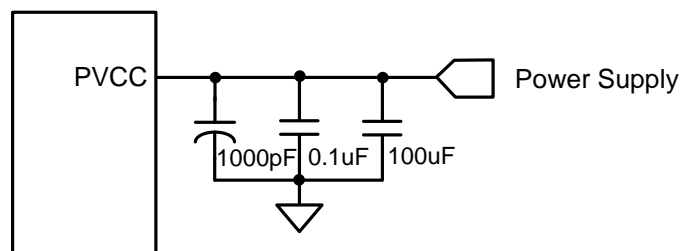
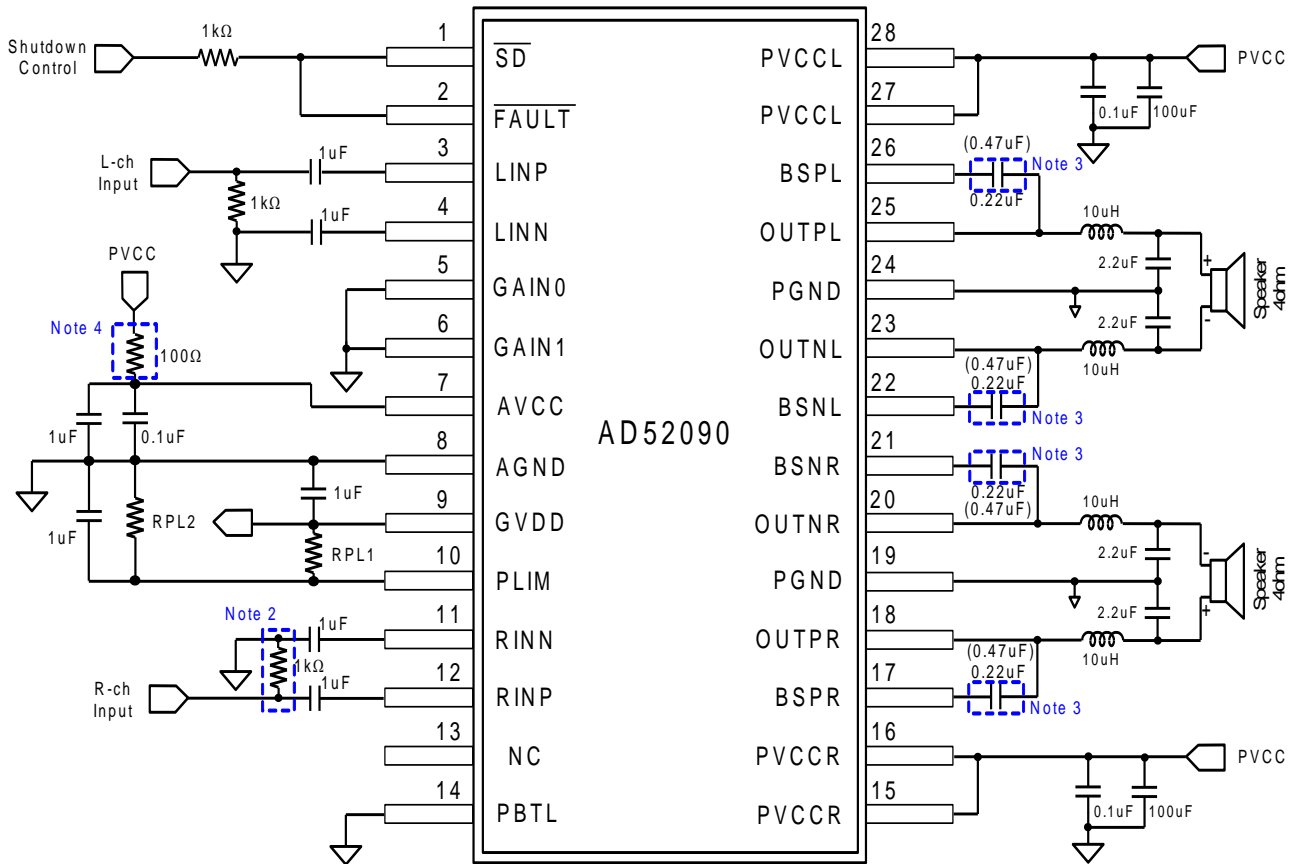


Figure 6. Recommended Power Supply Decoupling Capacitors.

Application Circuit Example

- Application circuit for BTL (Stereo) mode configuration and Single-Ended Input



Note 2: These resistances must be connected to ground, resistance=1Kohm.

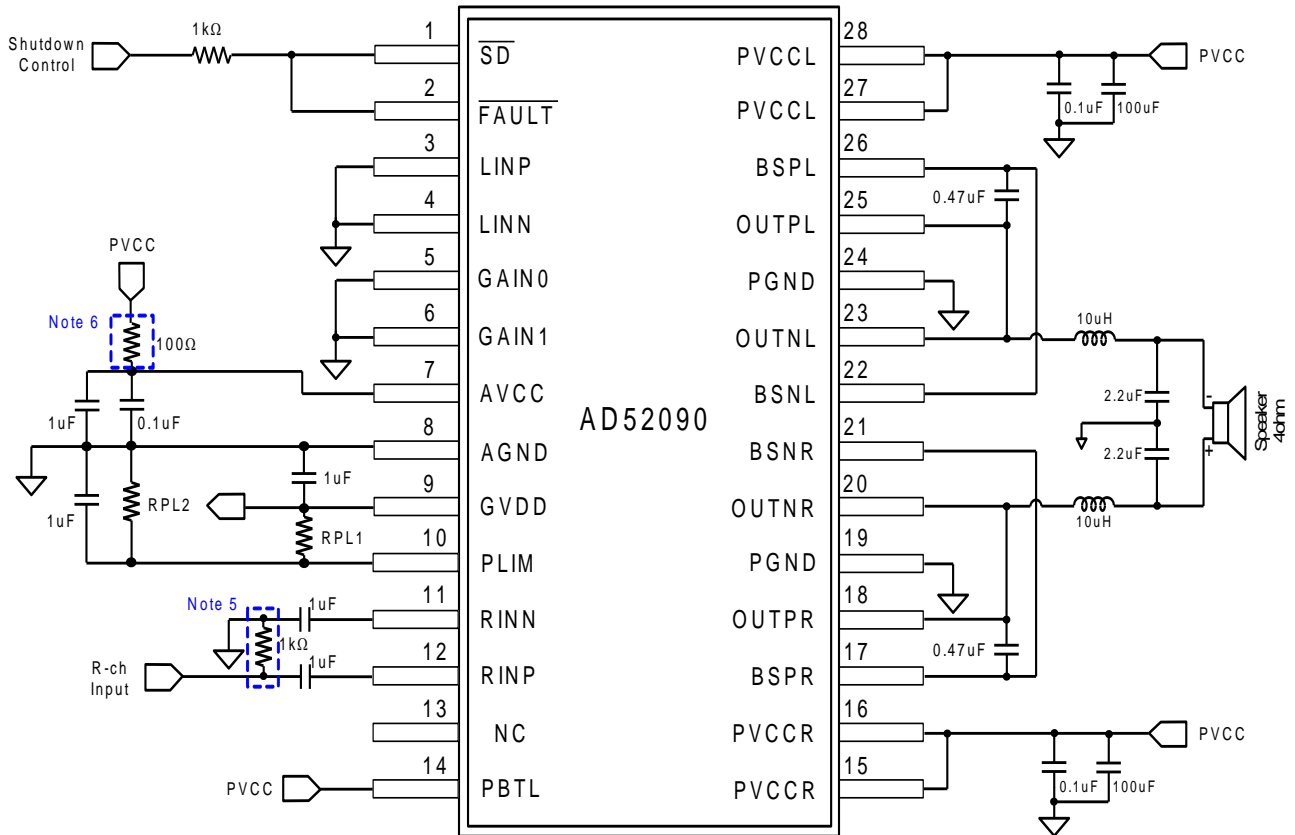
Note 3: These capacitors should be change to 0.47μF, while the PVCC<=5V.

Note 4: The under-voltage threshold for AVCC could be adjusted by R_{AVCC} , the formula will be

$$\text{followed } R_{AVCC} \leq \frac{PVCC - 4}{30} (k\Omega) \text{ to adjust it.}$$

Application Circuit Example

- Application circuit for parallel BTL (Mono) mode configuration and Single-Ended Input



Note 5: These resistances must be connected to ground, resistance=1Kohm.

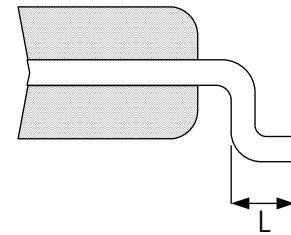
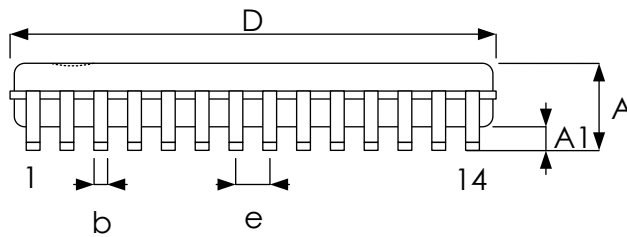
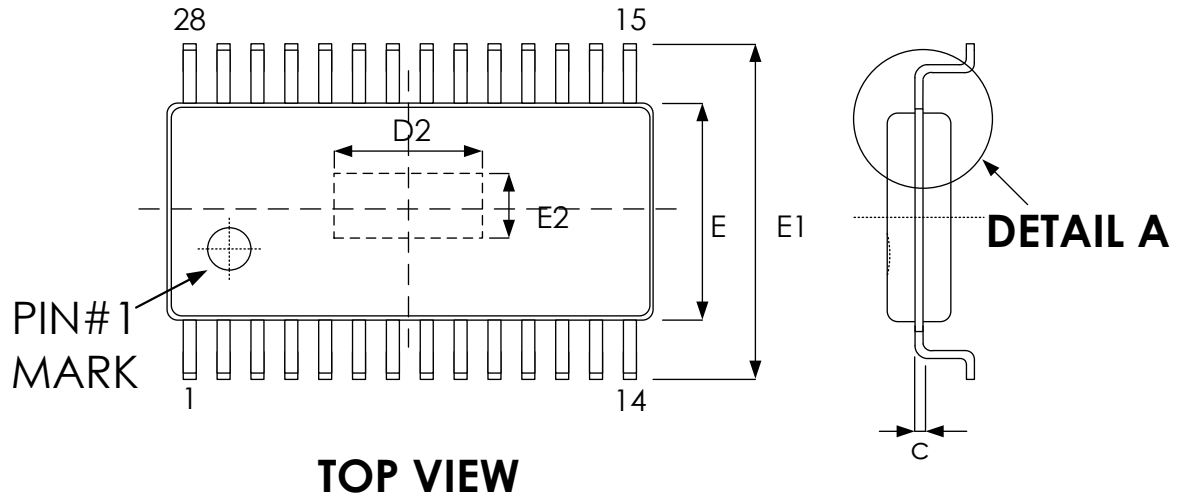
Note 6: The under-voltage threshold for AVCC could be adjusted by R_{AVCC} , the formula will be followed

$$R_{AVCC} \leq \frac{PVCC - 4}{30} (k\Omega) \text{ to adjust it.}$$

Note 7: Be noted that input should be applied on R-channel only for Mono application

Package Dimensions

- E-TSSOP 28L(173 mil)



| Symbol | Dimension in mm | |
|--------|-----------------|------|
| | Min | Max |
| A | -- | 1.20 |
| A1 | 0.05 | 0.15 |
| b | 0.19 | 0.30 |
| c | 0.09 | 0.20 |
| D | 9.60 | 9.80 |
| E | 4.30 | 4.50 |
| E1 | 6.30 | 6.50 |
| e | 0.65 BSC | |
| L | 0.45 | 0.75 |

Exposed pad

| | Dimension in mm | |
|----|-----------------|------|
| | Min | Max |
| D2 | 5.00 | 6.40 |
| E2 | 2.50 | 2.90 |

Revision History

| Revision | Date | Description |
|----------|------------|--|
| 0.1 | 2018.09.13 | Initial version. |
| 1.0 | 2019.01.07 | Remove "Preliminary" and reversion to 1.0 ver. & Modify gain max/min spec & modify Package Dimensions & modify plimit table 4.1~4.4. |
| 1.1 | 2019.03.15 | Update typical characteristics. |
| 1.2 | 2020.01.02 | Update operation descriptions for under-voltage detection. Update application circuit. |
| 1.3 | 2020.08.17 | Update absolute maximum ratings. Update application circuit example. |
| 1.4 | 2020.12.07 | Update application circuit example. |
| 1.5 | 2021.10.13 | 1) Added I_{AVCC} spec. into. 2) Modified OVP description. 4) Added power on/off sequence into. 3) Updated R_{AVCC} formula in application circuit. |

Important Notice

All rights reserved.

No part of this document may be reproduced or duplicated in any form or by any means without the prior permission of ESMT.

The contents contained in this document are believed to be accurate at the time of publication. ESMT assumes no responsibility for any error in this document, and reserves the right to change the products or specification in this document without notice.

The information contained herein is presented only as a guide or examples for the application of our products. No responsibility is assumed by ESMT for any infringement of patents, copyrights, or other intellectual property rights of third parties which may result from its use. No license, either express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of ESMT or others.

Any semiconductor devices may have inherently a certain rate of failure. To minimize risks associated with customer's application, adequate design and operating safeguards against injury, damage, or loss from such failure, should be provided by the customer when making application designs.

ESMT's products are not authorized for use in critical applications such as, but not limited to, life support devices or system, where failure or abnormal operation may directly affect human lives or cause physical injury or property damage. If products described here are to be used for such kinds of application, purchaser must do its own quality assurance testing appropriate to such applications.