15W Mono Class-D Audio Amplifier

Features

- Single supply voltage
  4.5V ~ 14.4V for loudspeaker driver
  Built-in LDO output 5.0V for others
- Loudspeaker power from 12V supply
  8W/CH into 8Ω @1% THD+N
  12W/CH into 4Ω @<1% THD+N
  15W/CH into 4Ω @10% THD+N
- 93% efficient Class-D operation eliminates need for heat sink
- Differential inputs
- Internal oscillator
- Short-Circuit protection with auto recovery option
- Under-Voltage detection
- Over-Voltage protection
- Pop noise and click noise reduction
- Output DC detection for speaker protection
- Filter-Free operation
- Over temperature protection with auto recovery
- Superior EMC performance

Applications

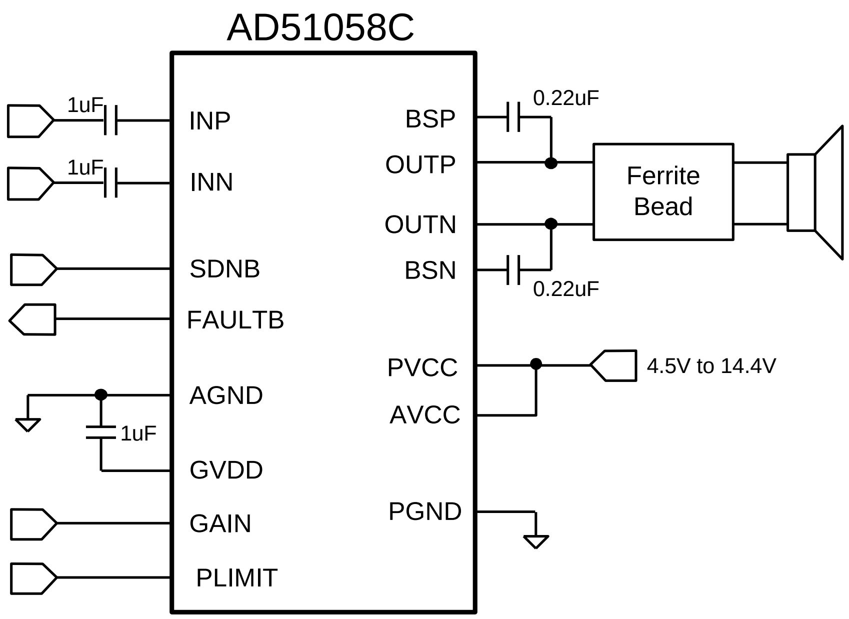
- TV audio
- Boom-Box
- Powered speaker
- Monitors
- Consumer Audio Equipment

Description

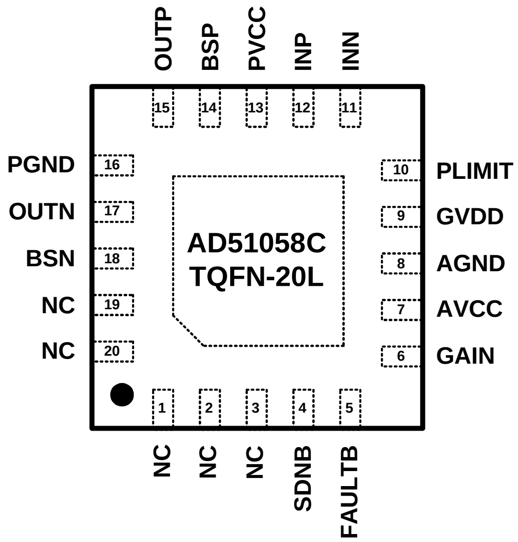
The AD51058C is a high efficiency mono class-D audio amplifier. The loudspeaker driver operates from 4.5V~14.4V supply voltage, it can deliver 15W output power into 4Ω loudspeaker within 10% THD+N at 12V supply voltage and without external heat sink when playing music.

Output DC detection prevents speaker damage from long-time current stress.AD51058C provides superior EMC performance for filter-free application. The output short circuit and over temperature protection include auto-recovery feature.

Simplified Application Circuit



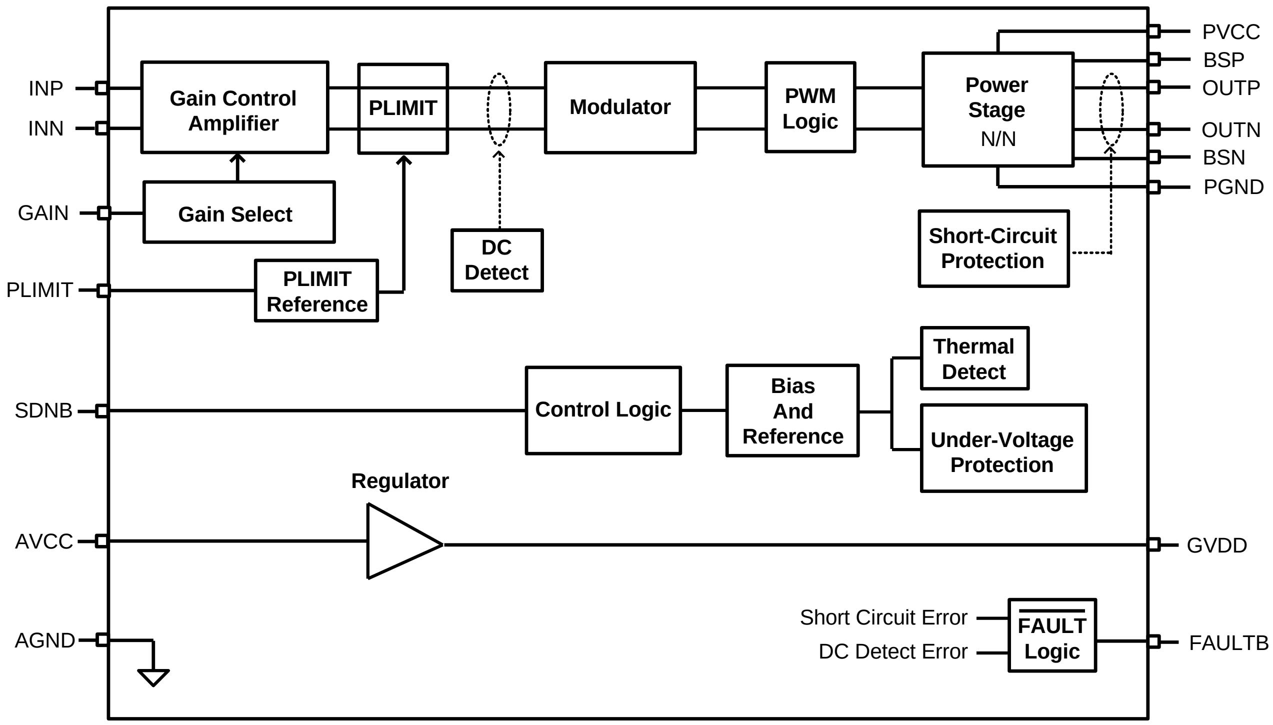
Pin Assignments



Pin Description

NAME	TQFN-20L	TYP	DESCRIPTION
N.C.	1,2,3	N/A	Not connected pin.
SDNB	4	I	Shutdown signal for IC (low = disabled, high = operational). Voltage compliance to AVCC, internal pull Low with a 227Kohm resistor.
FAULTB	5	O	Open drain output used to display short circuit or dc detect fault. Voltage compliant to AVCC. Short circuit faults can be set to auto-recovery by connectingFAULTBpin to SDNB pin. Otherwise, both short circuit faults and dc detect faults must be reset by cycling AVCC.
GAIN	6	I	Gain select least significant bit. Voltage compliance to AVCC.
AVCC	7	P	Analog supply.
AGND	8	P	Analog signal ground.
GVDD	9	P	5.0V regulated output.
PLIMIT	10	I	Power limit level adjustment. Connect a resistor divider from GVDD to GND to set power limit. Give V_{PLIMIT}0.3~2.7V to set power limit level. Connect to GVDD (>3V) or GND (<0.26V) to disable power limit function.
INN	11	I	Negative audio input.
INP	12	I	Positive audio input.
PVCC	13	P	High-voltage power supply.
BSP	14	P	Bootstrap I/O, positive high side FET.
OUTP	15	O	Class-D H-bridge positive output.
PGND	16	P	Power ground for the H-bridges.
OUTN	17	O	Class-D H-bridge negative output.
BSN	18	P	Bootstrap I/O, negative high side FET.
N.C.	19,20	N/A	Not connected pin.

Functional Block Diagram



Ordering Information

Product ID	Package	Packing / MPQ	Comments
AD51058C-HH20NRR	TQFN-20L (3mm×3mm)	Tape/Reel 5K Units/Reel	Green

Available Package

Package Type	Device No.	θ_{JA}(℃/W)	θ_{JT}(℃/W)	Ψ_{JT}(℃/W)	Exposed Thermal Pad
TQFN 20L	AD51058C	42.3	26.2	1.3	Yes (Note 1)

Note 1.1: ***The thermal pad is located at the bottom of the package. To optimize thermal performance, soldering the thermal pad to the PCB's ground plane is necessary.***

Note 1.2: ***θ_{JA} is simulatedon a room temperature (T_A=25℃), natural convection environment test board, which is constructed with a thermally efficient, 4-layers PCB (2S2P). The measurement is simulated using the JEDEC51-7 thermal measurement standard.***

Note 1.3: ***θ_{JT} represents the thermal resistance for the heat flow between the chip junction and the package's top surface. It's extracted from the simulation data with obtaining a cold plate on the package top.***

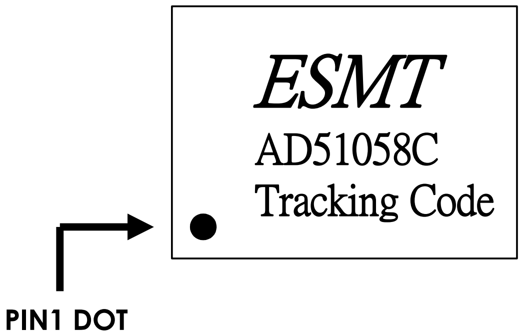
Note 1.4: ***Ψ_{JT}represents the thermal parameterfor the heat flow between the chip junction and the package's top surface center. It's extracted from the simulation data for obtainingθ_{JA}, using a procedure described in JESD51-7.***

Marking Information

AD51058C

- Marking Information

Line 1：LOGO
Line 2：Product No
Line 3：Tracking Code



Absolute Maximum Ratings

Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
PVCC	Supply voltage	PVCC, AVCC	-0.3	16	V
V_I	Interface pin voltage	SDNB, FAULTB	-0.3	16	V
T_A	Operating free-air temperature range		-40	85	^oC
T_J	Operating junction temperature range		-40	150	^oC
T_{stg}	Storage temperature range		-65	150	^oC
R_L	Minimum Load Resistance		3.2		Ω
ESD	Human Body Model			±2k	V
	ChargedDevice Model			±500	V

Recommended Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
PVCC	Supply voltage	PVCC, AVCC	4.5	14.4	V
V_I	Signal inputlevel voltage	INP, INN		2	Vrms
V_{IH}	High-level input voltage	SDNB	2		V
V_{IL}	Low-level input voltage	SDNB		0.8	V
V_{OL}	Low-level output voltage	FAULTB, $R_{PULL-UP}$=100k, PVCC=12V		0.8	V
I_{IH}	High-level input current	SDNB, VI=2V, PVCC=12V		50	uA
I_{IL}	Low-level input current	SDNB, V_I=0.8V, PVCC=12V		5	uA
T_A	Operating free-air		-40	85	^oC

General Electrical Characteristics

- PVCC=12V, R_L=4Ω, T_A=25°C (unless otherwise noted)

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
$I_{CC(q)}$	Quiescent supply current	SDNB=2V, no load, PVCC=12V		8	12	mA
$I_{CC(SD)}$	Quiescent supply current in shutdown mode	SDNB=0.8V, no load, PVCC=12V		<12	25	uA
$R_{DS(on)}$	Drain-source on-state resistance-High side NMOS	PVCC=12V, Id=500mA, T_J=25 °C		190		mΩ
	Drain-source on-state resistance-Low side NMOS			190		mΩ
$\|V_{OS}\|$	Class-D output offset voltage (measured differential)	PVCC=12V V_I=0V, Gain=26dB		1.5	10	mV
t_{ON}	Turn-on time	SDNB=2V		8		mS
t_{OFF}	Turn-off time	SDNB=0.8V		2		uS
GVDD	Regulator output	I_{GVDD}=0.1mA	4.75	5	5.25	V
G	Gain	GAIN=0.8V	25	26	27	dB
		GAIN=2V	35	36	37	

Electrical Characteristics and Specifications of Loudspeaker Driver

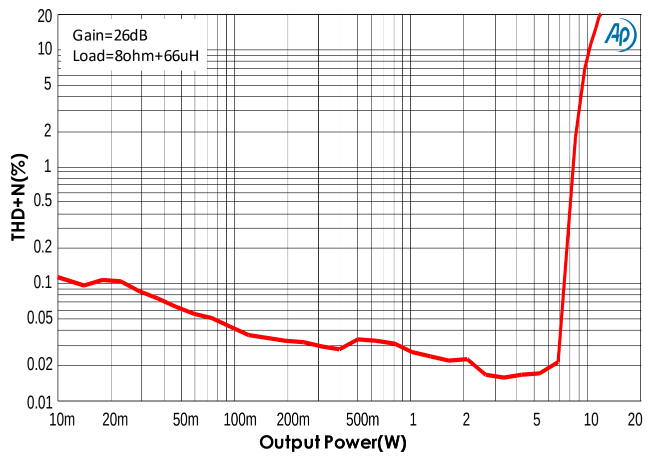
- PVCC=12V, R_L=4Ω, T_A=25°C (unless otherwise noted)

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
P_O	Output power	THD+N=10%, f=1kHz, 8Ω		10		W
		THD+N=10%, f=1kHz, 6Ω		14		
		THD+N<10%, f=1kHz, 4Ω		15		
THD+N	Total harmonic distortion plus noise	PVCC=12V, R_L=8Ω, f=1kHz, P_O=5W (half-power)		<0.02		%
		PVCC=12V, R_L=6Ω, f=1kHz, P_O=7W (half-power)		<0.02		
		PVCC=12V, R_L=4Ω, f=1kHz, P_O=7.5W (half-power)		<0.02		
SNR	Signal to noise ratio	Maximum output at THD+N<1%, f=1kHz, Gain=26dB, a-weighted		94		dB
V_n	Output integrated noise	F=20Hz ~ 20kHz, Gain=26dB, a-weighted filter, R_L=8Ω		100		uV
K_{SVR}	Power Supply Rejection Ratio	V_{ripple}=200mVpp at 1kHz, Gain=26dB, inputs ac-grounded		-70		dB
f_{OSC}	Oscillator frequency		250	310	370	kHz
T_{SENSOR}	Thermal trip point			160		°C
	Thermal hysteresis			25		°C

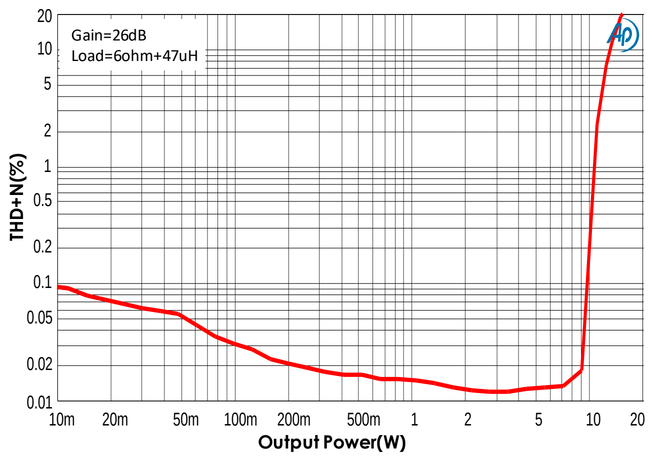
Typical Characteristics

- PVCC=12V, R_L=4Ω, T_A=25°C (unless otherwise noted)

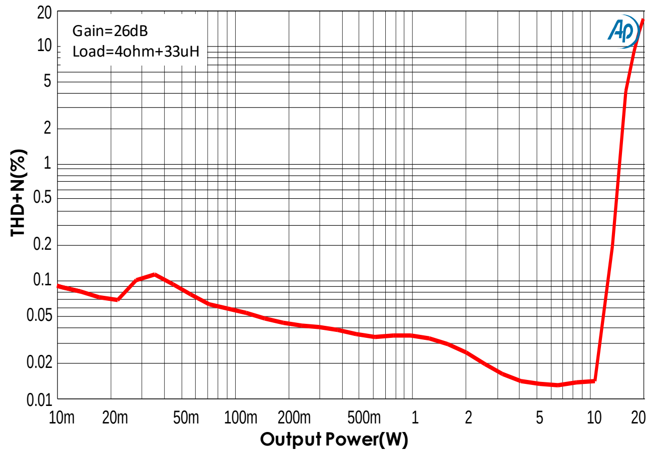
THD+N vs. Output Power,8Ω load



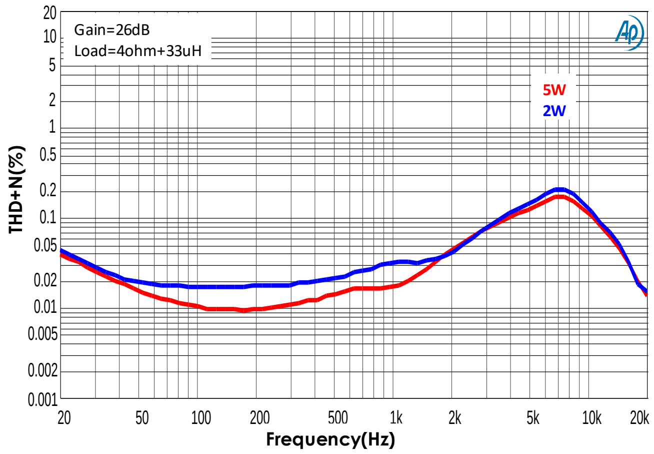
THD+N vs. Output Power,6Ω load



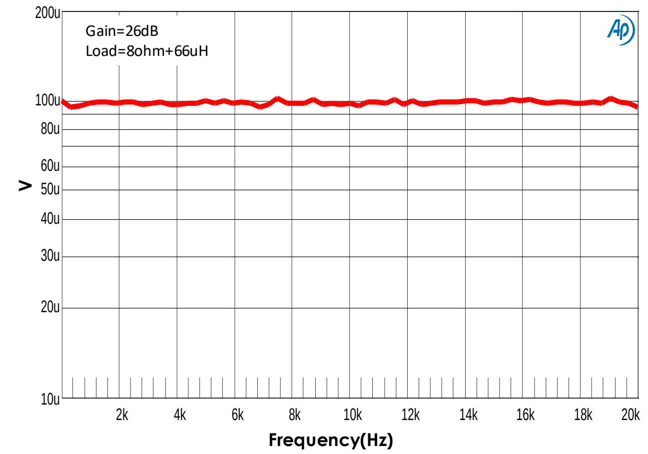
THD+N vs. Output Power,4Ω load



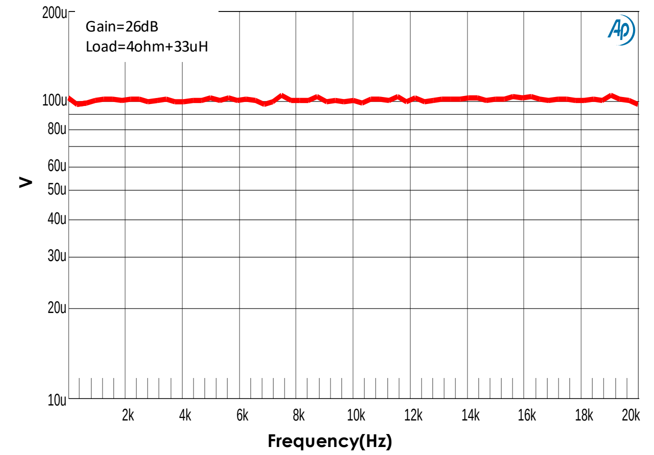
THD + N (%) vs. Frequency, 4Ω load

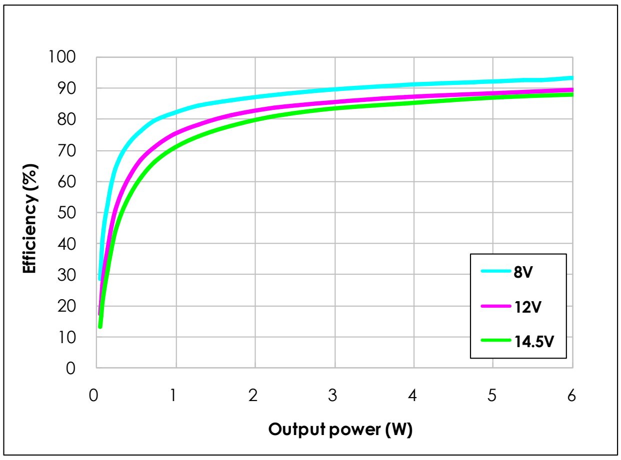
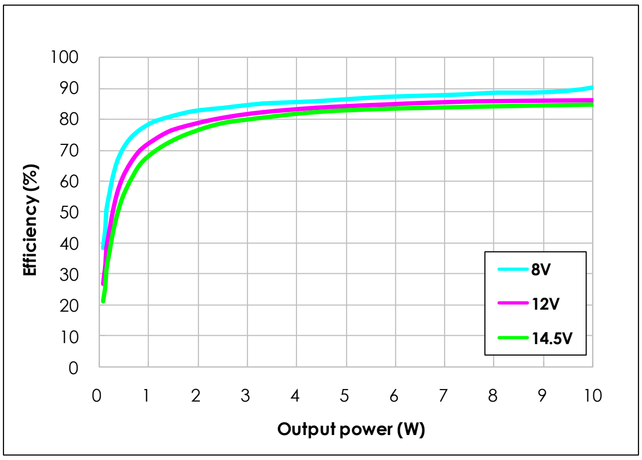
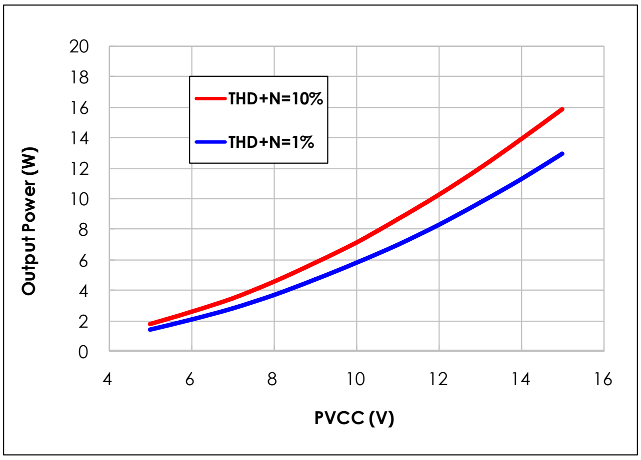
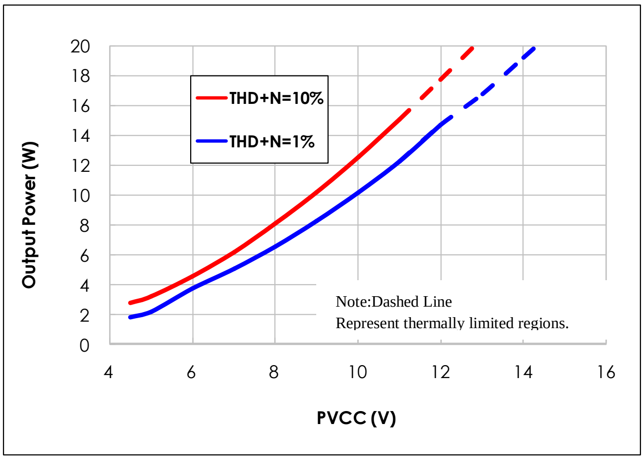


Noise, 8Ω load



Noise, 4Ω load



Efficiency (8Ω load)	Efficiency (4Ω load)
	
Supply voltage vs. Output Power, 8Ω load	**Supply voltage vs. Output Power, 4Ω load**
	

Operation Descriptions

●Gain settings

The gain of the AD51058C is set by input pins, GAIN. By varying input resistance in AD51058C, the various volume gains are achieved. The respective volume gain and input resistance are listed in Table 1. However, there is 20% variation in input resistance from production variation.

Table 1. Volume gain and input impedance

GAIN	Volume Gain (dB)	Input Resistance, R_{in} (kΩ)
0	26	30
1	36	9

● Shutdown control

Pulling SDNB pin low will let AD51058C operate in low-current state for power conservation. The AD51058C outputs will enter mute once SDNB pin is pulled low, and regulator will also disable to save power. If let SDNB pin floating, the chip will enter shutdown mode because of the internal pull low resistor. For the best power-off performance, place the chip in the shutdown mode in advance of removing the power supply.

● DC detection

AD51058C has dc detection circuit to protect the speakers from DC current which might be occurred as input capacitor defect or inputs short on printed circuit board. The detection circuit detects first volume amplifier stage output, when both differential outputs' voltage become higher than a determined voltage or lower than a determined voltage for more than 420ms, the dc detect error will occur and report to FAULTB pin. At the same time, loudspeaker drivers will disable and enter Hi-Z. This fault can not be cleared by cycling SDNB pin, it is necessary to cycle the PVCC supply.

The minimum differential input voltages required to trigger the DC detect function are shown in table1. The input voltage must keep above the voltage listed in the table for more than 340msec to trigger the DC detect fault. The equivalent class-D output duty of the DC detect threshold is listed in table2.

Table 1. DC Detect Threshold

AV (dB)	Vin (mV, differential)
26	125

Table 2. Output DC Detect Duty (for Either Channel)

PVCC (V)	Output Duty Exceeds
8	20.8%
12	20.8%

- **Thermal protection**

  If the internal junction temperature is higher than 160^{o}C, the outputs of loudspeaker drivers will be disabled and at low state. The temperature for AD51058Creturning to normal operation is about 135^{o}C. The variation of protected temperature is about 10%. Thermal protection faults are NOT reported on the FAULTB pin.

- **Short-circuit protection**

  To protect loudspeaker drivers from over-current damage, AD51058Chas built-in short-circuit protection circuit. When the wires connected to loudspeakers are shorted to each other or shorted to VSS or to PVCC, overload detectors may activate. Once one of right and left channel overload detectors are active, the amplifier outputs will enter a Hi-Z state and the protection latch is engaged. The short protection fault is reported on FAULTB pin as a low state. The latch can be cleared by reset via SDNBpin or power supply cycling.

  The short circuit protection latch can have auto-recovery function by connect the FAULTB pin directly to SDNB pin. The latch state will be released after 340msec, and the short protection latch will re-cycle if output overload is detected again.

- **Under-voltage detection**

  When the GVDD voltage is lower than 2.8V or the PVCC voltage is lower than 4V, loudspeaker drivers of right/left channel will be disabled and kept at low state. Otherwise, AD51058C return to normal operation.

- **Over-voltage protection**

  When the PVCC voltage is higher than 15.5V, loudspeaker will be disabled kept at low state. The protection status will be released as PVCC lower than 15V.

- **Power limit function**

  - The voltage at PLIMIT pin can used to limit the power of first gain control amplifier output. Add a resistor divider from GVDD to ground to set the voltage V_{PLIMIT} at the PLIMIT pin. The voltage V_{PLIMIT} sets a limit on the output peak-to-peak voltage.PLIMIT is adjustable from 0.3V~2.7V.

For normal operation:

$$Po@1\%THD = \frac{\left(V_P \times \left(\frac{R_L}{R_L + 2R_S}\right)\right)^2}{2R_L}$$

$$Po@10\%THD = 1.333 \times Po@1\%THD$$

Where:

R_S is the total series resistance including $R_{DS(on)}$, and any resistance in the output filter.
R_L is the load resistance.
V_P is the peak amplitude of the output, $V_P = 5.0666 \times V_{PLIMIT}$.

Connect PLIMIT pin to ground (<0.26V) or GVDD (>3V) to disable power limit function. The output variation during power limit feature enable may have +-20% variation due to process window.

Table 3. PLIMIT Typical Operation Ⅰ

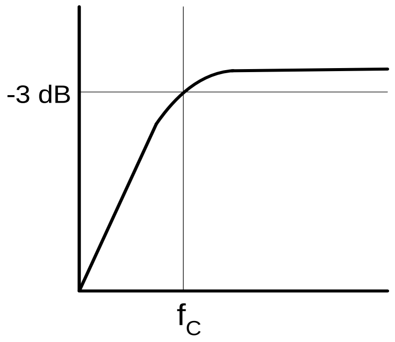
Test Conditions	Output P_O (W)	V_{PLIMIT} (V) @ THD+N=10%
PVCC=12V RL=8Ω	3	1.24
	5	1.60
	8	2.02
	9	2.15

Application information

- **Input capacitors (C_{in})**

The performance at low frequency (bass) is affected by the corner frequency (f_c) of the high-pass filter composed of input resistor (R_{in}) and input capacitor (C_{in}), determined in equation (2). Typically, a 0.1μF or 1μF ceramic capacitor is suggested for C_{in}. The resistance of input resistors is 30kΩat gain +26dB setting in AD51058C. However, there is 20% variation in input resistance from production variation.

$$f_c = \frac{1}{2\pi R_{in} C_{in}} \ (\mathrm{Hz}) \quad \cdots\cdots\cdots (2)$$



- **Ferrite Bead selection**

If the traces from theAD51058C to speaker are short, the ferrite bead filters can reduce the high frequency emissions to meet FCC requirements. A ferrite bead that has very low impedance at low frequency and high impedance at high frequency (above 1MHz) is recommended. The impedance of the ferrite bead can be used along with a small capacitor with a value around 1000pF to reduce the frequency spectrum of the signal to an acceptable level.

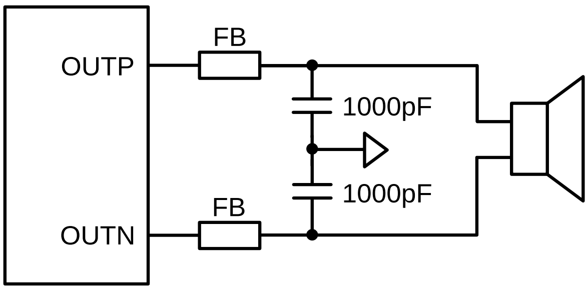


Figure 2. Typical Ferrite Bead Filter

- **Output LC Filter**

If the traces from theAD51058C to speaker are not short, it is recommended to add the output LC filter to eliminate the high frequency emissions. Figure 3 shows the typical output filter for 8Ω speaker with a cut-off frequency of 27 kHz and Figure 4 shows the typical output filter for 4Ω speaker with a cut-off frequency of 27 kHz.

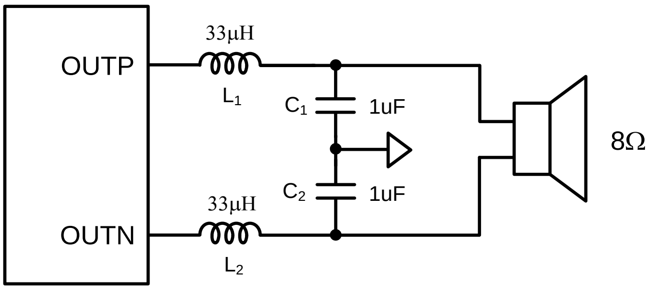


Figure 3. Typical LC Output Filter for 8Ω Speaker

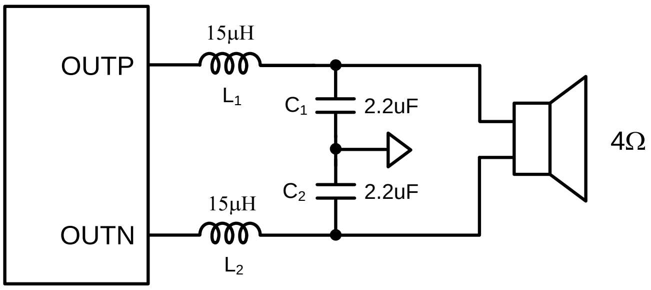


Figure 4. Typical LC Output Filter for 4Ω Speaker

- **Power supply decoupling capacitor (Cs)**

Because of the power loss on the trace between the device and decoupling capacitor, the decoupling capacitor should be placed close to PVCC and PGND to reduce any parasitic resistor or inductor. A low ESR ceramic capacitor, typically 1000pF, is suggested for high frequency noise rejection. For mid-frequency noise filtering, place a capacitor typically 0.1μF or 1μF as close as possible to the device PVCC leads works best. For low frequency noise filtering, a 100μF or greater capacitor (tantalum or electrolytic type) is suggested.

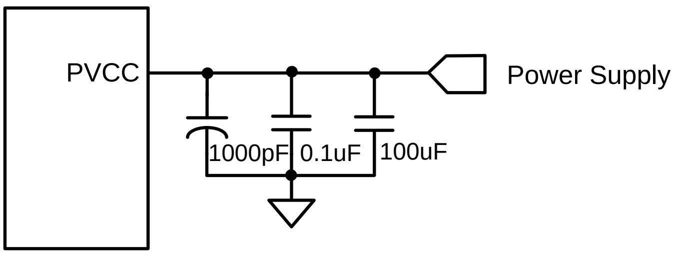
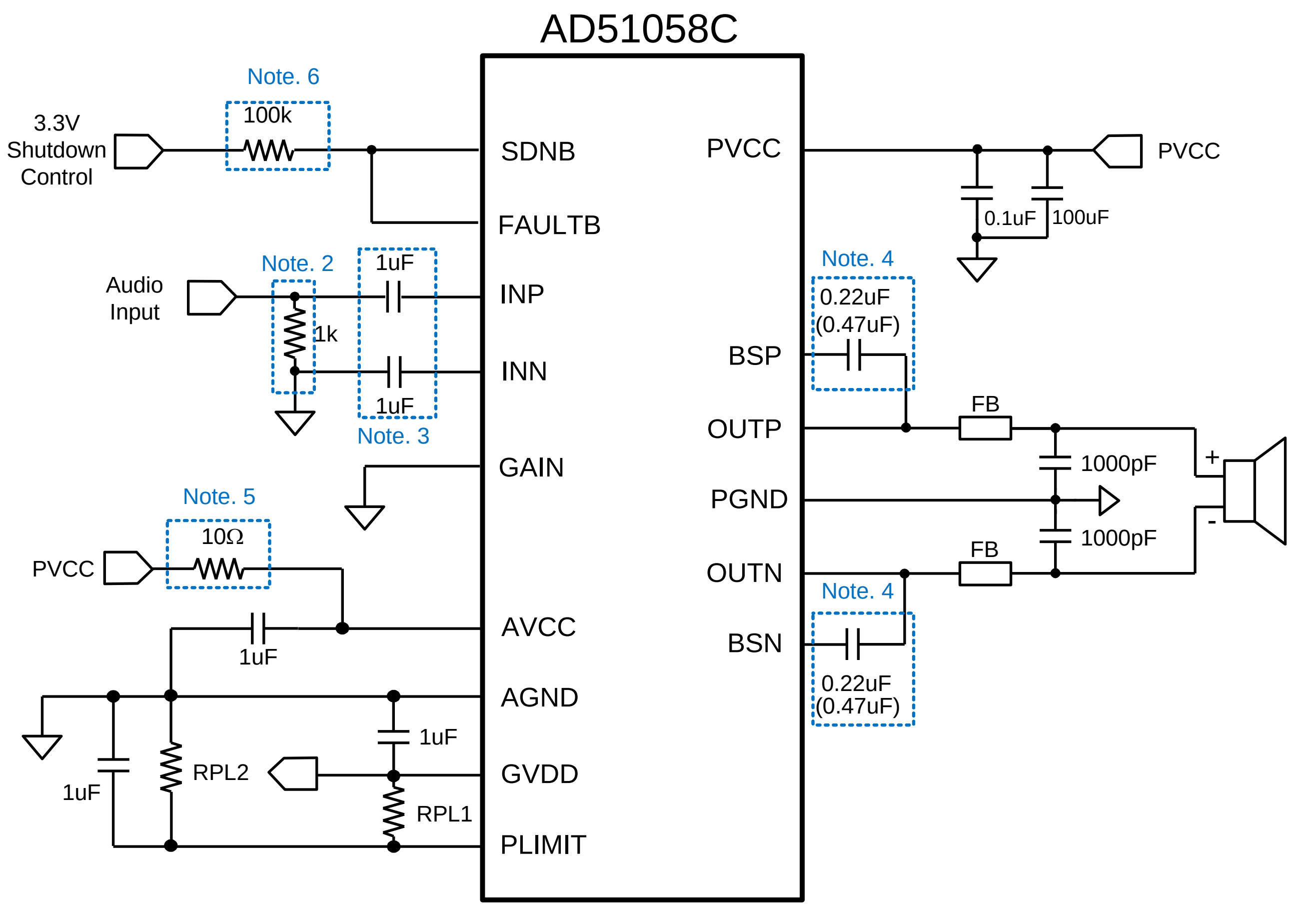


Figure 5. Recommended Power Supply Decoupling Capacitors.

Application Circuit Example

- Application circuit with Single-Ended Input



Note 2: These resistances must be connected to ground, resistance=1Kohm.

Note 3: The faster turn-on time 8ms is designed for AD51058C, the pop sound shall be take care with the input resistor (Rin) added into for input signal attenuation requirement. The longer shutdown release time is necessary if the input resistor (Rin) is adopted.

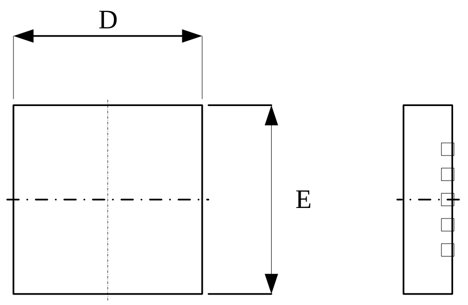
Note 4: These capacitors should be change to 0.47uF, while the PVCC<=5V.

Note 5: The under-voltage threshold for AVCC could be adjusted by RAVCC.

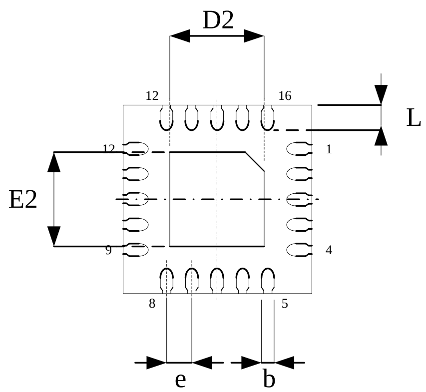
Note 6: The $R_{Shutdown}$ shall be adjusted depend on "Shutdown Control" voltage, the formula will be followed $R_{Shutdown} \leq \frac{(V_{Shutdown} - 2V) \times 210k}{2V} (\Omega)$ ***, $R_{Shutdown}$ ≧16.5kohm minimum is requirement in AD51058C.***

Package Dimensions

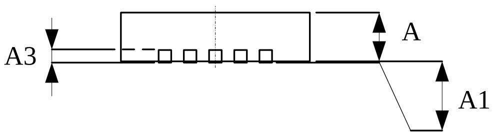
- **TQFN-20L (3x3 mm)**



TOP VIEW



BOTTOM VIEW



SIDE VIEW

Symbol	Dimension in mm	
	Min	Max
A	0.70	0.85
A1	0.00	0.05
A3	0.203 REF.	
b	0.15	0.25
D	2.90	3.10
E	2.90	3.10
e	0.40 BSC	
L	0.30	0.50

Exposed pad

	Dimension in mm	
	Min	Max
D2	1.55	1.75
E2	1.55	1.75

Revision History

Revision	Date	Description
0.1	2023.09.04	Initial version.

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