

GENERAL DESCRIPTION

The high-speed, dual-channel low-side driver SGM48522 is designed to drive GaN FETs and logic level MOSFETs. The application areas include LiDAR, time of flight, facial recognition, and power converters using low-side drivers. The SGM48522 provides 7A source and 6A sink output current capability. Split output configuration allows individual turn-on and turn-off time optimization depending on FET. The Flip-Chip TQFN package and pinout minimize parasitic inductances to reduce the rise and fall time and limit the ringing. Additionally, the 2ns propagation delay with minimized tolerances and variations allows efficient operation at high frequencies.

The driver has internal under-voltage lockout and over-temperature protection against overload and fault events.

The SGM48522 is available in a Green TQFN-2x2-10BL package.

FEATURES

- **5V Supply Voltage**
- **7A Peak Source and 6A Peak Sink Currents**
- **Ultra-Fast, Low-side Gate Driver for GaN and Si FETs**
- **Minimum Input Pulse Width: 1ns**
- **Up to 60MHz Operation**
- **Propagation Delay: 2ns (TYP)**
- **Rise Time: 750ps (TYP)**
- **Fall Time: 560ps (TYP)**
- **Protection Features:**
 - ◆ **Under-Voltage Lockout (UVLO)**
 - ◆ **Over-Temperature Protection (OTP)**
- **Available in a Green TQFN-2x2-10BL Package**

APPLICATIONS

- Laser Distance Measuring System (LiDAR)
- 5G RF Communication System
- Wireless Charging System
- GaN DC/DC Conversion System

TYPICAL APPLICATION

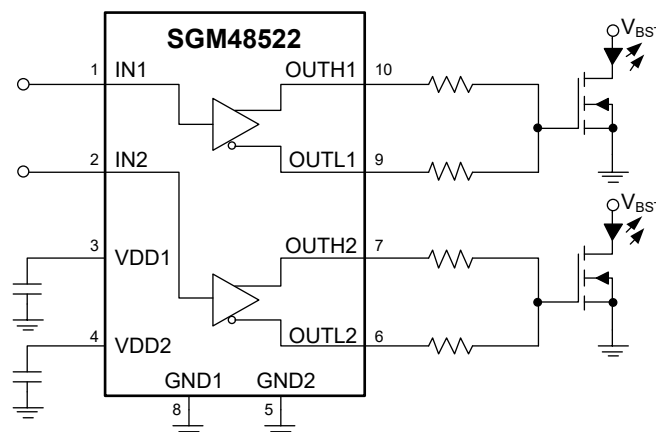


Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

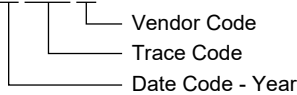
MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM48522	TQFN-2x2-10BL	-40°C to +125°C	SGM48522XTSW10G/TR	061 XXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXX = Date Code, Trace Code and Vendor Code.

YYY— Serial Number

XXXX



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD1} , V_{DD2}	-0.3V to 6V
IN1, IN2 Pin Voltage, V_{INX}	-0.3V to 6V
OUTH1, OUTH2 Pin Voltage, V_{OUTHX}	-0.3V to $V_{DD} + 0.3V$
OUTL1, OUTL2 Pin Voltage, V_{OUTLX}	
DC	-0.3V to 6V
Repetitive Pulse < 5ns	-2V to 7V
Package Thermal Resistance	
TQFN-2x2-10BL, θ_{JA}	81.8°C/W
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10s)	+260°C
ESD Susceptibility	
HBM	4000V
CDM	1500V

RECOMMENDED OPERATING CONDITIONS

Supply Voltage, V_{DD1} , V_{DD2}	4.5V to 5.5V
IN1, IN2 Pin Voltage, V_{INX}	0V to 5.5V
Operating Ambient Temperature Range	-40°C to +125°C

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

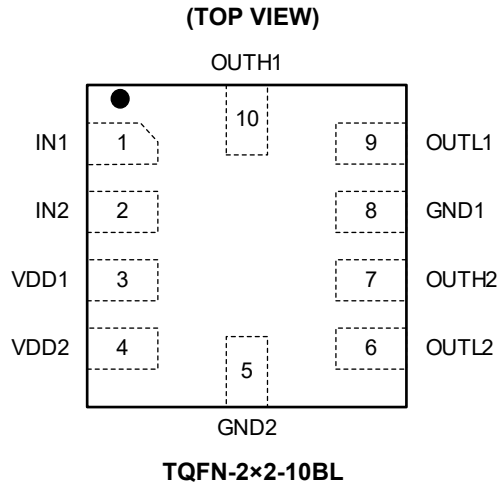
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



PIN DESCRIPTION

PIN	NAME	I/O	FUNCTION
1	IN1	I	Channel 1 Control Logic Input (Non-Inverting).
2	IN2	I	Channel 2 Control Logic Input (Non-Inverting).
3	VDD1	I	Channel 1 Input Voltage Supply. Bypass to GND with a low inductance ceramic capacitor.
4	VDD2	I	Channel 2 Input Voltage Supply. Bypass to GND with a low inductance ceramic capacitor.
5	GND2	—	Channel 2 Ground. Internally connected to GND1 by anti-parallel diodes.
6	OUTL2	O	Channel 2 Pull-Down Gate Drive Output. Connect it to the gate of the target transistor with an optional resistor.
7	OUTH2	O	Channel 2 Pull-Up Gate Drive Output. Connect it to the gate of the target transistor with an optional resistor. Internally connected to GND2 by anti-parallel diodes.
8	GND1	—	Channel 1 Ground.
9	OUTL1	O	Channel 1 Pull-Down Gate Drive Output. Connect it to the gate of the target transistor with an optional resistor.
10	OUTH1	O	Channel 1 Pull-Up Gate Drive Output. Connect it to the gate of the target transistor with an optional resistor.

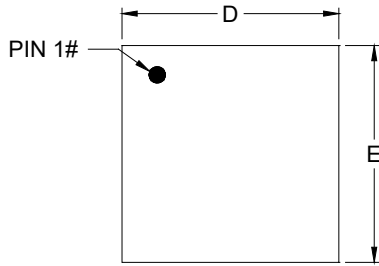
NOTE: I = input, O = output.

FUNCTION TABLE

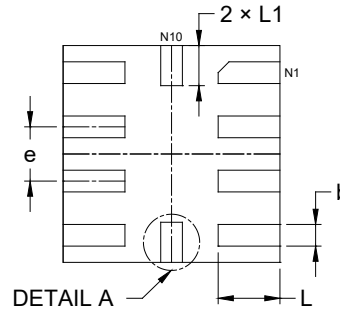
INx Pin	OUTHx Pin	OUTLx Pin
L	Open	L
H	H	Open

PACKAGE OUTLINE DIMENSIONS

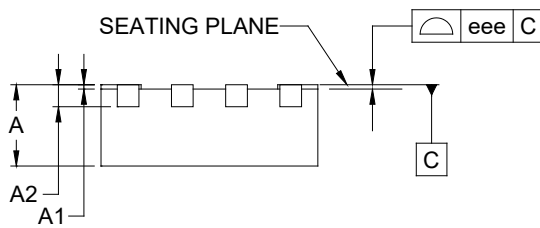
TQFN-2x2-10BL



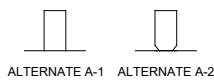
TOP VIEW



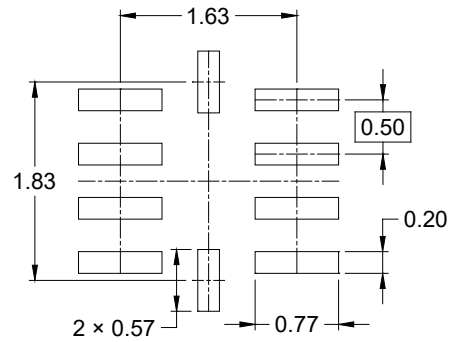
BOTTOM VIEW



SIDE VIEW



DETAIL A
ALTERNATE TERMINAL
CONSTRUCTION



RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions in Millimeters		
	MIN	MOD	MAX
A	0.700	-	0.800
A1	0.000	-	0.050
A2	0.203 REF		
b	0.150	-	0.250
D	1.900	-	2.100
E	1.900	-	2.100
e	0.500 BSC		
L	0.470	-	0.670
L1	0.270	-	0.470
eee	0.080		

NOTE: This drawing is subject to change without notice.

PACKAGE INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-2×2-10BL	7"	9.5	2.30	2.30	1.10	4.0	4.0	2.0	8.0	Q1

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PACKAGE INFORMATION

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7" (Option)	368	227	224	8
7"	442	410	224	18

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