SGM48534A/SGM48534B SGM48535A/SGM48535B Low-Side Gate Drivers with Fast Response Over-Current Protection

GENERAL DESCRIPTION

The SGM48534A, SGM48534B, SGM48535A, and SGM48535B are single-channel low-side power transistor gate drivers. Inputs are compatible with standard CMOS or LSTTL signals. The output is capable of delivering 2.6A sink and 4.2A source peak currents. The SGM4853XA/B have over-current protection functions. The OCP pin detects the over-current signal, and the EN/nFLT pin outputs the over-current status. Once the over-current protection is triggered, the fault pin is pulled down internally and outputs a low level. The EN/nFLT pin requires an external pull-up circuit to ensure the normal operation of the driver. The EN/nFLT pin can also be used as an enable pin for the driver. Pulling the EN/nFLT pin low can disable the driver. The driver has under-voltage protection function, and the output remains low when the V_{CC} voltage is lower than the operating voltage.

The SGM4853XA/B are all available in a Green SOT-23-6 package.

FEATURES

- **Over-Current Detection Threshold:**
  SGM4853XA: -0.25V Negative Voltage with ±6% Detection Accuracy
  SGM4853XB: +0.5V Positive Voltage with ±6% Detection Accuracy
- **Independent Fault Output and Enable Control Pin**
- **Programmable Fault Clearing Time and Over-Current Detection Response Time**
- **The Input Has CMOS Schmitt Trigger Circuit to Enhance Noise Immunity**
- **Inputs are Compatible with Standard CMOS or LSTTL Signals**
- **OCP Pin Withstands -10V DC Voltage**
- **Under-Voltage Lockout (UVLO)**
- **Available in a Green SOT-23-6 Package**

APPLICATIONS

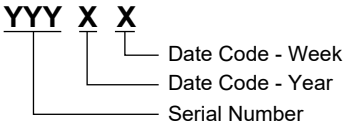
Switched-Mode Power Supplies
DC/DC Converters
Solar Inverters, Motor Control, UPS
Companion Gate-Driver Devices for Digital-Power Controllers
Renewable Energy Power Conversion

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM48534A	SOT-23-6	-40℃ to +125℃	SGM48534AXN6G/TR	002XX	Tape and Reel, 3000
SGM48534B	SOT-23-6	-40℃ to +125℃	SGM48534BXN6G/TR	003XX	Tape and Reel, 3000
SGM48535A	SOT-23-6	-40℃ to +125℃	SGM48535AXN6G/TR	000XX	Tape and Reel, 3000
SGM48535B	SOT-23-6	-40℃ to +125℃	SGM48535BXN6G/TR	001XX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XX = Date Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Fixed Supply Voltage, V_{CC} ..... -0.3V to 25V
Output Voltage (OUT), V_O .....-0.3V to V_{CC} + 0.3V
Voltage at Current Sense Pin (OCP), V_{OCP}
.....-10V to V_{CC} + 0.3V
Voltage at Enable and Fault Report Pin (EN/nFLT), $V_{EN/nFLT}$
.....-0.3V to V_{CC} + 0.3V
Logic Input Voltage (IN), V_{IN} .....-10V to V_{CC} + 0.3V
Power Dissipation, P_D @ T_A ≤ +25℃
SOT-23-6 .....0.88W
Package Thermal Resistance
SOT-23-6, θ_{JA} ..... 141℃/W
Junction Temperature.....+150℃
Storage Temperature Range .....-65℃ to +150℃
Lead Temperature (Soldering, 10s).....+260℃
ESD Susceptibility
HBM.....4000V
CDM 2000V

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

RECOMMENDED OPERATING CONDITIONS

Fixed Supply Voltage, V_{CC}
SGM48534A/B.....4.5V to 20V
SGM48535A/B..... 12.7V to 20V
Output Voltage, V_{OUT} .....COM to V_{CC}
Voltage at Current Sense Pin (OCP), V_{OCP} ..... -5V to V_{CC}
Voltage at Enable and Fault Report Pin (EN/nFLT), $V_{EN/nFLT}$
.....COM to V_{CC}
Logic Input Voltage (IN), V_{IN} ..... -5V to V_{CC}
Operating Ambient Temperature Range ..... -40℃ to +125℃

ESD SENSITIVITY CAUTION

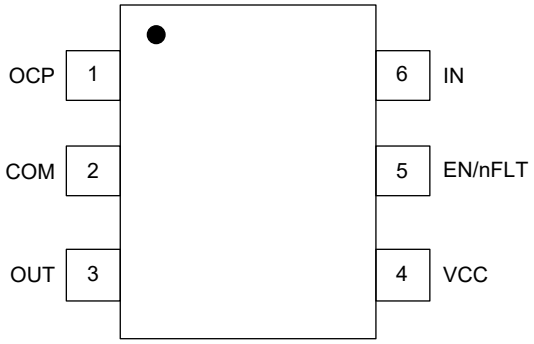
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

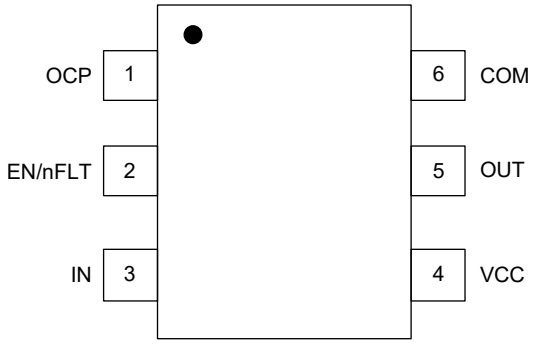
PIN CONFIGURATION

SGM48534A/SGM48535A (TOP VIEW)



SOT-23-6

SGM48534B/SGM48535B (TOP VIEW)



SOT-23-6

PIN DESCRIPTION

PIN		NAME	I/O	FUNCTION
SGM4853XA	SGM4853xB			
1	1	OCP	I	Current Sampling Signal Input.
2	6	COM	G	Ground. All signals Referenced to this pin.
3	5	OUT	O	Sourcing/Sinking Current Output of Driver.
4	4	VCC	P	Input Voltage Supply Pin. A 1μF or larger ceramic capacitor must be connected between VCC and COM pins as close to the device as possible.
5	2	EN/nFLT	I/O	Enable Control and Fault Report Pin: 1. Used as an enable pin: turn off the drive output when it is low. 2. Used as a fault report pin: when an over-current or under-voltage lockout event occurs, the pin outputs a low level. The pin needs to configure external pull-up resistor and capacitor. The resistor and capacitor determine the fault clear time.
6	3	IN	I	Non-Inverting Input. OUT pins are held low if IN is unbiased or floating.

NOTE: I: input, O: output, I/O: input or output, G: ground, P: power for the circuit.

INPUT/OUTPUT LOGIC TRUTH TABLE

IN	UVLO (1)	OCP (2)	EN/nFLT (3)	OUT	NOTE
L	H	L	H	L	OUT = L
H	H	L	H	H	OUT = H
X	L	X	L	L	OUT = L, EN/nFLT= L. UVLO protection will keep the output and EN/nFLT low until the fault is cleared.
X	H	H	L	L	OUT = L, EN/nFLT= L. OCP will keep the output and EN/nFLT low until the fault is cleared.
X	H	X	L	L	OUT = L. Pulling EN/nFLT low will turn off the drive output, and the output remains low until the EN/nFLT input returns to logic high.

NOTES:

1. "L" means that the under-voltage protection is triggered.
2. "H" means that over-current protection is triggered.
3. "H" means that the EN/nFLT pin is pulled up and the internal pull-down MOSFET is turned off.

TYPICAL APPLICATIONS

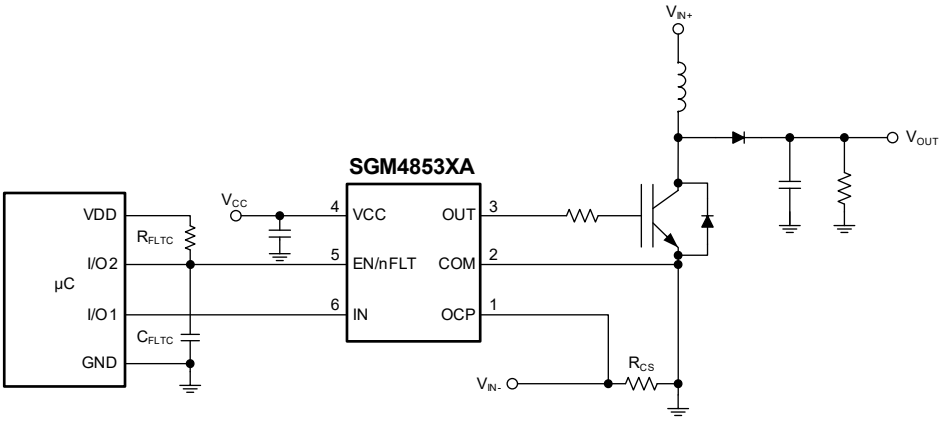


Figure 1. Typical Application Circuit of SGM4853XA

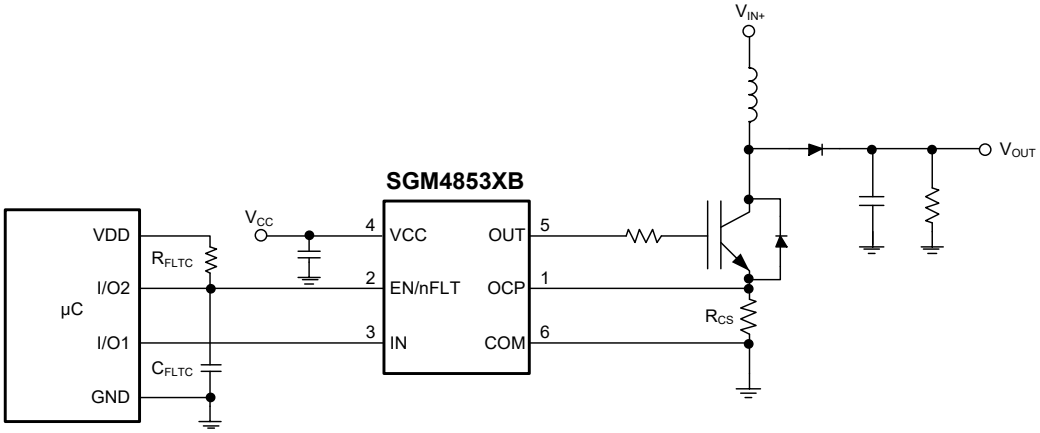


Figure 2. Typical Application Circuit of SGM4853XB

ELECTRICAL CHARACTERISTICS

(V_{CC} = 15V, T_A = +25℃, 1μF capacitor from V_{CC} to GND, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Static Characteristics							
VCC Supply Under-Voltage Positive Going Threshold	V_{CCUV+}	SGM48534A/B		4	4.21	4.38	V
		SGM48535A/B		11.2	12	12.7	
VCC Supply Under-Voltage Negative Going Threshold	V_{CCUV-}	SGM48534A/B			4.1		V
		SGM48535A/B		10.2	11	11.8	
VCC Supply Under-Voltage Lockout Hysteresis	V_{CCUVH}	SGM48534A/B			0.11	0.18	V
		SGM48535A/B			1.0		
Logic “0” Input Voltage (OUT = LO)	V_{INL}	T_A = -40℃ to +125℃		0.8	1.0	1.8	V
Logic “1” Input Voltage (OUT = HI)	V_{INH}	T_A = -40℃ to +125℃		1.9	2.1	3	V
Logic “0” Disable Voltage	V_{ENL}	T_A = -40℃ to +125℃		0.8	1.0	1.2	V
Logic “1” Enable Voltage	V_{ENH}	T_A = -40℃ to +125℃		1.8	2.1	2.4	V
High Level Output Voltage, V_{CC} - V_{OUT}	V_{OH}	I_{OUT} = 2mA			0.02	0.1	V
Low Level Output Voltage, V_{OUT}	V_{OL}	I_{OUT} = 2mA			0.02	0.1	V
Current Limit Threshold Voltage	V_{OCTH}	SGM4853XA		-265	-250	-235	mV
		SGM4853XB		+480	+500	+528	
IN Pin Logic “1” Input Bias Current	I_{IN+}	V_{IN} = 5V		35	55	70	μA
IN Pin Logic “0” Input Bias Current	I_{IN-}	V_{IN} = 0V		-1	-0.5		μA
Quiescent VCC Supply Current	I_{QCC}	V_{IN} = 0V or 5V			450	680	μA
Output Sourcing Short Circuit Pulsed Current (1)	I_{O+}	V_{OUT} = 0V, t_{PW} ≤ 2μs			4.2		A
Output Sinking Short Circuit Pulsed Current (1)	I_{O-}	V_{OUT} = 15V, t_{PW} ≤ 2μs			2.6		A
EN/nFLT Pull-Down Sinking Current	I_{nFLT}	$V_{EN/nFLT}$ = 0.4V		30			mA
Dynamic Characteristics (C_L = 1000pF)							
Turn-On Propagation Delay	t_{ON}	See Figure 6, V_{IN} pulse = 5V			15	30	ns
Turn-Off Propagation Delay	t_{OFF}	See Figure 6, V_{IN} pulse = 5V			15	30	ns
Turn-On Rise Time (1)	t_R	See Figure 6, V_{IN} pulse = 5V			5		ns
Turn-Off Fall Time (1)	t_F	See Figure 6, V_{IN} pulse = 5V			5		ns
Disable Propagation Delay	t_{DISA}	See Figure 12, V_{EN} pulse = 5V			15	30	ns
Over-Current Protection Propagation Delay	t_{OCPDEL}	R_{EN} = 10kΩ to V_{CC}, V_{OCP} pulse = -0.5V (SGM4853XA) or V_{OCP} pulse = 1V (SGM4853XB)			230	350	ns
OCP to Low Level EN/nFLT Signal Delay	t_{OCPFLT}	R_{EN} = 10kΩ to V_{CC}, V_{OCP} pulse = -0.5V (SGM4853XA) or V_{OCP} pulse = 1V (SGM4853XB)			220	320	ns
FAULT Clear Time	t_{FLTC}	See Figure 9 and Figure 10, V_{DD} = 3.3V, R_{FLTC} = 1MΩ to V_{DD}, C_{FLTC} = 240pF to COM		210	240	265	μs
Over-Current Protection Blanking Time (2)	t_{BLK}	R_{FLT} = 0Ω, C_{FLT} = NC, V_{OCP} pulse = -0.5V (SGM4853XA) or V_{OCP} pulse = 1V (SGM4853XB)			250		ns
VCC Supply UVLO Filter Time (1)	t_{VCCUV}	See Figure 8	SGM4853XA		4		μs
			SGM4853XB		3		

NOTES:
1. Guaranteed by design. Not production tested.
2. Verified by design, not tested in DC test.

FUNCTIONAL BLOCK DIAGRAM

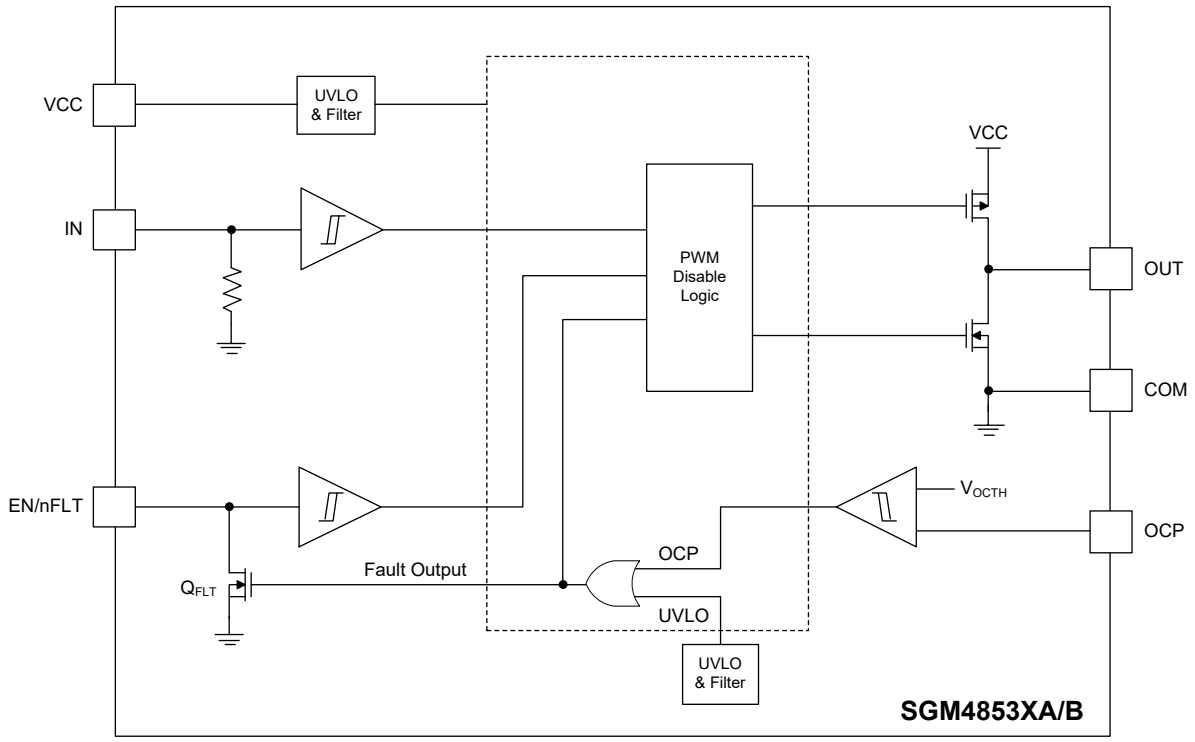


Figure 3. SGM4853XA/B Block Diagram

DETAILED DESCRIPTION

Low-side Single Channel Gate Driver

The SGM4853XA/B drivers are used to drive power transistors, including MOSFETs and IGBTs. Figure 4 is a path diagram of a source current. Figure 5 is a path diagram of a sink current. I_O is defined as the output current of the gate driver. V_{OUT} is defined as the output voltage of the gate driver.

Propagation Delay and Switching Time

Figure 6 shows the relationship between the input signal and output signal of the SGM4853XA/B. It defines the measurement method of time parameters t_{ON}, t_{OFF}, t_R and t_F.

Input Stage

The input pins of the SGM4853XA/B drivers are based on TTL/CMOS compatible input-threshold logic. With 2.1V (TYP) high threshold and 1.0V (TYP) low threshold, the logic-level thresholds can be conveniently driven with PWM control signals derived from 3.3V and 5V digital-power controllers. Wide hysteresis (1.1V, TYP) provides improved noise immunity. The input pin has an internal pull-down resistor to ensure that the drive output is low even if the input is floating. Figure 7 shows the relationship between the input signal threshold and IC logic.

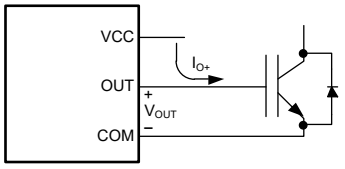


Figure 4. Gate Output Source Current

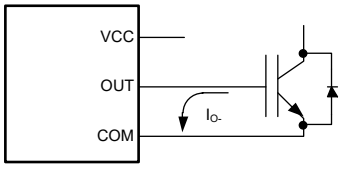


Figure 5. Gate Output Sink Current

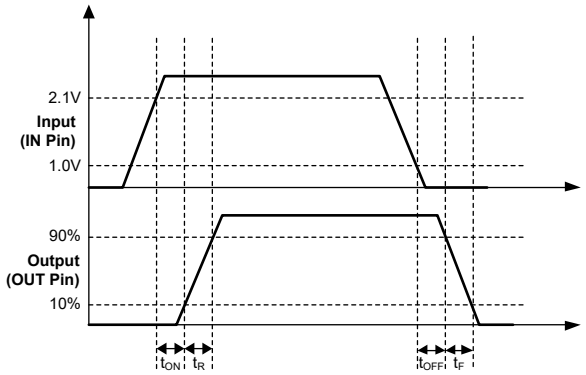


Figure 6. Switching Timing Diagram

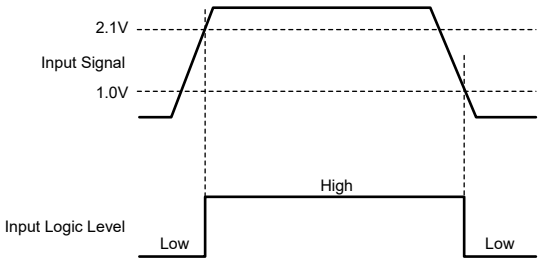


Figure 7. IN Input Thresholds

DETAILED DESCRIPTION (continued)

VCC and Under-Voltage Lockout (UVLO)

The SGM4853XA/B drivers integrate under-voltage protection on the VCC supply-circuit blocks. When the VCC bias voltage falls below Vccuv- and the UVLO duration is greater than t_{VCCUV}, the UVLO protection is triggered and the output remains low, ignoring the input status.

After UVLO is triggered, the internal switch Q_{FLT} is turned on, and EN/nFLT is pulled low to COM. When the UVLO state is removed, Q_{FLT} is turned off and the voltage on the EN/nFLT pin is charged by the external pull-up circuit, which is slowly rising. The fault clear time, t_{FLTC}, depends on the time constant that is set by R_{FLTC} and C_{FLTC}.

When the driver exits the UVLO state, the output remains low until the next high signal appears on the IN pin. See Figure 8 for more details.

The UVLO filtering time, t_{VCCUV}, helps to improve the noise immunity on the UVLO circuit.

Over-Current Detection Function

The SGM4853XA/B drivers implement the over-current protection function via the OCP pin. The pin voltage will trigger the protection mechanism when the voltage exceeds V_{OCTH}. The system connects the voltage drop on the current detection resistor to the OCP pin. The OCP pin is capable of withstanding negative 10V DC voltage. Figure 9 is a typical schematic of the SGM4853XA.

In order to prevent the OCP function from malfunctioning due to the noise caused by the fast switching process of the power device, the detection response time t_{OCPFLT} is set. The external RC filter circuit of the OCP pin will increase the response time of the over-current detection protection, and it is used in very harsh environments. When the OCP pin voltage exceeds V_{OCTH} and the time exceeds t_{OCPFLT}, the SGM4853XA/B drivers internally trigger OCP function. Simultaneously, Q_{FLT} is turned on and EN/nFLT is pulled low to COM.

When the OCP pin voltage exceeds V_{OCTH}, the gate output of the SGM4853XA/B is pulled low at once after the internal delay, t_{OCPDEL}, expires. See Figure 10. When the driver exits OCP fault event, the output remains low until the next high signal appears on the IN pin.

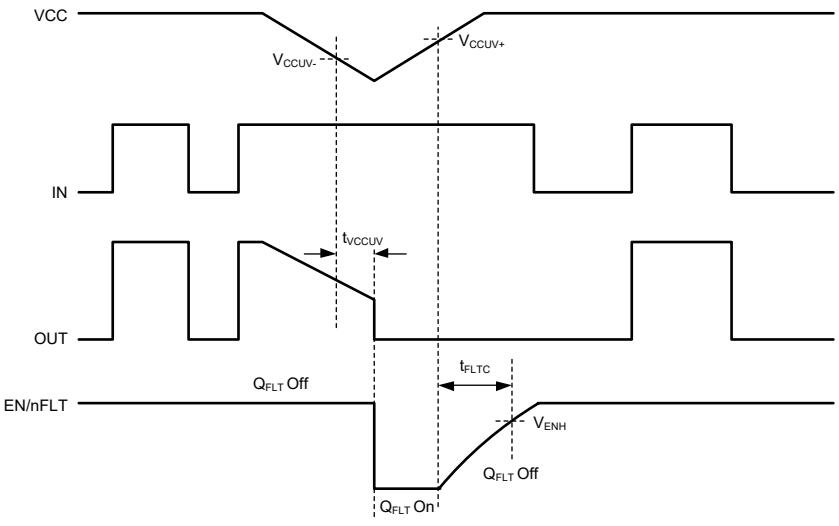


Figure 8. Definitions of VCC Under-Voltage Protection

DETAILED DESCRIPTION (continued)

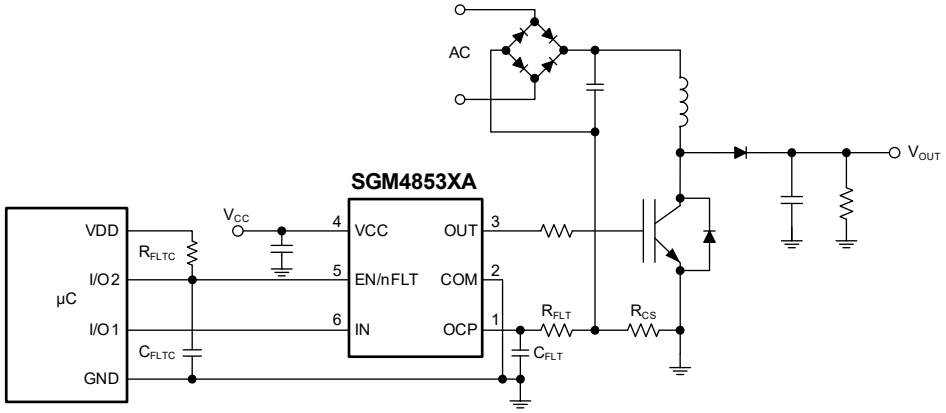


Figure 9. SGM4853XA in Boost Application

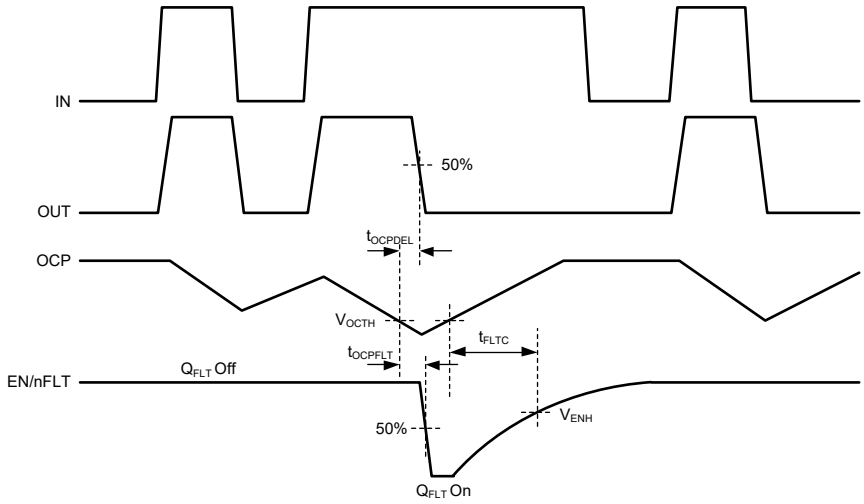


Figure 10. SGM4853XA OCP Fault Detection and Fault Clear Timing Diagram

Fault Report Function and Setting

The SGM4853XA/B drivers provide a fault report function, and the fault status is reported by the EN/nFLT pin. An under-voltage of VCC and an over-current event can cause the driver to indicate a fault. In the event of a fault, Q_{FLT} is turned on and EN/nFLT is pulled low to COM. The EN/nFLT output remains low until the fault condition is cleared. After the driver exits the fault event, Q_{FLT} is turned off and the voltage on the EN/nFLT pin is charged by the external pull-up circuit. The charging time constant is controlled by R_{FLTC} and C_{FLTC}. The fault clearing time t_{FLTC} depends on the exponential charging characteristic of the capacitor.

Figure 9 shows a typical circuit for the EN/nFLT pin. R_{FLTC} is pulled up to the external power supply (V_{DD}). C_{FLTC} capacitor is connected from the EN/nFLT pin to COM pin.

Assuming V_{DD} = 3.3V, the fault clearing time t_{FLTC} can be calculated by the following equation:

$$t_{FLTC} = -R_{FLTC} \times C_{FLTC} \times \ln(1 - \frac{V_{ENH}}{V_{DD}}) \quad (1)$$

Enable Function

The EN/nFLT pin also offers enable function. This pin can control the output of the drive. When the EN/nFLT voltage rises above V_{ENH}, the output is enabled. When the EN/nFLT pin voltage falls below V_{ENL}, the output is disabled.

Figure 11 to Figure 13 show the timing diagrams of the SGM4853XA/B, and the relationship between enable signal threshold and IC logic.

DETAILED DESCRIPTION (continued)

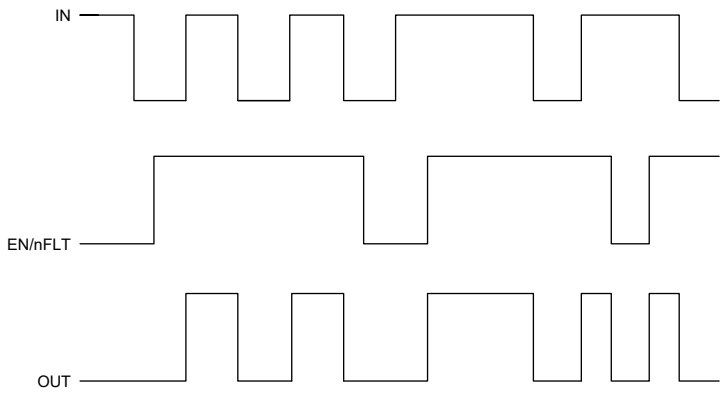


Figure 11. Input/Output/Enable Timing Diagram

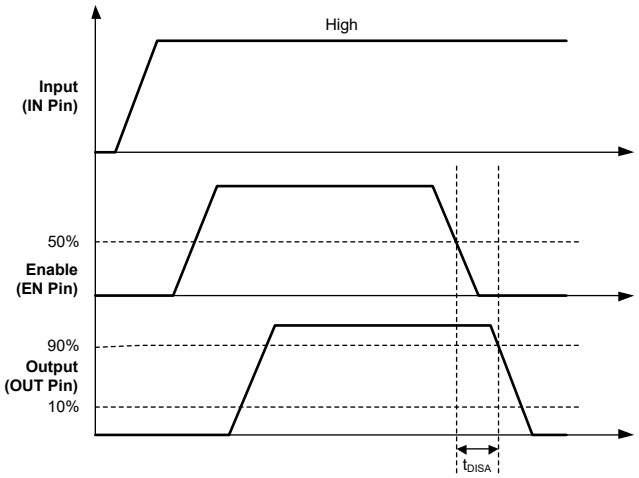


Figure 12. Enable Function

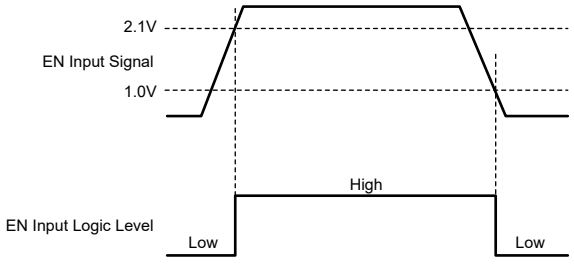


Figure 13. Enable Input Thresholds

REVISION HISTORY

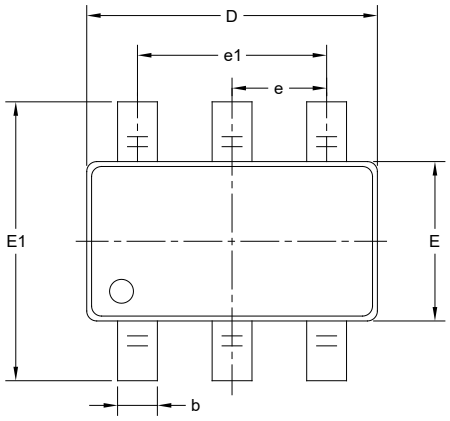
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

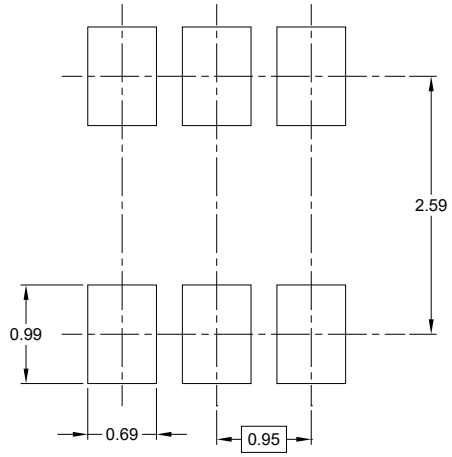
JULY 2023 – REV.A to REV.A.1	Page
Added Pin Description section	3

Changes from Original (JUNE 2023) to REV.A	Page
Changed from product preview to production data	All

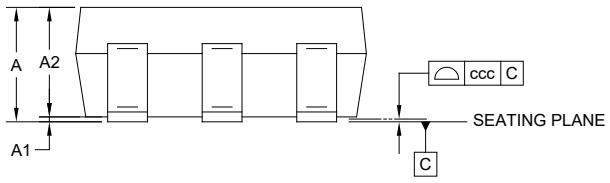
PACKAGE OUTLINE DIMENSIONS

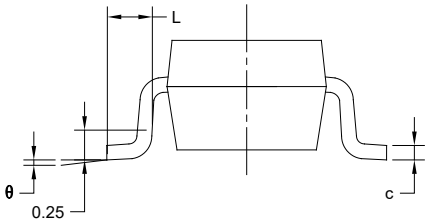
SOT-23-6





RECOMMENDED LAND PATTERN (Unit: mm)



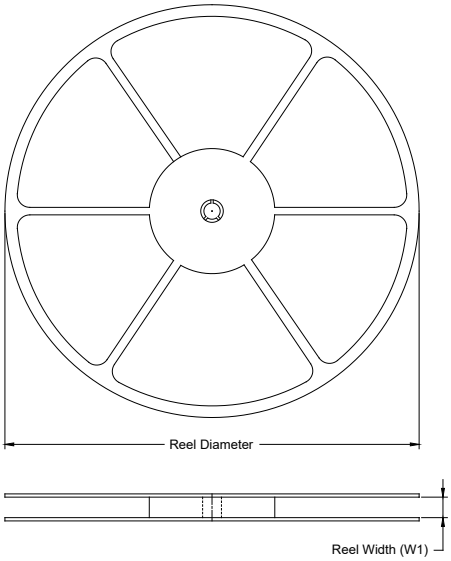


Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	-	-	1.450
A1	0.000	-	0.150
A2	0.900	-	1.300
b	0.300	-	0.500
c	0.080	-	0.220
D	2.750	-	3.050
E	1.450	-	1.750
E1	2.600	-	3.000
e	0.950 BSC		
e1	1.900 BSC		
L	0.300	-	0.600
θ	0°	-	8°
ccc	0.100		

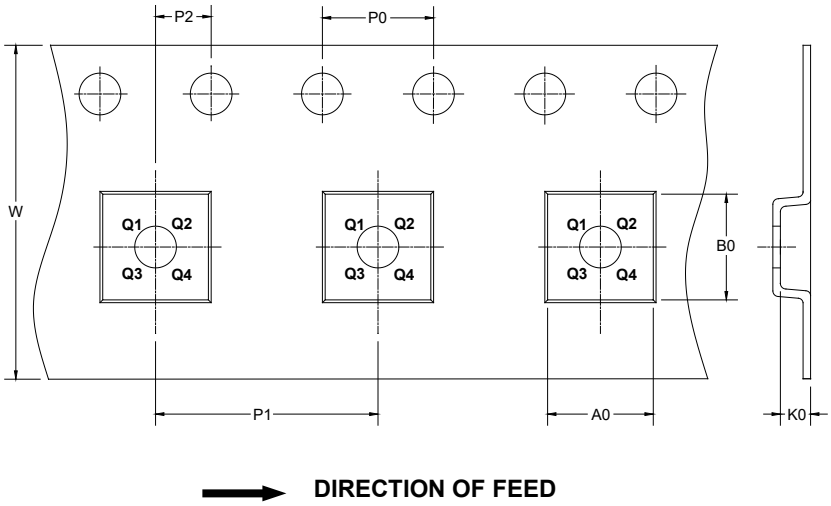
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-178.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



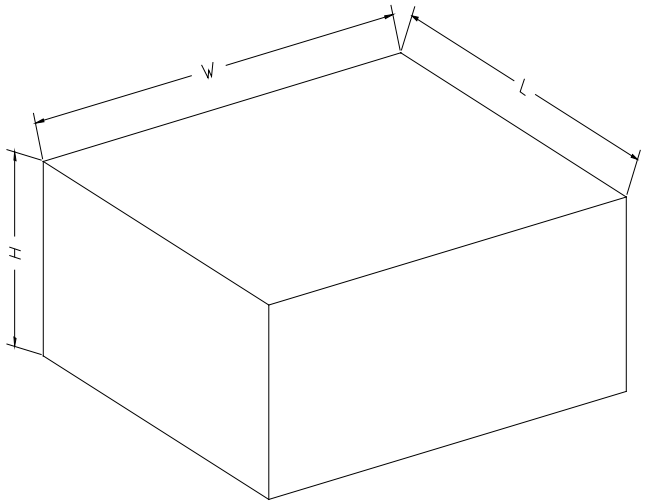
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOT-23-6	7″	9.5	3.23	3.17	1.37	4.0	4.0	2.0	8.0	Q3

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002