SGM48510
11A High-Speed Low-Side MOSFET Driver

GENERAL DESCRIPTION

The SGM48510 is a high-speed low-side gate driver for MOSFET power switches. It provides large peak source and sink current capability with capacitive loads.

The SGM48510 adopts separate output architecture. The separate output architecture allows independent control of the turn-on and turn-off speeds. An 8A peak current at the Miller plateau region improves the immunity of the device to the parasitic Miller conduction effect during switching transitions of the MOSFETs.

The SGM48510 is available in Green TDFN-2×2-8AL and SOIC-8 packages.

FEATURES

- **Input Voltage Range: 4.5V to 24V**
- **11A Source and 6A Sink Peak Currents**
- **TTL and CMOS Compatible Logic Threshold**
- **Logic Levels Independent of Supply Voltage**
- **Fast Rise Time: 4ns (TYP)**
- **Fast Fall Time: 4ns (TYP)**
- **Fast Propagation Delays: 13ns (TYP)**
- **Separate Pull-Up and Pull-Down Outputs**
- **Dual Input Design (Choice of an Inverting (IN-) or Non-Inverting (IN+) Driver Configuration)**
- **Available in Green TDFN-2×2-8AL and SOIC-8 Packages**

APPLICATIONS

Telecom Switch Mode Power Supplies
Power Factor Correction (PFC) Circuits
Solar Power Supplies
Motor Drives
High Frequency Line Drivers
Pulse Transformer Drivers
High Power Buffers

TYPICAL APPLICATION

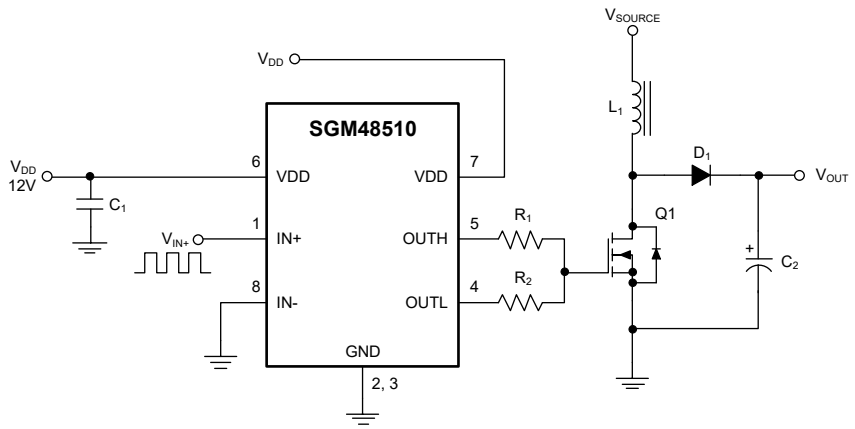


Figure 1. Typical Application Circuit

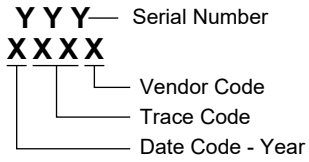
PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM48510	TDFN-2×2-8AL	-40℃ to +125℃	SGM48510XTDE8G/TR	MBZ XXXX	Tape and Reel, 3000
	SOIC-8	-40℃ to +125℃	SGM48510XS8G/TR	SGM 48510XS8 XXXXX	Tape and Reel, 4000

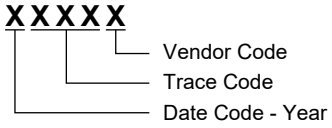
MARKING INFORMATION

NOTE: XXXX = Date Code, Trace Code and Vendor Code. XXXXX = Date Code, Trace Code and Vendor Code.

TDFN-2×2-8AL



SOIC-8



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD} ..... -0.3V to 28V
Output Current (DC), I_{OUT_DC} 0.6A
Output Current (1), I_{OUT_PULSE} 11A
Input Voltages, V_{IN+}, V_{IN-} ..... -6V to 24V
Output Voltages, V_{OUTH}, V_{OUTL} ..... -0.3V to V_{DD} + 0.3V
Output Voltages (Pulse < 0.5μs), V_{OUTH}, V_{OUTL}
..... -3.0V to V_{DD} + 3.0V
Package Thermal Resistance
TDFN-2×2-8AL, θ_{JA} ..... 63℃/W
SOIC-8, θ_{JA} ..... 131℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 3000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Supply Voltage, V_{DD} ..... 4.5V to 24V
Input Voltages, V_{IN+}, V_{IN-} ..... -5V to 24V
Operating Junction Temperature Range ..... -40℃ to +125℃

NOTE:
1. A 1μF load is connected from OUT (OUTH shorted to OUTL) to GND with 1kHz square wave input.

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

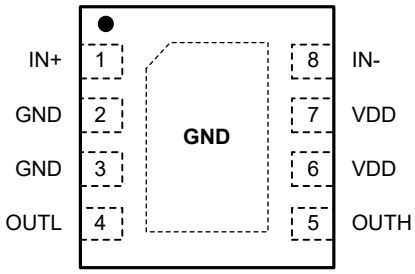
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

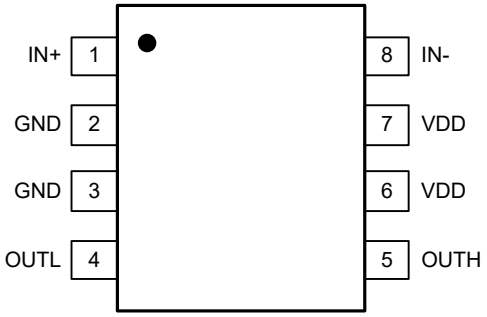
PIN CONFIGURATIONS

(TOP VIEW)



TDFN-2×2-8AL

(TOP VIEW)



SOIC-8

PIN DESCRIPTION

PIN	NAME	I/O	FUNCTION
1	IN+	I	Non-Inverting Input. The input threshold is compatible with TTL and CMOS logic. Connect IN+ to the VDD pin if unused. Do not leave this pin open.
2, 3	GND	G	Ground. Reference pin for all signals. Connect GND as close to the source of the power MOSFET as possible.
4	OUTL	O	Driver Sink Current Output. Connect it to the gate of an external MOSFET.
5	OUTH	O	Driver Source Current Output. Connect it to the gate of an external MOSFET.
6, 7	VDD	P	Power Supply Input.
8	IN-	I	Inverting Input. The input threshold is compatible with TTL and CMOS logic. Connect IN- to the GND pin if unused. Do not leave this pin open.
Exposed Pad	GND	—	Exposed Pad. It should be soldered to PCB board and connected to GND.

NOTE: I: input, O: output, G: ground, P: power for the circuit.

Table 1. Device Logic Table

IN+	IN-	OUTH	OUTL	OUT (OUTH and OUTL Tied Together)
L	L	High-Z	L	L
L	H	High-Z	L	L
H	L	H	High-Z	H
H	H	High-Z	L	L

ELECTRICAL CHARACTERISTICS

(V_{DD} = 12V, C_1 = 1μF, T_A = T_J = -40℃ to +125℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage						
Operating Current	I_{DD}	No switching		0.5	1	mA
VDD Under-Voltage Lockout Voltage	V_{CCR}	V_{DD} rising	3.7	3.9	4.1	V
	V_{CCF}	V_{DD} falling	3.4	3.6	3.9	V
VDD Under-Voltage Lockout Voltage Hysteresis	V_{CCH}			300		mV
VDD Under-Voltage Lockout to Output Delay		V_{DD} rising from 3V to 5V		10		μs
Inputs						
Input Signal High Threshold	V_{THH}	Input rising from logic low	1.8	2.1	2.3	V
Input Signal Low Threshold	V_{THL}	Input falling from logic high	1.1	1.3	1.5	V
Input Signal Hysteresis	V_{IN_HYS}			0.8		V
IN- Pull-Up Resistor	R_{IN-}			200		kΩ
IN+ Pull-Down Resistor	R_{IN+}			200		kΩ
Outputs						
Output Pull-Up Resistance	R_{OH}	I_{OUT} = -100mA		0.4	0.8	Ω
Output Pull-Down Resistance	R_{OL}	I_{OUT} = +100mA		0.4	0.8	Ω
Peak Source Current	I_{SOURCE}	C_{LOAD} = 1μF connected to GND, f_{PWM} = 1kHz		11		A
Miller Plateau Source Current	I_{SOURCE}	C_{LOAD} = 1μF connected to 5V, f_{PWM} = 1kHz		8		A
Peak Sink Current	I_{SINK}	C_{LOAD} = 1μF connected to GND, f_{PWM} = 1kHz		6		A
Miller Plateau Sink Current	I_{SINK}	C_{LOAD} = 1μF connected to 5V, f_{PWM} = 1kHz		6		A
Switching Characteristics						
Rise Time (1)	t_R	C_{LOAD} = 1.8nF		4		ns
Fall Time (1)	t_F	C_{LOAD} = 1.8nF		4		ns
Input to Output Propagation Delay (1)	t_{D1}	C_{LOAD} = 1.8nF		13		ns
	t_{D2}	C_{LOAD} = 1.8nF		13		ns

NOTE:
1. See timing diagrams as shown in Figure 2 and Figure 3.

TIMING DIAGRAMS

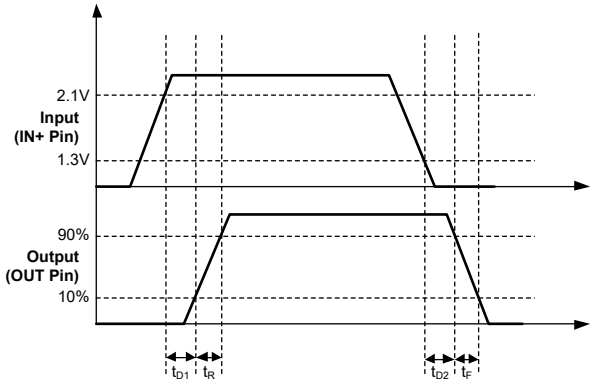


Figure 2. Non-Inverting Configuration

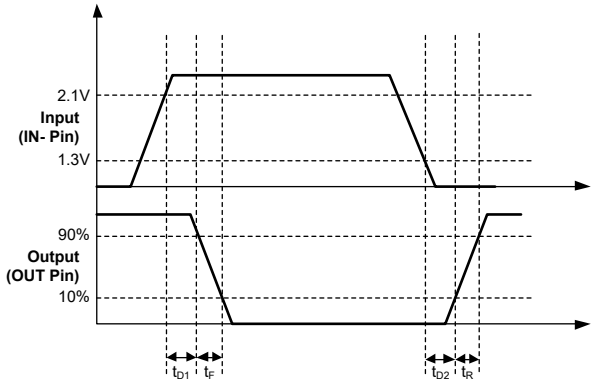
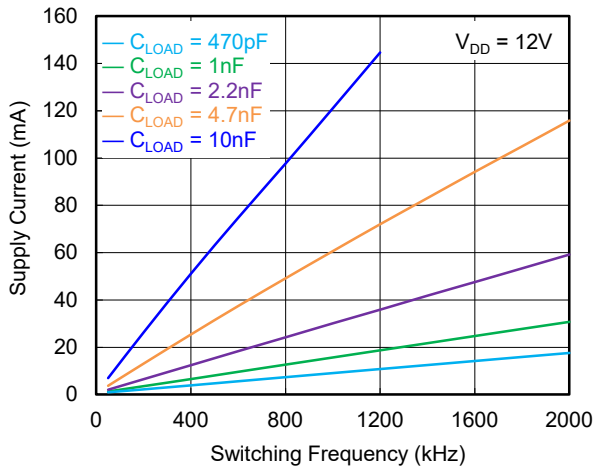


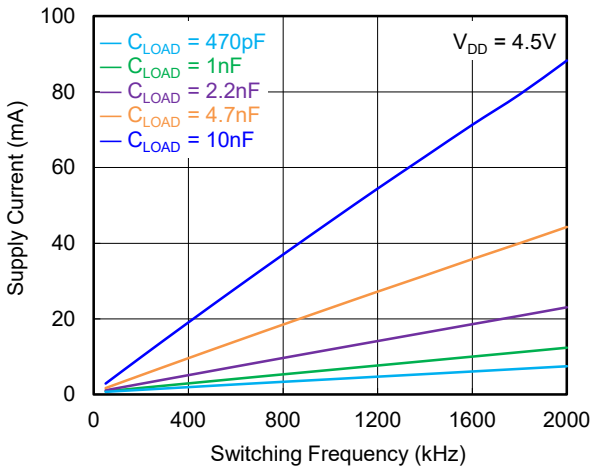
Figure 3. Inverting Configuration

TYPICAL PERFORMANCE CHARACTERISTICS

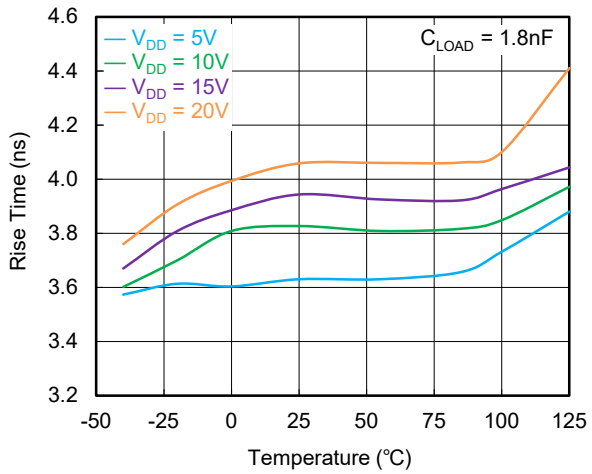
Supply Current vs. Switching Frequency



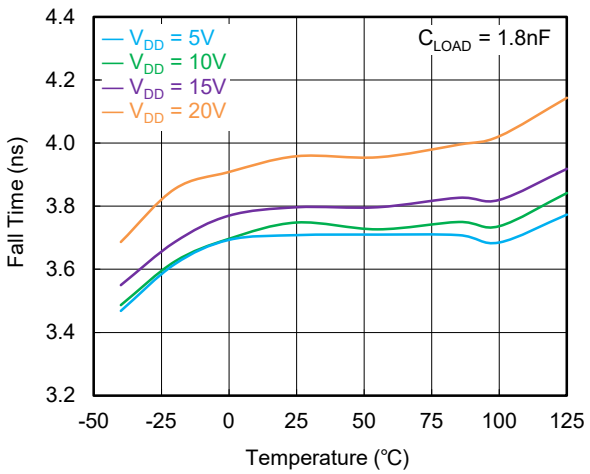
Supply Current vs. Switching Frequency



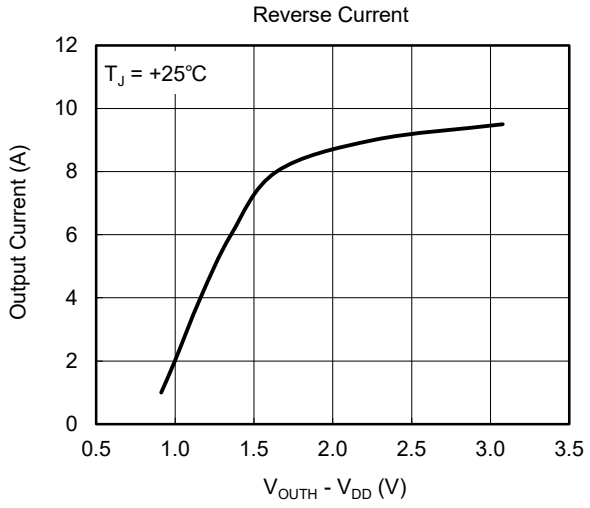
Rise Time vs. Temperature



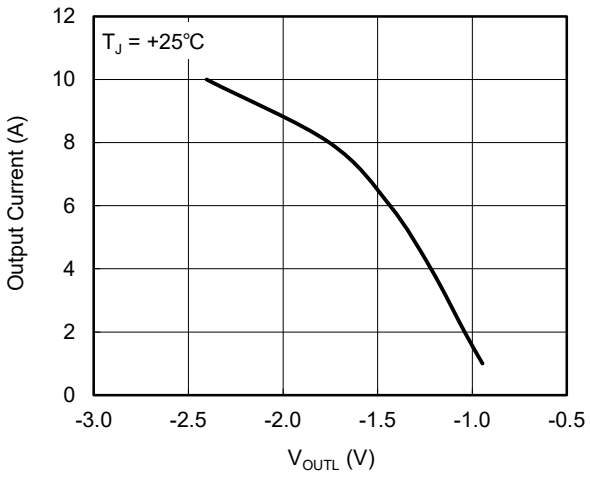
Fall Time vs. Temperature



Reverse Current

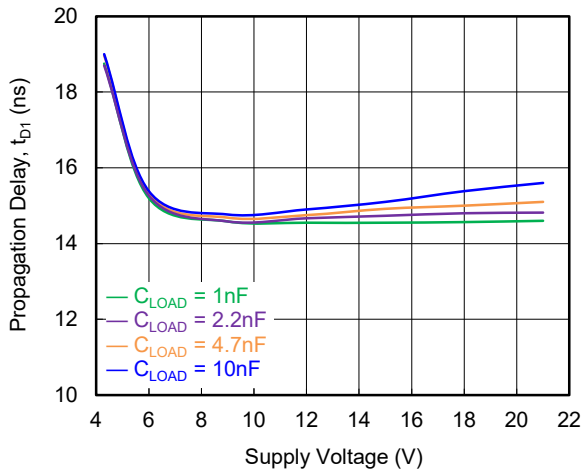


Reverse Current

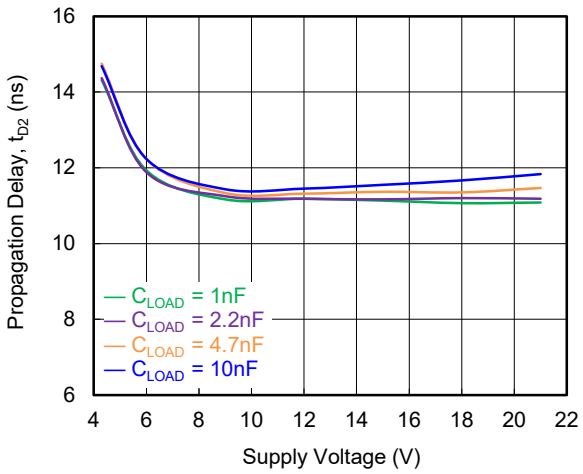


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

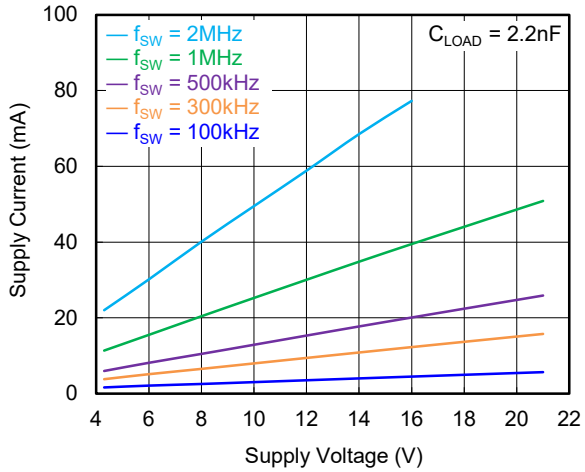
Propagation Delay (t_{D1}) vs. Supply Voltage



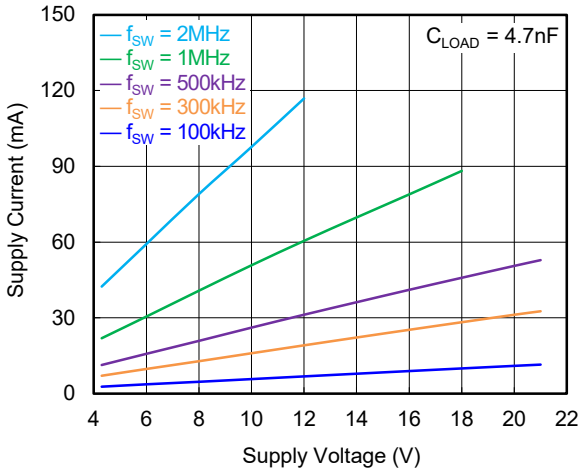
Propagation Delay (t_{D2}) vs. Supply Voltage



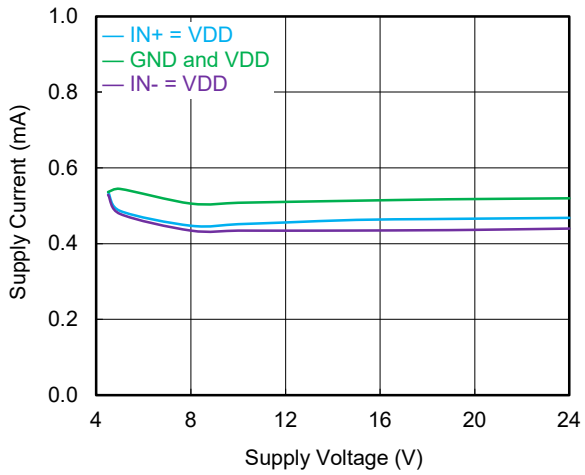
Supply Current vs. Supply Voltage



Supply Current vs. Supply Voltage

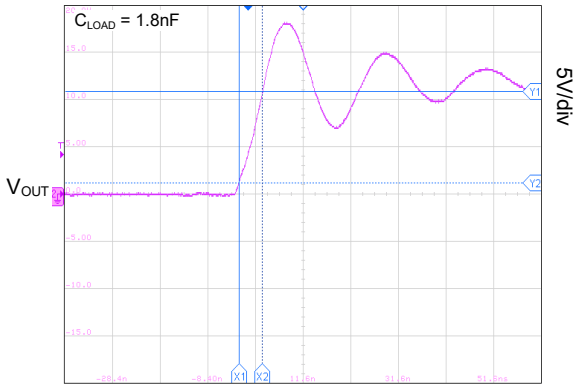


Supply Current vs. Supply Voltage

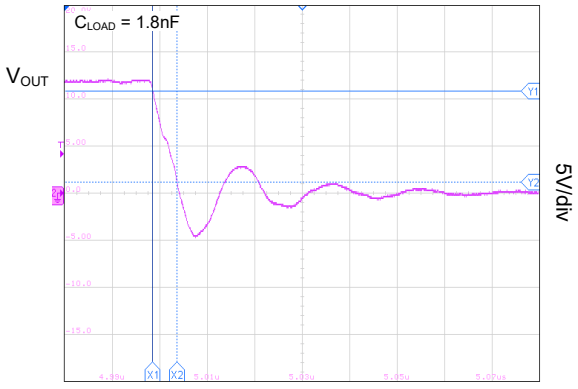


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

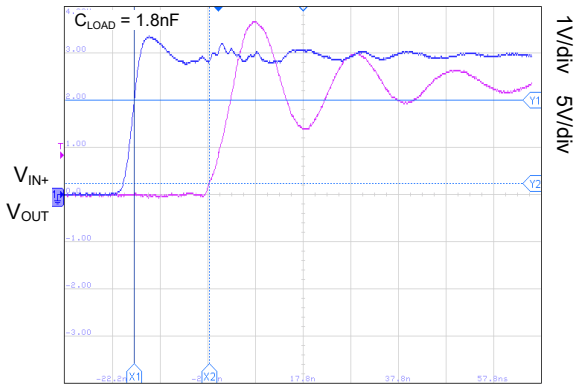
Non-Inverting Input Rise Time



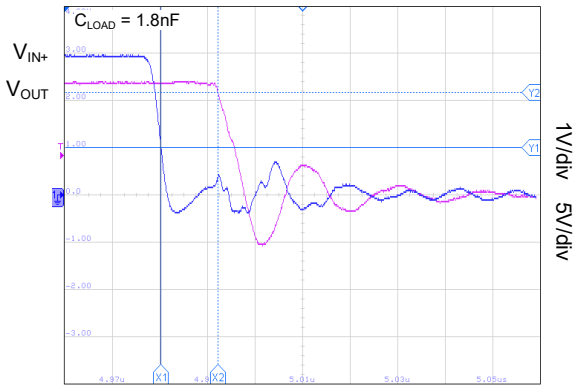
Non-Inverting Input Fall Time



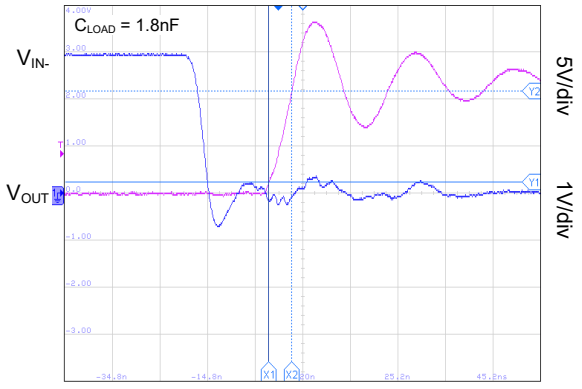
Non-Inverting Input Propagation Delays



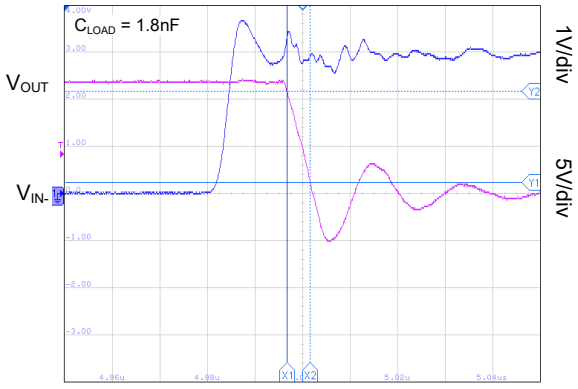
Non-Inverting Input Propagation Delays



Inverting Input Rise Time

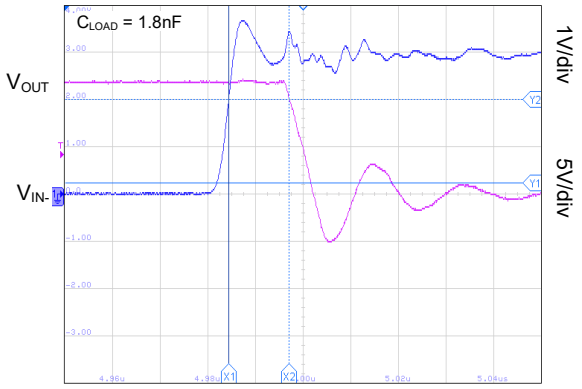


Inverting Input Fall Time



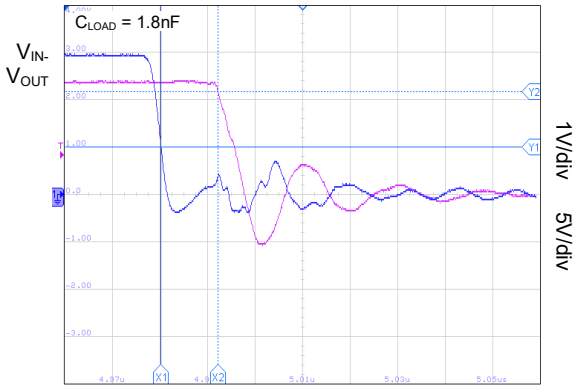
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Inverting Input Propagation Delays



Time (10ns/div)

Inverting Input Propagation Delays



Time (10ns/div)

FUNCTIONAL BLOCK DIAGRAM

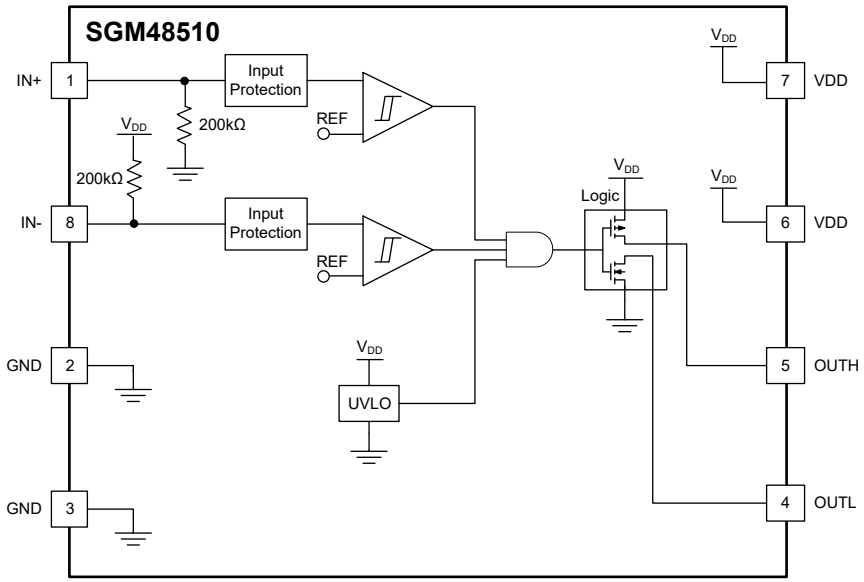


Figure 4. SGM48510 Block Diagram

DETAILED DESCRIPTION

PCB Layout

Proper PCB layout is an important design step in high current, fast switching circuits to provide proper device operation and design robustness. The SGM48510 gate driver integrates a short propagation delay and a powerful output stage, providing separate output architecture capable of delivering large current peaks with very fast rise time and fall time at the gate of the power switch. Very high di/dt can cause unacceptable ringing if trace length and impedance are not well controlled. The recommended layout guidelines are as follows in the design.

- Place the driver device as close as possible to the power device to minimize the length of high-current traces between the driver output pins and the gate of the power switch device.
- Place bypass capacitors between the VDD and GND pins as close as possible to the driver pins to minimize trace length and improve noise filtering. These capacitors support high peak current draw from VDD during power switch on. Low inductance surface mount components such as chip capacitors are strongly recommended.
- Turn-on and turn-off current loop paths (driver devices, power switches, and VDD bypass capacitors) should be minimized to keep stray inductance to a minimum.
- Wherever possible, parallel the source and return traces of a current loop, taking advantage of flux cancellation.
- Separate power and signal traces, such as output and input signals.
- Adding some gate resistors and/or snubbers can reduce switch node transients and ringing. These measures also reduce EMI.
- Use a ground plane to provide noise shielding. Do not use the ground plane as the current carrying path for any current loop. In addition to noise shielding, the ground plane also helps reduce power dissipation.
- Unused pins should be configured by referring to the pin description table to avoid output indeterminate states.

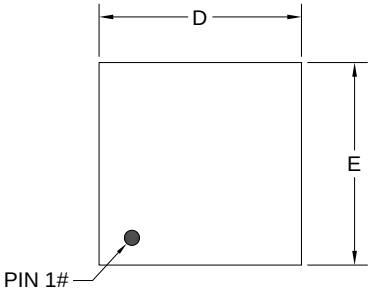
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

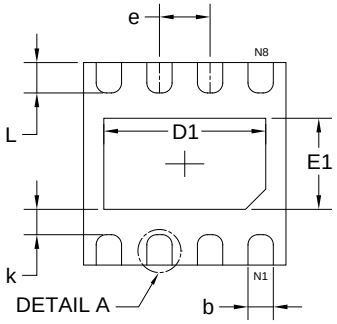
Changes from Original (DECEMBER 2022) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

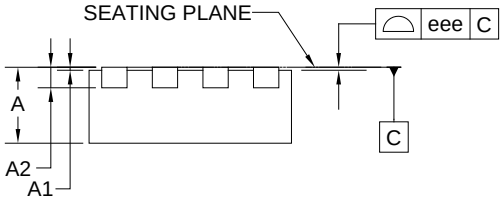
TDFN-2×2-8AL



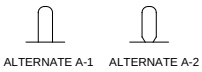
TOP VIEW



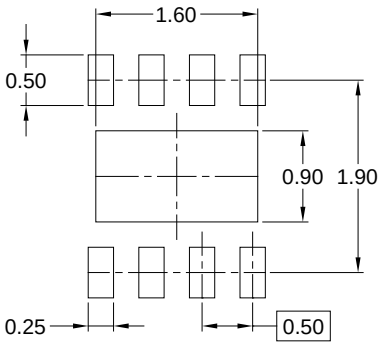
BOTTOM VIEW



SIDE VIEW



DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



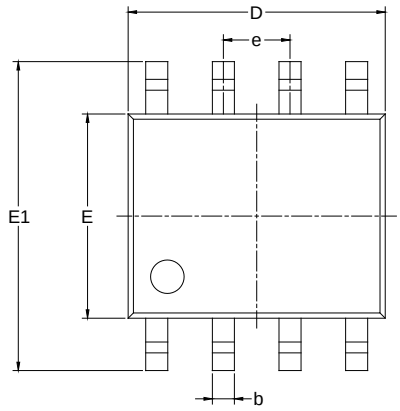
RECOMMENDED LAND PATTERN (Unit: mm)

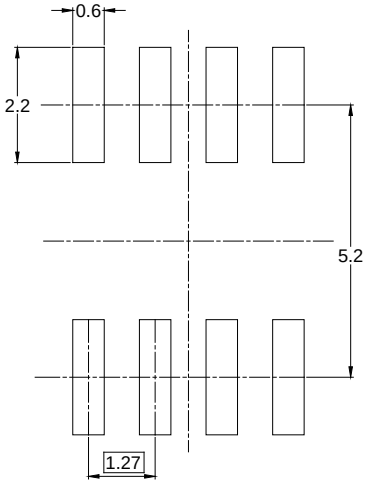
Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	0.700	0.750	0.800
A1	0.000	-	0.050
A2	0.203 REF		
b	0.200	0.250	0.300
D	1.900	2.000	2.100
D1	1.450	1.600	1.700
E	1.900	2.000	2.100
E1	0.750	0.900	1.000
k	0.150	0.250	0.350
e	0.450	0.500	0.550
L	0.200	0.300	0.400
eee	0.080		

NOTE: This drawing is subject to change without notice.

PACKAGE OUTLINE DIMENSIONS

SOIC-8





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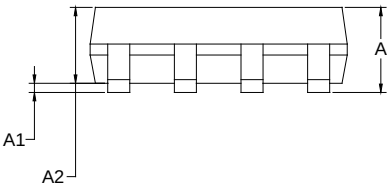
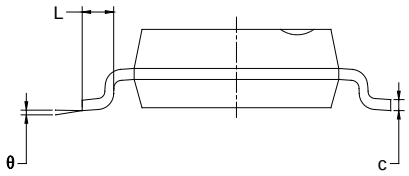


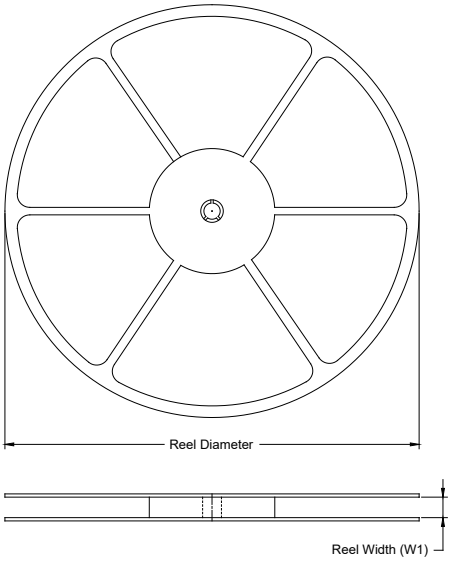


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.27 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

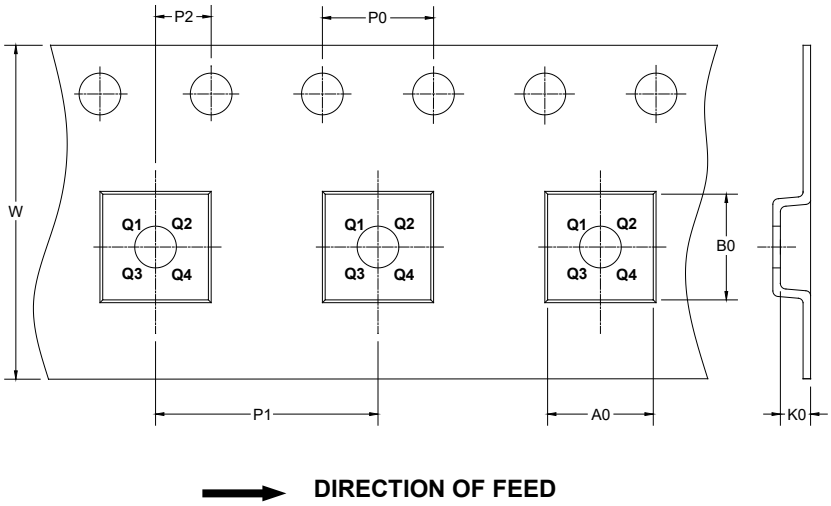
NOTES:
1. Body dimensions do not include mode flash or protrusion.
2. This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



DIRECTION OF FEED

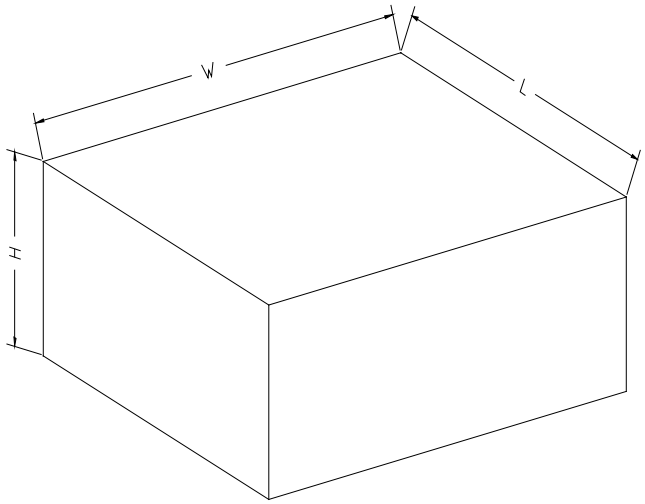
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TDFN-2×2-8AL	7″	9.5	2.30	2.30	1.10	4.0	4.0	2.0	8.0	Q1
SOIC-8	13″	12.4	6.40	5.40	2.10	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18
13″	386	280	370	5

DD0002